# 2.0 APPLICATION NOTES

## 2.1 Typical Board-level Configuration

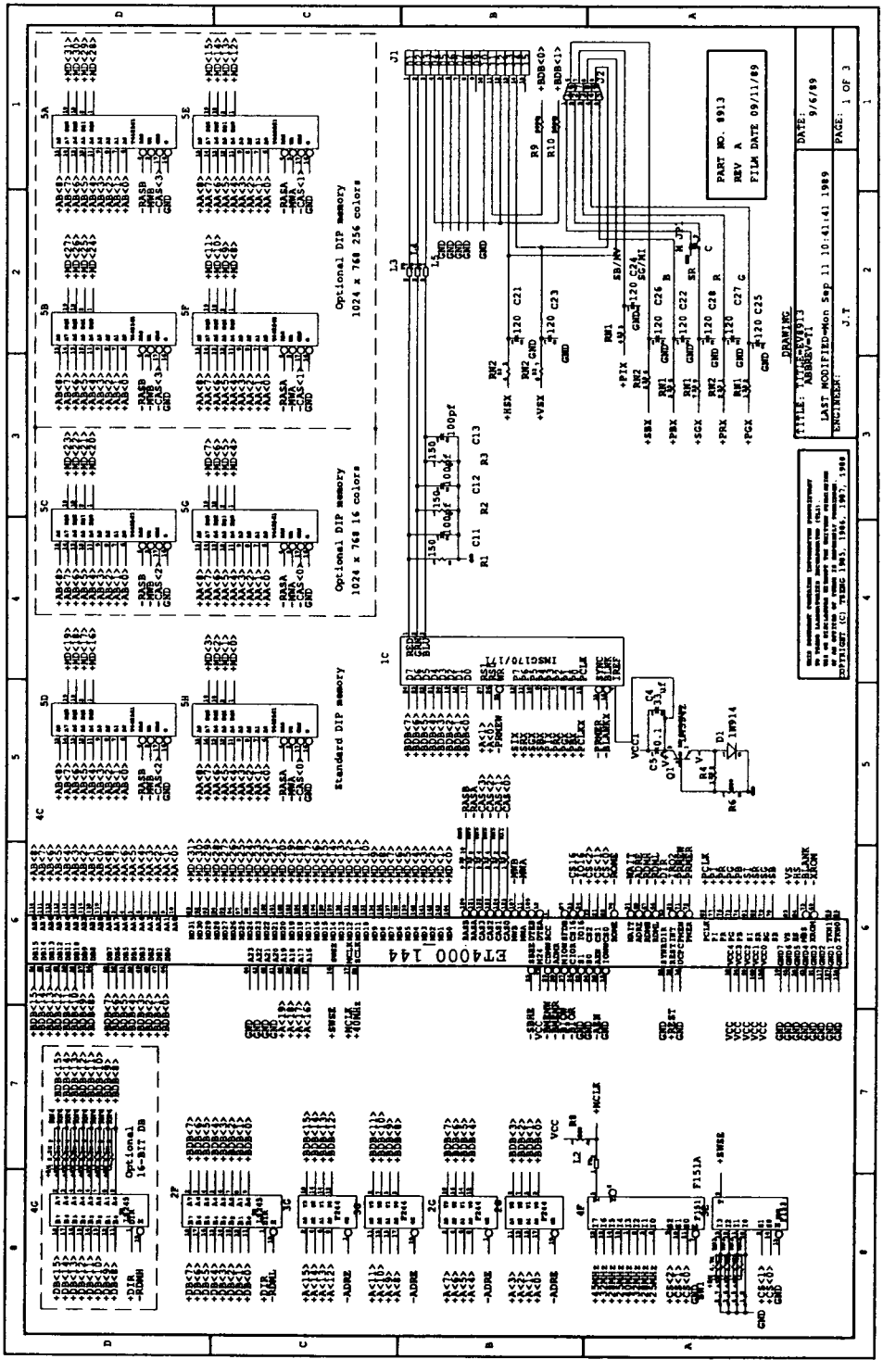



FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — AT BUS — 1 of 3

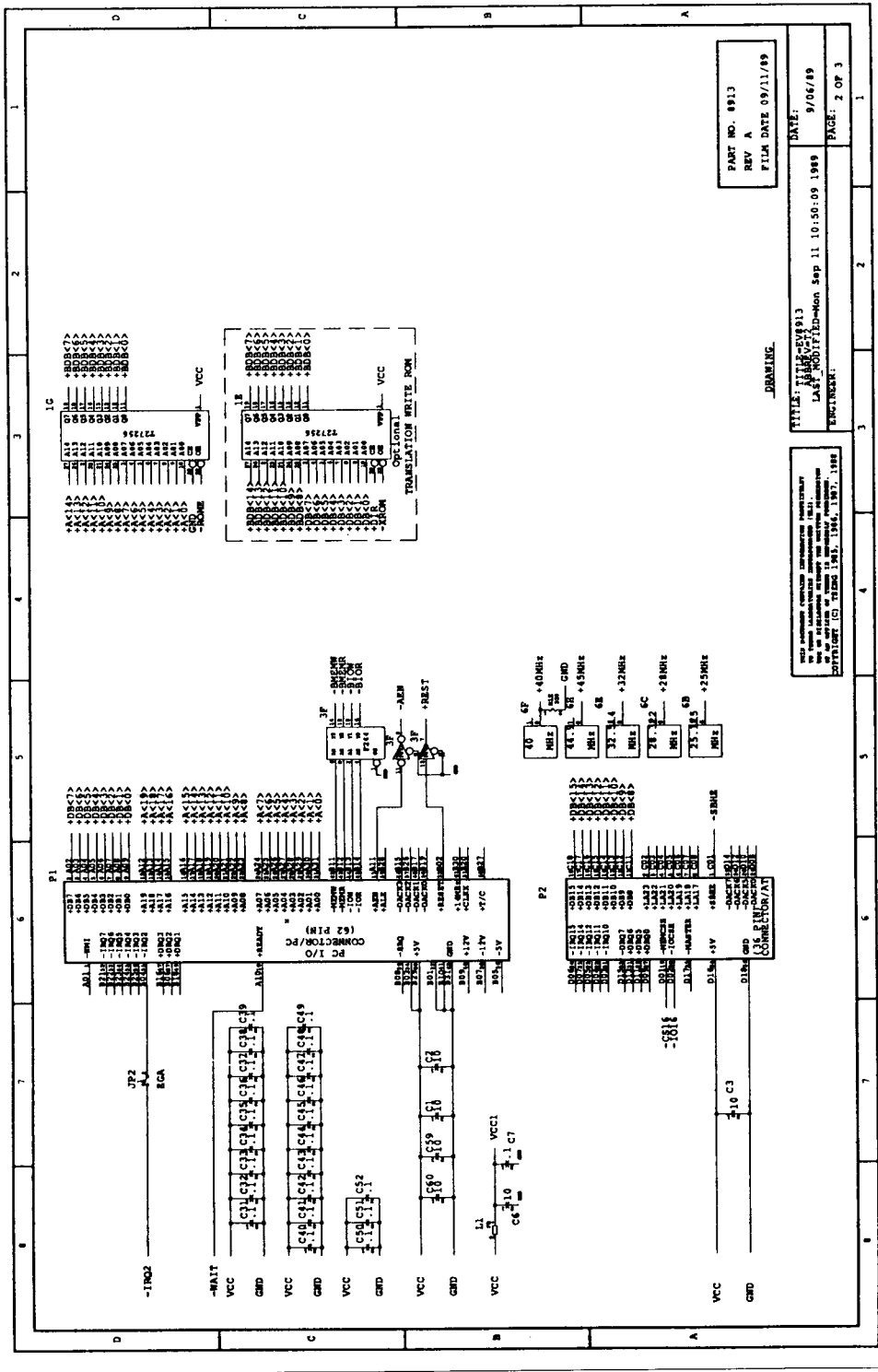


FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — AT BUS — 2 of 3

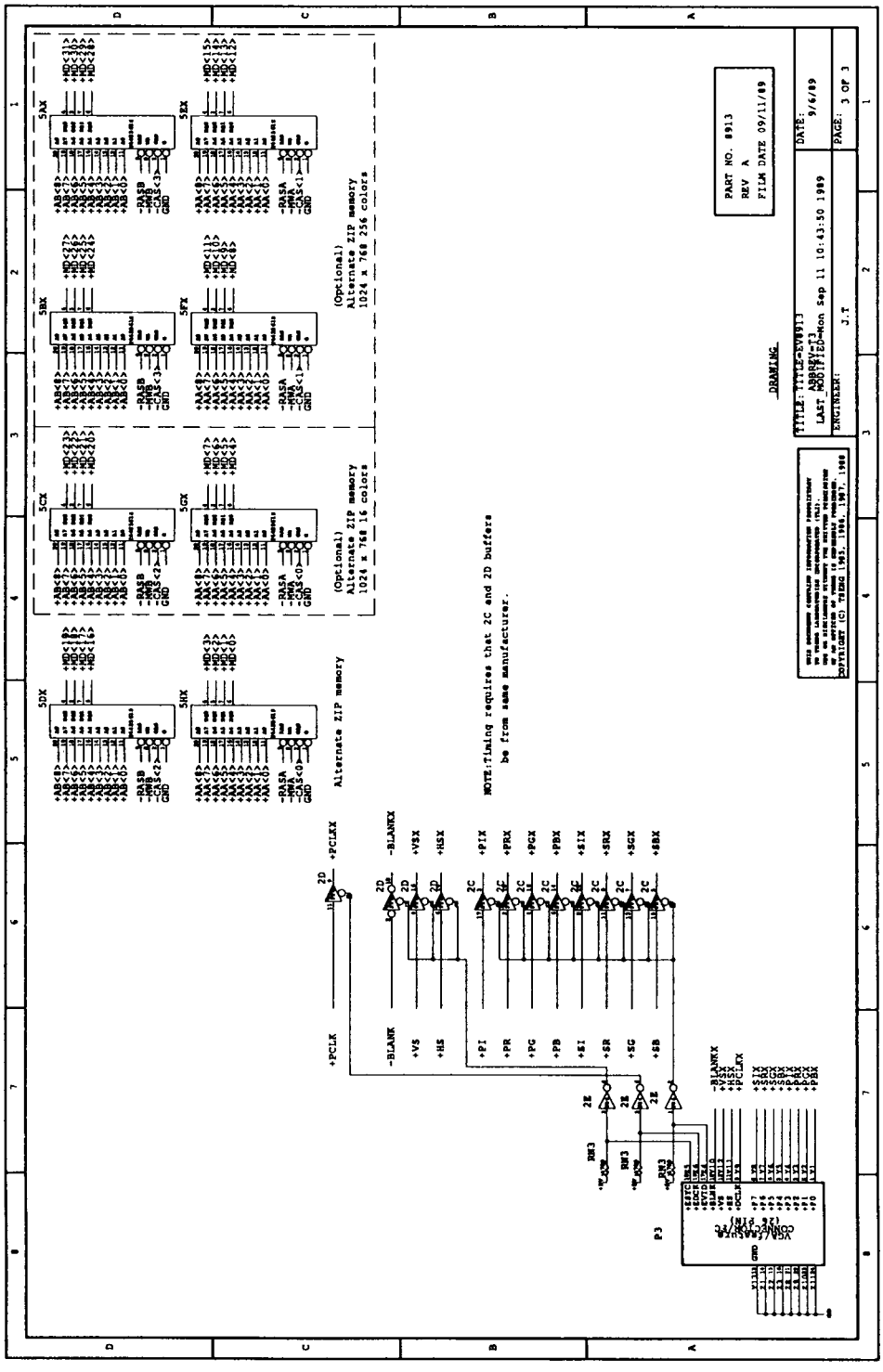



FIG. 2.1-1 TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) – AT BUS – 3 of 3

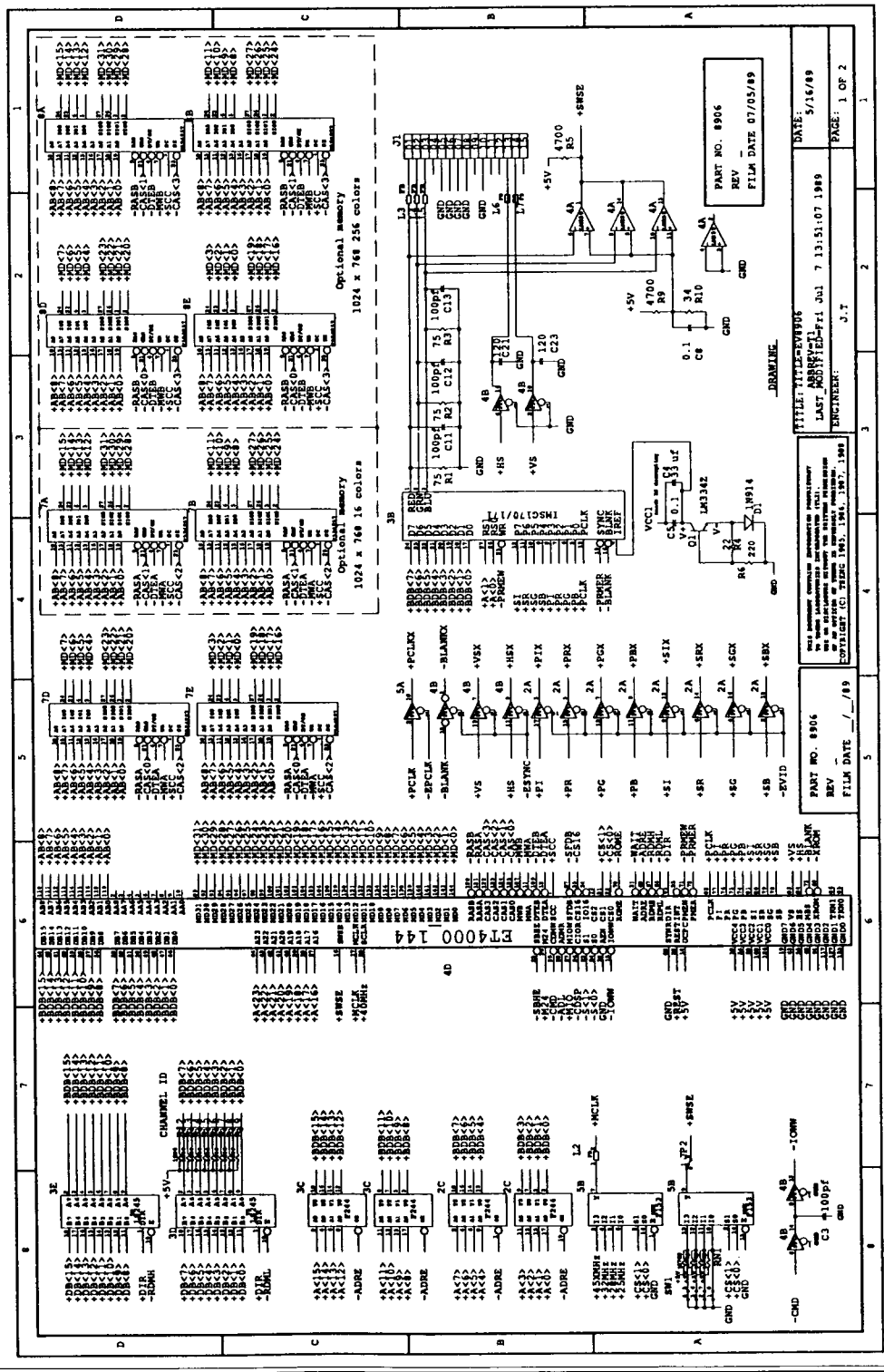


FIG. 2.1-1a TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) — MICRO CHANNEL BUS — 1 of 2

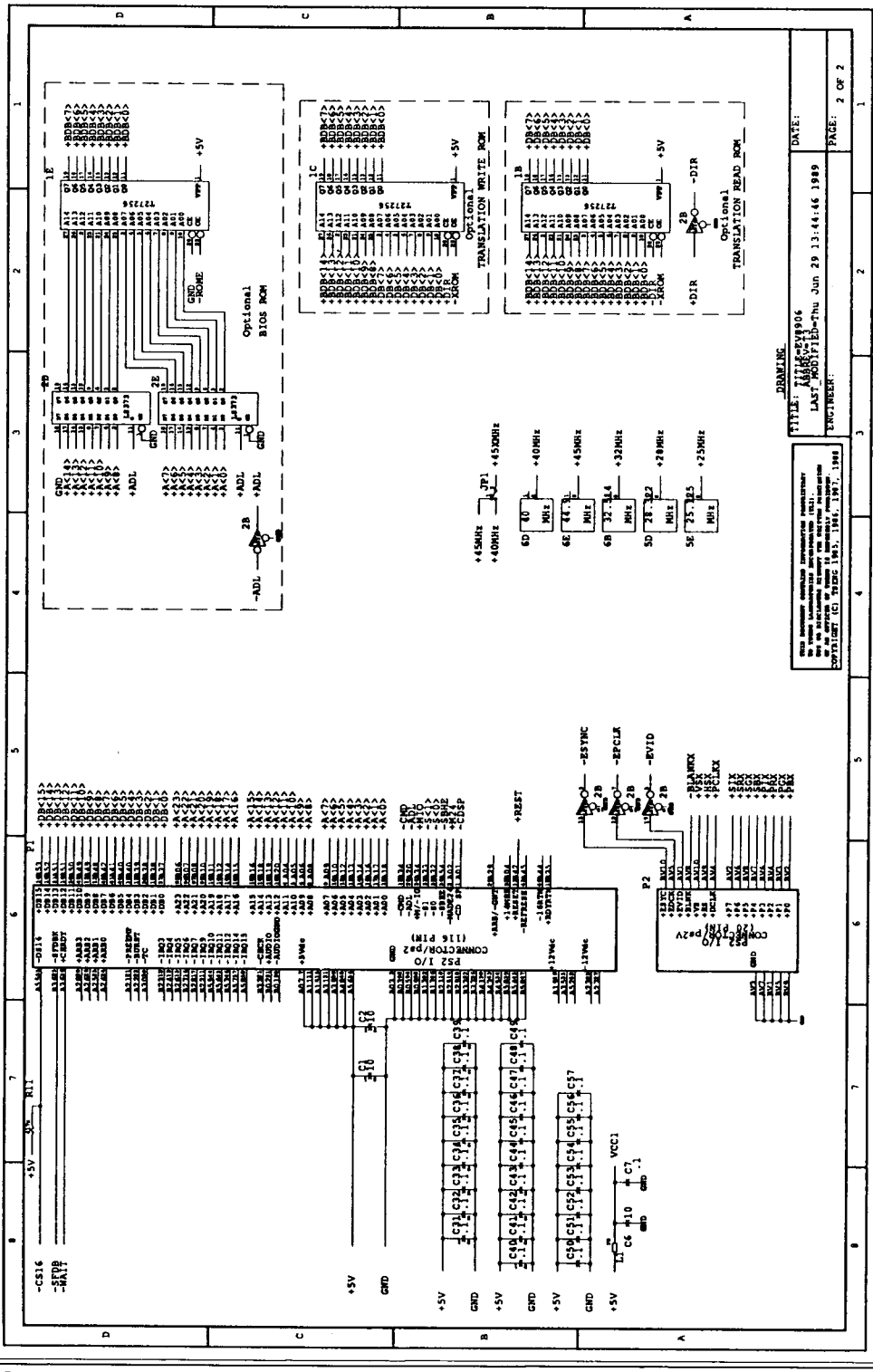


FIG. 2.1-1A TYPICAL ET4000-BASED BOARD DESIGN (SCHEMATIC) – MICRO CHANNEL BUS – 2 of 2

The ET4000 is a highly integrated, highly flexible single-chip controller that can propel a video design using a minimum number of components. A complete VGA design can use as few as 9 chips configured with only two 1MB DRAMs. The ET4000 requires no additional support chips to interface to the PC/AT and MCA busses. This means it uses less space and fewer overall components, and provides high performance, high reliability, and reduced cost. These attributes make the ET4000 ideal for video subsystem motherboard integration. Delivering resolutions up to 1024x768 with 256 simultaneous colors, interlaced or non-interlaced display scan, greater flexibility is provided for interfacing with a wide assortment of monitors.



The ET4000 can be easily programmed and configured to function as a VGA/EGA/CGA/MDA controller with only two 100ns 1MB DRAMs, and the typical board-level configurations based on the ET4000 chip described below.

As shown in Figs. 2.1-1 (standard PC/AT bus) and 2.1-1a (Micro Channel bus), a basic configuration consists of a single memory bank as display buffer, the ET4000 VLSI chip, an external color look-up DAC (Digital to Analog Converter), and data/address buffers/multiplexers as support logic.

The PS/2 Video connector allows interfacing to a color or monochrome monitor. The CPU bus interface shown in Fig. 2.1-1 is based on the IBM PC/XT bus timing, and Fig. 2.1-1a is based on the IBM PS/2 MCA bus timing.

Both configurations can be programmed, via a single register, to be 100% register-level compatible with a VGA/EGA/CGA, or MDA controller. All of the VGA/EGA text and graphic modes are supported, and all of the VGA/EGA hardware assist features including data latching, bit mask, rotation, logical functions and plane-selects are provided at a register-compatible level.

Major Components include:

## 2.1.1 ET4000 VLSI Chip

All major components of the ET4000 are contained within a single 144- or 160-pin Plastic Flat Package. The following is breakdown of the major elements of the ET4000 controller.

## CRT Controller (CRTC)

The ET4000 internal CRT Controller (CRTC) provides an 18-bit linear address cursor control and VS and HS controls to external raster-scan CRT displays. Internally, CRTC derives all reference timing in two dimensions: the horizontal display/blanking/sync and vertical display/blanking/sync. Each cycle in horizontal and vertical is evolved around the ET4000's CHARACTER and LINE reference logic. Each character is based on multiple of 8 or 9 MCLK. Both CHARACTER and LINE reference logic can be asynchronously initialized via the SYNR input pin.



## Memory Control Unit (MCU)

The Memory Control unit consists of four parts:

Memory control: RAS/CAS/MW/DTE/SCC timing/sequence control; the trp (RAS pre-charge), trcd (RAS to CAS delay), tcas (CAS pulse width), and tcp (CAS pre-charge), are programmable via RCONF register.

Memory address: provides up to 1 megabyte addressing space via AB(8:0) and AA(8:0).

Memory data: provides from 8-bit display memory data width to 32-bit data width via MD(31:0) data interface.

Memory refresh: programmable refresh frequency via CRTC Indexed Register 36.

## System Priority Control (SPC)

The SPC's main task is to orchestrate the ET4000's internal resources requests including: the FIFOs, Graphics Data Controller, Cache Controller, and RAM refresh. The system performance is based on two major factors: the ATC demand, i.e.; the display resolution and color; and the memory bandwidth, i.e.; the memory bus width and access time.

Other factors also can contribute to the overall performance. For example, the cache controller can be optimized for sequential access and CPU write operations. The 16-bit CPU bus interface also results in faster data transfer, particularly in the plane graphics mode (a 16-bit CPU write = up to a 64-bit data transfer). For further discussion refer to Memory Design Considerations, section 2.2.3.

## Timing Sequencer (TS)

The Timing Sequencer is a set of registers responsible for providing basic timing control for both the CRTC and ATC. Seven of these eight registers are internally indexed, which means that they are accessed via a common I/O address, with one of the seven registers that is selected by the TS Index register. Timings controlled by the TS registers include:

-Horizontal count resolution: 8 or 9 dots/character
-SCLK/2, MCLK/2, MCLK/4, and DCLK/2 (dotclock)
-Video load control: every 8, 16, or 32 dot clocks



## Graphics Display Controller (GDC)

The GDC optimizes bit-mapped display memory data manipulation by assisting the CPU in the operation of displaying memory data-related functions. This includes rotate/mask/z-plane, with any of four boolean functions—in response to a single CPU write. By putting basic bit map operations in high-speed hardware, the ET4000 dramatically increases graphics processing throughput over software-driven solutions. The data manipulation capability implemented in the GDC is, however, applicable only for Plane systems and not for Linear Byte systems. This is because all the processing functions are designed to manipulate pixel data with one bit sourced from each plane. For example, the color compare function allows four bits across four planes (one pixel) to be compared to a pre-defined color, thereby allowing eight pixels to be color-compared simultaneously by processing 32 bits of video data (one byte from each plane).

## Attribute Controller (ATC)

The internal Attribute Controller (ATC) provides flexible high-speed video shifting and attribute processing, designed for both text and graphics video display applications. The ATC can process up to 16-bits of display data at the rate of 45MHz or 8-bit display data at a rate of 84MHz. In graphics modes, memory bits are reformatted into pixel color data in groups of 16, 8, 2, or 1 adjacent bits, translated through an internal 16-element color look-up table, and sent out serially to the video display. Through this pixel mapper, the ATC supports "PLANE" (for 16 colors), "BYTE" (256 colors) and "WORD" (65,536 colors) oriented pixel structures.

In text mode, eight bits of character code data and eight bits of attribute data are loaded; the character code is used as a lookup into a font table that is then loaded as the 16 bits of font data. The attribute is then applied to the font/cursor data, translated through the color lookup table, and sent out serially to produce 16 colors of text data at speeds of up to 56MHz.

In high resolution modes, the SRC⟨0⟩ bit in the ATC auxiliary register will, when set to 1, process the pixel at half the MCLK rate internally and provide the full pixel clock (PCLK) at the same rate as MCLK. The high-resolution modes should be used when the desired PCLK is greater than 45MHz. Refer to the ET4000's BIOS mode tables starting in section 3.2.4.



## 2.1.2 Support Logic

*Display Memory*

In the basic configuration, 256KB of memory is needed as the display buffer. To support IBM-compatible 16-color graphics, a Plane system is employed where the 256KB of display buffer can be viewed as four simultaneously addressable bit planes of 64KB each. (See section 3.2.2 Two Major Types of System Configurations, for definitions of system configurations.) Each pixel is represented by four bits from the four planes, selecting up to 16 colors. To support 256 colors, a Linear Byte system is employed whereby the memory are mapped as a linear byte-oriented memory of 256K in depth. Each pixel is represented by one single byte, selecting up to 256 colors. Note that, in a linear byte system, the physical addressing space is four times greater than in the plane system. There is a memory Segment Select Register to provide all addressable points.

In summary, the memory interface consists of:
- 2 RAS (RASAL, RASBL), 4 CAS (CASL⟨3:0⟩)
- 2 Memory output transfer (DTEBL, DTEAL)
- 2 Memory output enable (SOEBL, SOEAL)*
- 2 Serial clock control (SCC)
- 2 Memory write (MWBL, MWAL)
- 32-bit memory data bus (MD⟨31:0⟩)
- 18-bit memory multiplexed address bus (AB⟨8:0⟩ and AA⟨8:0⟩)

* Derived from CAS⟨3:2⟩

On reading, an 18-bit address is used to access each of the 1024KB deep memory, with up to 32 bits read from memory. On writing, any one of four memory planes from either bank can be written by proper control of RASBL, RASAL, CASL⟨3:0⟩ and MWBL/MWAL lines.

*Host Interfaces*

Address buffers are needed to multiplex the host processor's lower 16-bit address, A⟨15:0⟩, so that they can be time-multiplexed over the 16-bit address/data bus (DB⟨15:0⟩) into the ET4000 chip. The address input enable signal (ADREL) is generated by the ET4000 to enable the 16-bit addresses onto ET4000's DB⟨15:0⟩ bi-directional data bus at the beginning of each memory or I/O operation.

Two bi-directional bus transceivers (LS245) are required to interface the upper DB⟨15:8⟩ and lower DB⟨7:0⟩ data bus from the host processor. Three separate control signals, RDMHL, RDMLL, and DIR, are provided to enable the transceivers and determine their direction, respectively.



*Master Clock Select*

A variable Master Clock (MCLK) (14-65MHz), is used internally by the ET4000 to derive the video, vertical, and horizontal timing for the various video modes. Depending on the video monitor and display timing desired, up to eight different frequencies can be selected using an external multiplexer as shown in Fig. 2.1-1. The clock source is controlled by clock select signals (CS⟨2:0⟩) generated by the ET4000 as programmed. (See also section 4.3, CRTC Indexed Register 34: 6845 Compatibility Control Register.)

*System Clock Select*

The System Clock (SCLK) is required to sequence the ET4000's internal control logic. In addition, the SCLK is used to produce the memory interface control timing: RAS, CAS and MW etc.

The SCLK also affects the overall "balance" of the ET4000's performance. Therefore, designers must fully understand the effect of SCLK when cost/performance trade-offs are considered. In general, the SCLK's cycle time should be equal to the CAS low pulse width and less than 25ns. (See also section 4.3, CRTC Indexed Register 32: RAS/CAS Configuration.)

*External Color Look-up DAC*

An external Palette RAM with Digital-to-Analog Converter (DAC) is used to translate 8- or 16 bits of digital video signal into the three Analog outputs (R, G, B).

For complete Palette RAM interface, the following output pins are available from the ET4000:

PMERL, PMEWL, PCLK, MBSL, SI, SR, SG, SB, PI, PR, PG, PB

### 2.1.3 ET4000 BIOS ROM

The ET4000 BIOS ROM contains modules that provide generic video BIOS functions to support both VGA- and EGA-compatible modes. (See section 3.2.4 for operation modes.) When the BIOS ROM option is employed, the CPU reads the BIOS ROM during the bootstrap operation, and the ROM Enable signal (ROMEL) will be activated to enable the ROM data onto the DB bus, with the DIR signal driven high to allow the ROM data to be read by the host processor.



## 2.2 Board-level Design Considerations

The following are some additional notes for board-level designs using the ET4000.

### 2.2.1 Display Support and Video Timing

VGA-compatible video subsystems are used as an example here to discuss display support and video timing for an ET4000-based video design. The VGA-compatible video subsystem supports attachment of 31.5kHz horizontal sweep frequency direct-drive analog displays. These displays have a vertical sweep frequency capability of 50 to 70 cycles per second, providing extended color and sharpness and reduced flicker in most modes. The following table summarizes the VGA-compatible analog display and high-resolution interlaced monitor characteristics.

| Parameter | Color | Monochrome | HiRes Color (Interlaced) |
|---|---|---|---|
| Horizontal Scan Rate | 31.5kHz | 31.5kHz | 35.5kHz |
| Vertical Scan Rate | 50 to 70 Hz | 50 to 70 Hz | 43.5 Hz |
| Video Bandwidth | 28MHz | 28MHz | 44.9MHz |
| Displayable Colors* | 256/256K Max. | 64/64 Shades Gray | 256/256K Max. |
| Max. Horiz. Resolution | 720 PELs | 720 PELs | 1024 PELs |
| Max. Vert. Resolution | 480 PELs | 480 PELs | 768 PELs |

* Controlled by Video Circuit

All IBM-compatible VGA/EGA modes have the same horizontal sweep rate. The vertical height of the display is controlled by the polarity of the vertical and horizontal pulses. This is done so that 350, 400, or 480 lines can be displayed without adjusting the height of the display.

The BIOS sets the ET4000 registers to generate the video modes. The video modes are shown in tables 1.1-1 and 1.1-2. All of these modes are 70 Hz vertical retrace except for modes 11 and 12. These two modes are 60 Hz vertical retrace. The ET4000 generates timings that are within the specifications for the supported displays using these modes.

The VGA-compatible analog displays operate from 50 to 70 Hz vertical retrace frequency. The following timing diagrams represent only the vertical frequencies set by the BIOS.



| VSYNC Polarity | HSYNC Polarity | Vertical Size |
|---|---|---|
| + | + | 768 lines |
| + | - | 400 lines |
| - | + | 350 lines |
| - | - | 480 lines |

| Signal Time | Typical |
|---|---|
| 1 | 2.765 milliseconds |
| 2 | 11.504 milliseconds |
| 3 | 0.985 milliseconds |
| 4 | 14.268 milliseconds |
| 5 | 0.064 milliseconds |



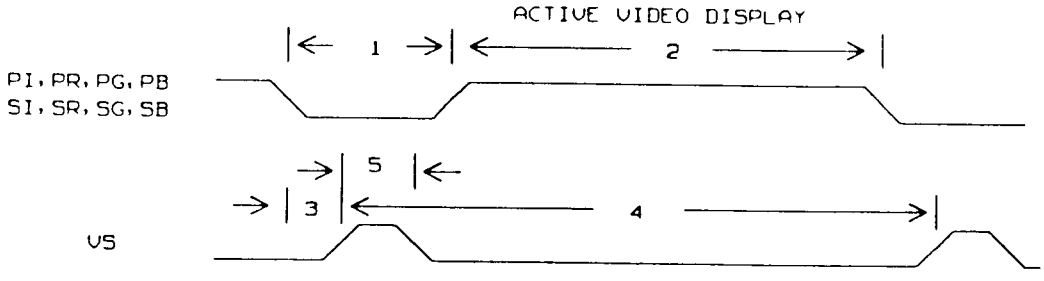



FIG. 2.2.1-1 DISPLAY VERTICAL SYNC, 350 LINES

| Signal Time | Typical |
|---|---|
| 6 | 1.112 milliseconds |
| 7 | 13.156 milliseconds |
| 8 | 0.159 milliseconds |
| 9 | 14.268 milliseconds |
| 10 | 0.064 milliseconds |



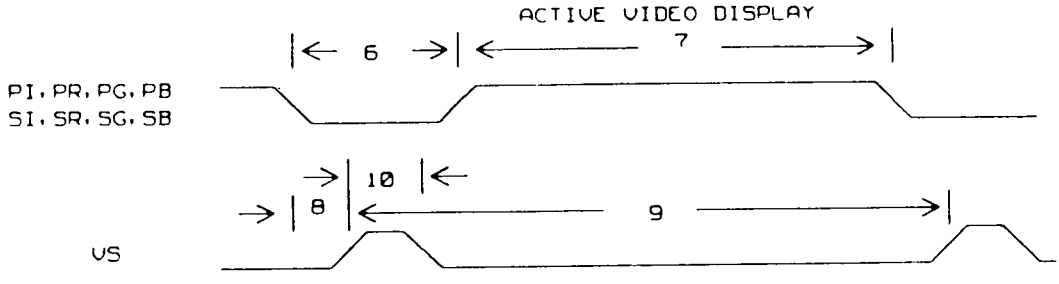



FIG. 2.2.1-2 DISPLAY VERTICAL SYNC, 400 LINES

| Signal Time | Typical |
|---|---|
| 11 | 0.922 milliseconds |
| 12 | 15.762 milliseconds |
| 13 | 0.064 milliseconds |
| 14 | 16.683 milliseconds |
| 15 | 0.064 milliseconds |



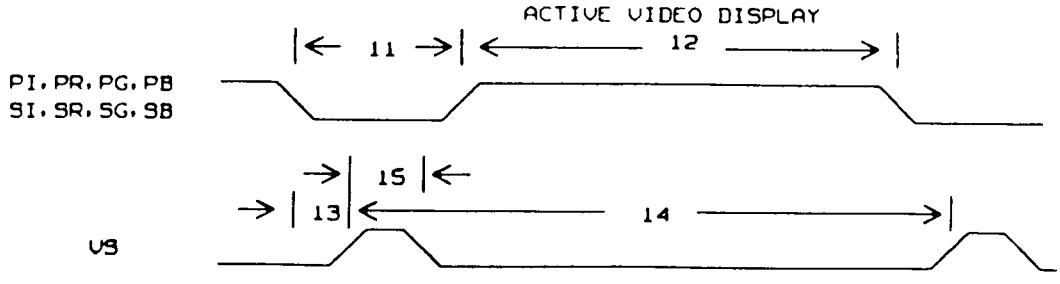



FIG. 2.2.1-3 DISPLAY VERTICAL SYNC, 480 LINES

| Signal Time | Typical |
|---|---|
| 16 | 5.720 microseconds |
| 17 | 26.058 microseconds |
| 18 | 0.318 microseconds |
| 19 | 3.813 microseconds |
| 20 | 1.589 microseconds |
| 21 | 31.778 microseconds |



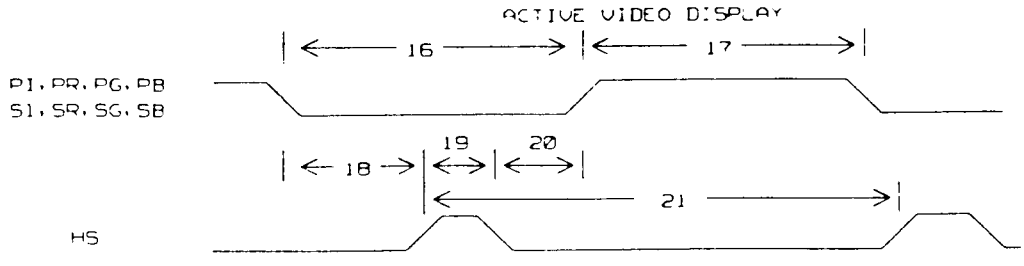



FIG. 2.2.1-4 DISPLAY HORIZONTAL TIMING, 80 COLUMN WITH BORDER

| Signal Time | Typical |
|---|---|
| 22 | 6.356 microseconds |
| 23 | 25.422 microseconds |
| 24 | 0.636 microseconds |
| 25 | 3.813 microseconds |
| 26 | 1.907 microseconds |
| 27 | 31.778 microseconds |



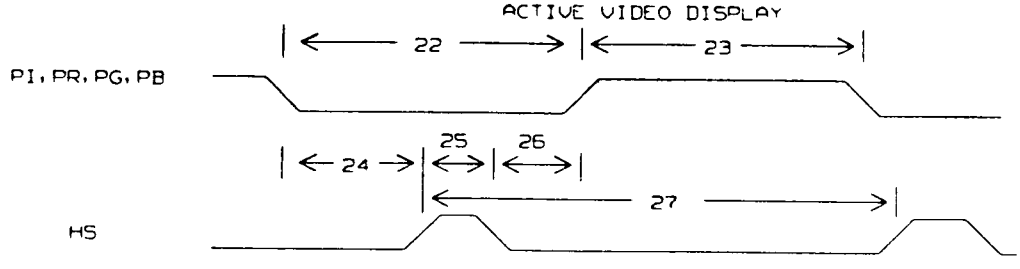



FIG. 2.2.1-5 DISPLAY HORIZONTAL TIMING, 40/80 COLUMN, NO BORDER

| Signal Time | Typical |
|---|---|
| 28 | 1.38 microseconds |
| 29 | 21.62 microseconds |
| 30 | 0.014 microseconds |
| 31 | 23.0 microseconds |
| 32 | 0.112 microseconds |



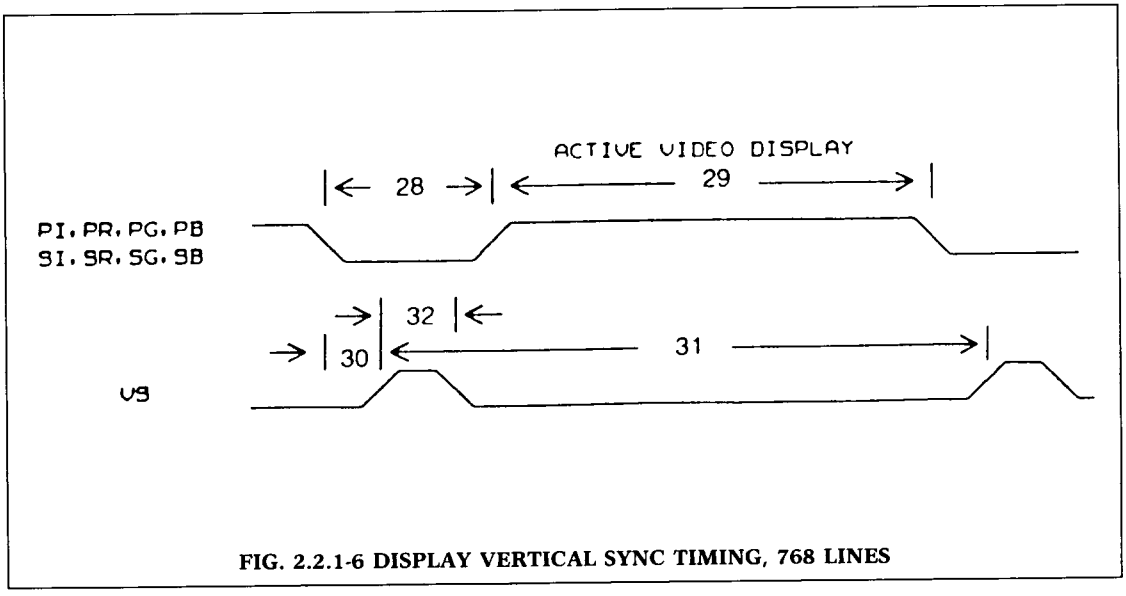



FIG. 2.2.1-6 DISPLAY VERTICAL SYNC TIMING, 768 LINES

## 2.2.2 Selection of Clock Frequency of MCLK

The MCLK can be selected by programming the Miscellaneous Output Register (I/O address = 3C2) bits (3,2) = Clock select CS⟨1,0⟩ (Refer to Fig. 2.1-1). The recommended hardware connection, and programming of the CS⟨1,0⟩ bits are shown below:

| Clock Inputs | Selected By | Type |
|---|---|---|
| CK1 = 25.175MHz | CS⟨1,0⟩ = 00 | VGA mode |
| CK2 = 28.322MHz* | = 01 | VGA mode/CGA* |
| CK3 = 32.514MHz | = 10 | EGA* mode |
| CK4 = 40.0MHz | = 11 | Extended mode |

* Use MCLK/2 internally to yield half MCLK.

The ET4000 provides one additional clock select CS⟨2⟩ for up to eight clock sources; CRTC Indexed Register 34 Bit 1, clock select CS⟨2⟩, when used in conjunction with CS⟨1:0⟩.

## 2.2.3 Memory Design Considerations

*Memory type considerations:*

ET4000 supports the following memory type and sizes:

| | Size | Min. # | Max. # | Total Size (Max) |
|---|---|---|---|---|
| DRAM | 64K x 4 | 2* | 8 | 256K x 8 |
| DRAM | 256K x 4 | 2 | 8 | 1024K x 8 |
| VRAM | 256K x 4 | 2 | 8 | 1024K x 8 |

* supports CGA/MDA/HERC modes only

During the power-up sequence, the BIOS determines the memory type and number of available memory devices: (assuming SCLK = 40MHz)

## Memory Width/Depth Determination

```
testmem(p) /* return 1 if there is display memory *p, else 0 */
char far *p;
{       int i:
  for (i=0; i<=40); i=i+8)p[i]=0x55;          /* write extra locations so char *p */
  if (*p!=0x55) return (0);                   /* will no longer be in cache */
  for (i=0; i<=40; i=i+8)p[i]=0xAA;
  if (*p!=0xAA) return (0);
  return (1);
}

  char far *fp=0xA000000L;                    /*A000:0000 */
  int memory__config;

start:
  /* set to linear graphics mode */

  outp(0x3C4,2);outp(0x3C5,0xF);              /* TS 2: enable all planes */
  outp(0x3C4,4);outp(0x3C5,0xC);              /* TS 4: chain 4, not odd/even */
  outp(0x3CE,1);outp(0x3CF,0);                /* GDC 1: no set/reset */
  outp(0x3CE,3);outp(0x3CF,0);                /* GDC 3: no rotate/func */

  outp(0x3CE,5);outp(0x3CF,0x40)              /* GDC 5 write/read mode 0 */

  outp(0x3CE,6);outp(0x3CF,5)                 /* GDC 6 memory map=A0000h for
                                              64K, graphics mode */
  outp(0x3CE,8);outp(0x3CF,OxFF);             /* GDC 8; bitmask=all bits */
  outp(0x3CD,0);                              /* select segment 0 */

  /* determine memory width here */
  /* assume the KEY is on ! */
  outp(0x3D4,0x37);                           /* CRTC VSCONF2 */
  outp(0x3D5,3);                              /* assume 32-bit */
  if (testmem (fp+3)) memory__config=3;
                                              /* test if memory in I plane (offset 3) */
  else {
    outp(0x3D4,0x37);                         /* CRTC VSCONF2 */
    outp(0x3D5,2);                            /* assume 16-bit */
    if (testmem (fp+3)) memory__config=2;
                                              /* test if memory in I plane (offset 3) */
```

```
    else {
      outp(0x3D4,0x37);                    /* CRTC VSCONF2 */
      outp(0x3D5,1);                       /* assume 8-bit */
      if (testmem (fp+3)) memory_config=1;
      else error("Minimum 8-bit of memory not found");
      }
  }
/* all width has been set, and determine memory depth here */
switch (memory_config) {
  case 1 :                                 /* 8-bit */
    outp(0x3CD,0x22);                      /* read/write segment 2,
                                              @128K boundry */
    break;
  case 2 :                                 /* 16-bit */
    outp(0x3CD,0x44);                      /* read/write segment 4,
                                              @256 boundry */
    break;
  case 3 :                                 /* 32-bit */
    outp(0x3CD,0x88);                      /* read/write segment 8,
                                              @512K boundary */
    break;
  }
if (testmem (fp))memory_config |= 8;       /* Set to 1MB memory else set
                                              to 256K memory */

/* now set the register */
outp(0x3D4,0x37);
outp(0x3D5,memory_config);
```

## Memory Type Programming

```
outp(0x3D4,0x32);                          /* CRTC RCCONF */
outp(0x3D5,0x70);                          /* use -10 memory */

/* some examples of memory timing: refer to Figure 2.3.2-2
 * 0x70: Trcd=75ns,Trsw=100ns,Trsp=75ns,Tcsw=25/50ns,Trc=200ns
 * 0x28: Trcd=75ns,Trsw=100ns,Trsp=75ns,Tcsw=25ns,Trc=175ns
 * 0x09: Trcd=50ns,Trsw=100ns,Trsp=75ns,Tcsw=50ns,Trc=175ns
 */
```

*Memory resource considerations:*

Depending on the intended modes of operations and operating clock frequencies, memory devices of different access times may be employed for the display buffer. The system clock (SCLK) is used to derive all display memory related timings.

The display memory in conjunction with the ET4000's Memory Control Unit (MCU) provide the supply side of system resources within a video subsystem. These resources consist of the number of display memory's I/O pins connected to the ET4000's DM(31:0) bus; the speed of the memory, including both the random access RAS cycle and the page mode CAS cycle; and whether DRAM or VRAM is being used.



The ET4000 supports up to eight 256K x 4 or 64K x 4 display memory devices. The total resource is represented in bit/ns. Consider the following:

SCLK = 40MHz and, 8 256K x 4 DRAM with RAS cycle time of 175ns and CAS cycle time of 50ns

Resource maximum = (8 x 4) bit/50ns or .64 bit/ns
Resource minimum = (8 x 4) bit/175ns or .183 bit/ns
Resource under ET4000's SPC controller with resource management efficiency of K = .85, then the resource of the ET4000 is approximately:

Resource ET4000 = .85((.64 x 14) + (.183 x 2)) /16 bit/ns or .495 bit/ns

**NOTE:** It is advisable to always keep the Tcas and Tcsp to 1 SCLK clock period.

Consider next, the system demands, taken in two parts: First the display requirements and then the CPU requirements.

*Display requirements:*

PCLK = 65MHz
Resolution = 1024 x 768
Color = 256
Display to scan line ratio = .8

then:
Demand disp = 8 x .8 bit x 65MHz or .416 bit/ns

therefore: the available resource Ra to CPU is the difference between Resource ET4000 and Demand disp:

Ra = (.495 -.416) bit/ns or .079 bit/ns

*CPU requirements:*

Using the above conditions, with the CPU performing a 16-bit write to display memory at a rate of one access every 200ns, the ET4000 is likely to keep up with CPU's demand with zero wait state. Furthermore, the designer should consider the proper memory resource requirements for the worse case display mode, with reasonable CPU performance.



Another important aspect of the memory design, from a reliability viewpoint, is that it is possible to reconfigure the video memory to fulfill minimum requirements via the BIOS when some memory defect occurs.

## 2.2.4 Extending BIOS ROM Address Space

The ET4000 is designed to decode C0000-C5FFF; C6800-C7FFF (hex) as the EROM address space on power-up, providing 30KB code size for the ET4000 BIOS ROM modules. This address space can be redefined to a full 32KB by programming TS Index Register 7 (TS Auxiliary Register) bits 5 and 3.

If the BIOS ROM is part of the main "motherboard" BIOS, then bits 5 and 3 of TS Indexed Register 7: Auxiliary Mode should be set to 0,1, thus disabling the decoding of ROM BIOS address space.

## 2.2.5 Translation of CRTC Index Registers and Clock Frequency

In order to support various video modes on a variety of monitors, the CRTC data registers and the Miscellaneous Output register need to be programmed accordingly to provide proper timing for the display. The ET4000 is designed to provide such adjustments via the hardware. The mechanism of translating the CRTC registers and Miscellaneous Output register is described in the following pages.

### Translation of CRTC data registers

Two alternatives are provided to allow the CRTC registers to be re-programmed to the desired values: (1) use of external translation ROM, (2) use of Non-Maskable Interrupt (NMI). These two approaches are further described as follows:

Use of Translation ROM:

*Hardware configuration* - (refer to board schematic, Figs. 2.1-1; 2.1-1a)

- ET4000 output pin "XROML" (active low) shall be used to enable both the read/write translation ROMs.
- ET4000 data bus bits 14 to 8 (BDB⟨14:8⟩) and the lower byte of the CPU data bus (DB⟨7:0⟩) (total of 15 bits) shall be used to address 32K bytes of write translation ROM
- ET4000 data bus bits 14 to 8 (BDB⟨14:8⟩) and the lower byte of the ET4000 data bus (BDB⟨7:0⟩) (total of 15 bits) shall be used to address 32K bytes of read translation ROM
- 8-bit data output of the write translation ROM shall be fed back to source the lower 8 bits of ET4000 data bus (BDB⟨7:0⟩)
- 8-bit data output of read translation ROM shall be fed back to source the lower 8 bits of the CPU data bus (DB⟨7:0⟩)
- The DIR output from the ET4000 should be used to enable the write translation ROM
- The DIR output from the ET4000 with logical inversion should be used to enable the read translation ROM



*Programming requirements* -

- 6845 Compatibility Control Register (CRTC Index 34) bit 5 = 1, to enable write translation mode
- 6845 Compatibility Control Register (CRTC Index 34) bit 4 = 1, to enable read translation mode
- Video System Configuration Register (CRTC Index 36) bit 7 = 0, to disable 16-bit I/O operation
- Feature Control Register (Port 3#A) bit 7 = 0 or not in 6845 mode

*Theory of operation* -

After the above programming, translation via use of read/write translation ROM is enabled:

In EGA/VGA modes:

Any I/O read/writes to the CRTC Index registers 0—1F, (port address = 3#5) will cause translation to occur as follows:

-BDB⟨15:8⟩ will be sourced by ET4000 (during XROML active) as follows:

BDB⟨15⟩ = TS Index 7 bit 7
BDB⟨14⟩ = CRTC Index 34 bit 7 (complemented)
BDB⟨13⟩ = Misc. Output Register bit 2
BDB⟨12:8⟩ = CRTC Index value to be written

-The translation ROM enabled by XROML goes from 1 to 0, BDB⟨15:8⟩ (sourced from ET4000) and DB⟨7:0⟩ (sourced from CPU) will address the translation ROM for the desired value to be written to the CRTC index register. See Fig. 2.2.5-1.

Similarly, an I/O write to the Miscellaneous Output register (port address 3C2) will cause the ET4000 to activate XROML and source BDB⟨15:8⟩, with the exception that BDB⟨12:8⟩ will be sourced as "11010", to access a desired value for the Miscellaneous Output register (MISCOUT).

Note that the CS⟨0⟩ bit (contained in the MISCOUT register) is also an address input to the translation ROM. The MISCOUT register should be set prior to setting the CRTC values in order to select the proper EGA-to-PS/2 translation table (see Figure 2.2.5-1). Since the table to be used is unknown when the MISCOUT register is set, identical values should be in both tables at index 1A (from which the MISCOUT register is translated).

The translation of the MISCOUT allows the clock select bits (bits 2,3) and horizontal and vertical sync polarity bits (bits 6,7) to be properly adjusted.

In CGA modes:

Any I/O writes to CRTC Index registers 0—F will cause the above translation to occur, allowing the 16 CRTC registers to be automatically adjusted.
Note that BDB⟨12⟩ = CRTC Index Register 24 bit 0.

Use of Non-Maskable interrupt:

*Hardware configuration* -

- Output pin XROML shall be connected to the NMI input to the processor, which is a tri-state output that will go active low, to generate NMI when CPU writes to CGA/MDA mode register (3#8)

*Programming requirements* -

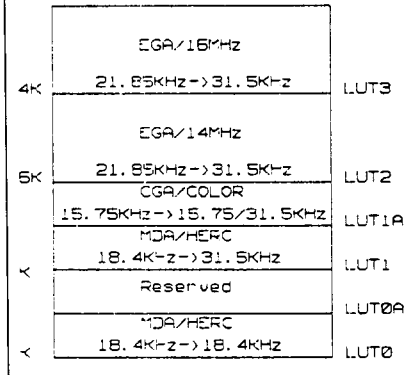
- 6845 Compatibility Control Register (CRTC Index 34) bit 7 = 1, to enable 6845 emulation
- 6845 Compatibility Control Register (CRTC Index 34) bit 5 = 0, to disable translation mode
- Feature Control Register (Port 3#A) bit 7 = 1, to enable generation of NMI

*Theory of operation -*

After the above programming, a NMI to the processor is enabled:

A mode switching (writing to the 6845 MODE register) will generate an NMI active low pulse to the processor, allowing all the CRTC index registers to be re-programmed by the interrupt service routine. Note that once the NMI is invoked, CRTC Index 0 - 9 will be write protected.






```
case A: EGA -> PS/2 analog monitor:
          Translate ROM mapping = LUT2 or 3
          Index 34= 2I or 21

case B: CGA -> PS/2 analog monitor:
          Translate ROM = LUT1A
          Set I/O port 03DE=01 (double scan)
          Select MCLK = 28 MHz
          Set bit 7 & 6 of Miscellaneous Output Reg = 0 1
          Index 34= E1

case C: CGA -> CGA/EGA  monitor:
          Translate ROM = LUT1A
          Select MCLK = 28/2 (14MHz)
          Set bit 7 & 6 of Miscellaneous Output Reg = 0 0
          Index 34= A1

case D: MDA/HERC -> PS/2 analog monitor:
          Translate ROM = LUT1
          Select MCLK = 28 MHz (MISCRW bit 2 = 1)
          Set bit 7 & 6 of Miscellaneous Output Reg = 1 0
          Index 34= A0

case E: MDA/HERC -> TTL monochrome monitor:
          Translate ROM = LUT0
          Select MCLK = 16 MHz (MISCRW bit 2 = 0)
          Set bit 7 & 6 of Miscellaneous Output Reg = 1 0
          Index 34= A0
```

**FIG. 2.2.5-1 TRANSLATION ROM**

## 2.2.6 16-bit Data Bus Interface

*Programming requirements -*

- Video System configuration Register (CRTC Index 36) bit 6 = 1, to enable 16-bit display memory access.
- Video System configuration Register (CRTC Index 36) bit 7 = 1, to enable 16-bit I/O access.



To support this 8-bit/16-bit interface, the hardware configuration is shown as in the board schematic (See Figures 2.1-1, 2.1-1a). The signals "SBHEL" and "A⟨0⟩" are inputs to the ET4000 to identify whether an 8-bit/16-bit read/write operation is intended. The ET4000 will respond to 16-bit bus operation via the CS16L/IO16L output pins. In the case of 16-bit I/O access, the leading edge of IOWWL input must ensure proper data set-up time as specified.

## 2.3 I/O Pin Description

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| **Clock Interface** | | | | | |
| MCLK | 17 | 18 | I | TTL | A variable frequency clock used to generate the necessary video, vertical and horizontal timing for the ET4000. Various video clocks can be selected as the proper clock frequency, by the output clock select signals CS⟨2:0⟩ from ET4000 depending on the display mode programmed by the host processor. |
| SCLK | 20 | 23 | I | TTL | System clock used to generate all memory timing and ET4000's internal states. |
| **General Host Interface** | | | | | |
| CDMWL | 29 | 33 | I | CMOS Schmitt-Trigger | PC: A low active memory write request generated by a host microprocessor, to write into the Display Memory.<br>MC:Command, a low activate command input for read/write cycle. |
| ADMRL | 28 | 32 | I | CMOS Schmitt-Trigger | PC: A low active memory read request generated by a host microprocessor, to read the Display Memory or BIOS ROM.<br>MC:Address/Status latch control input. |
| MIOWL | 27 | 31 | I | CMOS Schmitt-Trigger | PC: A low active I/O write request generated by a host microprocessor, to write to the ET4000 control registers.<br>MC:Memory/Input Output, when this signal is high,it indicates a memory cycle. A low indicates an I/O cycle. |

## 2.3 I/O Pin Description (continued)



| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| CIORL | 26 | 29 | I | CMOS Schmitt-Trigger | PC: A low active I/O read request generated by a host microprocessor, to read the ET4000 control registers.<br>MC:Card Setup input driven by system board. |
| IOWWL | 15 | 16 | I | TTL | PC: A low active I/O write request derived from IOW command.<br>MC:A low active I/O write request derived from CMD command.<br>**NOTE:** This input is used only if: 16-bit I/O is enabled and the DB⟨15:0⟩ set-up time to IOW (PC bus) or CMD (MC bus) command is less than the specified timing requirement. Otherwise, this input can be terminated with a logical 0. |
| A⟨23:16⟩ | 44,43, 42,41, 40,39, 38,37 | 48,47, 46,45, 44,43, 42,41 | I | TTL | Upper 8 bit address bus interfaced to an external host microprocessor. |
| M24 | 36 | 40 | I | TTL | Extended address enable. This line must be driven active high during all memory accesses. |

## 2.3 I/O Pin Description (continued)

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| DB⟨7:0⟩ | 53,52, 51,50, 49,48, 47,46 | 58,57, 56,55, 54,53, 52,51 | I/O | TTL/TS | Data bus, 8-bit address/data time multiplexed bus, interfaced to an external host microprocessor. INPUTS lower 8-bit processor address, 8-bit lower data (memory or I/O writes) or OUTPUTS lower 8-bit data (memory or I/O reads) for memory or I/O operations initiated by host processor. During power-up RESET low to high transition, state of DB⟨7:0⟩ are latched internally. For micro channel interface, these 8-bit latched data are channel ID. Additionally, the bit 0 and 1 of latched data are available to be read back via Status Register Zero for the monitor ID. |
| DB⟨15:8⟩ | 64,62, 61,60, 59,58, 57,56 | 72,69, 68,67, 66,65, 64,63 | I/O | TTL/TS | Data bus, 8-bit address/datatime multiplexed bus, interfaced to an external host microprocessor. INPUTS middle 8-bit processor address, 8-bit upper data (memory or I/O writes) or OUTPUTS upper 8-bit data (memory or I/O reads) for memory or I/O operations initiated by host processor. |
| WAITL | 31 | 35 | O | TTL/TS | A low active signal generated to asynchronously stretch the host microprocessor during memory read/write and I/O (in micro channel) operations. |
| ADREL | 68 | 76 | O | TTL | Low active enable signal, enables the lower 16-bit processor address signals for the DB⟨15:0⟩ inputs. |
| RDMHL | 67 | 75 | O | TTL | A low active signal, used to enable upper 8-bit of external bi-directional bus drivers connecting the Data Bus (DB⟨15:8⟩) to the data bus of the host microprocessor. |

## 2.3 I/O Pin Description (continued)



| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| RDMLL | 66 | 74 | O | TTL | A low active signal, used to enable lower 8-bit of external bi-directional bus drivers connecting the Data Bus (DB⟨7:0⟩) to the data bus of the host microprocessor. |
| DIR | 65 | 73 | O | TTL | A signal used to control the direction of bidirectional drivers connecting the Data Bus (DB⟨15:0⟩) to the data bus of the host microprocessor. A logical 1 will be generated during memory and I/O reads to allow the ET4000 to drive the data bus. A logical 0 will be generated during write operations, allowing the ET4000 to receive data from the host. |
| CS16L | 35 | 39 | O | TS | This is the -CD DS16 (n) signal for identifying a 16-bit memory device on the PC/MC microprocessor bus and I/O device on the MC microprocessor bus. This signal shall be high impedance for 8-bit data transfers, and low for 16-bit data transfers. This signal should be pulled high using a 1K resistor in microchannel applications to conform to Micro Channel specifications. |
| IO16L | 34 | 38 | O | TS | This is the -CD IO16 (n) signal for identifying a 16-bit I/O device on the PC microprocessor bus. This signal shall be high impedance for 8-bit data transfers, and low for 16-bit data transfers. |
| REST | 32 | 36 | I | TTL | High active system reset signal generated by the host processor to reset the ET4000's internal registers. |

## 2.3 I/O Pin Description (continued)

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| AENL | 30 | 34 | I | TTL | Low active I/O address valid enable signal. |
| SBHEL | 33 | 37 | I | TTL | An input signal to the ET4000 which, along with A⟨0⟩, identify whether an 8- or 16-bit read/write operation is intended. |
| SFDBL | 87 | 96 | O | TTL | Card Select Feedback, active low output to indicate to micro channel host the availability of ET4000's Memory and I/O resources.<br>PC Mode: 16-bit Memory Access Enable. This signal can be used to generate early CS16 if required in certain high-speed motherboard designs. |
| S⟨1:0⟩ | 23,24 | 26,27 | I | TTL | Status bit 1 and 0: These lines defines the current cycle is read or write.<br>**NOTE:** In PC bus configuration, these lines should be terminated to logical 0. |
| **DRAM/VRAM Memory Interface** | | | | | |
| RASAL | 121 | 134 | O | TTL/TS | DRAM: Row address AA⟨8:0⟩ latch control for lower memory plane pairs MD⟨15:0⟩.<br>VRAM: Row address AB⟨8:0⟩latch for first 512KB memory bank A.<br>**NOTE:** AA⟨8:0⟩ is not used in VRAM configuration. |
| RASBL | 120 | 133 | O | TTL/TS | DRAM: Row address AB⟨8:0⟩ latch control for upper memory plane pairs MD⟨31:16⟩.<br>VRAM: Row address AB⟨8:0⟩ latch for first 512KB memory bank B. |

## 2.3 I/O Pin Description (continued)

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| CASL⟨0⟩ | 125 | 138 | O | TTL/TS | DRAM: Column address AA⟨8:0⟩ latch control for lower plane MD⟨7:0⟩.<br>VRAM: Column address AB⟨8:0⟩ latch control for lower 8-bit memory plane MD⟨7:0⟩. |
| CASL⟨1⟩ | 124 | 137 | O | TTL/TS | DRAM: Column address AA⟨8:0⟩ latch control for lower plane MD⟨15:8⟩.<br>VRAM: Column address AB⟨8:0⟩ latch control for upper 8-bit memory plane MD⟨15:8⟩. |
| CASL⟨2⟩ | 123 | 136 | O | TTL/TS | DRAM: Column address AB⟨8:0⟩ latch control for upper plane pair MD⟨23:16⟩.<br>VRAM: Serial output enable for first 512KB memory bank A. |
| CASL⟨3⟩ | 122 | 135 | O | TTL/TS | DRAM: Column address AB⟨8:0⟩ latch control for upper plane pairs MD⟨31:24⟩.<br>VRAM: Serial output enable for second 512KB memory bank B. |
| MWAL | 11 | 12 | O | TTL/TS | Write Command to display memory.<br>DRAM: write control for lower memory planes MD⟨15:0⟩.<br>VRAM: write control for first 512KB memory bank A. |
| MWBL | 107 | 119 | O | TTL/TS | Write Command to display memory.<br>DRAM: write control for upper memory planes MD⟨31:24⟩.<br>VRAM: write control for second 512KB memory bank B. |
| DTEAL | 12 | 13 | O | TTL/TS | VRAM: Low active output enable signal, used to enable VRAM memory access to first 512KB memory bank A, comprised of four 256Kx4 memory devices.<br>DRAM: DRAM's OE input pin to enable the output data bus during a read operation (AA<8:0>). |

## 2.3 I/O Pin Description (continued)

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| DTEBL | 109 | 121 | O | TTL/TS | VRAM: Low Active Output Enable signal, used to enable VRAM memory access to second 512KB memory bank B, comprised of four 256Kx4 memory devices.<br>DRAM: DRAM's OE input pin to enable the output data bus during a read operation (AB⟨8:0⟩). |
| MD⟨7:0⟩ | 137,138, 139,140, 141,142, 143,144 | 153,154, 155,156, 157,158, 159,160 | I/O | TTL/TS | DRAM: Memory Data Bus bit 7-0.<br>VRAM: Memory Data Bus bit 7-0. |
| MD⟨15:8⟩ | 128,129, 130,131, 132,133, 134,136 | 143,144, 145,146, 147,148, 149,152 | I/O | TTL/TS | DRAM: Memory Data Bus bit 15-8.<br>VRAM: Memory Data Bus bit 15-8. |
| MD⟨23:16⟩ | 99,100, 101,102, 103,104, 105,106 | 111,112, 113,114, 115,116, 117,118 | I/O | TTL/TS | DRAM: Memory Data Bus bit 23-16.<br>VRAM: Serial Data Bus bit 7-0. |
| MD⟨31:24⟩ | 89,92, 93,94, 95,96, 97,98 | 98,103, 104,105, 106,107, 108,109 | I/O | TTL/TS | DRAM: Memory Data Bus bit 31-24.<br>VRAM: Serial Data Bus bit 15-8. |
| AA⟨8:0⟩ | 2,3, 4,5, 6,7, 8,9, 10 | 2,3, 4,5, 6,7, 8,9, 11 | O | TTL/TS | DRAM: Row/Column address time multiplexed bus addressing memory plane pairs MD⟨15:0⟩.<br>**NOTE:** AA⟨8:0⟩ is only used in DRAM configuration. |
| AB⟨8:0⟩ | 110,111, 112,113, 114,115, 116,118, 119 | 122,123, 124,125, 126,127, 128,131, 132 | O | TTL/TS | DRAM: Row/Column address time multiplexed bus addressing memory plane pairs MD⟨31:16⟩.<br>VRAM: Time multiplexed row address for both 512KB memory banks A/B. |
| SCC | 1 | 1 | O | TTL/TS | DRAM: High active graphics Status output.<br>VRAM: Serial clock control. |

## 2.3 I/O Pin Description (continued)



| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| **Display Output Interface** | | | | | |
| PCLK | 82 | 91 | O | TTL/TS | Pixel clock used to load the video output signals (PI,PR,PG,PB,SI,SR,SG,SB) into the Digital to Analog Converters (DAC). The video output signals shall be loaded using the rising edge of the Pixel clock. |
| SI | 81 | 89 | O | TTL/TS | Secondary intensity, video color look-up table address bit 7. |
| SR | 80 | 88 | O | TTL/TS | Secondary red, video color look-up table address bit 6. |
| SG | 79 | 87 | O | TTL/TS | Secondary green, video color look-up table address bit 5. |
| SB | 78 | 86 | O | TTL/TS | Secondary blue, video color look-up table address bit 4. |
| PI | 77 | 85 | O | TTL/TS | Primary intensity, video color look-up table address bit 3. |
| PR | 76 | 84 | O | TTL/TS | Primary red, video color look-up table address bit 2. |
| PG | 75 | 83 | O | TTL/TS | Primary green, video color look-up table address bit 1. |
| PB | 74 | 82 | O | TTL/TS | Primary blue, video color look-up table address bit 0. |
| MBSL | 73 | 81 | O | TTL/TS | A low signal indicates that a blanking period is active. During this time, the video output lines shall be cleared. This signal shall be used in conjunction with the digital video output to external DAC to produce the required R,G,B analog output. |

## 2.3 I/O Pin Description (continued)

| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| PMERL | 72 | 80 | O | TTL/TS | Low active select for external Digital to Analog Converter (DAC) register during I/O read. |
| PMEWL | 71 | 79 | O | TTL/TS | Low active select for external Digital to Analog Converter (DAC) register during I/O write. |
| VS | 83 | 92 | O | TTL/TS | Vertical retrace synchronization signal, supplied to the CRT monitor. |
| HS | 84 | 93 | O | TTL/TS | Horizontal retrace synchronization signal, supplied to the CRT monitor. |
| **General Input Interface** | | | | | |
| UCPC | 14 | 15 | I | TTL | Bus type select input: when set to a logical 1, the ET4000 will respond to all microprocessor interfaces according to micro channel specification. When this input is set to a logical 0, the ET4000 will respond to all microprocessor interfaces according to PC bus specification. |
| SYNR | 88 | 97 | I | TTL | A active high synchronous reset signal. When this signal is high, it indicates a request to reset the ET4000's internal LINE and CHARACTER counters. |
| SWSE | 16 | 17 | I | TTL | Input status, can be read via input status 0 bit 4. |

## 2.3 I/O Pin Description (continued)



| ET4000 I/O PIN LIST AND SIGNAL DESCRIPTION | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PIN# 144-PIN PFP | PIN# 160-PIN PFP | I/O | TYPE | FUNCTION |
| **General Output Interface** | | | | | |
| ROMEL | 70 | 78 | O | TTL | Low active signal, used to enable external BIOS ROM. |
| CS⟨2:0⟩ | 13,21, 22 | 14,24, 25 | O | TTL | Clock select signal, to select 1 of 8 possible MCLK clock. |
| TKN⟨1:0⟩ | 86,85 | 95,94 | O | TTL/TS | Token Status output:<br>TKN⟨1⟩ = ET4000's MCU is processing font cycle.<br>TKN⟨0⟩ = ET4000's MCU is processing pixel cycle.<br>TKN⟨1:0⟩ are redefined if CRTC index 35 bit 5 = 1:<br>TKN⟨1⟩ = interlace mode active.<br>TKN⟨0⟩ = even field. |
| XROML | 69 | 77 | O | TTL | A low active signal. It is used to enable an external translation read/write ROMs. |
| INTL | 25 | 28 | O | TTL/TS | Low active interrupt request signal to host microprocessor. |
| **Power Source Interface** | | | | | |
| VSS | 19,45, 55,63, 91,117, 127,135 | 10,21, 22,30, 49,50, 61,62, 70,71, 90,101, 102,110, 129,130, 141,142, 150,151 | I | GND | Ground. |
| VDD | 18,54, 90,108, 126 | 19,20, 59,60, 99,100, 120,139, 140 | I | +5V | +5V. |

## ELECTRICAL SPECIFICATIONS

### MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | -40 to +125 deg C |
| Operating free-air temperature range | 0 to +70 deg C |
| Supply Voltage Applied to Ground Potential | -0.5 to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | -0.5 to Vdd max. |
| DC Input Voltage | -0.5 to +5.25 V |
| Supply Current | 70mA typ 160mA max. |



### ELECTRICAL CHARACTERISTICS

The following condition Applies Unless Otherwise Specified.

T(A) = 0 to + 70 deg C Vdd = 5.0 V +/- 5%

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE

| | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| V(OH) Output High Voltage I(OH) = 2.0 mA | 4.0 | | | Volts |
| V(OL)Output Low Voltage I(OL) = 4 mA | 0.4 | | | Volts |
| RASAL, RASBL, CASL⟨3:0⟩, PCLK, DB⟨15:0⟩, VS, HS, ADREL = 4 mA* | 0.4 | | | Volts |
| AA⟨8:0⟩, AB⟨8:0⟩, MWAL, MWBL, SCC, SFDBL, WAITL, DIR, CS16L, I016L, INTL = 6 mA* | 0.4 | | | Volts |
| All Others = 2 mA* | 0.4 | | | Volts |
| V(IH)Input High Level I(IH) = +/- 10 μA | 2.0 | | | Volts |
| V(IL)Input Low Level I(IL) = 10 μA | | | 0.8 | Volts |

*See Addendum 6.1 for ET4000AX Rev. E revised voltages

**NOTE:** Stress beyond those listed under "Maximum Ratings" may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability.

2.0

## Life Support Disclaimer

Tseng Labs, Inc. does not sanction, authorize, or certify any chip-level or board-level products for use in the design, construction, or use in or as critical components of life-support systems or devices. Products of this nature are defined as follows:

a) Life-support systems and/or devices are those which are used to support/sustain life, or are used to the same effect when applied as a surgical implant, and whose failure to perform may result in serious injury or fatality.

b) Critical components are those which are integral and essential to the design and construction of life-support devices which are used to support/sustain life, and whose failure to perform can be expected to significantly reduce the effectiveness of said devices, which may result in serious injury or fatality.

## 2.3.1 Timing Specification

Refer to timing diagrams shown in Figures 2.3.2-1 to 2.3.2-17

| Clock Interface | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 1 | c(MCLK) | MCLK Period | 11.9 | | ns |
| 2 | c(SCLK) | SCLK Period | 24.0 | | ns |
| 3 | tw(SCLKH) | SCLK High Pulse width | 11.5 | | ns |
| 4 | tw(SCLKL) | SCLK Low Pulse width | 11.5 | | ns |
| 5 | tw(MCLKH) | MCLK High pulse width | 5.5 | | ns |
| 6 | tw(MCLKL) | MCLK Low pulse width | 5.5 | | ns |
| **General Host Interface** | | | | | |
| No. | Symbol | Description | min. | max. | unit |
| 10 | tw(RESTH) | REST high pulse width | 10 | | ns |
| 11 | tw(WAITL) | Wait line low during CPU read/write display memory | 0 | (*2) | ns |
| 20 | td(ROMEL) | Delay from memory read to ROMEL Low | 5.6 | 26.0 | ns |
| 21 | td(ROMEH) | Delay from memory read to ROMEL High | 3.8 | 17.4 | ns |
| 22 | td(ADREH) | Delay from Read or Write Command to ADREL High | 5.9 | 22.8 | ns |
| 23 | td(ADREL) | Delay from Read or Write Command to ADREL Low | 3.4 | 13.0 | ns |
| 24 | td(XROML) | Delay from Read or Write Command to XROML Low | 9.0 | 42.5 | ns |
| 25 | td(XROMH) | Delay from Read or Write Command to XROML High | 6.0 | 30.2 | ns |
| 26 | td(RDMEL) | Delay from Read or Write Command to RDMHL or RDMLL Low | 6.8 | 26.4 | ns |
| 27 | td(RDMEH) | Delay from Read or Write Command to RDMHL or RDMLL High | 5.0 | 19.1 | ns |
| 28 | td(DIRH) | Delay from Read Command to DIR High | 3.3 | 16.8 | ns |
| 29 | td(DIRL) | Delay from Read Command to DIR Low | 5.5 | 24.0 | ns |
| 30 | td(IORDA) | Delay from I/O Read command to DB out | 5 | 30 | ns |

## 2.3.1 Timing Specification (continued)

| No. | Symbol | Description | min. | max. | unit |
|---|---|---|---|---|---|
| 31 | td(CSNH) | Delay from MCLK to INTL low to High-Z | 8.7 | 33.7 | ns |
| 32 | td(CSNH) | Delay from I/O Write Command to CS⟨2:0⟩ High | 4.5 | 28.5 | ns |
| 33 | td(CSNL) | Delay from I/O Write Command to CS⟨2:0⟩ Low | 4.5 | 29.5 | ns |
| 34 | td(XRDB) | Delay from XROML low to DB⟨15:8⟩ valid translation ROM address | - 5.0 | 2.5 | ns |
| 40 | ts(ADIOWW) | I/O address setup time to IOWWL | 10 | | ns |
| 41 | ts(DWRCS) | CPU Write Data set up time | 30 | | ns(*4,6) |
| 42 | ts(DRDCS) | CPU Read Data set up time | 20 | | ns(*6) |
| 43 | ts(IRDCS) | I/O Read Data set up time | 20 | | ns(*6,11) |
| 44 | ts(IWRCS) | I/O Write Data set up time | | | ns(*6,12) |
| | | 16-bit I/O write | 5 | | ns |
| | | 8-bit I/O write | 10 | | ns |
| 50 | th(IWRCH) | I/O Write Data hold time | 10 | | ns(*6) |
| 51 | th(IRDCH) | I/O Read Data hold time | 13 | 20 | ns(*6) |
| 52 | th(DWRCH) | CPU Write Data hold time | 5 | | ns(*6) |
| 53 | th(DRDCH) | CPU read Data hold time | 10 | 20 | ns(*6,11) |

**PC Bus Host Interface**

| No. | Symbol | Description | min. | max. | unit |
|---|---|---|---|---|---|
| 60 | tw(IORWL) | I/O Read or Write pulse width low | 30 | | ns(*3) |
| 61 | tw(IORWH) | I/O Read or Write pulse width high | 20 | | ns(*3) |
| 62 | tw(MEMRW) | Memory Read or Write Command pulse width low (active) | 30 | | ns(*9,10) |
| 63 | tw(MEMRW) | Memory Read or Write Command pulse width high | 20 | | ns |
| 64 | td(WAITL) | Delay from Memory Read or Write Command (ADMRL,CDMWL) to WAITL low | 6.0 | 23.4 | ns |
| 65 | td(CS16L) | Delay from host address to CS16L low | 6.4 | 24.8 | ns(*6) |
| 66 | td(IO16L) | Delay from host address to I016L | 6.0 | 24.2 | ns |
| 67 | ts(ADRIO) | Host address setup time to I/O read or write command | 10 | | ns(*6) |
| 68 | ts(ADRMIO) | Host address setup time to read or write command | 10 | | ns(*6) |
| 69 | th(MEMADR) | Host address hold time from memory read or write command | 10 | | ns(*6) |

## 2.3.1 Timing Specification (continued)

| Micro Channel Bus Host Interface | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 75 | tw(ADRLL) | ADMRL pulse width low | 10 | | ns |
| 76 | tw(ADRLH) | ADMRL pulse width high | 10 | | ns |
| 77 | tw(CDML) | Command (CDMWL) pulse width low | 30 | | ns |
| 78 | tw(CDMH) | Command (CDMWL) pulse width high | 20 | | ns |
| 79 | tw(S01H) | Status (S0,S1) pulse width high | 20 | | ns |
| 80 | td(SCDM) | Command (CDMWL) delay from status | 20 | | ns |
| 81 | td(CS16L) | CS16L delay from status (S0,S1) for I/O read or write | 5.7 | 21.8 | ns |
| 82 | td(SFDS) | SFDBK delay from status (S0,S1) | | | |
| | | a. for I/O read or write | 4.5 | 17.3 | ns |
| | | b. for display memory read or write | 6.9 | 26.5 | ns |
| 83 | td(WAITL) | WAITL delay from status (S0,S1) low | | | |
| | | a. for I/O reads and writes | 5.7 | 21.8 | ns |
| | | b. for memory reads or writes | 7.1 | 27.0 | ns |
| 90 | ts(MIOADL) | MIOWL set up time from ADMRL high | 10 | | ns |
| 91 | ts(ADRAL) | Host Address setup time to ADMRL low | 10 | | ns(*6) |
| 92 | ts(S01ADL) | S0,S1 setup time to ADMRL low | 10 | | ns |
| 93 | ts(WRCDM) | Write data setup time to CDMWL high | 10 | | ns(*6) |
| 94 | ts(SBHADL) | SBHEL setup time to ADMRL low | 10 | | ns |
| 100 | th(WRCDM) | Write data hold time from CDMWL high | 0 | | ns(*6) |
| 101 | th(S01ADL) | S0,S1 hold time from ADMRL high | 5 | | ns |
| 102 | th(ADRADL) | Host Address hold from ADMRL high | 5 | | ns(*6) |
| 103 | th(MIOADL) | MIOWL hold time from ADMRL high | 5 | | ns |
| 104 | th(SBEADL) | SBHEL hold time from ADMRL high | 5 | | ns |

## 2.3.1 Timing Specification (continued)



| DRAM/VRAM Memory Timing | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 110 | tw(RSW) | RASAL or RASBL Low pulse width | nc- 3.0 | nc- 1.5 | ns(*4,5,7) n=3-5 |
| 111 | tw(RSP) | RASAL or RASBL High pulse width | nc+ 1.7 | nc+ 2.9 | ns(*4,5,8) n=2-5 |
| 112 | tw(CSW) | CASL Low pulse width | nc- 2.9 | nc- 2.1 | ns(*4,5)n=1-2 |
| 113 | tw(CSP) | CASL High pulse width | nc+ 0.8 | nc+ 2.5 | ns(*4,5) n=1-2 |
| 114 | tw(MWL) | MWAL or MWBL Low pulse width | nc- 2.9 | nc- 1.5 | ns(*4,5) n=1-2 |
| 119 | td(CAC) | Delay from CASL to read data valid | 5.0 | c+ 5.0 | ns(*4,5) |
| 120 | td(RCD) | Delay from RASAL or RASBL to CASL | nc- 2.7 | nc+ 3.7 | ns(*4,5)n=2-3 |
| 121 | ts(MWL) | MWAL or MWBL CAS set up time | 1.0 | 2.0 | ns |
| 122 | ts(ASR) | AA, AB Address RAS set up time | c+11.5 | c+12.5 | ns(*5)(*14) |
| 123 | ts(ASC) | AA, AB Address CAS set up time | c-13.5 | c-11.0 | ns(*5)(*14) |
| 124 | ts(DS) | Memory Write Data Set up time | 4.5 | 9.5 | ns(*1)(*14) |
| 130 | th(RAH) | AA, AB Address RAS hold time | nc-12.0 | nc+5.0 | ns(*4,5) n=2-3(*13) |
| 131 | th(CAH) | AA, AB Address CAS hold time | c+5.5 | c+13.0 | ns(*5) |
| 132 | th(DH) | Memory Write Data hold time | 48.0 | 51.1 | ns(*1) |
| 133 | th(RAL) | RAS hold time from AA, AB address | nc+11.5 | nc+14.0 | ns(*4,5) n=0-1 |
| 134 | th(OFF) | Memory read Data hold time | 5 | | ns |

| VRAM Memory Timing | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 140 | tw(SC) | SCC high pulse width | hc+0.8 | hc+3.5 | ns(*5) |
| 141 | tw(SCP) | SCC low pulse width | lc-3.5 | lc-0.8 | ns(*5) |
| 142 | tw(DTEL) | DTEAL, DTEBL pulse width low | nc-0.5 | nc-3.5 | ns(*4,5) n=1-6 |
| 150 | td(SCC) | Delay From SCLK High to SCC High | 5.4 | 20.5 | ns |
| 151 | td(SCC) | Delay From SCLK Low to SCC Low | 6.2 | 24.0 | ns |
| 152 | td(TSD) | First SCC delay from DTEAL or DTEBL for read transfer cycles | c-0.3 | c-1.3 | ns(*5) |
| 153 | td(SCA) | Delay from SCC to serial data valid | 5.0 | c+5.0 | ns(*5) |
| 160 | ts(TLS) | DTEAL, DTEBL setup to RAS low | c+0.0 | c+1.0 | ns(*5) |
| 161 | th(TRD) | DTEAL, DTEBL hold to RAS high | -nc-0.0 | -nc-3.0 | ns(*4,5) n=0-1 |

| General Output Timing | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 170 | td(TKN0H) | TKN0 high delay from SCLK high | 19.7 | 47.2 | ns |
| 171 | td(TKN0L) | TKN0 low delay from SCLK high | 23.0 | 60.0 | ns |
| 172 | td(TKN1H) | TKN1 high delay from SCLK high | 18.7 | 43.7 | ns |
| 173 | td(TKN1L) | TKN1 low delay from SCLK high | 7.9 | 30.8 | ns |
| 174 | td(PMEL) | Delay from I/O Read or Write Command to PMERL or PMEWL Low | 6.3 | 24.5 | ns |
| 175 | td(PMEH) | Delay from I/O Read or Write Command to PMERL or PMEWL High | 4.6 | 17.5 | ns |

## 2.3.1 Timing Specification (continued)

| Display Timing | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Description | min. | max. | unit |
| 180 | td(CO) | Delay from MCLK to HS, VS outputs | 5.9 | 39.6 | ns |
| 181 | td(PCLKH) | Delay from MCLK to PCLK High | | | |
| | | High Resolution Mode | 3.0 | 11.4 | ns |
| | | High Color Mode | 6.3 | 24.4 | ns |
| | | Normal Mode | 4.5 | 17.1 | ns |
| 182 | td(PCLKL) | Delay from MCLK to PCLK Low | | | |
| | | High Resolution Mode | 4.5 | 17.3 | ns |
| | | High Color Mode | 7.6 | 29.4 | ns |
| | | Normal Mode | 6.2 | 24.1 | ns |
| 183 | td(IRGB) | Video/blank delay time from PCLK High | | | |
| | | High Resolution Mode | 2.0 | 12.0 | ns |
| | | High Color Mode | - 5.8 | 1.0 | ns |
| | | Normal Mode | 2.0 | 12.0 | ns |
| 184 | td(IRGB) | Video/blank delay time from PCLK Low | | | |
| | | High Color Mode | - 10.0 | - 1.4 | ns |

**NOTES:**

(*1) Depending on the clock frequency and duty cycle.
The assumptions for this timing specification are:
SCLK (c) = 40MHz, 50% duty cycle.

(*2) Maximum WAIT delay varies dependent on the minimum available memory Band Width to CPU.

(*3) Width may increase if slower (access time) translation EPROM is used.

(*4) n = programmable, n is the result of programmed value according to CRTC index 32.

(*5) c = SCLK cycle time
hc = SCLK high pulse width
lc = SCLK low pulse width

(*6) Times indicated do not reflect any delays on the address/data bus due to board logic delay (74F244 = 5 ns, EPROM = 150 ns delay etc..).

(*7) Based on random cycle.

(*8) Based on back to back RAS cycles.

(*9) This value must be greater than the SCLK period.

(*10) Width may increase if slower (access time) BIOS EPROM is used.

(*11) If ROMEL or PMERL active, then DB⟨15:0⟩ bus is in tri-state condition.

(*12) In 16-bit I/O write, ts(IWRCS) is measured from leading edge of IOWWL.
In 8-bit I/O write, ts(IWRCS) time is measured from trailing edge of MIOWL or IOWWL.

(*13) ET4000AX Rev. E RAS addresses hold time reduced from n = 2 to n = 1 to improve external font access timing.

(*14) See Addendum 6.1 for ET4000 Rev. E adjustments to timing.

## 2.3.1 Timing Specification (continued)



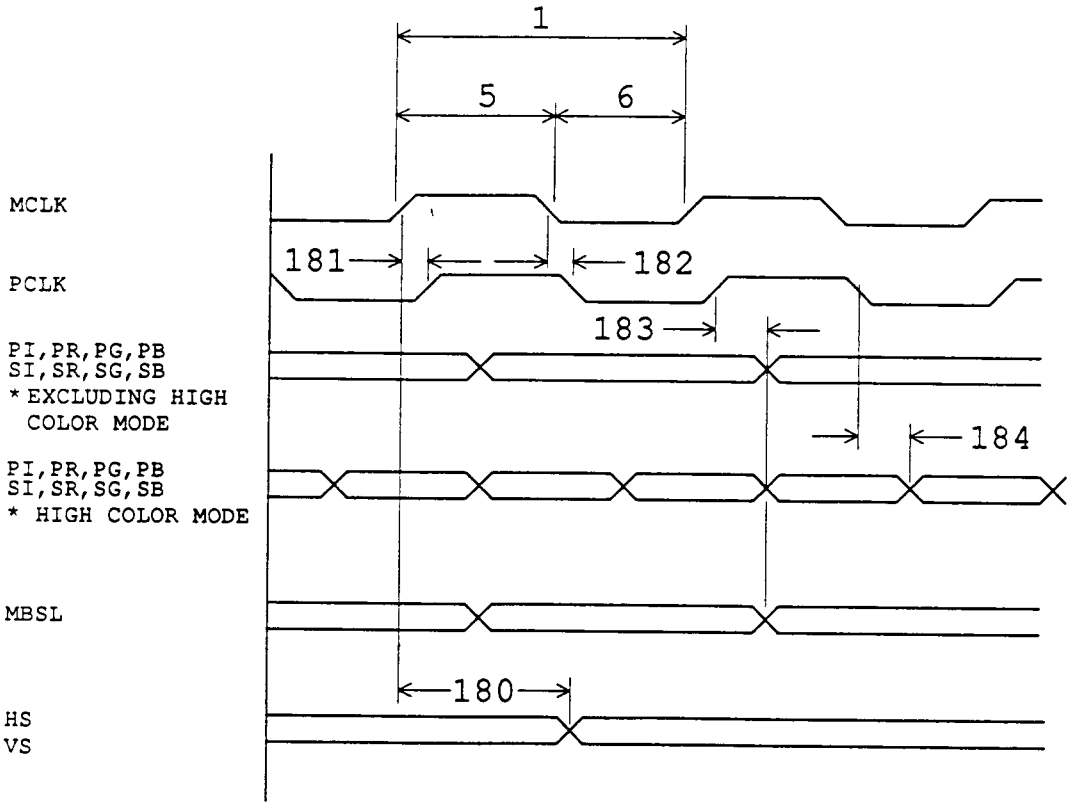



FIG. 2.3.2-1 CRTC OUTPUT TIMING

## 2.3.1 Timing Specification (continued)



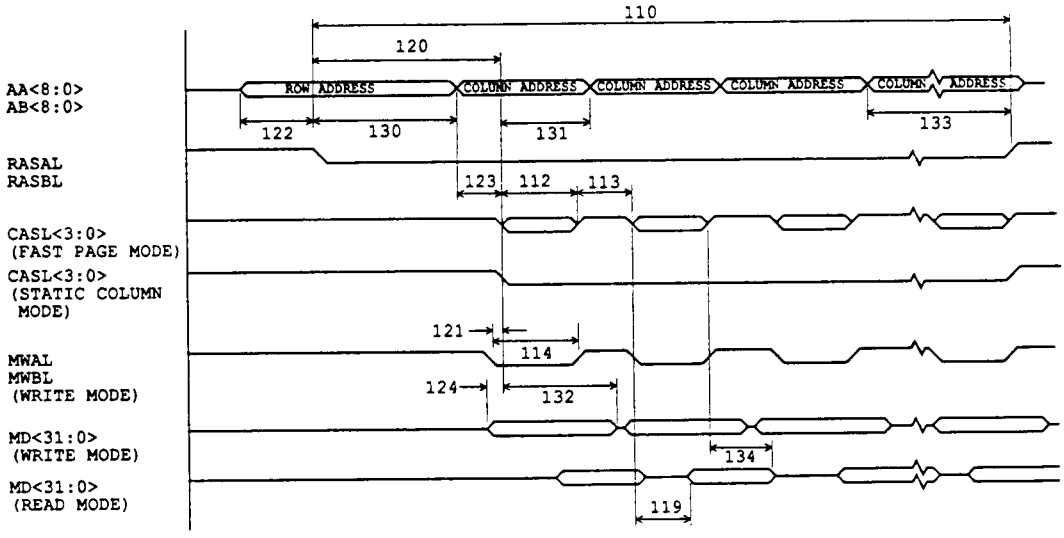



FIG. 2.3.2-2 DISPLAY MEMORY READ/WRITE TIMING

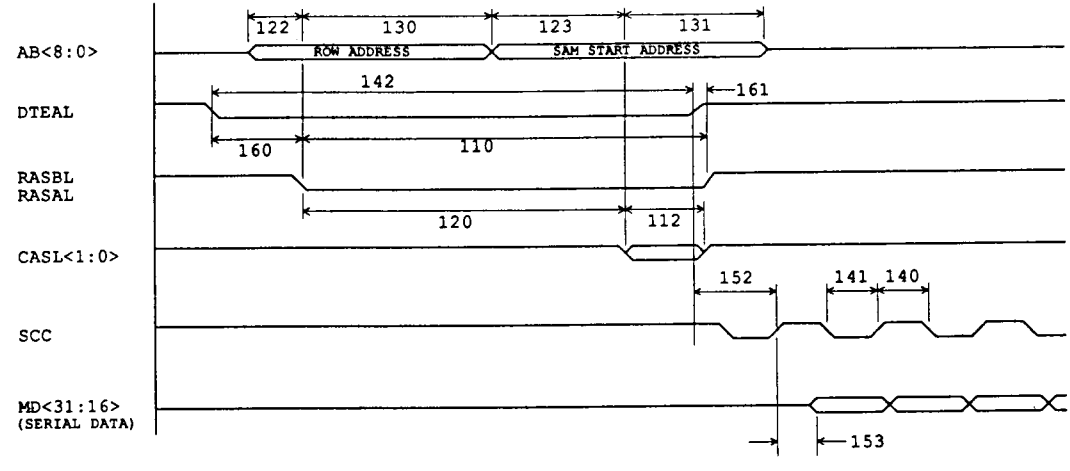



FIG. 2.3.2-3 VRAM TRANSFER CYCLE AND SERIAL READ TIMING

## 2.3.1 Timing Specification (continued)



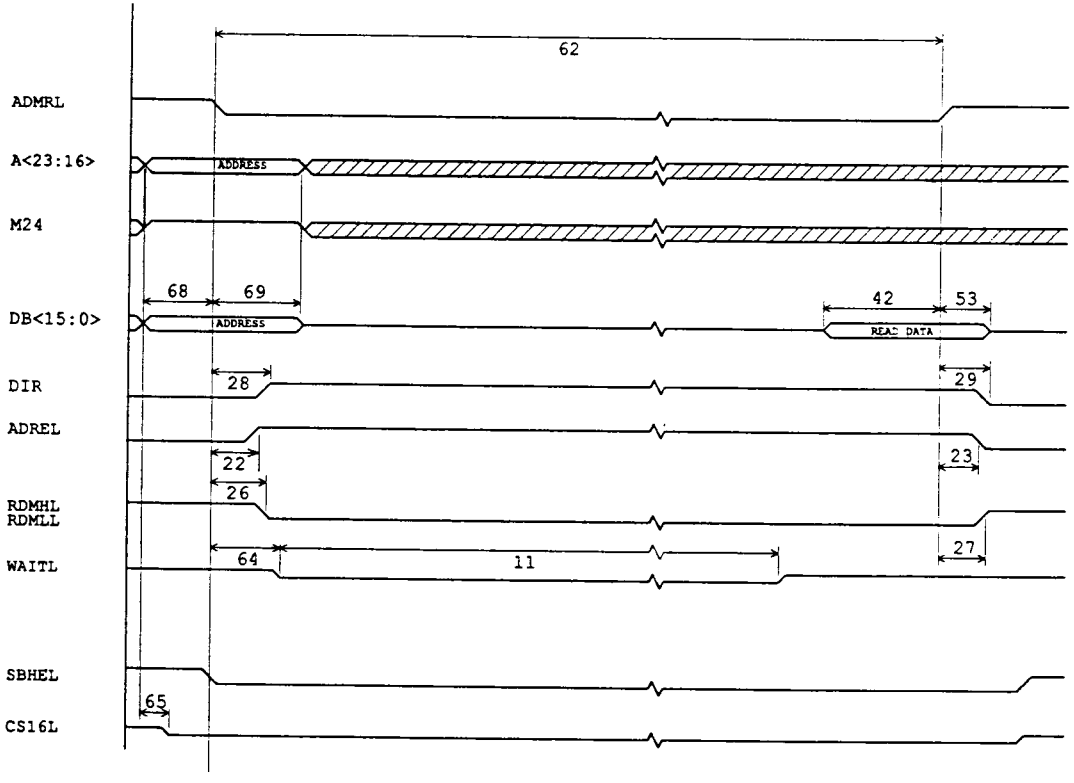



FIG. 2.3.2-4 DISPLAY MEMORY READ TIMING (CPU CYCLE – AT BUS)

## 2.3.1 Timing Specification (continued)

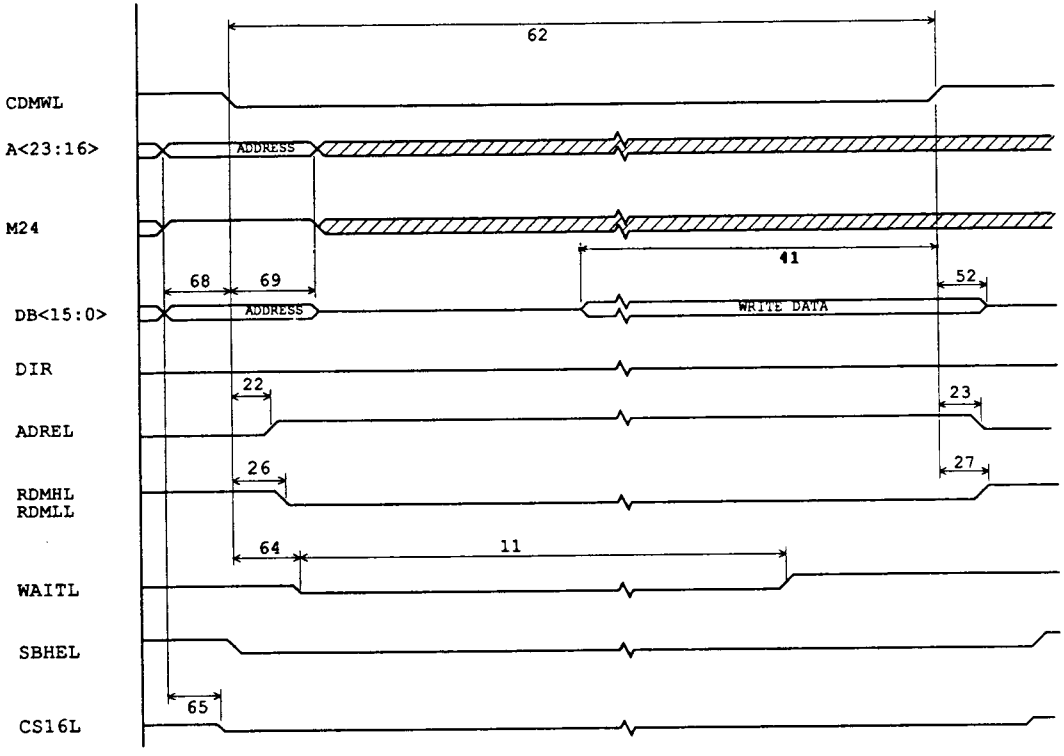



FIG. 2.3.2-5 DISPLAY MEMORY WRITE TIMING (CPU CYCLE — AT BUS)

## 2.3.1 Timing Specification (continued)



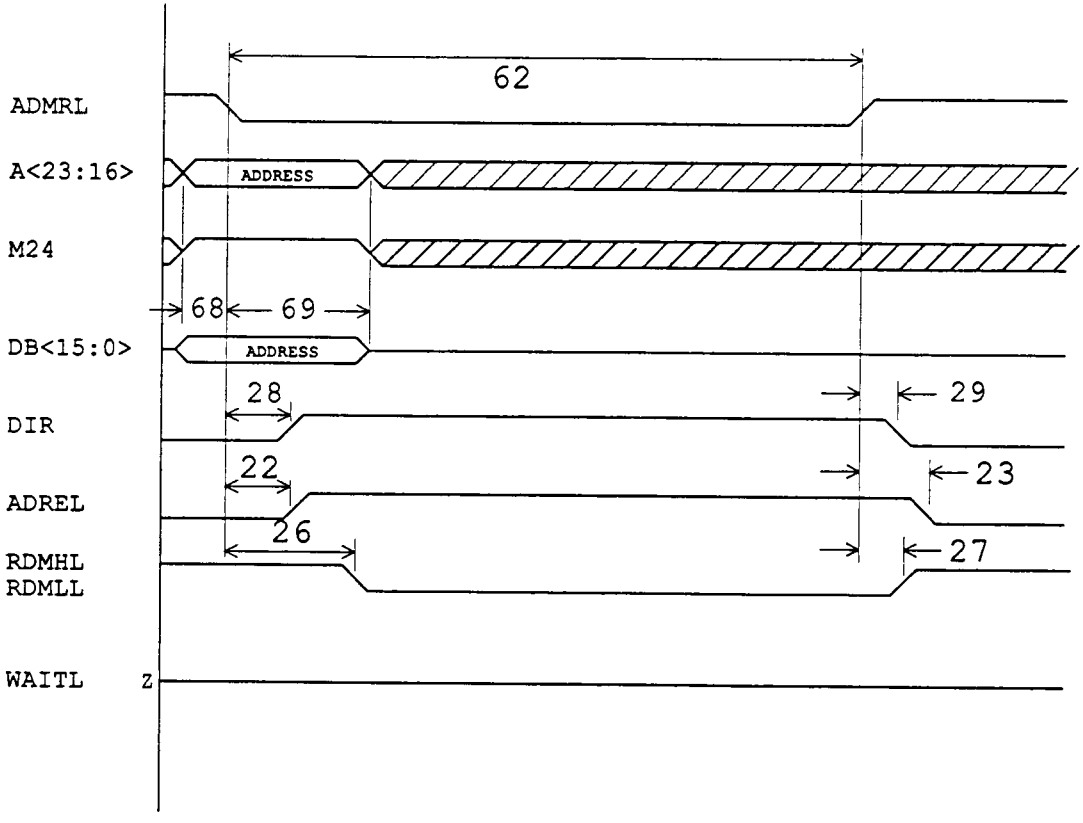



FIG. 2.3.2-6 BIOS EPROM MEMORY READ TIMING (CPU CYCLE – AT BUS)

## 2.3.1 Timing Specification (continued)



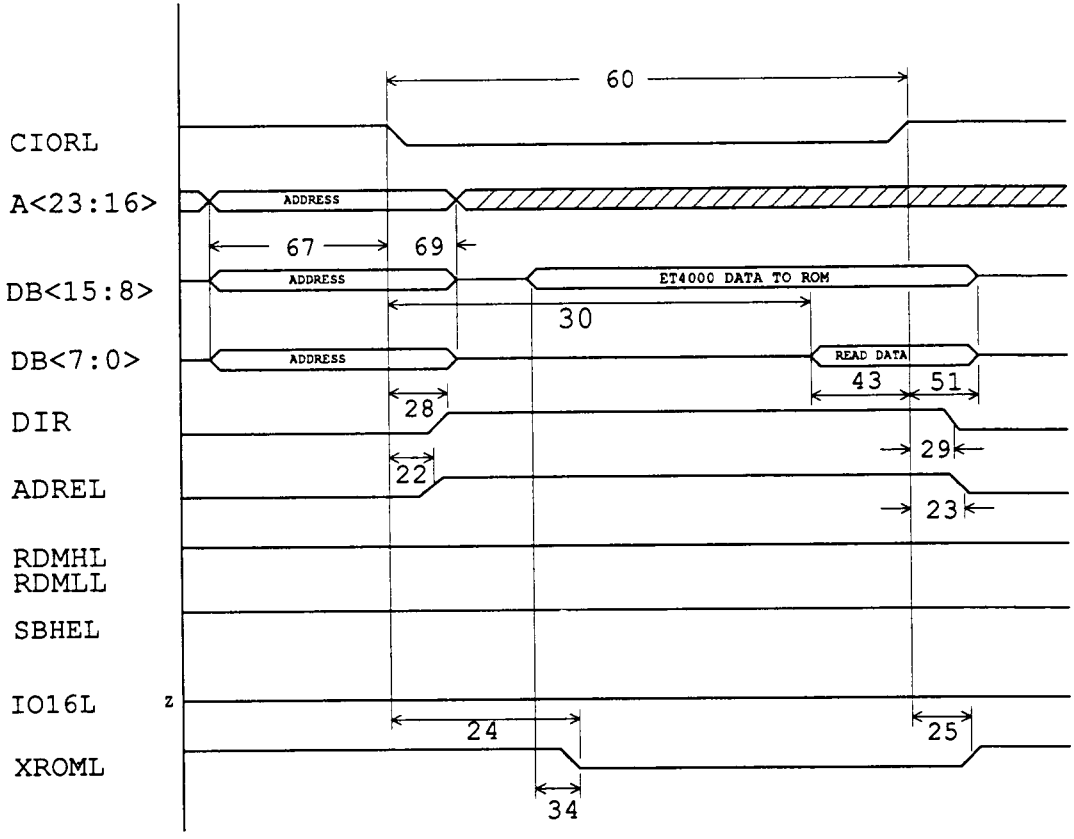



FIG. 2.3.2-7 I/O READ TIMING (CPU CYCLE – AT BUS)
(WITH TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)



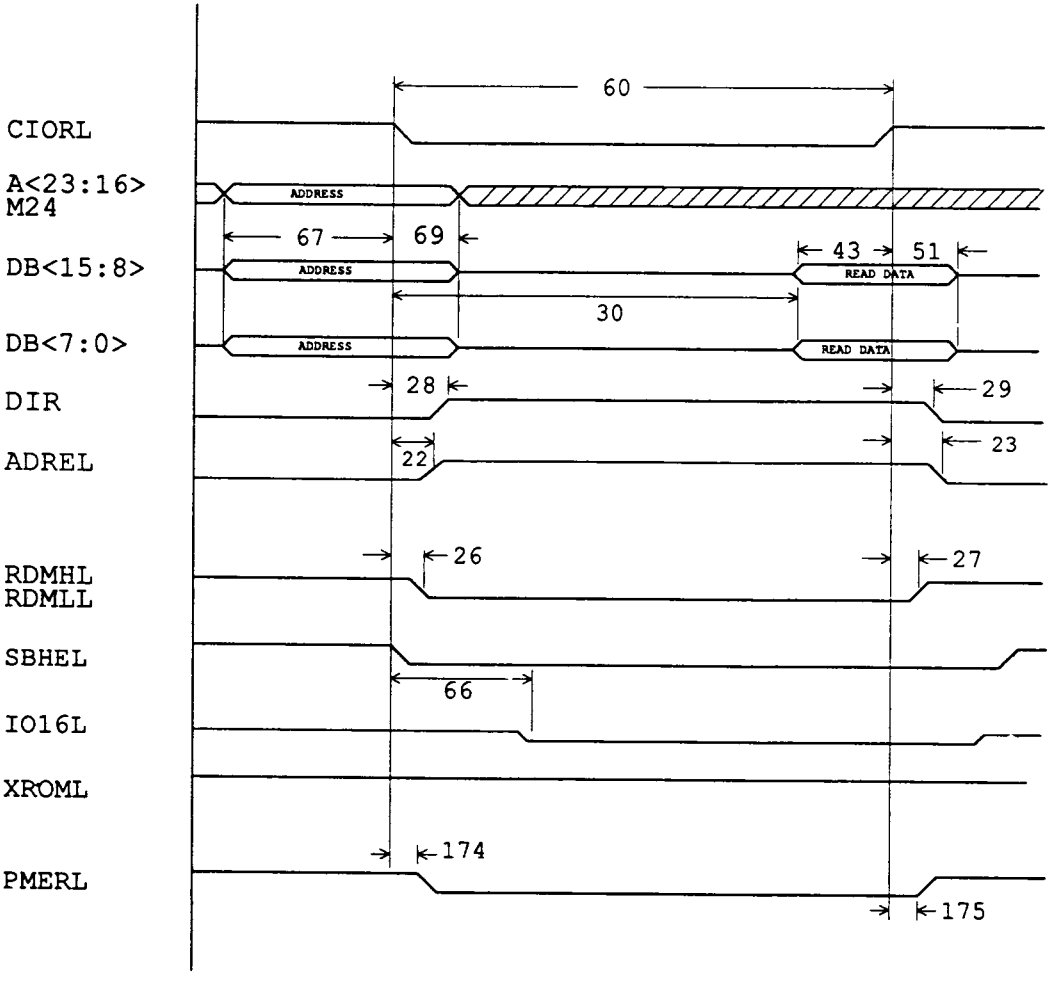



FIG. 2.3.2-8 I/O READ TIMING (CPU CYCLE – AT BUS)
(WITHOUT TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)



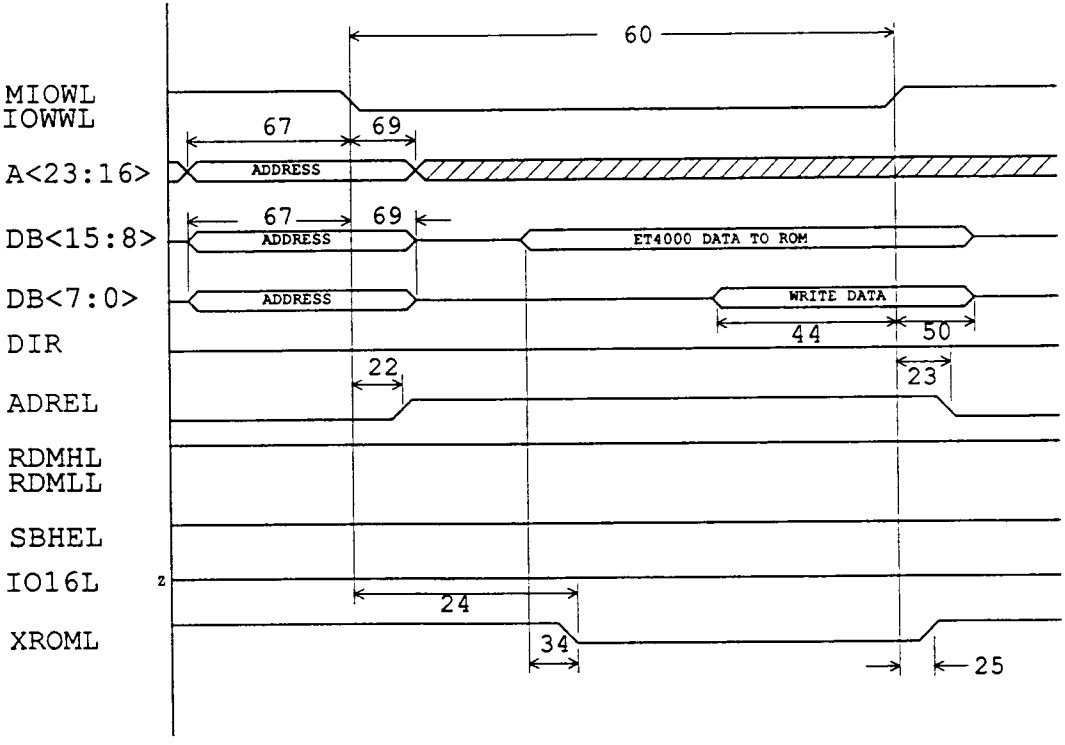



FIG. 2.3.2-9 I/O WRITE TIMING (CPU CYCLE – AT BUS)
(WITH TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)



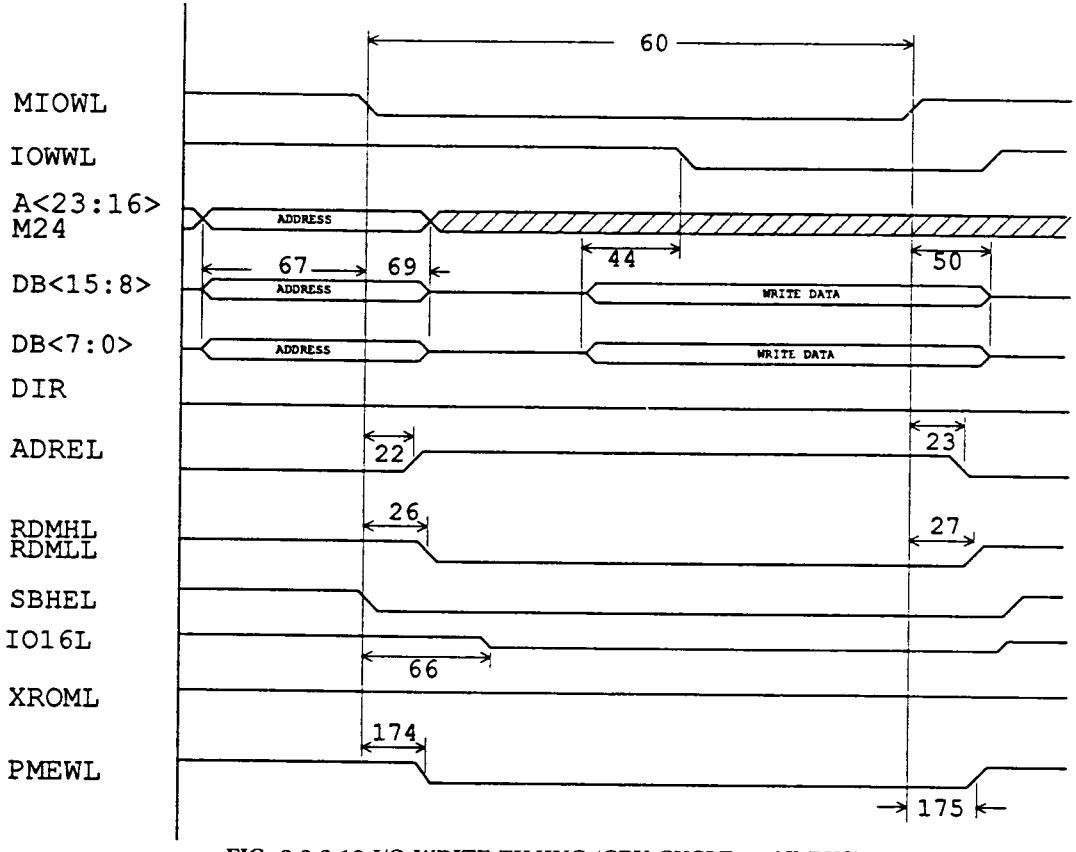



FIG. 2.3.2-10 I/O WRITE TIMING (CPU CYCLE — AT BUS)
(WITHOUT TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)



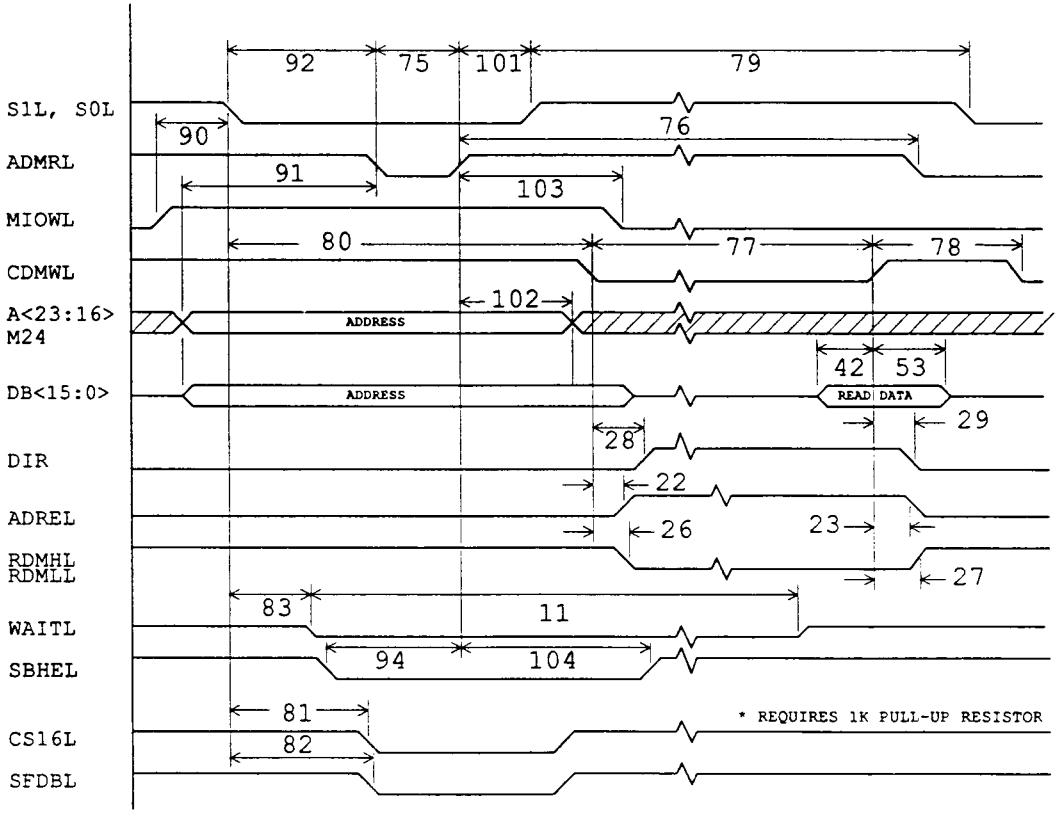



FIG. 2.3.2-11 DISPLAY MEMORY READ TIMING (CPU CYCLE – MICRO CHANNEL BUS)

## 2.3.1 Timing Specification (continued)



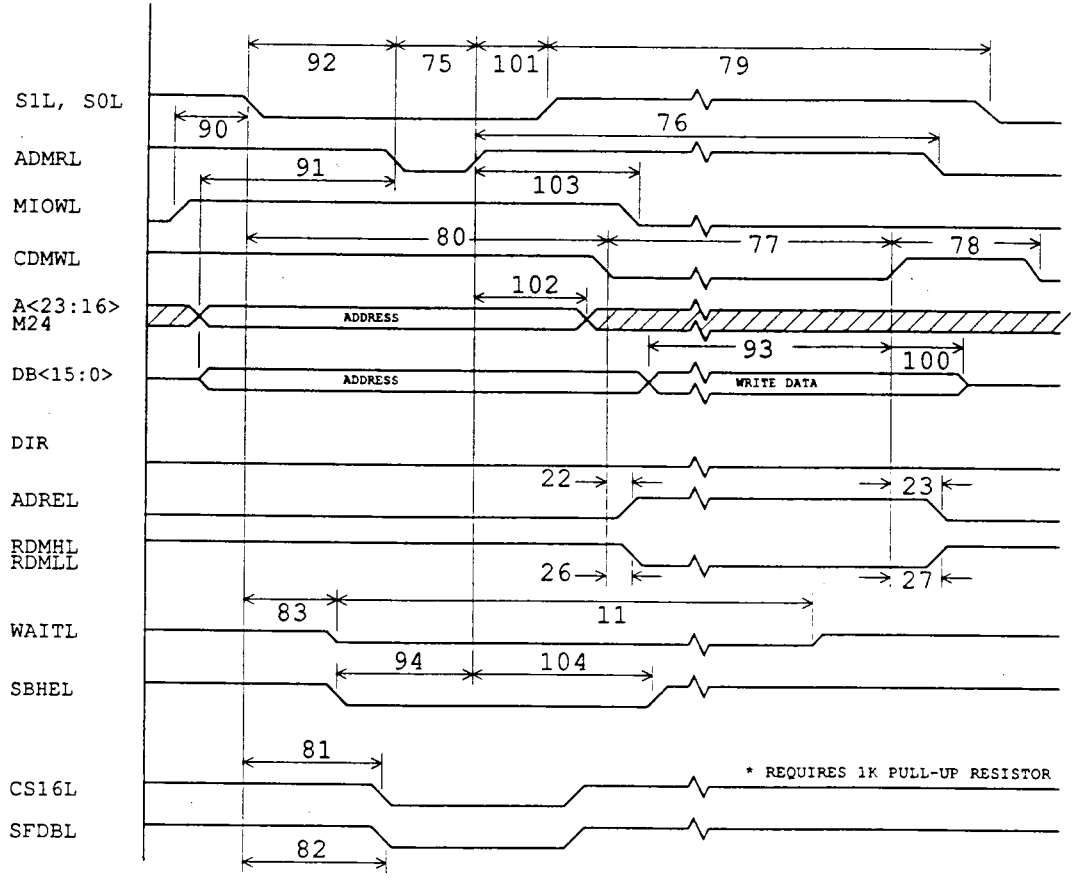



FIG. 2.3.2-12 DISPLAY MEMORY WRITE TIMING (CPU CYCLE – MICRO CHANNEL BUS)

## 2.3.1 Timing Specification (continued)



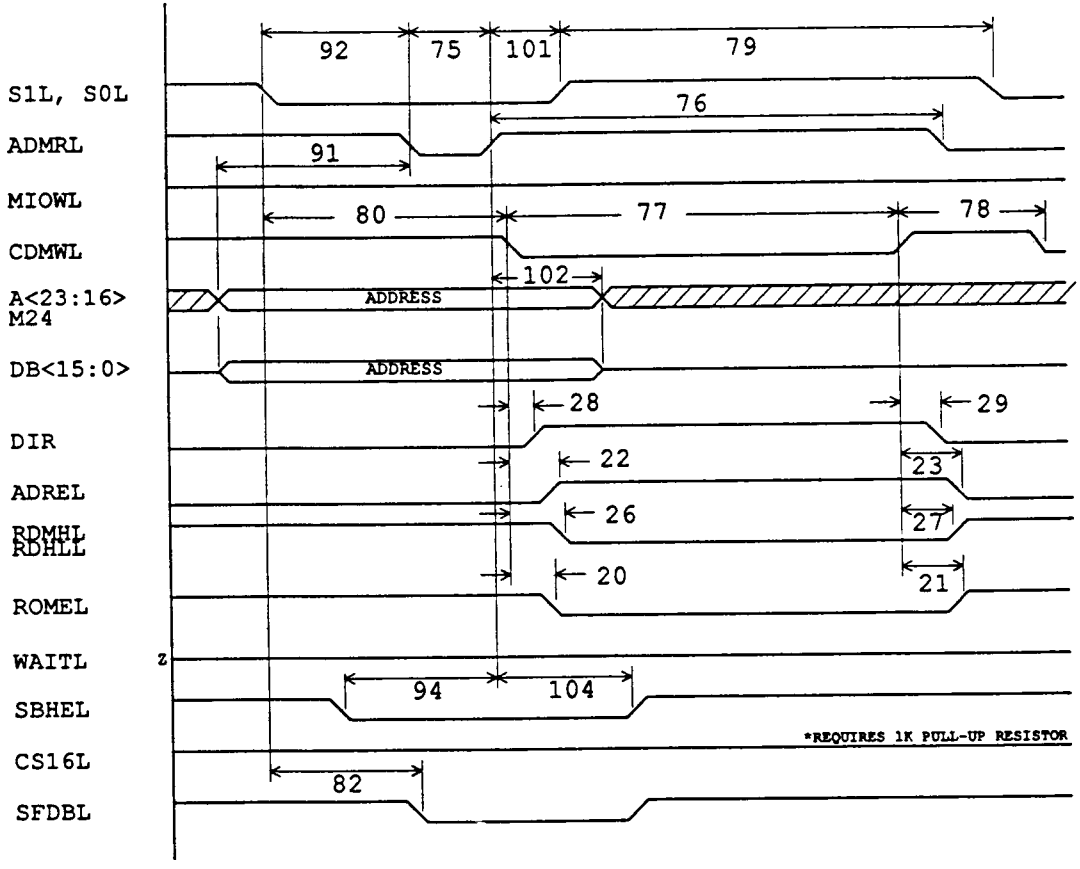



FIG. 2.3.2-13 BIOS EPROM MEMORY READ TIMING (CPU CYCLE — MICRO CHANNEL BUS)

## 2.3.1 Timing Specification (continued)



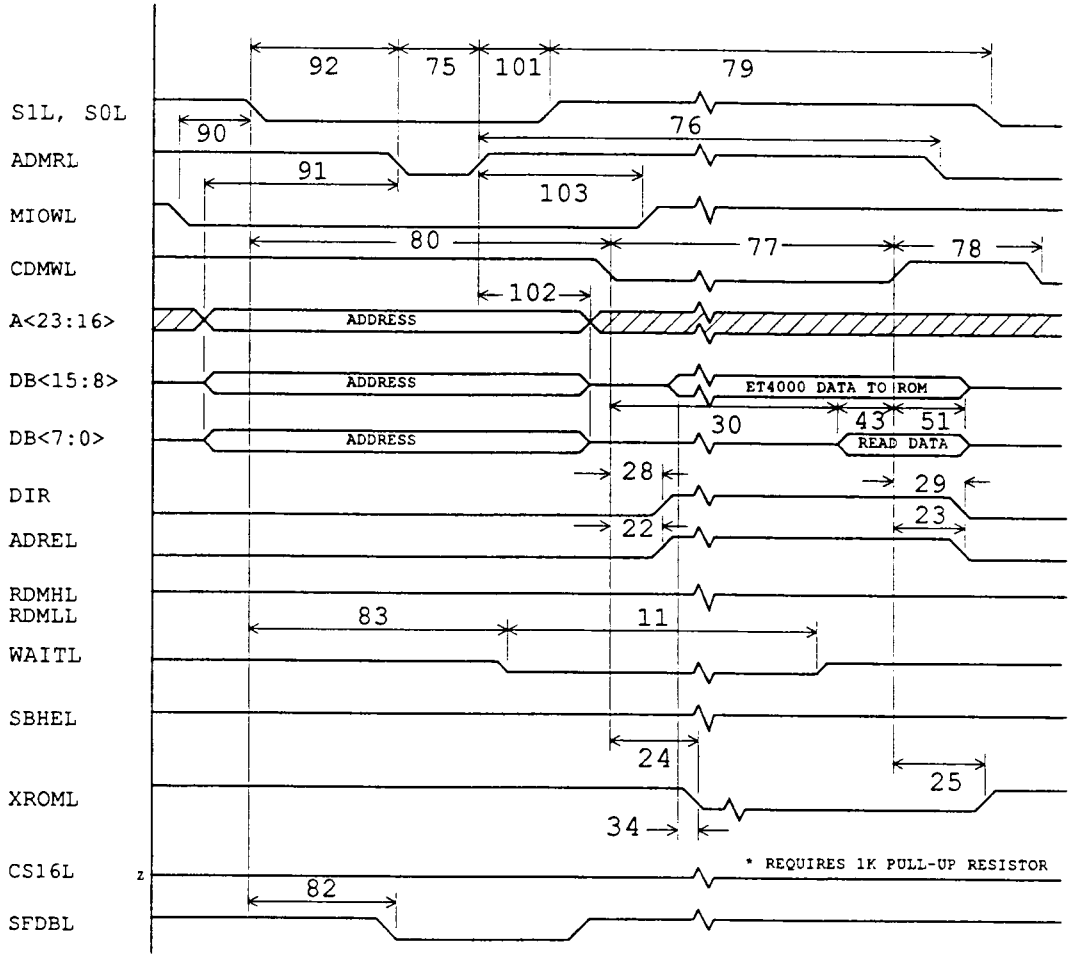



FIG. 2.3.2-14 I/O READ TIMING (CPU CYCLE — MICRO CHANNEL BUS)
(WITH TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)

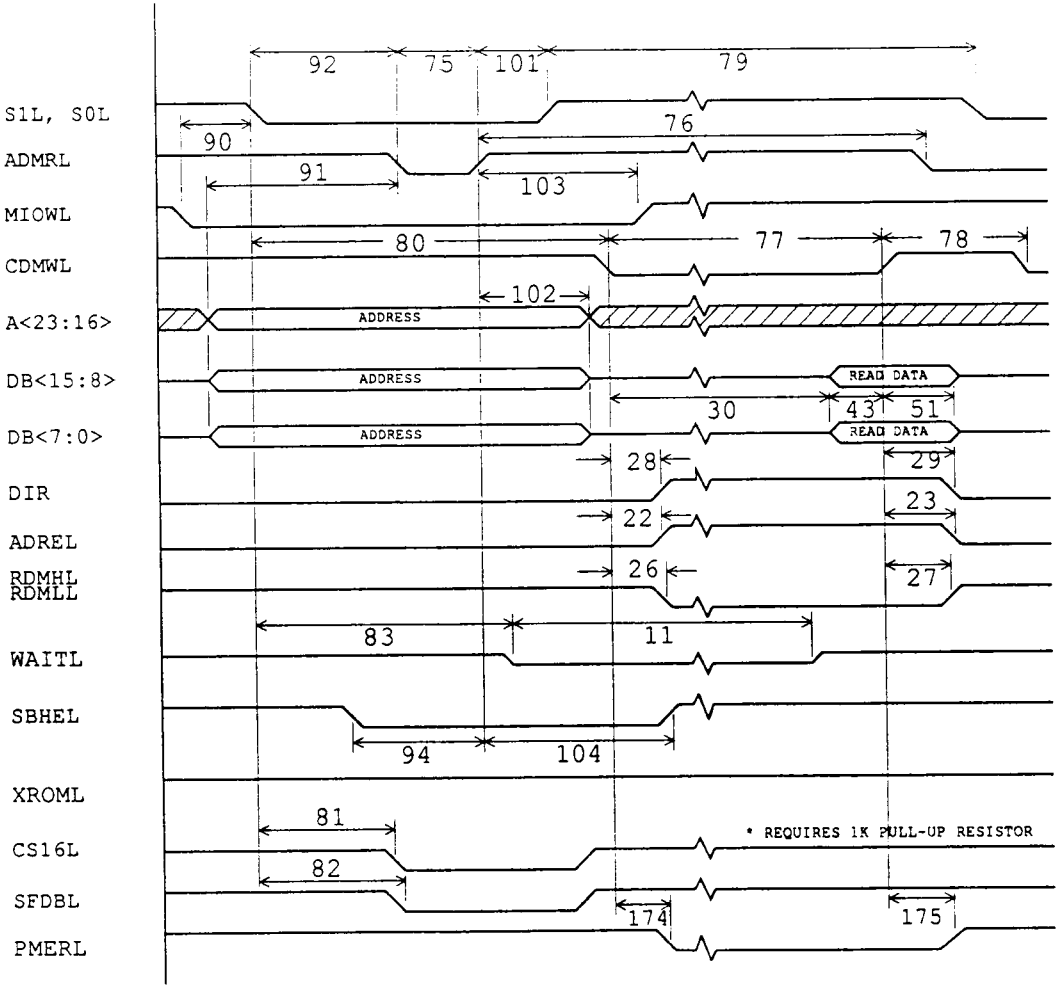



FIG. 2.3.2-15 I/O READ TIMING (CPU CYCLE – MICRO CHANNEL BUS)
(WITHOUT TRANSLATION ROM ACCESS)

## 2.3.1 Timing Specification (continued)



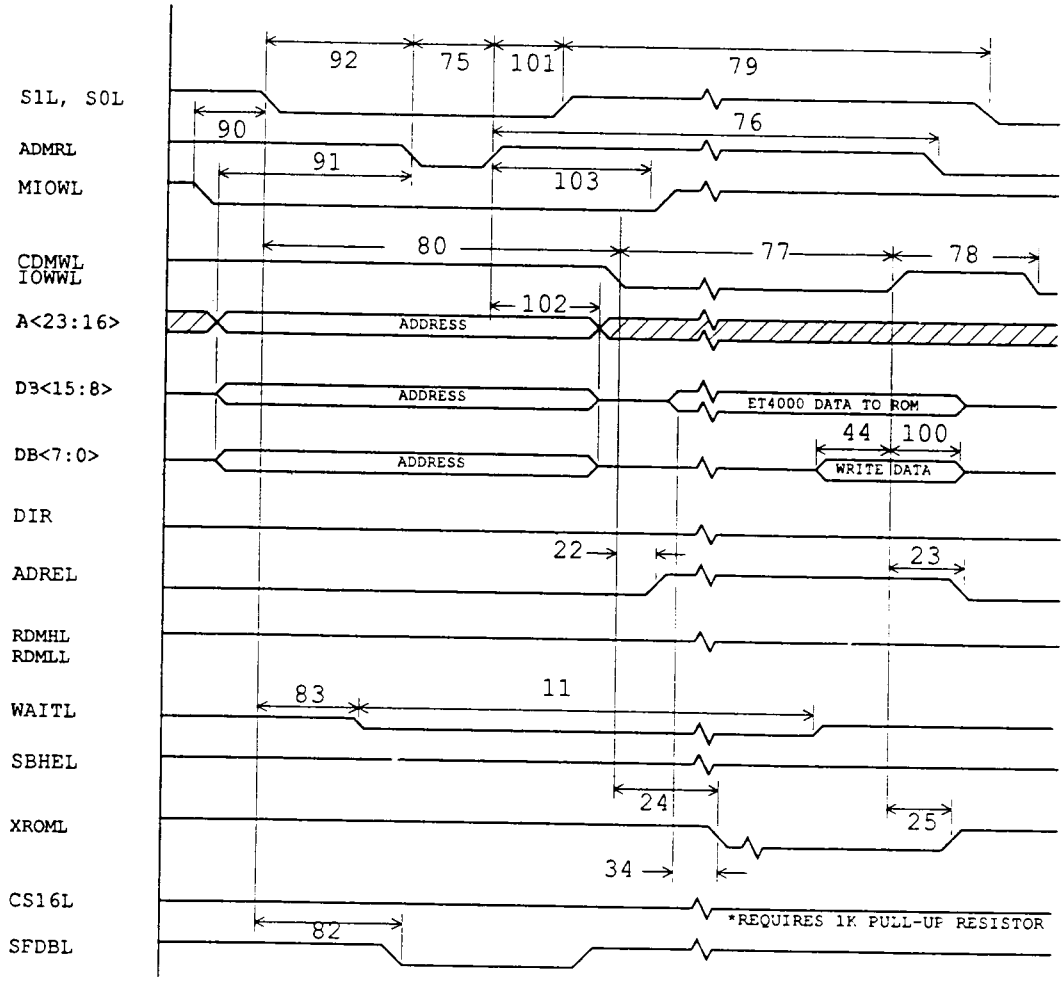



**FIG. 2.3.2-16 I/O WRITE TIMING (CPU CYCLE – MICRO CHANNEL BUS) (WITH TRANSLATION ROM ACCESS)**

## 2.3.1 Timing Specification (continued)



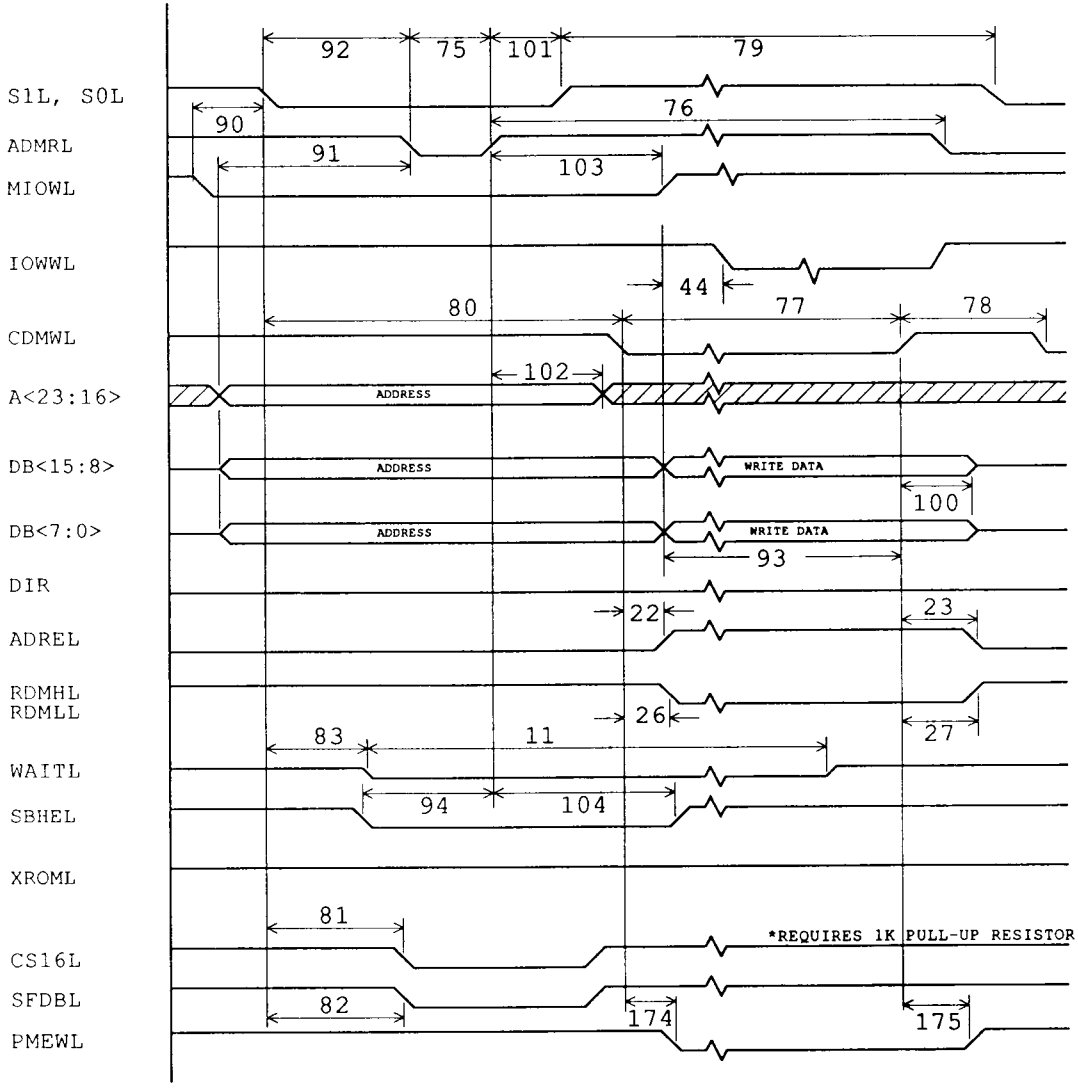



**FIG. 2.3.2-17 I/O WRITE TIMING (CPU CYCLE — MICRO CHANNEL BUS) (WITHOUT TRANSLATION ROM ACCESS)**