YAMAHA LSI

CONFIDENTIAL

YMF711 OPL™

OPL3-SA2

OPL3 Single-chip Audio System 2

■ OUTLINE

YMF711 (OPL3-SA2) is a single audio chip that integrates OPL3 and its DAC, 16bit Sigma-delta CODEC, MPU401 MIDI interface, and joytick with timer, which is very suitable for multi-media application. This LSI is fully compliant with Plug and Play ISA 1.0a and supports all the necessary feature, i.e. 16bit address decode, more IRQs and DMAs in compliance with PC'96. This LSI also supports the expandability, i.e. Zoomed video port, Modem and CDROM interface in a Plug and Play manner and power management that is very important for power-conscious application.

■ FEATURES

- Supports industry standard PC Game compatibility.
- Supports Windows Sound System compatibility.
- Supports Plug & Play ISA 1.0a compatibility.
- Supports multi-purpose pin function.
  (Support 16-bit address decode, DAC interface for OPL4-ML,
  Zoomed Video port, EEPROM interface, MODEM interface, IDE CDROM interface).
- Register Compatible with YMF262 (OPL3) and YMF289 (OPL3-L).
- Built-in 16-bit Sigma-Delta Stereo CODEC.
- Programmable Sample Rate from 5.5kHz to 48kHz for Recording / Playback.
- Hardware and software master volume control.
- Dual DMA (supports DMA Demand Mode) with FIFO for Full Duplex .
- Supports IMA ADPCM, A-Law and μ -Law Compression / Decompression.
- MPU-401 Compatible MIDI Interface.
- Joystick Port with Timer (NE558).
- Built-in 6-channel Stereo Mixer (LINE, AUX1, SYNTH(AUX2), SB, CODEC, MIC).
- Supports 5-channel analog input (LINE, AUX1(CD), AUX2(External Synthesizer), MIC, MIN).
- 24mA TTL bus drive capability.
- All registers are readable.
- Supports Power Management.
- Dual Master Clock Input (24.576MHz, 33.8688MHz).
- 5V or 3.3V power supply for digital, 5V power supply for analog.
- 100 pin SQFP package (YMF711-S).

■ PIN DESCRIPTION

ISA bus interface: 36 pins					
name	pins	I/O	type	Size	function
D7-0	8	I/O	TTL	24mA	Data Bus
A11-0	12	I	TTL	-	Address Bus
AEN	1	I	TTL	-	Address Bus Enable
/IOW	1	I	Schmitt	-	Write Enable
/IOR	1	I	Schmitt	-	Read Enable
RESET	1	I	Schmitt	-	Reset
IRQ3,5,7,9,10,11	6	T	TTL	12mA	Interrupt request
DRQ0, 1, 3	3	T	TTL	12mA	DMA Request
/DACK0, 1, 3	3	I	TTL	-	DMA Acknowledge

Analog Input & Output : 24 pins					
name	pins	I/O	type	size	function
OUTL	1	O	-	-	Left mixed analog output
OUTR	1	O	-	-	Right mixed analog output
VREFI	1	I	-	-	Voltage reference input
VREFO	1	O	-	-	Voltage reference output
AUX1L	1	I	-	-	Left AUX1 input
AUX1R	1	I	-	-	Right AUX1 input
AUX2L	1	I	-	-	Left AUX2 input
AUX2R	1	I	-	-	Right AUX2 input
LINEL	1	I	-	-	Left LINE input
LINER	1	I	-	-	Right LINE input
MIC	1	I	-	-	MIC input
MIN	1	I	-	-	Monaural input
SBSHL	1	-	-	-	Left SBDAC sample / hold capacitor
SBSHR	1	-	-	-	Right SBDAC sample / hold capacitor
SBFLTL	1	-	-	-	Left SBDAC filter
SBFLTR	1	-	-	-	Right SBDAC filter
SYNSHL	1	-	-	-	Left SYNDAC sample / hold capacitor
SYNSHR	1	-	-	-	Right SYNDAC sample / hold capacitor
ADFLTL	1	-	-	-	Left input filter
ADFLTR	1	-	-	-	Right input filter
VOCOL	1	O	-	-	Left voice output
VOCOR	1	O	-	-	Right voice output
VOCIL	1	I	-	-	Left voice input
VOCIR	1	I	-	-	Right voice input

■ FUNCTION OVERVIEW

1. Multi-purpose pin

1-1. Multi-purpose function

OPL3-SA2 can support the various functions listed below of MP0-MP9 pins, by programming SEL2-0 pins.

A. 16-bit address decode
B. EEPROM interface
C. Zoomed video port
D. CPU and DAC interface for OPL4-ML
E. MODEM interface
F. IDE CD-ROM interface

Following table shows what combinations of the above functions are available for each SEL2-0 pins.

SEL	16bit Dec.	EEPROM	ZV port	OPL4-ML	MODEM	CDROM	Remark
0	-	-	-	-	-	-	Test mode
1	*1	YES	-	*2	YES	YES(*1)	S/C,C/C (add-in)
2	YES	YES	-	*3	YES	-	S/C (add-in)
3	*4	YES	-	YES	-	-	S/C (add-in)
4	*4	-	YES	YES	-	-	Note PC
5	YES	-	YES	*3	YES	-	Note PC
6	-	-	-	-	-	-	Reserved
7	YES	-	-	YES	-	-	M/B, Note PC

Where,

S/C : Sound Card
C/C : Combo Card (Sound and Modem)
M/B : Desktop Mother Board

	SEL=0	SEL=1	SEL=2	SEL=3	SEL=4	SEL=5	SEL=6	SEL=7
SEL0 pin	0	1	0	1	0	1	0	1
SEL1 pin	0	0	1	1	0	0	1	1
SEL2 pin	0	0	0	0	1	1	1	1

Notice

*1) External PAL is needed.
*2) External wave table synthesizer (ex.OPL4-ML) is mixed as analog signal using external DAC.
*3) Clock module (ex.MK1420) is used to generate the clock for OPL4-ML and it will be mixed analog singal by having an additional DAC.
*4) External TTLs (ex.LS138) is needed.

See section 1-2 and 1-3 for implementation detail.

1-2. Pin description

	SEL=0	SEL=1	SEL=2	SEL=3	SEL=4	SEL=5	SEL=6	SEL=7
MP0	-	/MCS	/MCS	/EXTEN	/EXTEN	/MCS	-	/EXTEN
MP1	-	MIRQ	MIRQ	/SYNCS	/SYNCS	MIRQ	-	/SYNCS
MP2	-	ROMCLK	ROMCLK	ROMCLK	BCLK_ZV	A12	-	A12
MP3	-	ROMCS	ROMCS	ROMCS	LRCK_ZV	A13	-	A13
MP4	-	ROMDI	ROMDI	ROMDI	SIN_ZV	A14	-	A14
MP5	-	ROMDO	ROMDO	ROMDO	/XRST	A15	-	A15
MP6	-	/CDCS0	A12	BCLK_ML	BCLK_ML	BCLK_ZV	-	BCLK_ML
MP7	-	/CDCS1	A13	LRCK_ML	LRCK_ML	LRCK_ZV	-	LRCK_ML
MP8	-	CDIRQ	A14	SIN_ML	SIN_ML	SIN_ZV	-	SIN_ML
MP9	-	CLKO	A15	CLKO	CLKO	/XRST	-	CLKO

Note: Do not select SEL=0 and SEL=6.
SEL=0; Yamaha Test Mode SEL=6; Reserved

Mutil-purpose pins:		
name	I/O	function
/MCS	O	Chip select output for MODEM chip (COM)
MIRQ	I+	Interrupt request input for MODEM (COM)
ROMCLK	O	Serial data clock output for external EEPROM
ROMCS	O	Chip select output for external EEPROM
ROMDI	I+	Serial data input for external EEPROM
ROMDO	O	Serial data output for external EEPROM
CDCS0	O	Chip select output for IDE CD-ROM (/CS1FX)
CDCS1	O	Chip select output for IDE CD-ROM (/CS3FX)
CDIRQ	I+	Interrupt request input for IDE CD-ROM
A12 - 15	I+	Address bus for ISA-bus
/EXTEN	I+	Enable OPL4-ML interface
/SYNCS	O	Chip select output for OPL4-ML
BCLK_ML	I+	Bit clock input for OPL4-ML
LRCK_ML	I+	L/R clock input for OPL4-ML
SIN_ML	I+	Serial data input for OPL4-ML
CLKO	O	Master clock output (33.8688MHz)
BCLK_ZV	I+	Bit clock input for Zoomed Video port (I^2S)
LRCK_ZV	I+	L/R clock input for Zoomed Video port (I^2S)
SIN_ZV	I+	Serial data input for Zoomed Video port (I^2S)
/XRST	O	Inverted RESET output

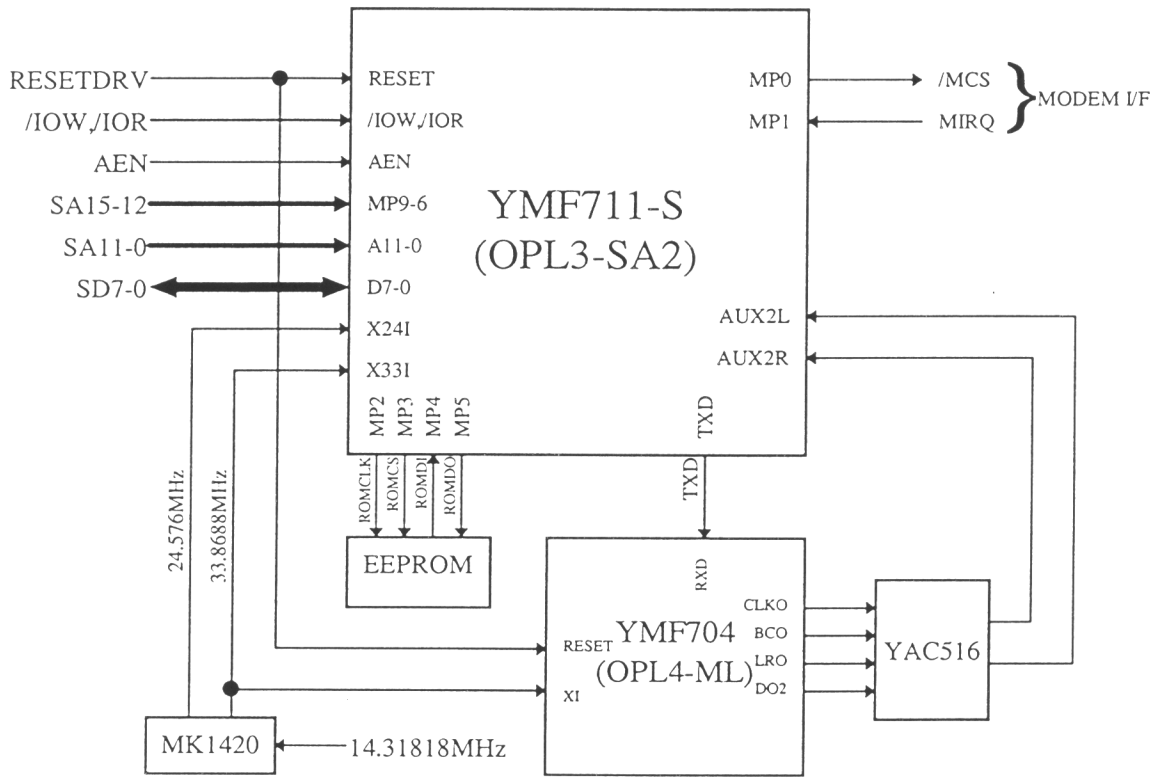
2.Master Clock

Both 33.8688MHz and 24.576MHz are used or 14.31818MHz and clock module (ex.MK1420 by Micro Clock) are used.

3.YMF704(OPL4-ML)

The external DAC (YAC516) is necessary for wavetable upgrade.

(2) SEL=2 (Sound Card and Combo Card for Add-in)



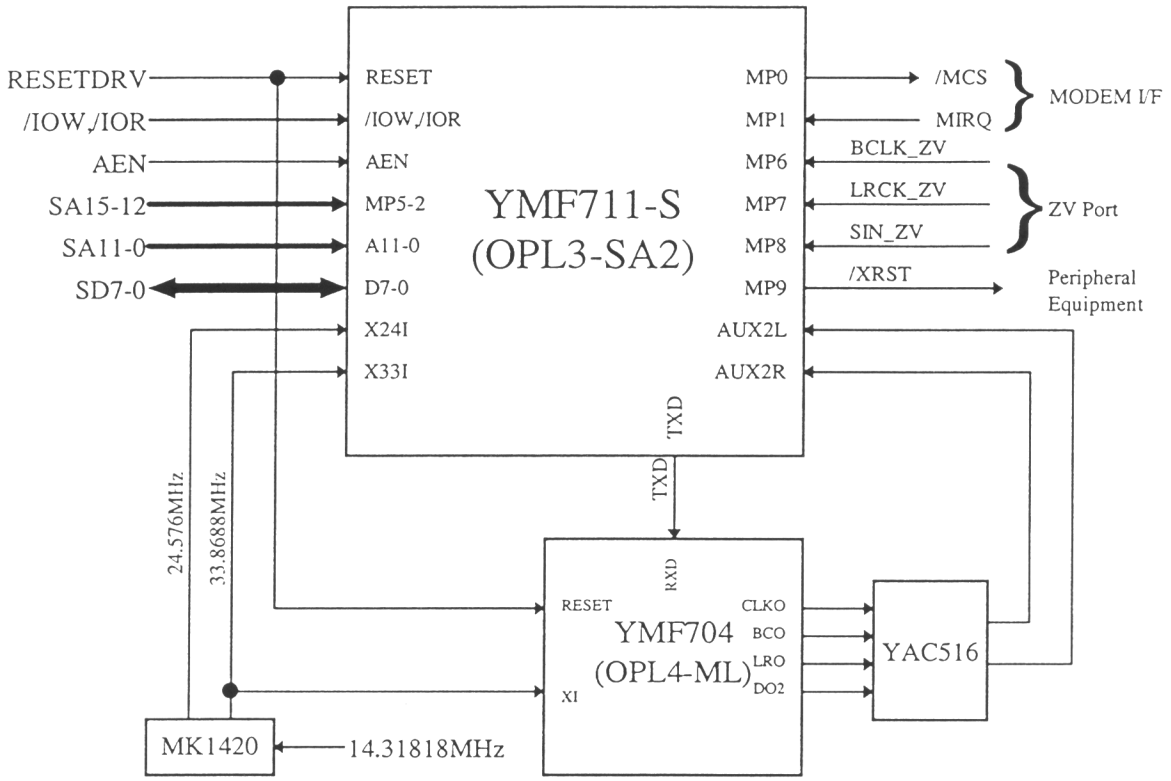
1.YMF704(OPL4-ML)

The external DAC (YAC516) and the clock module (ex.MK1420 by Micro Clock) are necessary for wavetable upgrade.

2.MK1420

The MK1420 is the clock module that generates all clocks necessary for this chipset . It is by Micro Clock and its package is SOP8.

(5) SEL=5 (for Notebook PC)



1.Internal DAC

The internal OPL3 and the ZV Port shares the internal DAC, which is very similar to the case mentioned the previous chapter.

(i) either internal OPL3 or ZV port is active at a time and simultaneous use is not possible.

(ii) which function the internal DAC is used for is determined by the SA2 control register, index 02h, VZE bit.

2.YMF704(OPL4-ML)

The external DAC (YAC516) and the clock module (ex.MK1420) are necessary for wave table upgrade.

2. ISA Interface

OPL3-SA2 supports ISA Plug and Play (PnP) that frees the users from configuring the I/O address, IRQ and DMA channel. Those system resources are set automatically by the system. However even when used in Non PnP system, , the configuration can be changed with software.

2-1. PnP Auto-Configuration mode

OPL3-SA2 has the following I/O port to support the Plug and Play ISA.

Address port:	279h
Write Data Port:	A79h
Relocatable Read Data Port:	203h - 03FFh

The following four Logical Devices are supported by OPL3-SA2.

Logical Device No. 0

Sound Blaster Playback system	(SB Base)
16-bit CODEC	(WSS Base)
MPU401	(MPU Base)
OPL3	(AdLib Base)
OPL3-SA2 control register	(CTRL Base)

Logical Device No. 1

Joy Stick

Logical Device No. 2 (Optional)

MODEM (COM port)

Logical Device No. 3 (Optional)

IDE CD-ROM interface

Logical Device Number = 0 : SA2 Sound System

30h	R/W	Activate
60h	R/W	I/O port base address[15..8], Descriptor 0 (SB base)
61h	R/W	I/O port base address[7..0], Descriptor 0 (SB base)
62h	R/W	I/O port base address[15..8], Descriptor 1 (WSS base)
63h	R/W	I/O port base address[7..0], Descriptor 1 (WSS base)
64h	R/W	I/O port base address[15..8], Descriptor 2 (AdLib base)
65h	R/W	I/O port base address[7..0], Descriptor 2 (AdLib base)
66h	R/W	I/O port base address[15..8], Descriptor 3 (MPU base)
67h	R/W	I/O port base address[7..0], Descriptor 3 (MPU base)
68h	R/W	I/O port base address[15..8], Descriptor 4 (CTRL base)
69h	R/W	I/O port base address[7..0], Descriptor 4 (CTRL base)
70h	R/W	Interrupt request level select 0 (for IRQ-A)
71h	R	Interrupt request type select 0 (for IRQ-A)
72h	R/W	Interrupt request level select 1 (for IRQ-B)
73h	R	Interrupt request type select 1 (for IRQ-B)
74h	R/W	DMA channel select 0 (for DMA-A)
75h	R/W	DMA channel select 1 (for DMA-B)

Logical Device Number = 1 : Joystick

30h	R/W	Activate
60h	R/W	I/O port base address[15..8]
61h	R/W	I/O port base address[7..0]

Logical Device Number = 2 : MODEM (Optional)

30h	R/W	Activate
60h	R/W	I/O port base address[15..8]
61h	R/W	I/O port base address[7..0]
70h	R/W	Interrupt request level select
71h	R	Interrupt request type select

Logical Device Number = 3 : CD-ROM (Optional)

30h	R/W	Activate
60h	R/W	I/O port base address [15..8], Descriptor 0 (/CDCS0)
61h	R/W	I/O port base address [7..0], Descriptor 0 (/CDCS0)
62h	R/W	I/O port base address [15..8], Descriptor 1 (/CDCS1)
63h	R/W	I/O port base address [7..0], Descriptor 1 (/CDCS1)
70h	R/W	Interrupt request level select
71h	R	Interrupt request type select

2-3. Recommended Resource Data

The recommended resource data is the followings.

(1) LDN=0:SA2 Sound System

I/O (SB base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	220h	240h	220-280h	<-
Length	16	16	16	<-
Alignment	-	-	16	<-

I/O (WSS base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	530h	F40h	530-F48h	<-
Length	8	8	8	<-
Alignment	-	-	8	<-

I/O (AdLib base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	388h	<-	388-3F8h	<-
Length	8	<-	8	<-
Alignment	-	-	8	<-

I/O (MPU base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	330h	300h	300-334h	<-
Length	2	2	2	<-
Alignment	-	-	2	<-

I/O (CTRL base): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	370h	100-FFEh	<-	<-
Length	2	2	<-	<-
Alignment	2	2	<-	<-

(4) LDN=3:CD-ROM

I/O (/CDCS0): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	1E0h	100-1F8h	<-	<-
Length	8	8	<-	<-
Alignment	-	8	<-	<-

I/O (/CDCS1): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	3E6h	306-3F6h	<-	<-
Length	1	1	<-	<-
Alignment	-	8	<-	<-

IRQ: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	11	3,5,7,9,10,11	<-	<-

2-4. Manual Configuration Mode

When OPL3-SA2 is in the Wait for Key state, it can be changed to the Manual Configuration mode by sending the following YAMAHA key to Address_Port. The Manual Configuration mode is used for downloading the resource data to EEPROM and internal SRAM, setting up the OPL3-SA2 without PnP protocol.

YAMAHA Key:
B1h, D8h, 6Ch, 36h, 9Bh, 4Dh, A6h, D3h,
69h, B4h, 5Ah, ADh, D6h, EBh, 75h, BAh,
DDh, EEh, F7h, 7Bh, 3Dh, 9Eh, CFh, 67h,
33h, 19h, 8Ch, 46h, A3h, 51h, A8h, 54h

In the Manual Configuration mode, PnP registers can be accessed by the host without PnP protocol. Right after OPL3-SA2 is switched to the Manual Configuration mode, set **"81h"** in CSN register to put OPL3-SA2 in "Sleep" State. And when **"81h"** is written to Wake [CSN], it becomes possible to access to Configuration register of each logical device from the host.
To return from the Manual Configuration mode to PnP auto-configuration mode, the Wait for Key command should be sent.

Note:
The Manual Configuration mode can not be used in the system with more than one OPL3-SA2's card installed in the ISA slot.

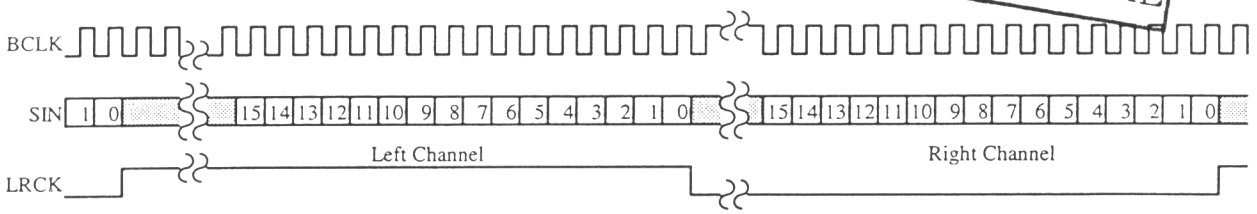


Fig.6-1 Conventional DAC Interface Format for OPL4-ML

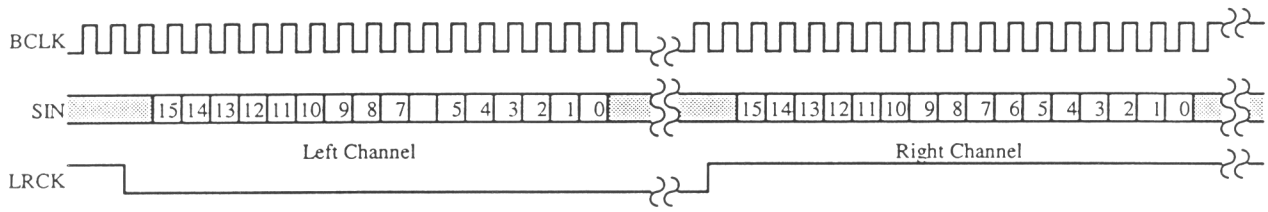


Fig.6-2 I²S Format for Zoomed Video Port

7. Power Management

Power management is categorized into three types.

(1) Power Save Mode 1,2

In this mode, all the clocks and analog power supplies are cut off except analog VREF and analog mixing blocks. Clock generator can be controlled under either two options.

(i) Power Save Mode 1 (Clock Generator Control : Disabled (stop)) (PSV=PDX="1")

It is necessary to take some time before clock oscillation to stabilize. Power dissipation of digital portion becomes about 1/200 of that in normal operation, and that of analog portion becomes about one tenth of that in normal operation.

(ii) Power Save Mode 2 (Clock Generator Control : Enabled (crystals keep on oscillating)) (PSV="1" and PDX="0")

Leaving power save mode gets the OPL3-SA2 back into function instantly. Power dissipation of digital portion becomes about one fifth of that in normal operation, and that of analog portion becomes about one tenth of that in normal operation.

SA2 control register, index 01h, PSV and PDX bits, implement these controls.In these mode, the OUTL/R pins will keep the VREF voltage.

(2) Power Down Mode (PDN=PDX="1")

In this mode, clock generator control (clock oscillation) is disabled (stop), and all the clocks and analog power supplies are cut off. It is necessary to take some time before clock oscillation to stabilize. Total dissipation becomes about 1/600 of that in normal operation.

SA2 control register, index 01h, PDN and PDX bits, implement this control.VREF voltage slowly decays to ground on transition into this mode, and quickly returns to VREF on transition from this mode.

During power down/save mode, master volume is automatically muted, so all audio sources can not heard. After resuming from this mode, master volume is still muted.

(3) Master clock out and internal FM Disable

(i) CLKO Disable (CLKO="1")

Master clock(33.8688MHz) is disabled, which appears on the pin MP9(SEL=3,4,7).

SA2 control register, index 01h, CLKO bit implements this control.

(ii) internal FM Power Down

Setting SA2 control register, index 01h, FMPS bit to"1" makes the OPL3 portion in power down mode, when /EXTEN="L" or VZE="1".

8-1-2-1. DSP Command

Listed below are the supported commands of DSP defined Sound Blaster Pro.

CMD	Function	Support
10h	8bit direct mode digitized sound I/O output	o
14h	8bit single-cycle DMA mode digitized sound output	o
16h	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output	*
17h	8bit to 2bit ADPCM single-cycle DMA mode digitized sound output with ref. byte	*
1Ch	8bit auto-init DMA mode digitized sound output	o
1Fh	8bit to 2bit ADPCM auto-init DMA mode digitized sound output with ref. byte	*
20h	8bit direct mode single byte digitized sound input	*
24h	8bit single-cycle DMA mode digitized sound input	*
2Ch	8bit auto-init DMA mode digitized sound input	*
30h	Polling mode MIDI input	*
31h	Interrupt mode MIDI input	*
34h	UART polling mode MIDI I/O	*
35h	UART interrupt mode MIDI I/O	*
36h	UART polling mode MIDI I/O with time stamping	*
37h	UART interrupt mode MIDI I/O with time stamping	*
38h	MIDI output	*
40h	Set digitized sound transfer Time Constant	o
48h	Set DSP block transfer size	o
74h	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output	o
75h	8bit to 4bit ADPCM single-cycle DMA mode digitized sound output with ref. byte	o
76h	8bit to 3bit ADPCM single-cycle DAM mode digitized sound output	*
77h	8bit to 3bit ADPCM single-cycle DMA mode digitized sound output with ref. byte	*
7Dh	8bit to 4bit ADPCM auto-init DMA mode digitized sound output with ref. byte	o
7Fh	8bit to 3bit ADPCM auto-init DMA mode digitized sound output with ref. byte	*
80h	Pause DAC for a duration	o
90h	8bit high-speed auto-init DMA mode digitized sound output	o
91h	8bit high-speed single-cycle DMA mode digitized sound output	o
98h	8bit high-speed auto-init DMA mode digitized sound input	*
99h	8bit high-speed single-cycle DMA mode digitized sound input	*
A0h	Set input mode to mono	*
A8h	Set input mode to stereo	*
D0h	Pause 8bit DMA mode digitized sound I/O	o
D1h	Turn on speaker	*
D3h	Turn off speaker	*
D4h	Continue 8bit DMA mode digitized sound I/O	o
D8h	Get speaker status	*
DAh	Exit 8bit auto-init DMA mode digitized sound I/O	o
E1h	Get DSP version number	o

Note: 1)The commands marked "*" are performed in state-machine, but they are not effective.

2)Additional undocumented commands are included.

8-1-2-2. Sound Blaster Pro Mixer

The table below is the register map of mixer of Sound Blaster Pro.

Index	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset Mixer							
04h	Voice Vol. Lch			-	Voice Vol. Rch			
0Ah	-	-	-	-	-	MIC Vol.		-
0Ch	-	-	Input Filter	-	Low Pass Filter	Input Source		-
0Eh	-	-	Output Filter	-	-	-	Stereo SW	-
22h	Master Vol. Lch			-	Master Vol. R			-
26h	MIDI Vol. Lch			-	MIDI Vol. Rch			-
28h	CD Vol. Lch			-	CD Vol. Rch			-
2Eh	Line Vol. Lch			-	Line Vol. Rch			-

The bit remarked ▒▒▒ indicates that these can be read and written but not effective.

The actual value written to the Master Vol.,MIDI Vol.,CD Vol. and Line Vol. is based on the table shown below. And when read, actual value cannot be read and written value to each register is read instead.

Table

		Voice Vol. (04h), CD Vol. (28h), Line Vol. (2Eh)							
		0	1	2	3	4	5	6	7
Master Volume (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-28.5dB	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB
	2	mute	-22.5dB	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB
	3	mute	-16.5dB	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB
	4	mute	-10.5dB	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB
	5	mute	-7.5dB	-3.0dB	0dB	0dB	0dB	0dB	0dB
	6	mute	-3.0dB	0dB	0dB	0dB	0dB	0dB	0dB
	7	mute	0dB	0dB	0dB	0dB	0dB	0dB	0dB

8-1-3. CS4231 compatible 16-bit CODEC

The follwings are the I/Os for Window Sound System compatibility.

WSS base	(R)	WSS Configuration Register port
WSS base + 3h	(R)	WSS Status Register port
WSS base + 4h	(R/W)	WSS CODEC Direct Register Index address port
WSS base + 5h	(R/W)	WSS CODEC Direct Register Index data port
WSS base + 6h	(R/W)	WSS CODEC Direct Register Status port
WSS base + 7h	(R/W)	WSS CODEC Direct Register PIO Data port

WSS Configuration Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+0h	"0"	"0"	IRQ			DMA		

This register is used to indicate what resources is assigned and it is read only register.

IRQ:

"0": No interrupt channel is available
"1": IRQ7 is available
"2": IRQ9 is available
"3": IRQ10 is available
"4": IRQ11 is available
"5"-"7": reserved

DMA:

"0": No DMA channel is available
"1": DMA0
"2": DMA1
"3": DMA3
"4"-"7": reserved

Notice:

In the case that CODEC is in Dual DMA mode, only playback DMA channels are valid and recording DMA channels are ignored.

WSS Status Register (RO):

port	D7	D6	D5	D4	D3	D2	D1	D0
+03h	SBHC	"0"	"04h"					

WSS CODEC Direct Registers (R/W):

port	D7	D6	D5	D4	D3	D2	D1	D0
+4h	INIT	MCE	TRD	Index Address				
+5h	Index Data							
+6h	CU/L	CL/R	CRDY	SER	PU/L	P/R	PRDY	INT
+7h	PIO Data							

12h:LineL = 88h

13h:LineR = 88h

1Ah:MonoIn = C0h

8-1-4. MPU401

The followings are the I/Os for MPU401 compatibility.

MPU base	(R/W)	MIDI Data port
MPU base +1	(R)	Status Register port
MPU base + 1	(W)	Command Register port

8-1-5. OPL3-SA2 control register

This register is used to control the additional functions (ex. power management).

CTRL base	(R/W)	Control Register Index port
CTRL base +1	(R/W)	Control Register Data port

Power Management (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
01h	SRST	-	-	CLKO	FMPS	PSV	PDN	PDX

SRST (Software reset)... When set to "1", only CODEC portion is reset.

CLKO... When set to "1", Master Clock(33.8688MHz) is disable, which appears on the pin MP9(SEL=3,4,7).

FMPS... Setting this bit to"1" makes the OPL3 portion in power down mode, when /EXTEN="0" or VZE="1".
When set to "0", normal operations active.

PSV (power save)... Setting this bit to "1" makes OPL3-SA2 in power save mode that is categorized into two types.

Power save mode 1

where PSV=PDX="1", clock oscillation is disabled and power dissipation of digital portion becomes about 1/200 of that in normal operation, and that of analog portion becomes one tenth of that in normal operation.

Power save mode 2

where PSV="1" and PDX=0, clock oscillation is active. However power dissipation of digital portion becomes about one fifth of that in normal operation, and that of analog portion becomes one tenth of that in normal operation.

PDN (Power down)... Setting this bit to "1" makes OPL3-SA2 in power down mode.

PDX (Oscillation stop)... Setting this bit to "1" makes the clock oscillation of OPL3-SA2 halt.

default:00h

DMA configuration (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
	DMA-B				DMA-A			
06h	-	SB	WSS-R	WSS-P	-	SB	WSS-R	WSS-P

There are three devices (WSS-P (Windows Sound System CODEC playback), WSS-R (Windows Sound System CODEC recording) ,SB (Sound Blaster playback)) that may use a DMA channel. However 2 DMA channels (DMAA and DMAB) are available at maximum, this register specifies which device is routed to the physical DMA channels. And the device written to "1" is assigned to the corresponding DMA channel.

default:61h

DMA-A: WSS-P

DMA-B: WSS-R + SB

Notice)

Do not assign a device to both DMA-A and DMA-B.

Master Volume Lch (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
07h	MVLM	-	-	-	MVL3	MVL2	MVL1	MVL0

This register specifies the master volume of left channel.

MVLM... Setting to "1" to this bit makes Master Volume Left Channel muted.

MVL3-0... These bits determine the attenuation level of Master Volume Left Channel by -2dB step. When all bits are set to "0", volume is maximum(0dB) and when all bits are set to "1", volume is minimum (-30dB).

default: 07h (-14dB)

Notice)

During the power on reset and power down/save mode, master volume is automatically muted. In resuming from power down/save mode, it is still muted.

Master Volume Rch (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
08h	MVRM	-	-	-	MVR3	MVR2	MVR1	MVR0

This register specifies the master volume of left channel.

MVRM... Setting to "1" to this bit makes Master Volume Right Channel muted.

MVR3-0... These bits determine the attenuation level of Master Volume Right Channel by -2dB step. When all bits are set to "0", volume is maximum (0dB) and when all bits are set to "1", volume is minimum (-30dB).

default: 07h (-14dB)

Notice)

During the power on reset and power down/save mode, master volume is automatically muted. In resuming from power down/save mode, it is still muted.

8-2. Joystick

port	D7	D6	D5	D4	D3	D2	D1	D0
xxh	JBB2	JBB1	JAB2	JAB1	JBCY	JBCX	JAXY	JACX

JACX... Joystick A, Coordinate X
JACY... Joystick B, Coordinate Y
JBCX... Joystick A, Coordinate X
JBCY... Joystick B, Coordinate Y
JAB1... Joystick A, Button 1
JAB2... Joystick A, Button 2
JBB1... Joystick B, Button 1
JBB2... Joystick B, Button 2

8-3. MODEM

The following pins are for MODEM interface with PnP supported.

/MCS... chip select (eight consecutive byte I/O)
MIRQ... interrupt signal

And MIN is the analog input to mix the telephone line.

MIN... analog input

8-4. CD-ROM

The following pins are for IDE CD-ROM interface with PnP supported.

/CDCS0... chip select for CD-ROM
/CDCS1... chip select for CD-ROM
CDIRQ... interrupt signal

Other signals needed for CD-ROM must be generated by the external PALs,which is described in chapter 1-3.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CMOS Output pins						
High Level Output Voltage 2	V_{OH2}	I_{OH}=2mA	0.8V_{DD}			V
Low Level Output Voltage 2	V_{OL2}	I_{OL}=2mA			0.4	V
Output Leakage Current	O_L	Hi_Z:V_{IN}=V_{SS},V_{DD}	-10		10	μ A
Output Capacitance	C_O				10	pF

Note:DV_{SS}=AV_{SS}=0[V], T_{OP}=0～70℃, DV_{DD}=5.0±0.25[V]

AC Characteristics (Digital)

CPU Interface & DMA BUS Cycle :Fig.13-1,2,3,4,5,6,7,8

Item	Symbol	Min.	Typ.	Max.	Unit
/DACK inactive to /IOW,/IOR falling edge	t_{AKS}	50			ns
/DACK active from /IOW,/IOR rising edge	t_{AKH}	10			ns
Address set up to /IOW,/IOR active	t_{AS}	40			ns
Address hold to /IOW,/IOR inactive	t_{AH}	10			ns
/IOW Wirte Pulse Width	t_{WW}	90			ns
Write Data set up to /IOW active	t_{WDS}	20			ns
Write Data hold to /IOW inactive	t_{WDH}	10			ns
/IOR Read Pulse Width	t_{RW}	90			ns
Read Data access time	t_{ACC}			80	ns
Read Data hold from /IOR inactive	t_{RDH}	0			ns
DRQ hold from /IOW,/IOR falling edge	t_{DGH}	0		20	ns
/DACK set up to /IOW,/IOR falling edge	t_{SF}	25			ns
/DACK hold to /IOW,/IOR rising edge	t_{HR}	25			ns
Time between rising edge of /IOW,/IOR to next falling edge of /IOW,/IOR	t_{NX}	100			ns
Valid Address from /SYNCS or /MCS or /CDCS1-0	t_{EX1}			40	ns
/SYNCS or /MCS or /CDCS1-0 hold to Valid Address	t_{EX2}			20	ns
RESET Pulse Width	t_{RST}	9			μ s

Note:DV_{SS}=AV_{SS}=0[V], T_{OP}=0～70℃, DV_{DD}=5.0±0.25[V]

I/O Write Cycle

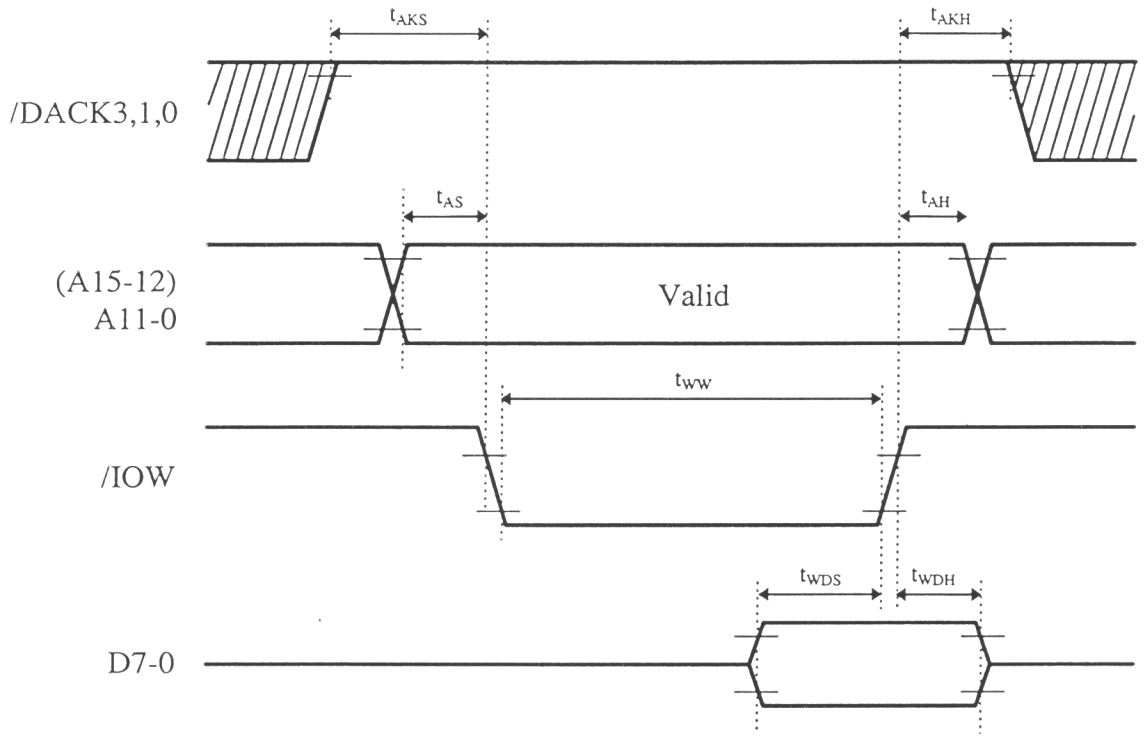


Fig.1

I/O Read Cycle

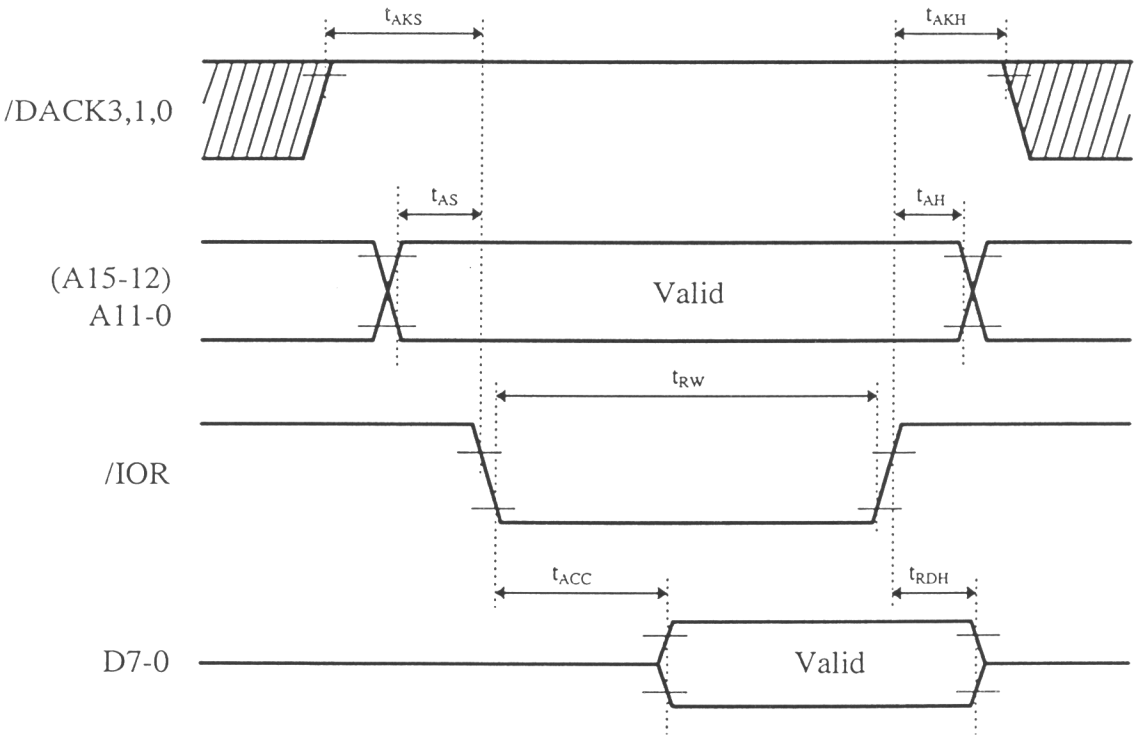


Fig.2

8bit Stereo or 16bit Mono DMA Cycle

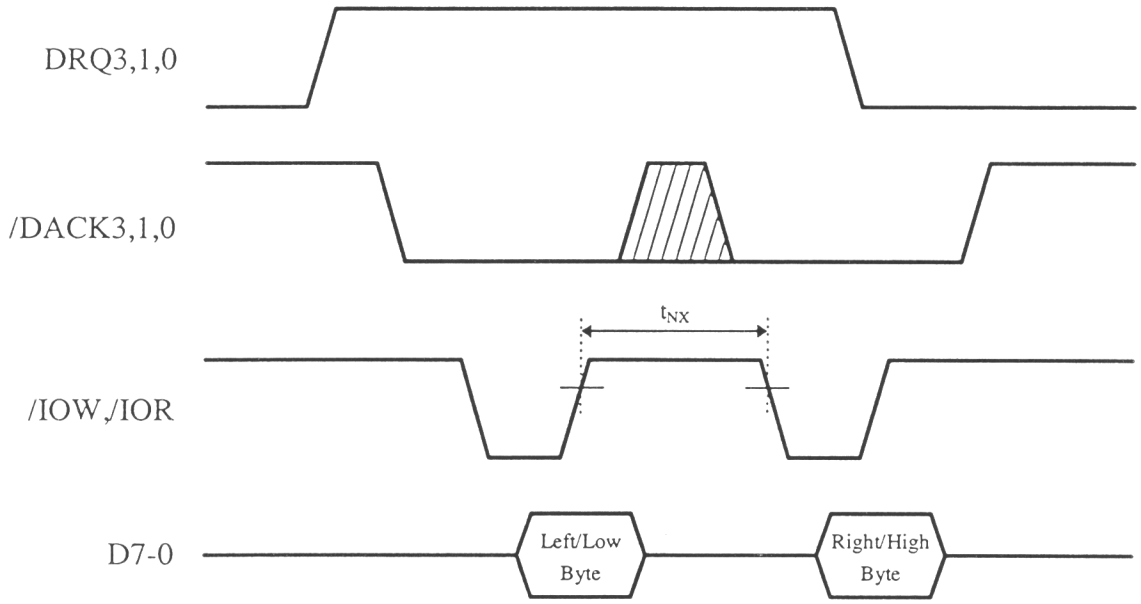


Fig.5

16bit Stereo DMA Cycle

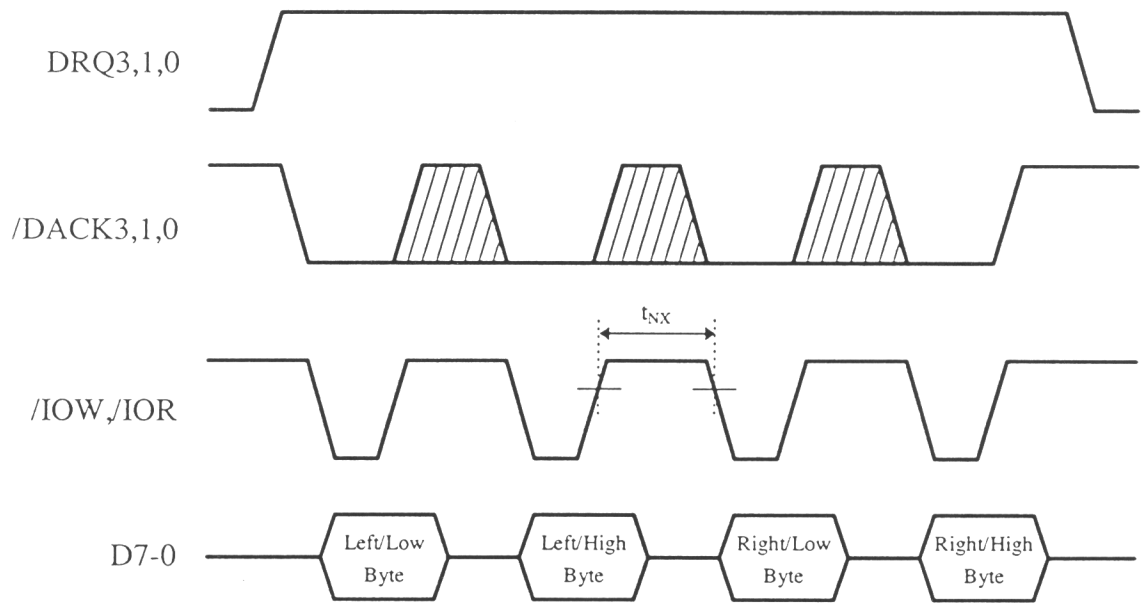


Fig.6

Analog Characteristics

Analog Input Characteristics

Item	Condition	Min.	Typ.	Max.	Unit
Full Scale V_Input					
· LINE/AUX1,2/MIN/MIC		2.5	2.8	3.1	Vpp
· MIC	+20dB	0.25	0.28	0.31	Vpp
ADC Resolution		16			bit
Recording Path(ADC)					
Dynamic Range					
· LINE/AUX1,2/MIN/MIC			80		dB
· MIC	+20dB		75		dB
Distortion			0.05		%
Interchannel Isolation		70			dB
L/R Channel Separation		70			dB
Gain Mismatch	from Spec.			0.5	dB
Frequency Response	20 to 15kHz	-3.0		0.5	dB
Input Resistance		20		100	k Ω
Input Capacitance				15	pF

Note:$DV_{SS}=AV_{SS}=0$[V], $T_{OP}=0\sim70$℃, $DV_{DD}=AV_{DD}=5.0$[V]

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Analog Output Characteristics

Item	Condition	Min.	Typ.	Max.	Unit
Full Scale Line Output					
· OLB=1		2.4	2.8	3.1	Vpp
· OLB=0		1.7	2.0	2.2	Vpp
DAC Resolution					
· WSS DAC		16			bit
· SB_DAC		8			bit
· FM_DAC		16			bit
Frequency Response					
· WSS_DAC	10 to 17.4 kHz	-0.5		0.5	dB
· SB_DAC	10 to 15 kHz	-3.0		0.5	dB
· FM_DAC	10 to 15 kHz	-3.0		0.5	dB
Mix_path Total					
Dynamic Range					
· from Input			85		dB
· from WSS_DAC			80		dB
· from SB_DAC			50		dB
Distortion					
· from Input			0.01		%
· from WSS_DAC			0.05		%
· from SB_DAC			0.30		%
FM Floating DAC					
· Dynamic Range			85		dB
· Distortion			0.30		%
Interchannel Islolation		70			dB
L/R Channel Separation		70			dB
Gain Mismatch	from Spec.			0.5	dB
Mute Attenuation		-80			dB
VREFO Voltage output		2.0	2.2	2.4	V

Note:DV_{SS}=AV_{SS}=0[V], T_{OP}=0～70℃, DV_{DD}=AV_{DD}=5.0[V]

External Interface (External Synthesizer, CD ROM, Modem)

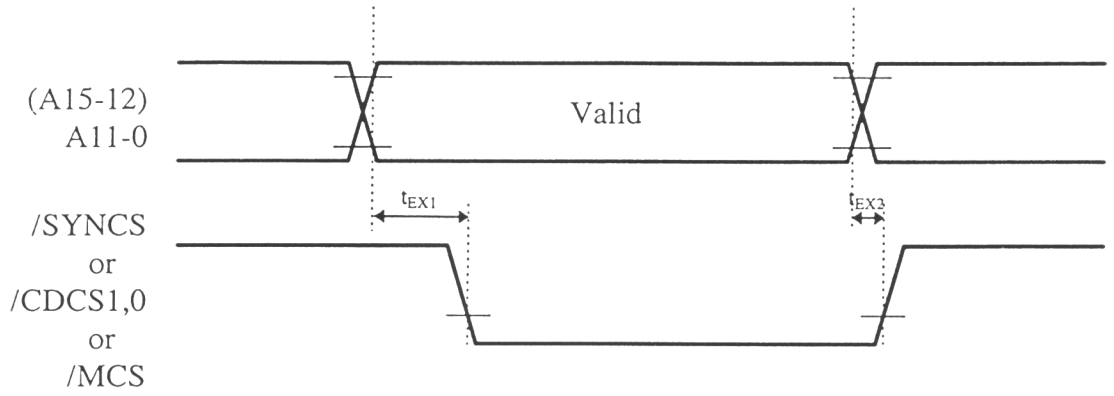


Fig.7

Reset Pulse Width

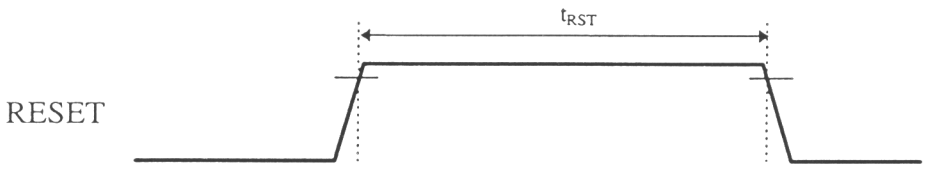


Fig.8

Serial Audio Interface

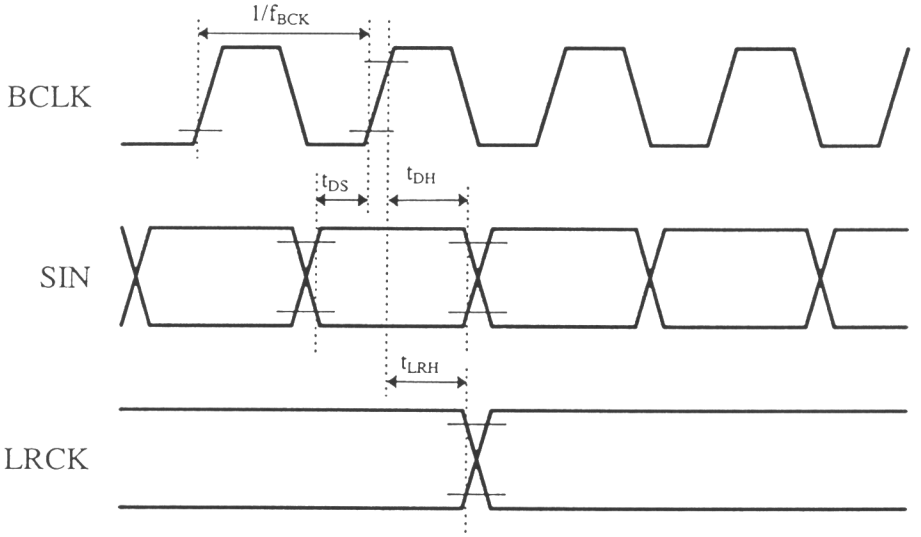


Fig.9

8bit Mono & ADPCM DMA Write Cycle

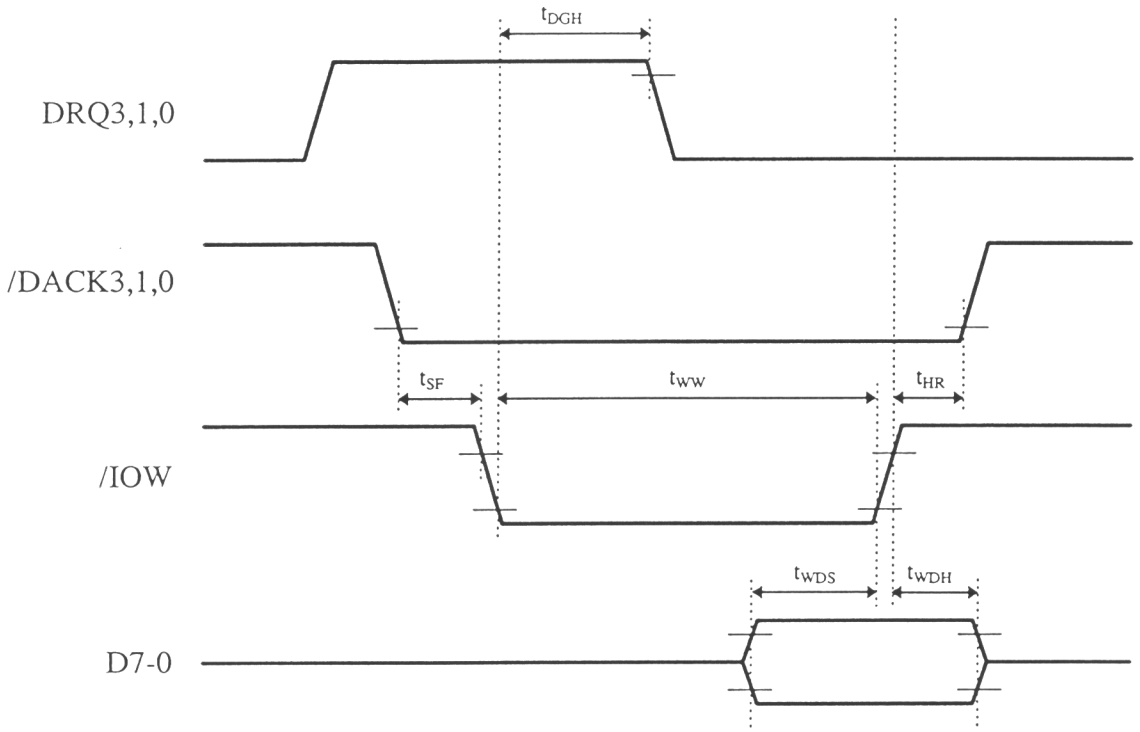


Fig.3

8bit Mono & ADPCM DMA Read Cycle

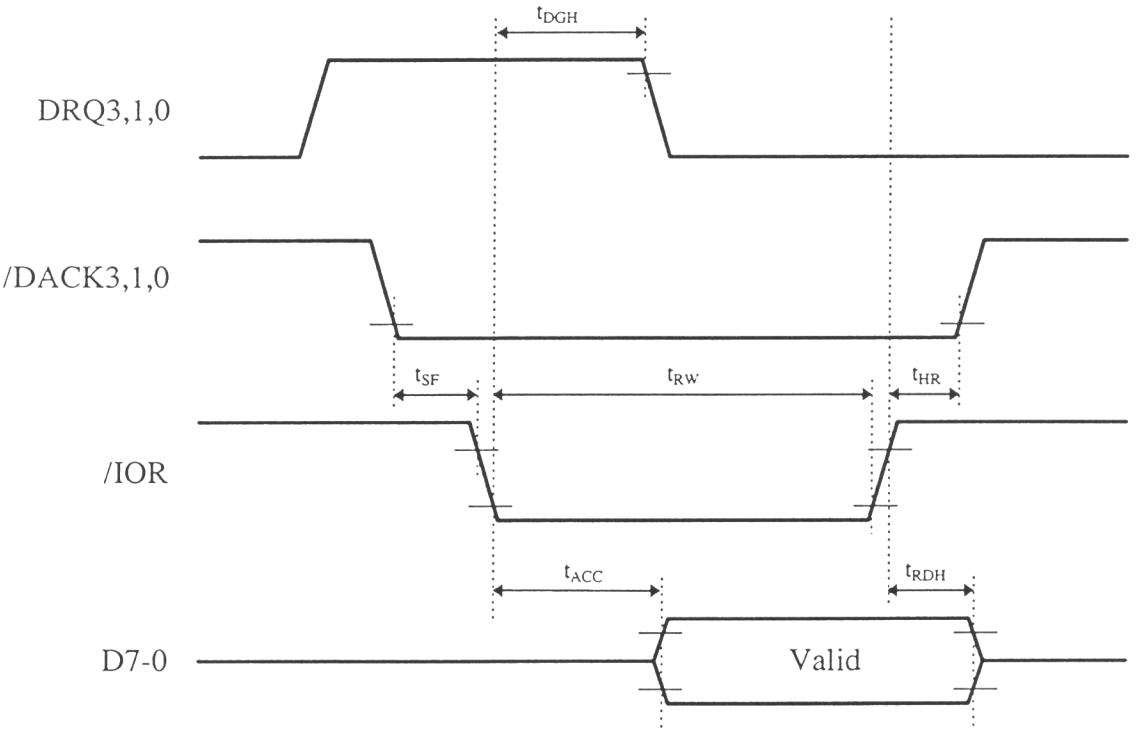


Fig.4

Serial Audio (Zommed Video) Interface Input :Fig.9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCLK Cycle	f_{BCK}		32fs	48fs	64fs	kHz
BCLK Duty	D_{BCLK}		40	50	60	%
LRCK Hold Time	t_{LRH}	BCLK ↑ /LRCK	-120		120	ns
SIN Set up Time	t_{DS}	BCLK ↑ /SIN	20			ns
SIN Hold Time	t_{DH}	BCLK ↑ /SIN	20			ns
CLKO Frequency	f_{CLKO33}			33.8688		MHz
CLKO Duty	D_{CLKO33}	f_{33}=50%	40	50	60	%

Note:DV_{SS}=AV_{SS}=0[V], T_{OP}=0～70℃, DV_{DD}=5.0±0.25[V]

Duty Serch Point is 1/2 V_{DD}

Miscellaneous

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock Frequency	f_{33}	DV_{DD}=5.0±0.25[V]		33.8688		MHz
(X'tal 33) Duty	D_{f33}	DV_{DD}=3.3±0.3[V]	40	50	60	%
Master Clock Frequency	f_{24}	DV_{DD}=5.0±0.25[V]		24.5760		MHz
(X'tal 24) Duty	D_{f24}	DV_{DD}=3.3±0.3[V]	40	50	60	%
Power Consumption	P_{OP1}	DV_{DD}=5.0[V]		450	500	mW
(Normal)	P_{OP2}	DV_{DD}=3.3[V]		300	350	mW
Power Supply Current (Power Down Mode)	Mode1-1	DV_{DD}=5.0±0.5[V]		5		mA
	Mode1-2	DV_{DD}=3.3±0.3[V]		5		mA
	Mode2-1	DV_{DD}=5.0±0.5[V]		300		μA
	Mode2-2	DV_{DD}=3.3±0.3[V]		200		μA

Note:DV_{SS}=AV_{SS}=0[V], T_{OP}=0～70℃, AV_{DD}=5.0[V]

Duty Serch Point is 1/2 V_{DD}

Mode1: Power Save 1 (Clock oscillation is disabled)

Mode2: Power Down

■ Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Power Supply Voltage (Analog/Digital)	V_{DD}	V_{SS}-0.5	V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.3	V_{DD}+0.3	V
Input Current	I_{IN}	-20	20	mA
Storage Temperature	T_{STG}	-50	125	℃

Note: $V_{DD}=DV_{DD}=AV_{DD}$, $V_{SS}=DV_{SS}=AV_{SS}=0$[V]

Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Power Supply 1	(Analog)	AV_{DD}	4.75	5.00	5.25	V
5.0V Spec.	(Digital)	DV_{DD}	4.75	5.00	5.25	V
Power Supply 2	(Analog)	AV_{DD}	4.75	5.00	5.25	V
3.3V Spec.	(Digital)	DV_{DD}	3.00	3.30	3.60	V
Operating Ambient Temperature		T_{OP}	0	25	70	℃

Note: $DV_{SS}=AV_{SS}=0$[V]

DC Characteristics (Digital)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TTL-Input Pins						
High Level Input Voltage 1	V_{IH1}	Except	2.0			V
Low Level Input Voltage 1	V_{IL1}	schmitt inputs			0.8	V
CMOS-Input Pins						
High Level Input Voltage 2	V_{IH2}		$0.7V_{DD}$			V
Low Level Input Voltage 2	V_{IL2}				$0.2V_{DD}$	V
Schmitt Vt- (H to L)	V_t-		0.8		1.4	V
Schmitt Vt+ (L to H)	V_t+		1.5		2.1	V
Schmitt Hysteresis	V_h		0.4			V
Input Leakage Current	I_L	$V_{IN}=V_{SS},V_{DD}$	-10		10	μA
Input Capacitance	C_I				10	pF
Pull up Register	R_{U1}	RXD	20	50	100	kΩ
	R_{U2}	GP7～4	30	100	200	kΩ
	R_{U3}	Otherwise	50	200	400	kΩ
TTL-Output Pins						
High Level Output Voltage 1	V_{OH1}	$I_{OH1,2,3}$	2.4			V
Low Level Output Voltage 1	V_{OL1}	$I_{OL1,2,3}$			0.4	V
D7～0 pins	I_{OHL1}		24			mA
IRQn, DRQn pins	I_{OHL2}		12			mA
Other pins	I_{OHL3}		2			mA

Note: $DV_{SS}=AV_{SS}=0$[V], $T_{OP}=0$～70℃, $DV_{DD}=5.0\pm0.25$[V]

MIC Volume (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
09h	MICM	-	-	MCV4	MCV3	MCV2	MCV1	MCV0

This register specifies the master volume of MIC.

MICM... Setting to "1" to this bit makes Mic Volume muted.

MCV4-0... These bits determine the gain level of Mic volume by -1.5dB step. When all bits are set to "0", volume is maximum(+12dB) and when all bits are set to "1", volume is minimum (-34.5dB).

default:88h

Miscellaneous:

Index	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	VEN	-	-	MCSW	MODE	VER2	VER1	VER0

VEN... This bit enables the hardware volume control.

MCSW... This bit determines whether Mic input or internal mono output is fed to MUX of Rch Mic that is connected to A/D. This will be useful to support the echo cancellation.

MODE... This bit indicates the SB or WSS mode.If MODE=0, it is the SB mode.This bit is read only.

VER2-0... These bits indicate the version of OPL3-SA2 and read only (VER2=VER1="0", VER0="1").

default:81h

CODEC Base counter (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	Playback Base Counter (Low)							
0Ch	Playback Base Counter (High)							
0Dh	Recording Base Counter (Low)							
0Eh	Recording Base Counter (High)							

These registers reflects the content of Base Counter used for DMA transfer. Initial value is FFh and whenever the Playback Base register and Recording Base register of CODEC is set , its value is loaded into these registers and decremented by one sample transferred.

The DMA counter is set by writing these registers. When high byte is written, actual value is loaded to these register.

These registers are used mainly to support the suspend/resume feature that is very important for Notebook PC application.

Set the value that is calculated by inverting all bits after subtracting one from the actual value to be transferred.(2's complement)

System control (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
02h	SBHE	-	-	-	-	IDSEL1	IDSEL0	VZE

SBHE... When AT-bus is used,set to "0" and set to "1" in case of XT-bus.

IDSEL1, IDSEL0... These two bits specify the DSP version of Sound Blaster.

VZE... I^2S audio format can be fed to BCLK(ZV),LRCK(ZV),SIN(ZV) pins of OPL3-SA2 by setting this bit to "1" regardless of the /EXTEN,when Zoomed Video port is in use.

default:00h

Interrupt Channel configuration (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
03h	IRQ-B				IRQ-A			
	OPL3	MPU	SB	WSS	OPL3	MPU	SB	WSS

There are four devices (WSS (Windows Sound System CODEC),SB (Sound Blaster),OPL3,MPU (MPU401)) that can be an interrupt source. This register specifies what interrupt source is routed to two physical interrupt (IRQA and IRQB) of OPL3-SA2. The device written to "1" is assigned to the corresponding interrupt. And by writing all "1" to upper or lower half byte, it is possible to share all interrupt sources to a single physical interrupt line.

default:69h

IRQ-A: WSS + OPL3

IRQ-B: SB + MPU401

Notice)

Do not assign a device to both IRQA and IRQB.

Interrupt (IRQ-A) status (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
04h	-	-	OPL3	MPU	SB	TI	CI	PI

This register is the status register that indicates which is the interrupt source of IRQA. When an interrupt occurs, the corresponding bit becomes "1" and its flag is cleared when the interrupt routine is completed. This register is not cleared by writing to this register.

CI: recording flag of CODEC

PI: playback flag of CODEC

TI: timer flag of CODEC

Interrupt (IRQ-B) status (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
05h	-	-	OPL3	MPU	SB	TI	CI	PI

This register is the status register that indicates which is the interrupt source of IRQB. When an interrupt occurs, the corresponding bit becomes "1" and its flag is cleared when the interrupt routine is completed. This register is not cleared by writing to this register.

CI: recording flag of CODEC

PI: playback flag of CODEC

TI: timer flag of CODEC

WSS CODEC Indirect Registers (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0	Function
00h	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0	Left Inpput Control
01h	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0	Right inpput Control
02h	LX1M	-	-	LX1G	LX1G	LX1G	LX1G	LX1G	Left Aux #1 Inpput Control
03h	RX1M	-	-	RX1G	RX1G	RX1G	RX1G	RX1G	Right Aux #1 Inpput Control
04h	LX2M	-	-	LX2G	KX2G	LX2G	LX2G	LX2G	Left Aux #2 Inpput Control
05h	RX2M	-	-	RX2G	RX2G	RX2G	RX2G	RX2G	Right Aux #2 Inpput Control
06h	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0	Left Output Control
07h	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0	Right Output Control
08h	FM1	FM0	C/L	S/M	CFS2	CFS1	CFS0	CSL	Playback data
09h	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN	Interface Configratiion
0Ah	XTL1*	XTL0*	-	-	-	-	IEN	-	Pin Control
0Bh	COR	PUR	ACI	DRS	"0"	"0"	"0"	"0"	Test and Intialization
0Ch	MID	MODE	-	-	ID3	ID2	ID1	ID0	Misc. Information
0Dh	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE	Loopback Control
0Eh	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0	Playback Upper Base Register
0Fh	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0	Playback Lower Base Register
10h	OLB	TE	CMCE	PMCE	-	-	-	DACZ	Alternate Feature Enable 1
11h	-	-	-	-	-	-	-	HPF*	Alternate Feature Enable 2
12h	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0	Left Line Input Control
13h	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0	Right Line Input Control
14h	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	Timer Low Byte
15h	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0	Timer High Byte
16h	-	-	-	-	-	-	-	-	Reserved
17h	-	-	-	-	-	-	-	-	Reserved
18h	-	TI	CI	PI	CU	CO	PO	PU	Alternate Feature Status
19h	V2	V1	V0	-	-	CID2	CID1	CID0	Version / ID
1Ah	MIM	-	-	-	MIA3	MIA2	MIA1	MIA0	Mono Input & Output
1Bh	-	-	-	-	-	-	-	-	Reserved
1Ch	FMT1	FMT0	C/L	S/M	-	-	-	-	Cupture Data Format
1Dh	-	-	-	-	-	-	-	-	Reserved
1Eh	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0	Capture Upper Base Register
1Fh	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0	Capture Upper Base Register

The bit remarked * indicates that these can be read and written but not effective.

Mixer default:

02h:AUX1L = 88h
03h:AUX1R = 88h
04h:AUX2L = 05h
05h:AUX2R = 05h
06h:DACL = 80h
07h:DACR = 80h

		MIDI Vol. (26h)							
		0	1	2	3	4	5	6	7
Master Volume (22h)	0	mute	mute	mute	mute	mute	mute	mute	mute
	1	mute	-24.0dB	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB
	2	mute	-18.0dB	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB
	3	mute	-12.0dB	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB
	4	mute	-6.0dB	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	5	mute	-3.0dB	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	6	mute	+1.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB
	7	mute	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB	+4.5dB

Mixer register

SB Mixer		**WSS Mixer**
MIDI Vol.	→	AUX2 Vol.
CD Vol.	→	AUX1 Vol.
Line Vol.	→	Line Vol.

default

SB Mixer

Master Vol. = (99h)
MIDI Vol. = +4.5dB (99h)
Voice Vol. = 0dB (99h)
CD Vol. = mute (11h)
Line Vol. = mute (11h)

WSS Mixer

AUX2 Vol. = +4.5dB (05h)
AUX1 Vol. = mute (88h)
Voice Vol. = mute (80h)
Line Vol. = mute (88h)
Mono Vol. = mute(MIN,MOUT) (C0h)

SA2 CTRL

Master Vol. = -14dB (07h)
MIC Vol. = mute (88h)

OPL3 Data Register Array 1 (R/W)

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
04h	-	-	CONNECTION SEL					
05h	-	-	-	-	-	*	*	NEW
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

The bit remarked * indicates that these can be read and written but not effective.

8-1-2. Sound Blaster Pro

The followings are the I/Os for Sound Blaster Pro compatibility.

SB base	(R)	OPL3 Status port
SB base	(W)	OPL3 Address port for Register Array 0
SB base + 1h	(R/W)	OPL3 Data register
SB base + 2h	(W)	OPL3 Address port for Register Array 1
SB base + 3h	(R/W)	OPL3 Data port
SB base + 4h	(W)	SB Mixer Address port
SB base + 5h	(R/W)	SB Mixer Data port
SB base + 8h	(R)	OPL3 Status port
SB base + 8h	(W)	OPL3 Address port for Register Array 0
SB base + 9h	(R/W)	OPL3 Data port
SB base + Ah	(R)	DSP Read Data port
SB base + Ch	(R)	DSP Write-buffer status port
SB base + Ch	(W)	DSP Write Command/Data port
SB base + Eh	(R)	DSP Read-buffer status port

8. Register description

8-1. SA Sound System

8-1-1. OPL3

Listed below are the OPL3-L register for AdLib compatibility.

AdLib base	(R)	Status Register port
AdLib base	(W)	Address port for Register Array 0
AdLib base + 1	(R/W)	Data port
AdLib base + 2	(W)	Address port for Register Array 1
AdLib base + 3	(R/W)	Data port

When OPL3-SA2 is used with /EXTEN driven "L" for wavetable upgrade as a chipset with OPL4-ML,additional I/O ports listed below can also be accessed. In case of SB mode, AdLib base + 2, 3 is write only registers.

AdLib base + 4	(R)	Status port for Wavetable Register
AdLib base + 4	(W)	Address port for Wavetable Register
AdLib base + 5	(R/W)	Data port Wavetable Register
AdLib base + 6	(R/W)	reserved
AdLib base + 7	(R/W)	reserved

OPL3 Status Register (RO):

Index	D7	D6	D5	D4	D3	D2	D1	D0
xxh	IRQ	FT1	FT2	-	-	BUSY	-	BUSY

OPL3 Data Register Array 0 (R/W):

Index	D7	D6	D5	D4	D3	D2	D1	D0
00 - 01h	LSI TEST							
02h	TIMER 1							
03h	TIMER 2							
04h	RST	MT1	MT2	-	-	-	ST2	ST1
08h	-	NTS	-	-	-	-	-	-
20 - 35h	AM	VIB	EGT	KSR	MULT			
40 - 55h	KSL		TL					
60 - 75h	AR				DR			
80 - 95h	SL				RR			
A0 - A8h	F-NUM (L)							
B0 - B8h	-	-	KON	BLOCK			F-NUM (H)	
BDh	DAM	DVB	RHY	BD	SD	TOM	TC	HH
C0 - C8h	*	*	CHR	CHL	FB			CNT
E0 - F5h	-	-	-	-	-	WS		

3. Download Resource data

When OPL3-SA2 is in the Configuration state, the host can download the resources data to EEPROM and internal SRAM via 20h: Resource Data Write. To switch OPL3-SA2 into configuration mode, there are two methods.

First method is to use the normal PnP protocol. After CSN was assigned for all ISA cards by PnP soft ware, get CSN from CM (configuration manager) and write the CSN to Wake [CSN], then OPL3-SA2 switches into configuration state.

Second method is to use the YAMAHA Key sequence which is described in the Manual Configuration mode section. After OPL3-SA2 detects YAMAHA key, OPL3-SA2 switches into the Sleep state. Writing "81h" to Wake [CSN] register changes OPL3-SA2 into Configuration state.

After OPL3-SA2 switches into the Configuration state, download the Resource data to EEPROM and internal SRAM by using following sequence.

1. Write "01h" to 21h: Resource Data Write Enable register to reset internal address counter and to enable downloading the data.
2. Write Resource data to 20h: Resource Data Write register until downloading data is completed.
3. Write "00h" to 21h: Resource Data Write Enable register to disable downloading .

4. External EEPROM

The resource data information of OPL3-SA2 used for PnP auto configuration is stored in external EEPROM. And either 256 x 16-bit EEPROM or 128 x 16-bit EEPROM, such as 93C55, 93C56, 93C65, 93C66 should be used.

5. Hardware Volume Control

Two digital input pins; /VOLUP and /VOLDW can control the master volume of OPL3-SA2.

When /VOLUP is low level, register value of master volume is decremented. When the value reaches to "00h", the input signal will not be effective.

When /VOLDW is low level, register value of master volume is incremented. When the value reaches to "0Fh", the input signal will not be effective. Increment and decrement occur at the falling edge of the input signal.

When both of the /VOLUP and /VOLDW are low level simultaneously, volume is muted. However, the register value keeps the previous value. When the rising edge of either /VOLUP and /VOLDW is detected, the previous value becomes effective, and volume is no mute.

6. DAC interface

OPL3-SA2 supports two types of DAC interface format. One is the conventional DAC interface format (very common for the consumer audio product) for OPL4-ML. Another is the I^2S format for Zoomed Video port.

These two types of the formats are shown in the following Fig.6-1,2.

IRQ-A: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	10	7	5,7,9,10,11	<-

IRQ-B: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	5	11	5,7,9,10,11	<-

DMA-A:8bit, count by byte, type-A, B, F

Index	Best	Acceptable1	Acceptable2	Acceptable3
DMA	0	1	0,1,3	<-

DMA-B:8bit, count by byte, type-A, B, F

Index	Best	Acceptable1	Acceptable2	Acceptable3
DMA	1	0,3	0,1,3	<-

(2) LDN=1:Joystick

I/O (Game Port): 16bit address decode

Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	201h	201-20Fh	<-	<-
Length	1	1	<-	<-
Alignment	-	1	<-	<-

(3) LDN=2:MODEM

I/O (/MCS): 16bit address decode

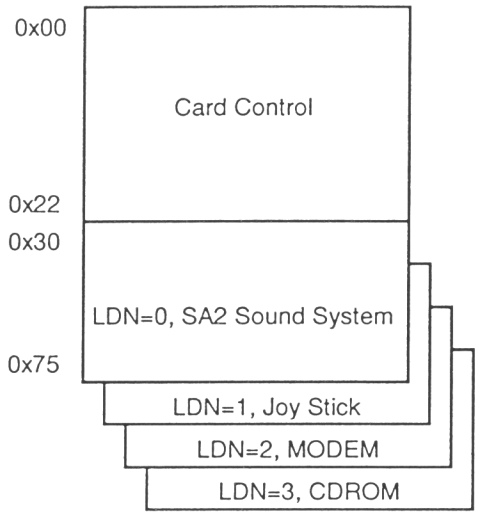
Index	Best	Acceptable1	Acceptable2	Acceptable3
I/O	2F8h	<-	100-FFFh	<-
Length	8	<-	8	<-
Alignment	-	-	8	-

IRQ: high-active, edge-sense

Index	Best	Acceptable1	Acceptable2	Acceptable3
IRQ	3	<-	<-	<-

2-2. PnP ISA Configuration Register

OPL3-SA2 has the following Registers defined in the PnP ISA software.



Listed below is the register map of card control register and logical device registers. For the detailed description of each register, please refer to the *Plug and Play ISA Specification 1.0a*

Card Control Registers

Index	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	W	Set RD_DATA							
01h	R	Serial Isolation							
02h	W	Config Control							
03h	W	Wake [CSN]							
04h	R	Resource Data							
05h	R	Status							
06h	R/W	Card Select Number							
07h	R/W	Logical Device Number							
20h	W	Resource Data Write							
21h	W							IKD	RDWE

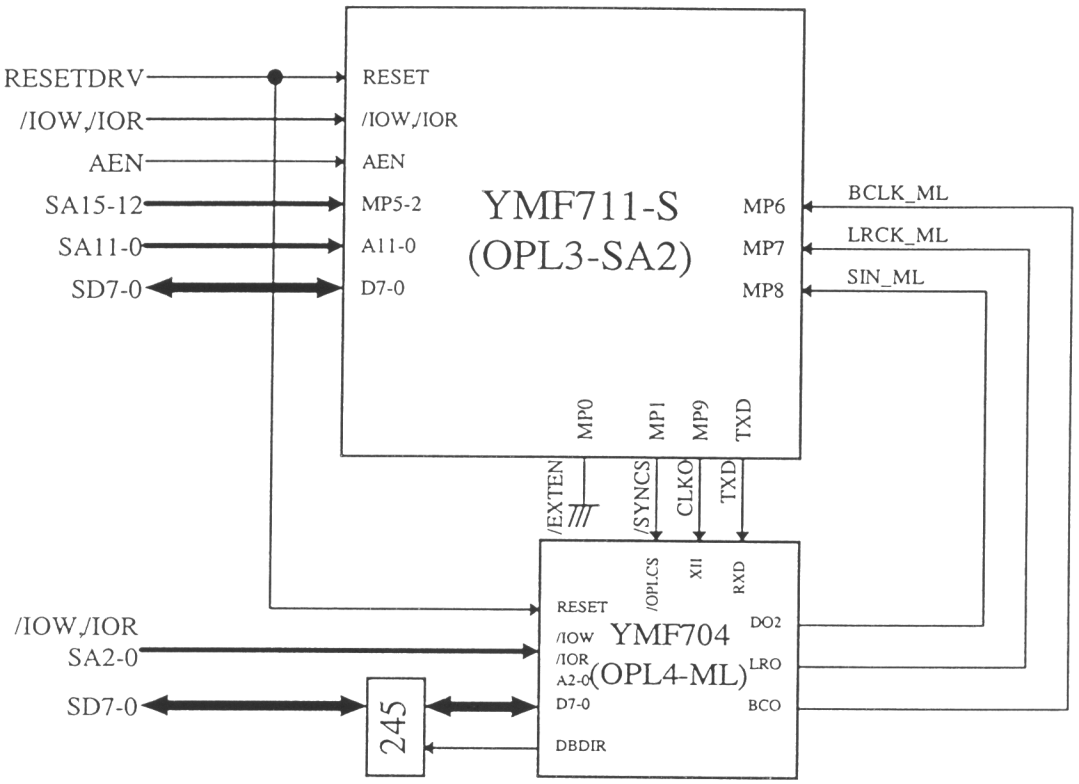
RDWE : Resource Data Write Enable

Setting to "1" this bit means the host can download the resources data to EEPROM and internal SRAM via Card Control Register, index 20h, Resource Data Write.

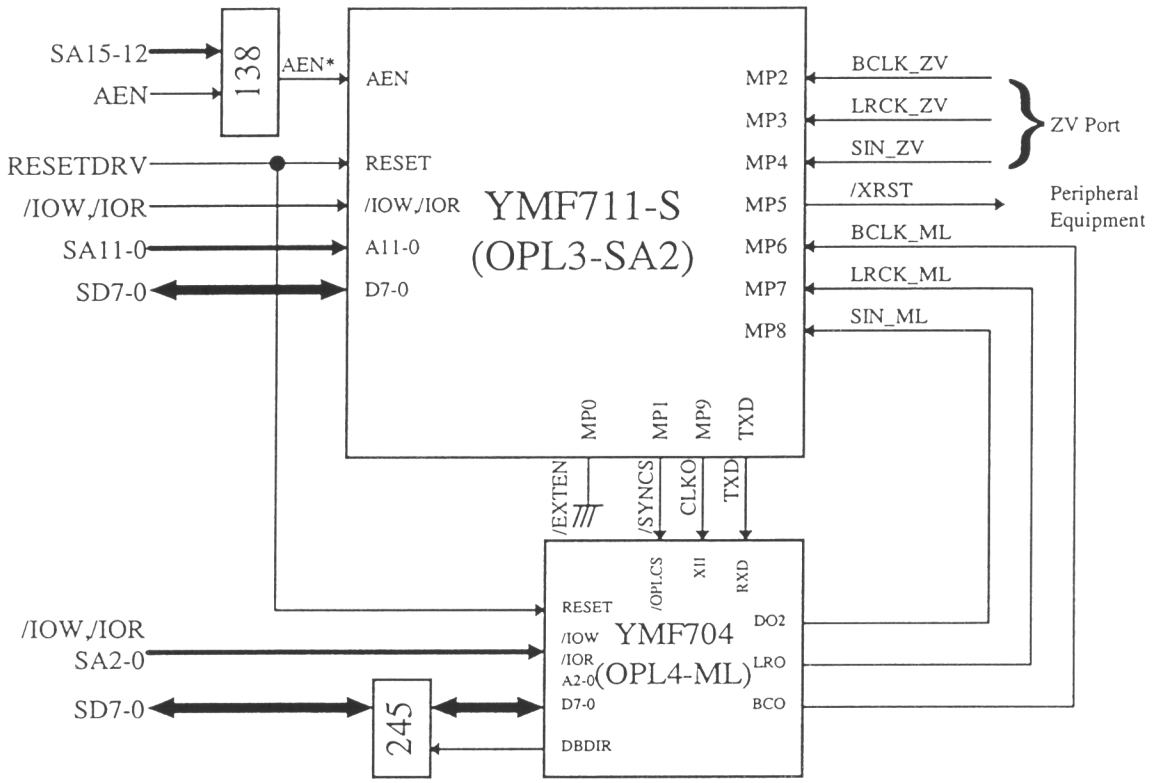
IKD : Initiation Key Disable

Setting to "1" this bit means OPL3-SA2 should not detect the initiation key in the Wait for Key state.

(6) SEL=7 (for Notebook PC,Desktop PC)



(4) SEL=4 (for Notebook PC)



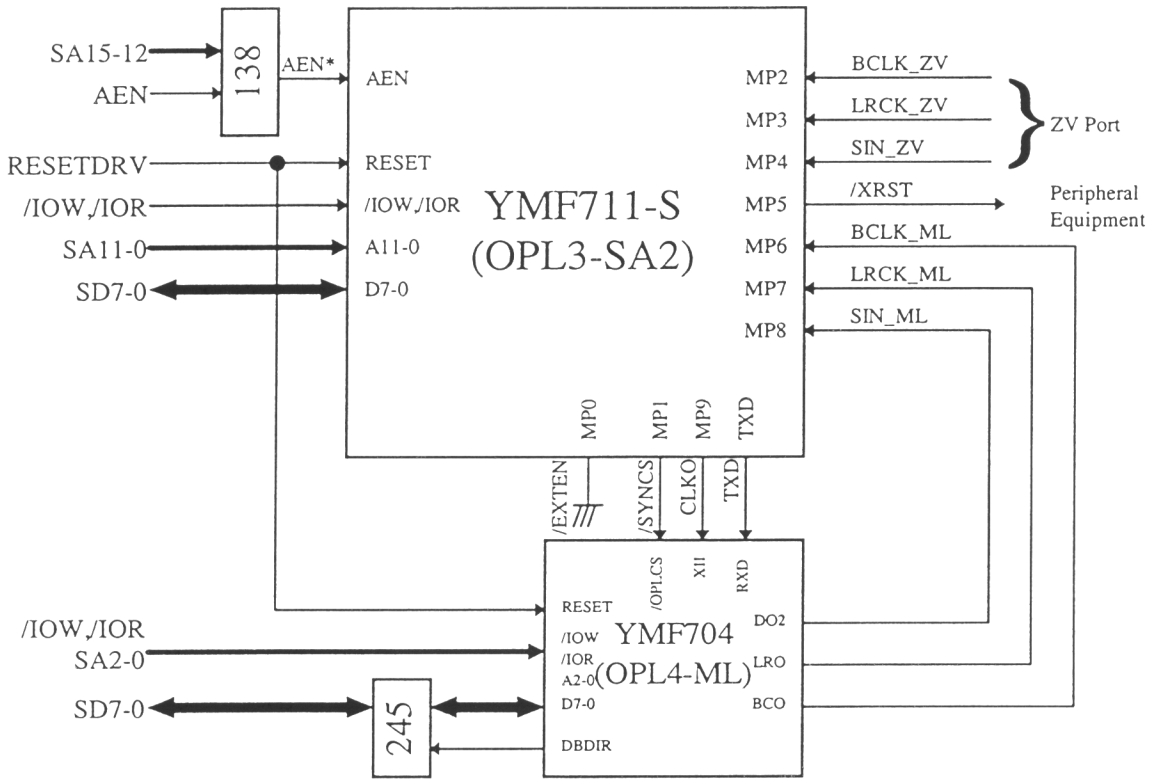
1.ZV Port and YMF704(OPL4-ML) I/F

ZV port is supported by using the internal DAC of YMF711-S(OPL3-SA2) that is originally dedicated for the use of internal OPL3.

(i) either OPL4-ML or ZV port is active at a time and simultaneous use is not possible.

(ii) which function the internal DAC is used for is determined by the SA2 Control register, index 02h, VZE bit.

(4) SEL=4 (for Notebook PC)



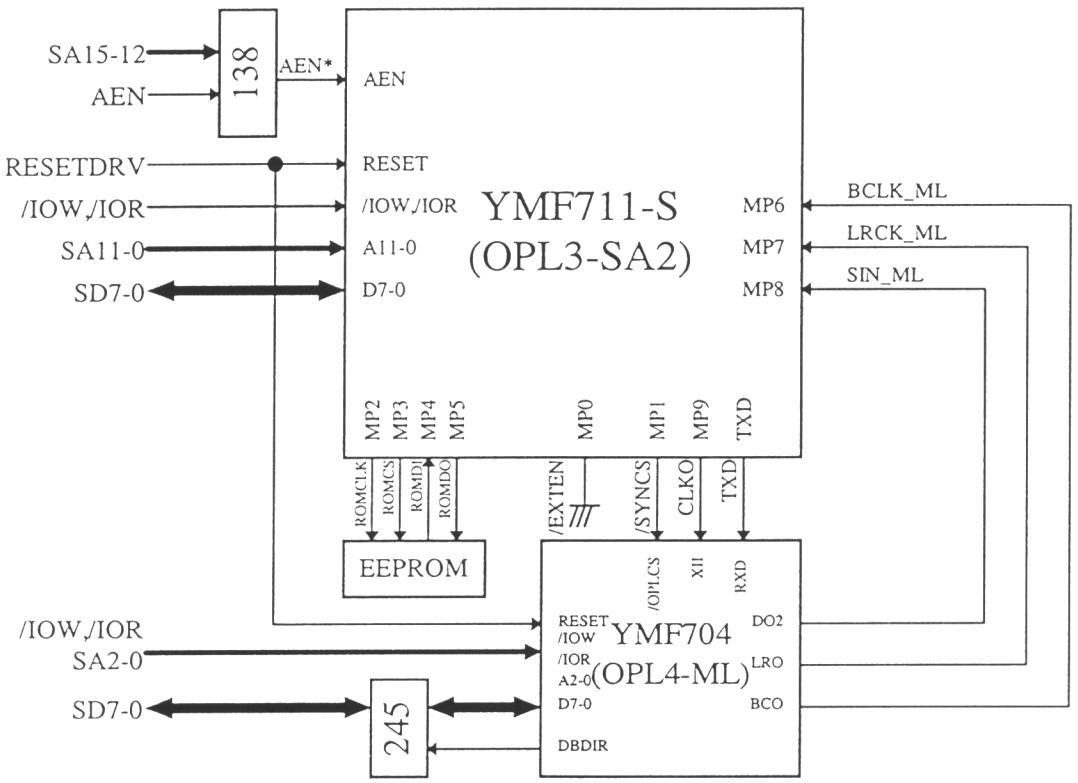
1.ZV Port and YMF704(OPL4-ML) I/F

ZV port is supported by using the internal DAC of YMF711-S(OPL3-SA2) that is originally dedicated for the use of internal OPL3.

(i) either OPL4-ML or ZV port is active at a time and simultaneous use is not possible.

(ii) which function the internal DAC is used for is determined by the SA2 Control register, index 02h, VZE bit.

(3) SEL=3 (Sound Card for Add-in)

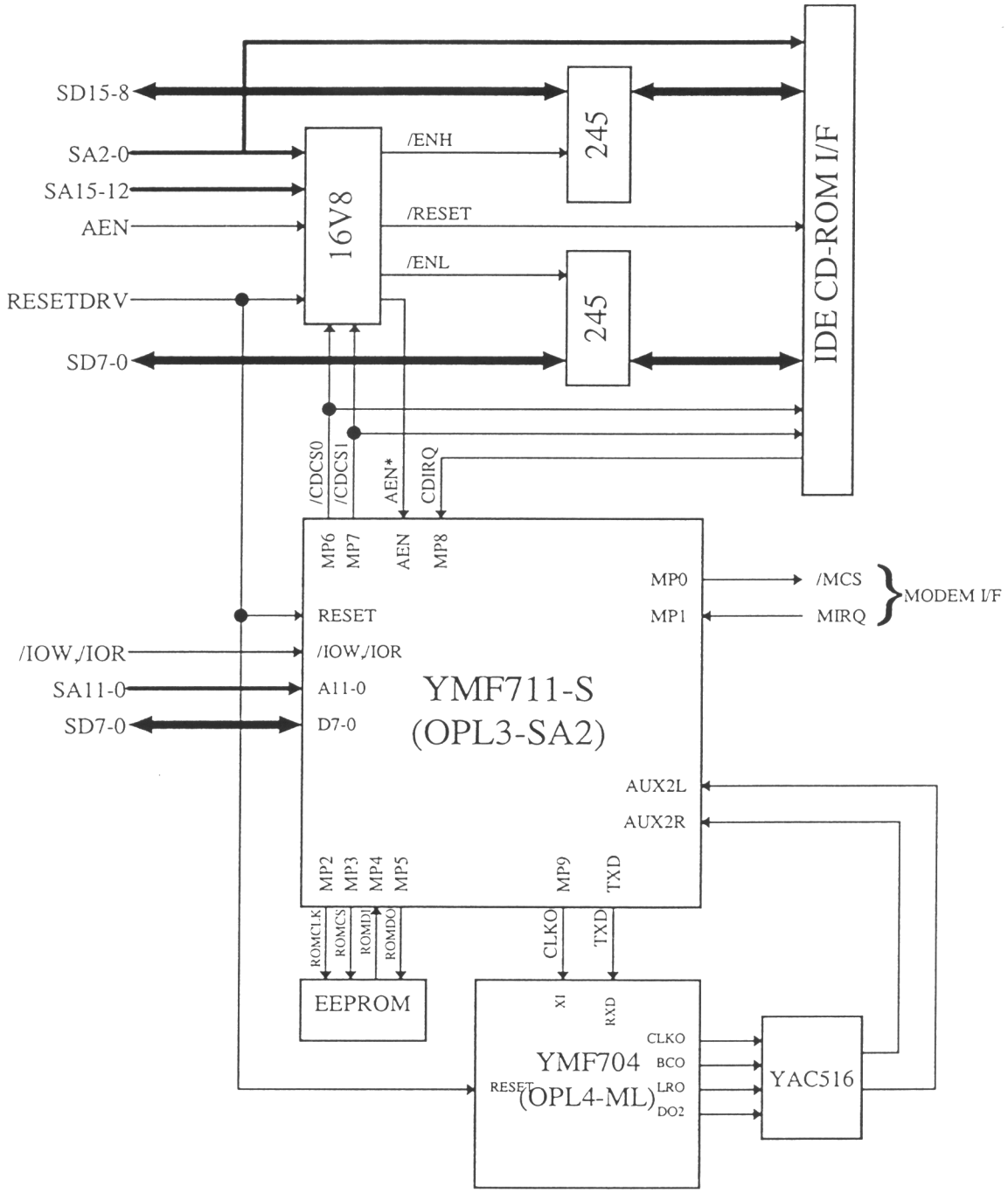


1.16bit Address Decode

The signal AEN* generated by decoding SA15-12 and AEN needs to be connected to the AEN of YMF711-S(OPL3-SA2).

1-3. System Block Diagram

(1) SEL=1 (Sound Card and Combo Card Add-in)



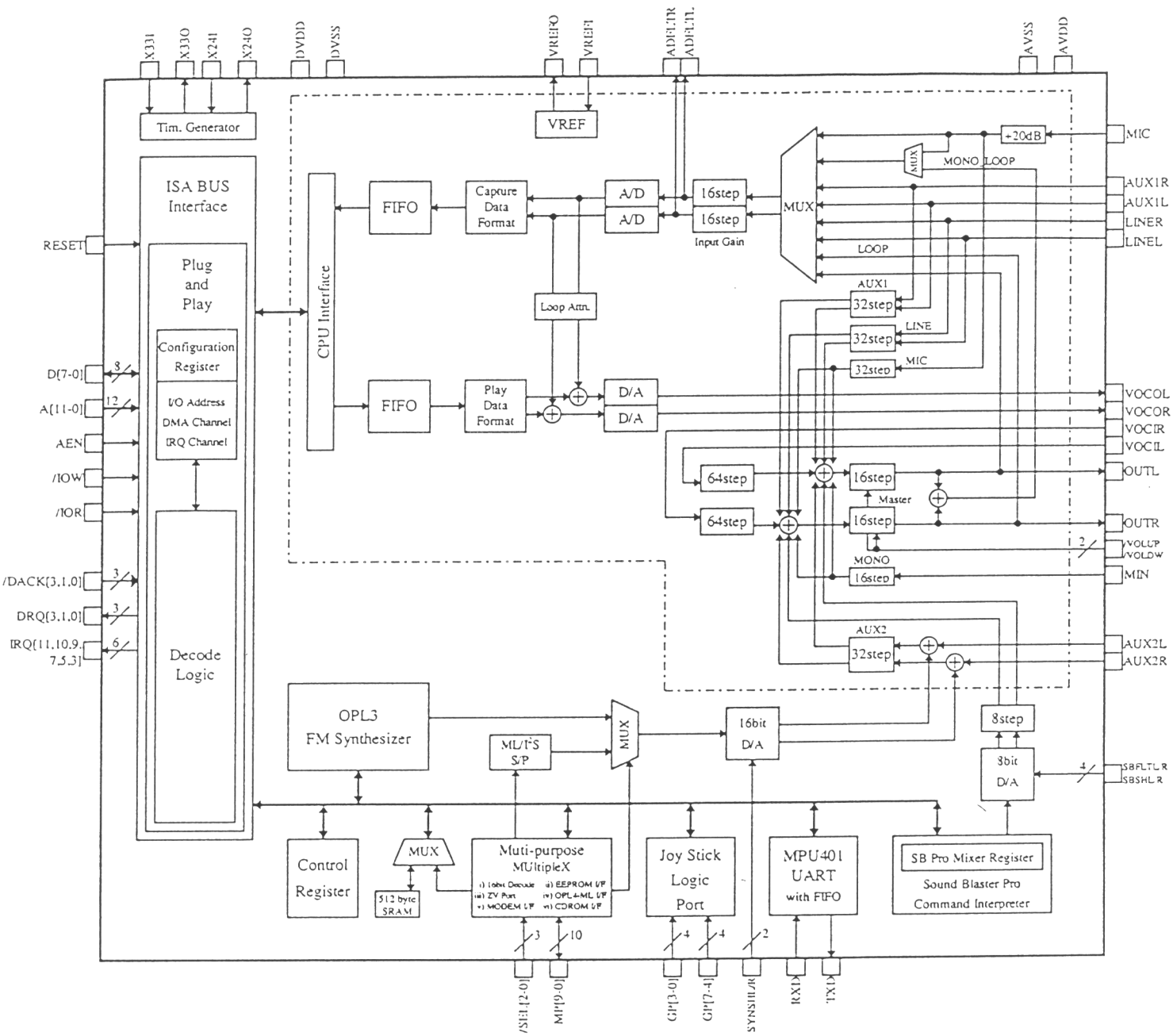
1.External PAL(16V8)

(i) connect the signal AEN* generated by decoding SA15-12 and AEN to the AEN of YMF711-S (OPL3-SA2).

(ii) generate the /G(enable) signal for Data Bus Buffer (LS245) by decoding the /CDCS1-0 and SA2-0.

(iii) generate the /RESET signal from RESETDRV.

■ BLOCK DIAGRAM



Multi-purpose pins : 13 pins					
name	pins	I/O	type	size	function
SEL2-0	3	I+	CMOS	-	Refer to "Multi-purpose pins" section
MP9-0	10	I+/O	TTL	4mA	Refer to "multi-purpose pins" section

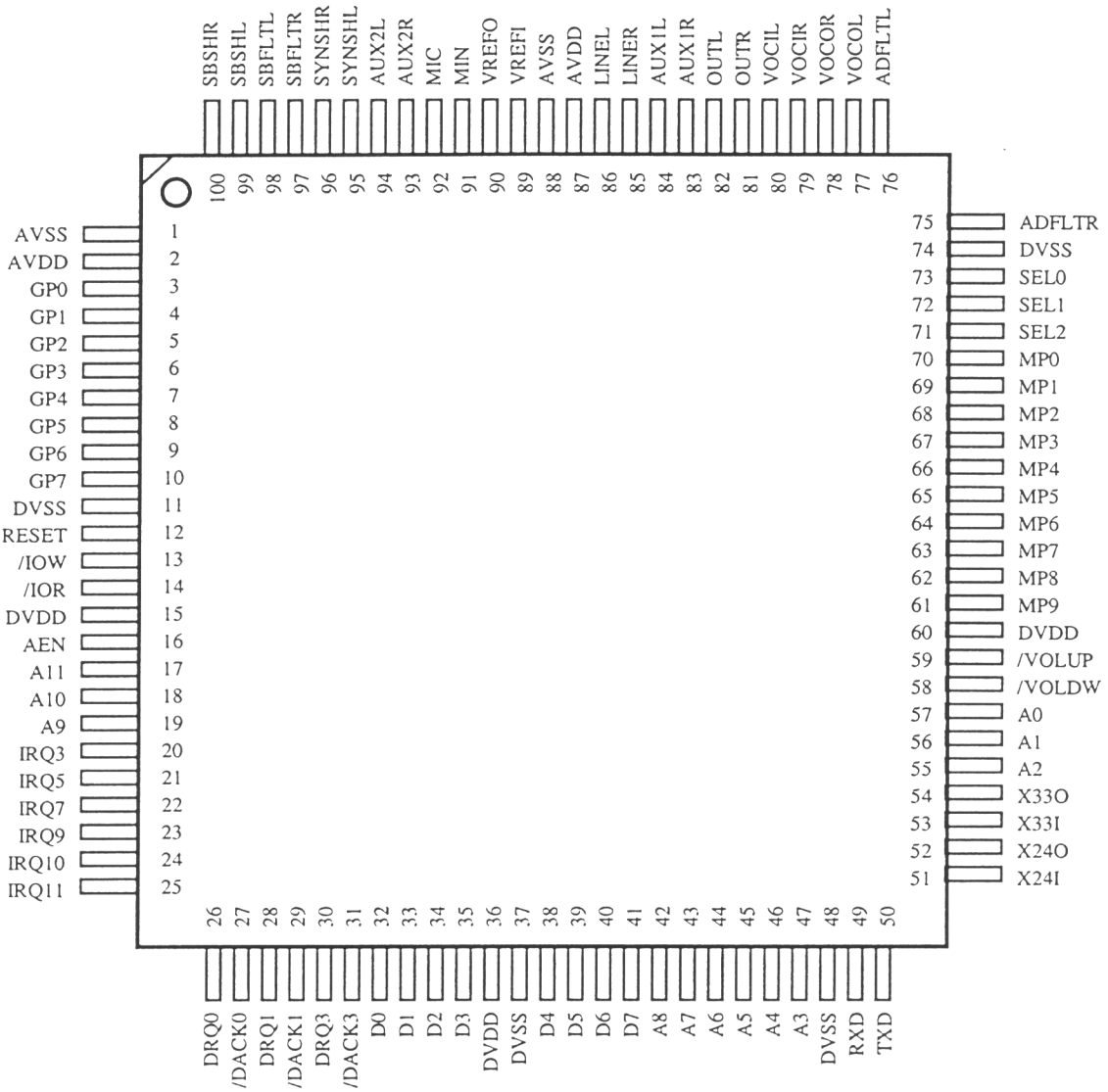
Others : 27 pins					
name	pins	I/O	type	size	function
GP0 - GP3	4	IA	-	-	Game Port
GP4 - GP7	4	I+	Schmitt	-	Game Port
RXD	1	I+	Schmitt	-	MIDI Data Receive
TXD	1	O+	TTL	4mA	MIDI Data Transfer
/VOLUP	1	I+	Schmitt	-	Hardware Volume (Up)
/VOLDW	1	I+	Schmitt	-	Hardware Volume (Down)
X33I	1	I	CMOS	-	33.8688 MHz
X33O	1	O	CMOS	2mA	33.8688 MHz
X24I	1	I	CMOS	-	24.576 MHz
X24O	1	O	CMOS	2mA	24.576 MHz
AVDD	2	-	-	-	Analog Power Supply (put on +5.0V)
DVDD	3	-	-	-	Digital Power Supply (put on +5.0 V or +3.3V)
AVSS	2	-	-	-	Analog GND
DVSS	4	-	-	-	Digital GND

Total : 100 pins

Note:
- I+: Input Pin with Pull up Resistor
- Schmitt: TTL-Schmitt input pin
- O+: Output Pin with Pull up Resistor
- T: TTL-tri-state output pin
- IA: Analog Input pin

■ PIN CONFUGLATION

YMF711-S



100 pin SQFP Top View