D2801, JUNE 1984 – REVISED JANUARY 1989

- **Each Circuit Contains 3 Programmable Tone Generators**
- **Programmable White-Noise Generator**
- **Programmable Attenuation**
- **Simultaneous Sounds**
- **Up to 500 kHz Clock Input for SN76494 and 4 MHz for SN76496**
- **External Audio Input for SN76496 May Be Summed with Internally Generated Tones**
- **The SN76494A and SN76496A are Interchangeable with the SN76494 and SN76496, Respectively**

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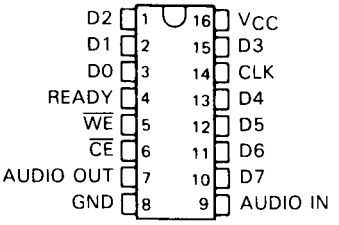
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

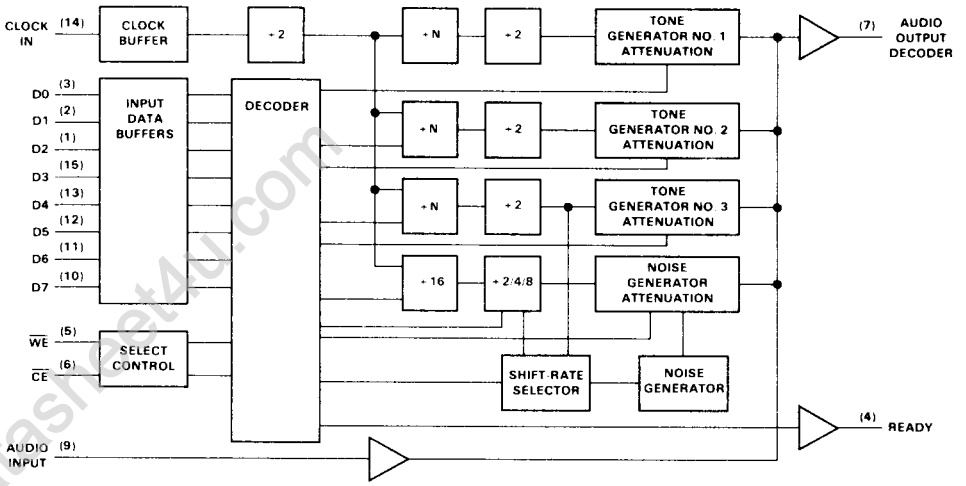
The SN76494 and SN76494A digital complex sound generators are integrated injection logic (I^2L) tone generators designed to provide low-cost tone or noise generation capability in microprocessor systems. The SN76494 and SN76494A are data-bus-based input-output peripheral devices that interface the microprocessor through 8 data lines and 3 control lines.

The SN76494 and SN76494A are identical to the SN76496 and SN76496A except that the maximum clock input frequency for SN76494 and SN76494A is 500 kHz and for SN76496 and SN76496A, it is 4 MHz. A "divide-by-eight" stage is deleted from the SN76496 and SN76496A circuitry so that only 4 clock pulses are required to load the data into the SN76494 and SN76494A, compared to 32 pulses for the SN76496 and SN76496A.

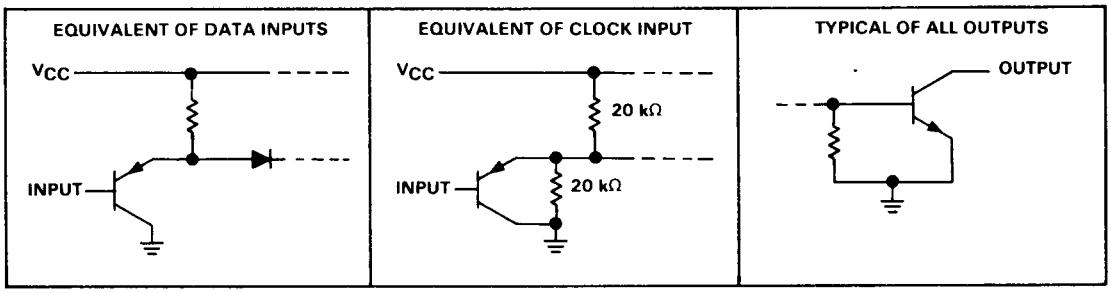
Either of these devices may also be used as a replacement for the SN76489A in all applications if pin 9 is left open or grounded. The output load must be limited to 10 mA.

When audio input is not desired in the SN76494, SN76494A, SN76496 or SN76496A, the audio input pin should be grounded.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: Audio input . . . . . 0.9 V
All other inputs . . . . . 7 V
Output current at pin 7 . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		SN76494, SN76494A			SN76496, SN76496A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_I	Audio input current	0		1.8	0		1.8	mA
V_{OH}	High-level output voltage (pin 4)			5.5			5.5	V
I_{OL}	Low-level output current (pin 4)			2			2	mA
f_{clock}	Input clock frequency			0.5			4	MHz
$t_{d(WE)}$	Delay time, $\overline{CE}$ low to $\overline{WE}$ low	0			0			ns
t_{su}	Setup time, data before $\overline{WE}\downarrow$ or $\overline{CE}\downarrow$	0			0			ns
t_h	Hold time, data after READY↑	0			0			ns
T_A	Operating free-air temperature	0		70	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current (pin 4)		V_O = 5.5 V			10	µA
I_{IH}	High-level input current (All digital inputs)		$V_I = V_{CC}$			10	µA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_I = 0		−25	−175	µA
		All other digital inputs			−10	−70	
V_{IB}	Input bias voltage, audio (pin 9)		R = 4.7 kΩ to V_{CC}	0.5	0.7	0.9	V
V_{OH}	High-level output voltage (pin 7)					5.5	V
V_{OL}	Low-level output voltage (pin 4)		I_{OL} = 2 mA		0.25	0.4	V
V_{OPP}	Peak-to-peak output voltage (pin 7)		V_{CC} = 5 V, Attenuation: Generator under test = 0 dB, All other generators = 30 dB	260			mV
I_{CC}	Supply current				30	50	mA
	Attenuation	2 dB NOM	See Table 1	1	2	3	dB
		4 dB NOM		3	4	5	
		8 dB NOM		7	8	9	
		16 dB NOM		15	16	17	
C_i	Input capacitance					15	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level RDY output from $\overline{CE}$	C_L = 225 pF, R_L = 2 kΩ to V_{CC}		90	150	ns
t_{PHL}	Propagation delay time high-to-low level, RDY output from $\overline{WE}$			90		ns
t_{PLH}	Propagation delay time low-to-high level, RDY output from CLK			90		ns

PARAMETER MEASUREMENT INFORMATION

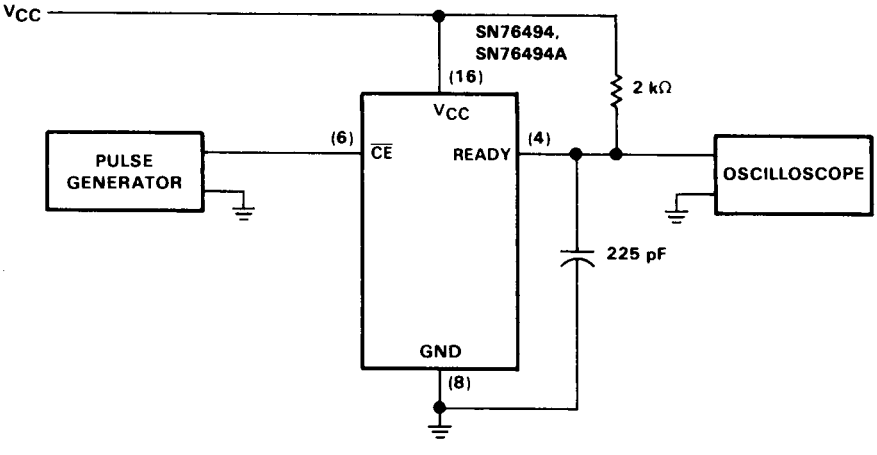


FIGURE 1. t_{PHL} TEST CIRCUIT

pin assignments and functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{CE}$	6	I	Chip Enable. When chip enable is low, the device is operational, input terminals are enabled, and data may be entered.
D0 (MSB)	3	I	D0 through D7 – Input data bus
D1	2	I	
D2	1	I	
D3	15	I	
D4	13	I	
D5	12	I	
D6	11	I	
D7 (LSB)	10	I	
V_{CC}	16	I	Supply voltage (5 V nom)
GND	8	O	Ground reference
CLOCK	14	I	Input Clock
$\overline{WE}$	5	I	Write Enable. When $\overline{CE}$ is enabled and $\overline{WE}$ is active (low), input on the data bus is accepted. $\overline{CE}$ and $\overline{WE}$ must be held low until READY returns high (four clock cycles for the SN76494 and SN76494A or 32 clock cycles for the SN76496 and SN76496A). If $\overline{WE}$ remains low throughout four additional clock cycles for the SN76494 and SN76494A (32 clock cycles for the SN76496 and SN76496A) a new write cycle will be initiated.
READY	4	O	When low, READY indicates that a write cycle is in progress; data on the input bus must remain valid until READY returns high.
AUDIO IN	9	I	Audio input from external source
AUDIO OUT	7	O	Audio Drive Out

PRINCIPLES OF OPERATION

tone generators

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (f). F0 is the most significant bit and F9 is the least significant bit. This information is loaded into a 10-stage tone counter, which counts down at an N/2 rate where N is the input clock frequency. When the tone counter counts down to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{4n} \text{ for SN76494 and SN76494A, or } f = \frac{N}{32n} \text{ for SN76496 and SN76496A}$$

where N = clock in Hz
n = 10-bit binary number

The output level of each tone/noise generator may be selected by programming a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 30 dB.

TABLE 1. ATTENUATION CONTROL

BIT POSITION				WEIGHT
A0	A1	A2	A3	(In dB)
0	0	0	1	2
0	0	1	0	4
0	1	0	0	8
1	0	0	0	16
1	1	1	1	OFF

noise generator

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR-feedback network. The feedback network has provisions to protect the shift register from being locked in the zero state.

TABLE 2. NOISE FEEDBACK CONTROL

FEEDBACK	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 3. NOISE GENERATOR FREQUENCY CONTROL

BITS		SHIFT RATE
NF0	NF1	
0	0	N/64
0	1	N/128
1	0	N/256
1	1	Tone generator #3 output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

output buffer/amplifier

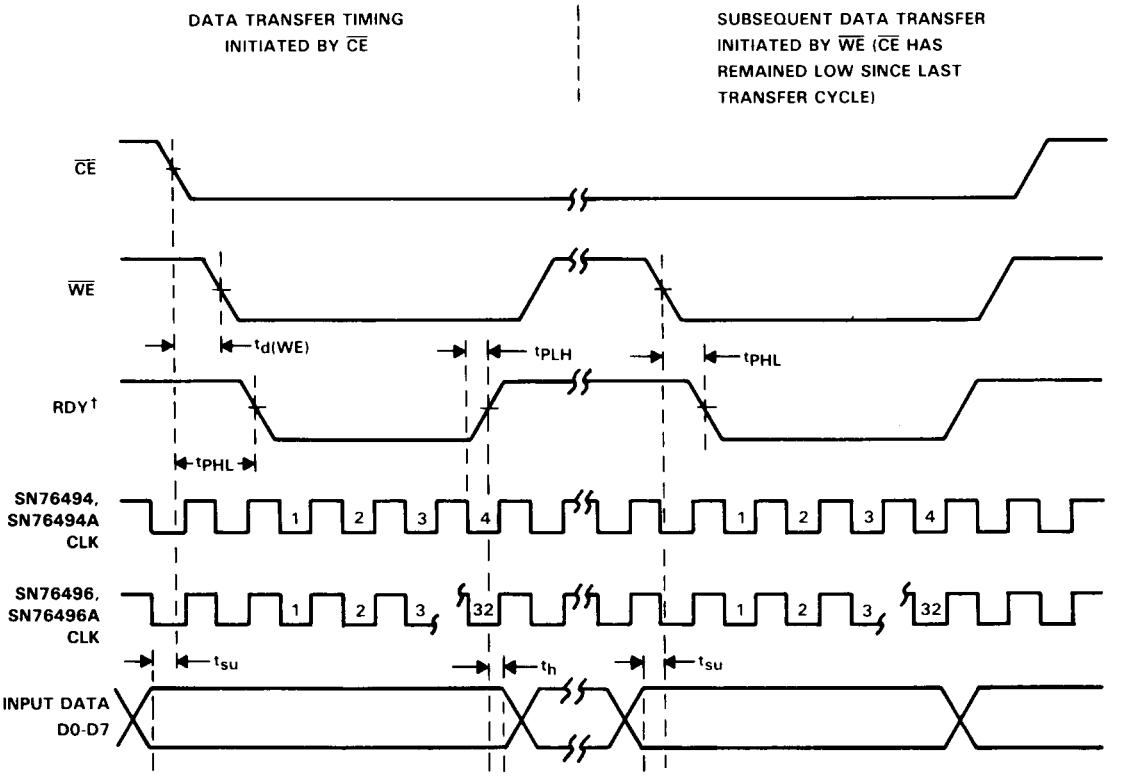
The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, the noise generator output, and any audio input through pin 9. The output buffer will generate up to 10 mA.

To prevent oscillations in the output buffer, the output (pin 7) should be decoupled. This is done by putting 10 ohms in series with 0.1 μF from pin 7 to ground (see Figure 3).

data transfer

The microprocessor selects the SN76494, SN76494A, SN76496, or SN76496A by taking $\overline{CE}$ low (low voltage). Unless $\overline{CE}$ is low, no data transfer can occur. When $\overline{CE}$ is low, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

The SN76494 and SN76494A require approximately 4 clock cycles to load the data into the control register. The SN76496 and SN76496A require approximately 32 clock cycles. The open-collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low) immediately following the falling edge of $\overline{CE}$ (or $\overline{WE}$ when data transfer is initiated by $\overline{WE}$). READY will go high upon completion of the data transfer cycle. The data transfer timing is shown below.



† $\overline{WE}$ must be returned high (inactive) within 4 clock pulses for the SN76494 and SN76494A (32 clock pulses for the SN76496 and SN76496A) after RDY returns high. Otherwise, a new data transfer cycle will be initiated.

FIGURE 2. DATA TRANSFER TIMING

TABLE 4. FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

This table is valid when the device is:
(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

CPU interface to SN76494, SN76494A, SN76496 or SN76496A

The microprocessor interfaces with the SN76494, SN76494A, SN76496, or SN76496A by means of the 8 data lines and 3 control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and four bits of information to select the attenuation. A frequency selection requires a double-byte transfer, while an attenuator selection requires a single-byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the six most significant bits to be quickly modified for frequency sweeps.

control registers

The devices have 8 internal registers that are used to control the 3 tone generators and the noise source. During all data transfers to the devices, the first byte contains a 3-bit field that determines the destination control register. The register address codes are shown in Table 5.

TABLE 5. REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

data formats

The formats required to transfer data are shown below.

	REG ADDR			DATA			
1	R0	R1	R2	F6	F7	F8	F9

BIT 0 FIRST BYTE BIT 7

UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)

	DATA						
0	x	F0	F1	F2	F3	F4	F5

BIT 0 SECOND BYTE BIT 7

	REG ADDR					SHIFT	
1	R0	R1	R2	x	FB	NF0	NF1

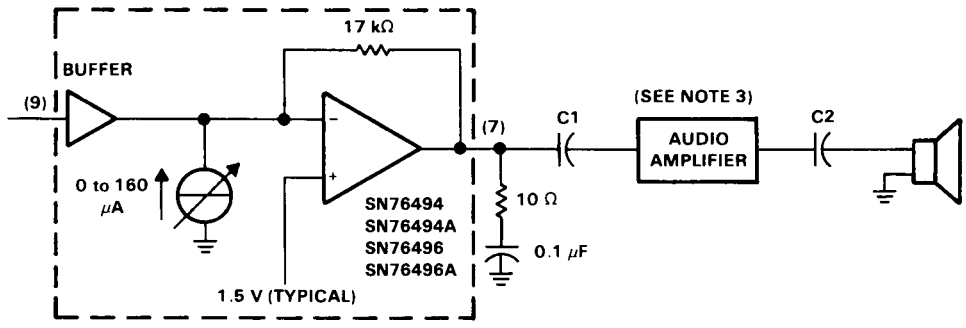
BIT 0 BIT 7

UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)

	REG ADDR			DATA			
1	R0	R1	R2	A0	A1	A2	A3

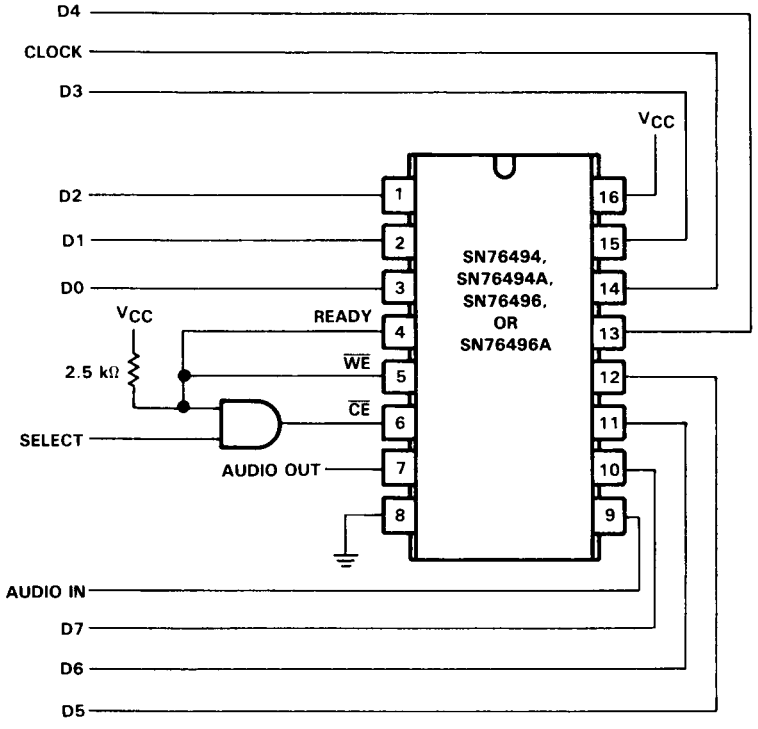
BIT 0 BIT 7

TYPICAL APPLICATION DATA



NOTE 3: The capacitance values of C1 and C2 are determined by the frequency response desired and the audio amplifier used.

FIGURE 3. EXTERNAL AUDIO OUTPUT INTERFACE



NOTES: 4. The data lines must be latched so that the data remains on them at least 32 clock cycles for the SN76496 and SN76496A or (4 clock cycles for the SN76494 and SN76494A) after the select line goes low.
5. The select pulse should be a negative-going pulse with minimum duration of 150 ns.

FIGURE 4. MICROCOMPUTER PARALLEL PORT INTERFACE