ESS Technology, Inc.

ES1988 Allegro™ PCI Audio-Modem Accelerator Product Brief

DESCRIPTION

The ES1988 Allegro™ PCI audio-modem accelerator combines advanced audio and modem functionality in a highly integrated PCI solution. Utilizing one PCI load, the ES1988 provides a two-chip audio-modem solution with digital interface capability to an AC'97 codec in the dock (a.k.a. digital docking). The ES1988 is designed to provide a low-cost, high-performance solution for notebook PC applications.

The high-bandwidth PCI bus and an integrated high-fidelity codec are utilized to deliver advanced PC audio features, such as DirectSound™ acceleration and HRTF 3D positional audio. The ES1988 implements multistream DirectSound and DirectSound3D acceleration with digital mixing, sample rate conversion, and HRTF 3D filtering for two-speaker 3D positional audio.

The programmable audio signal processor provides support for multiple audio streams. With its built-in DSP core, the ES1988 uses its dedicated direct memory access (DMA) engine to handle complex signal processing tasks with a bus-mastering PCI interface. The support functions ensure efficient transfer of audio data streams to and from system memory buffers, providing a system solution with maximum performance and minimal host CPU loading. The architecture enables implementation of communications over the Internet from multiple sources.

The ES1988 maintains full DOS legacy audio compatibility over the standard PCI 2.1 and PCI 2.2 bus. Full DOS game compatibility is ensured through either PC/PCI, distributed DMA (DDMA), or transparent DMA (TDMA).

The ES1988 includes an HSP modem interface via its secondary AC-Link connecting with the ES2828 MC'97 codec. The MC'97 is used as the analog front end for the modem and DAA control. The V.90 modem runs on the host while the ES1988 serves as the bidirectional buffer for data transmission and reception. The modem functions include the standard AT command set, V.42***bis*** and Group 3 fax.

The ES1988 provides a high-quality docking solution through proven AC-link-based digital docking. This is accomplished by using only a five-wire digital connection. The secondary AC'97 link (extension 2.1 compliant) of the ES1988 interfaces to a secondary AC'97 codec in the dock to provide high-quality audio in the dock.

The ES1988, which operates at 3.3V digitally and 5.0V in analog, is compliant with the Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.0, and PCI Power Management Interface (PPMI) 1.0. The ES1988 supports D0, D1, D2, and D3 (hot and cold) power-saving modes for power efficiency when the audio system is both active and idle. CLKRUN# support is also available.

The ES1988 is available in an industry-standard 100-pin low-profile quad flat pack (LQFP) package.

AUDIO FEATURES

- High-performance single-chip PCI audio acceleration
- Integrated high-fidelity AC'97 codec
- Multistream DirectSound and DirectSound 3D acceleration
- Sensaura® CRL positional 3D
- High-quality sample rate conversion and digital mixing
- Direct music support
- Realtime effects processing
- S/PDIF output for PCM or AC-3 content
- Full legacy DOS game support, using TDMA, PC/PCI, or DDMA hardware implementation methods
- Supports one additional PCI bus master devices
- HSP modem interface via MC'97 link
- Digital docking via secondary AC-Link

MODEM FEATURES

- Data mode capabilities:
  - V.90 56 kbps
  - V.34 33.6 kbps and fallbacks
  - Standard AT command set
  - V.42 (LAPM) and MNP error correction
  - V.42***bis***/MNP 5 data compression
  - 3.3V power supply with 5V-tolerant inputs
- Fax mode capabilities:
  - ITU-T V.17, V.21 ch2, V.27ter, V.29
  - Group 3 (TIA/EIA 578 Class 1 and Class 2)
- Supports wake-on-ring from $D3_{hot}$ and $D3_{cold}$ states

POWER MANAGEMENT

- Compliance with APM 1.2, ACPI 1.0, and PPMI 1.1
- Compliance with Intel's Mobile Power Guidelines '99
- 3.3V digital operation with 5V-tolerant inputs
- 5.0V analog operation

COMPATIBILITY

- Supports PC DOS games and applications for Sound Blaster™ and SoundBlaster Pro™
- Meets PC99 /PC2001and WHQL specifications
- Compliant with Intel's audio-modem riser card and mini-PCI specifications

ES1988 PINOUT

Figure 1 shows the ES1988 Allegro pinout diagram.

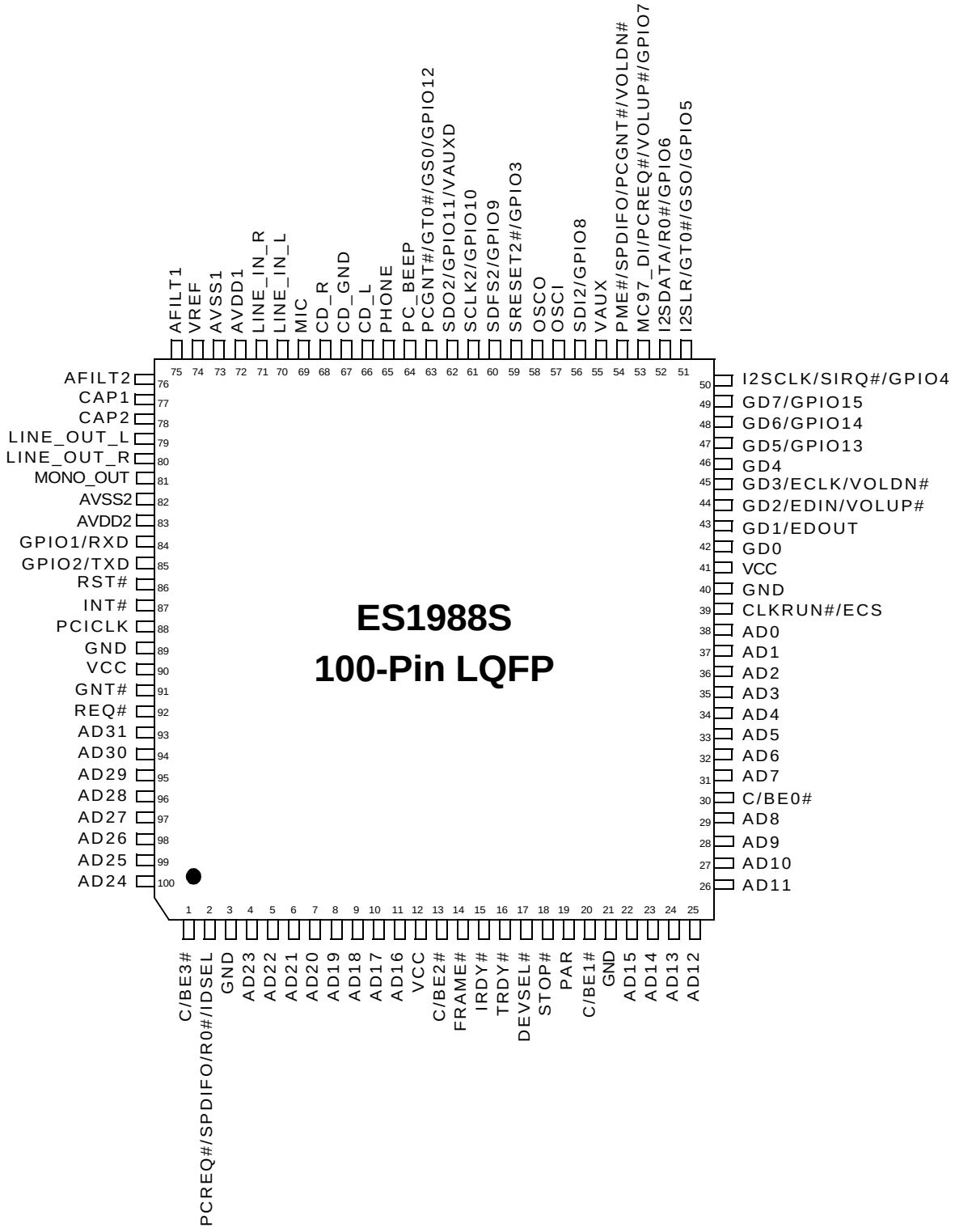

Figure 1 ES1988 Allegro Pinout Diagram

PIN DESCRIPTION

Table 1 lists the ES1988 pin descriptions

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Table 1 ES1988 Pin Descriptions

Names	Pin Numbers	I/O	Descriptions
C/BE[3:0]#	1, 13, 20, 30	I/O	PCI command/byte enable. During address phase of a transaction, these pins define the bus command. During data phase, these pins define the byte enable.
IDSEL	2	I	ID select. When pin 2 is configured as a multifunction pin (see pin 2 note), IDSEL is selected internally to AD24.
R0#		I	PCI bus request 0 input from external PCI master device. RO# is enabled by setting the PCIx2 arbiter bit PCI 58h [0] = 1. Select RO# from pin 2 by setting PCI 58h [10] = 1, and pin 2 must be configured as a multifunction pin. Either pin 2 or pin 52 may be used for R0#.
SPDIFO		O	S/PDIF output. Enable SPDIFO by setting PCI 53h [0] = 1. Select SPDIFO from pin 2 by setting PCI 58h [1] = 1, and pin 2 must be configured as a multifunction pin. Either pin 2 or pin 54 may be used for SPDIFO.
PCREQ#		O	PC/PCI request output. Enable PCREQ# by setting PCI 50h [10:8] = 010. Pin 53 is used as PCREQ# when configured as an audio-only device. PCREQ# can only be used from pin 2 when the ES1988 is configured as a multifunction device (see pin 60 note). Pin 2 must be configured as a multifunction pin.
GND	3, 21, 40, 89	I	Digital ground.
AD[31:0]	4:11, 22:29, 31:38, 93:100	I/O	Address and data lines from the PCI bus.
VCC	12, 41, 90	I	Digital supply voltage, 3.3V.
FRAME#	14	I/O	Cycle frame.
IRDY#	15	I/O	Initiator ready.
TRDY#	16	I/O	Target ready.
DEVSEL#	17	I/O	Device select.
STOP#	18	I/O	Stop transaction.
PAR	19	I/O	Parity.
CLKRUN#	39	I/O	Input/output for PCI Clock status and an output to start or accelerate clock function by enabling PCI 52h [11] = 1.
ECS		O	Chip select output to EEPROM chip select input. ECS is active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
GD[0]	42	I/O	Game port data input/output.
GD[1]	43	I/O	Game port data input/output.
EDOUT		O	Data output to EEPROM data input. EDOUT goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
GD[2]	44	I/O	Game port data input/output.
EDIN		I	Data input from EEPROM data output. EDIN goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
VOLUP#		I	Hardware volume control (volume up). Used in combination with pin 45 (VOLDN#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 44:45 are selected for hardware volume control by setting PCI 52h [5] = 1. Pins 53:54 may also be used for hardware volume control.

Table 1 ES1988 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Descriptions
GD[3]	45	I/O	Game port data input/output.
ECLK		O	Clock output to EEPROM clock input. ECLK goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
VOLDN#		I	Hardware volume control (volume down). Used in combination with pin 44 (VOLUP#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 44:45 are selected for hardware volume control by setting PCI 52h [5] = 1. Pins 53:54 may also be used for hardware volume control.
GD[4]	46	I	Game port data input.
GD[5:7]	47:49	I	Game port data input.
GPIO[13:15]		I/O	General-purpose input/output.
I2SCLK	50	I	I²S serial clock input. I²S input is enabled by setting Allegro_Base+37h [15] = 1.
SIRQ#		I/O	Serial interrupt request. Optional PC/PCI system implementation. Serial IRQ is enabled by setting PCI 40h [14] = 1.
GPIO4		I/O	General-purpose input/output.
I2SLR	51	I	I²S frame sync input. I²S input is enabled by setting Allegro_Base+37h [15] = 1.
GTO#		O	Grant to PCI master. GTO# is enabled by setting PCIx2 arbiter bits PCI 58h [0] = 1 and PCI 58h [11] = 1. Select GT0#/GSO from pin 51 by enabling PCI 58h [10] = 0. Pin 63 may also be used as GT0#/GSO.
GSO		O	Grant select 0 output to control external quick switch to grant PCI master phase. GSO is enabled by setting PCIx2 arbiter bit PCI 58h [0] = 1 and PCI 58h [11] = 0. Select GS0/GT0# from pin 51 by enabling PCI 58h [10] = 0. Pin 63 may also be used as GT0#/GSO.
GPIO5		I/O	General-purpose input/output.
I2SDATA	52	I	I²S data input. I²S input is enabled by setting Allegro_Base+37h [15] = 1.
R0#		I	PCI bus request 0 input from external PCI master device. RO# is enabled by setting the PCIx2 arbiter bit PCI 58h [0] = 1. Select R0# from pin 52 by enabling PCI 58h [10] = 0. Either pin 2 or pin 52 may be used for R0#.
GPIO6		I/O	General-purpose input/output.
MC_97DI	53	I	Modem codec data input. Enabled by setting Allegro_Base+38h [3] = 1.
PCREQ#		O	PC/PCI request output. Enable PCREQ# by setting PCI 50h [10:8] = 010. Pin 53 is used as PCREQ# when configured as an audio-only device. PCREQ# can only be used from pin 2 when configured as a multifunction device (see pin 60 note).
VOLUP#		I	Hardware volume control (volume up). Used in combination with pin 54 (VOLDN#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 53:54 are selected for hardware volume control by setting PCI 52h [5] = 0. Pins 44:45 may also be used for hardware volume control.
GPIO7		I/O	General-purpose input/output.
PME#	54	O	PME# output to wake the system. PME is enabled by setting the PME_EN bit (PCI C5h [0] = 1).
SPDIFO		O	S/PDIF output. Enable SPDIFO by setting PCI 53h [0] = 1. Select SPDIFO from pin 54 by setting PCI 58h [1] = 0. Either pin 2 or pin 54 may be used for SPDIFO.
PCGNT#		I	PC/PCI grant input. Enable PC/PCI by setting PCI 50h [10:8] = 010. Select PCGNT# from pin 54 by setting Allegro_Base+58h [6] = 1. Either pin 54 or pin 63 may be used for PCGNT#.
VOLDN#		I	Hardware volume control (volume down). Used in combination with pin 53 (VOLUP#). Hardware volume control is enabled by setting PCI 52 [7] = 1. Pins 53:54 are selected for hardware volume control by setting PCI 52h [5] = 0. Pins 44:45 may also be used for hardware volume control.
VAUX	55	I	3.3V V_{AUX} voltage supply input. If V_{AUX} is not supported, then V_{AUX} (pin 55) should be connected to VCC and V_{AUXD} (pin 62) should be pulled down.

Table 1 ES1988 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Descriptions
SDI2	56	I	External AC-link serial data input. Select secondary codec by enabling Allegro_Base+38h [5] = 1.
GPIO8		I/O	General-purpose input/output.
OSCI	57	I	49.152-MHz crystal input.
OSCO	58	O	49.152-MHz crystal output.
SRESET2#	59	O	Reset output for AC-Link interface. Select secondary codec by enabling Allegro_Base+38h [5] = 1.
GPIO3		I/O	General-purpose input/output.
SDFS2	60	O	Serial data frame sync output for AC-Link interface. Select secondary codec by enabling Allegro_Base+38h [5] = 1.
GPIO9		I/O	General-purpose input/output.
(note)			If a pull-down resistor is used on this pin, the ES1988 is configured as a multifunction device (audio-modem). Otherwise, the ES1988 is configured as a single function audio-only device.
SCLK2	61	O	Serial clock for AC-link interface. Select secondary codec by enabling Allegro_Base+38h [5] = 1.
GPIO10		I/O	General-purpose input/output.
SDO2	62	O	External AC-link serial data output. Select secondary codec by enabling Allegro_Base+38h [5] = 1.
GPIO11		I/O	General-purpose input/output.
VAUXD		I	V_{AUX} detect. During the reset period, the V_{AUXD} pin is driven high to indicate ACPI support in the ***D3$_{cold}$*** state, and is driven low to indicate ACPI is not supported in the ***D3$_{cold}$*** state. If V_{AUX} is not supported, then V_{AUX} (pin 55) should be connected to VCC and V_{AUXD} (pin 62) should be pulled down.
PCGNT#	63	I	PC/PCI grant input. Enable PC/PCI by setting PCI 50h [10:8] = 010. Select PCGNT# from pin 63 by setting Allegro_Base+58h [6] = 0. Either pin 54 or pin 63 may be used for PCGNT#.
GT0#		O	Grant to PCI master. GTO# is enabled by setting PCIx2 arbiter bits PCI 58h [0] = 1 and PCI 58h [11] = 1. Select GT0#/GSO from pin 63 by enabling PCI 58h [10] = 1. Pin 51 may also be used as GT0#/GSO.
GS0		O	Grant select 0 output to control external quick switch to grant PCI master phase. GSO is enabled by setting PCIx2 arbiter bit PCI 58h [0] = 1 and PCI 58h [11] = 0. Select GS0/GT0# from pin 63 by enabling PCI 58h [10] = 1. Pin 51 may also be used as GT0#/GSO.
GPIO12		I/O	General-purpose input/output.
PC_BEEP	64	I	PC Speaker input.
PHONE	65	I	Mono input.
CD_L	66	I	CD-audio left channel input.
CD_GND	67	I	CD-audio ground input.
CD_R	68	I	CD-audio right channel input.
MIC	69	I	Microphone input.
LINE_IN_L	70	I	Line left channel input.
LINE_IN_R	71	I	Line right channel input.
AVDD[2:1]	83, 72	I	Analog supply voltage, 5V.
AVSS[2:1]	82, 73	I	Analog ground.
VREF	74	O	Reference voltage.

Table 1 ES1988 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Descriptions
AFILT[2:1]	76:75	O	Anti-aliasing filter cap for the ADC channel.
CAP[2:1]	78:77	O	ADC and DAC reference caps.
LINE_OUT_L	79	O	Line left channel output.
LINE_OUT_R	80	O	Line right channel output.
MONO_OUT	81	O	Mono output.
RXD	84	I	MIDI receive data input. Enable MIDI I/O (MPU-401 I/O) by setting PCI 40h [3] = 1.
GPIO1		I/O	General-purpose input/output.
TXD	85	O	MIDI transmit data output. Enable MIDI I/O (MPU-401 I/O) by setting PCI 40h [3] = 1.
GPIO2		I/O	General-purpose input/output.
(note)			If a pull down resistor is used on this pin, then pin 2 is enabled for multifunctionality (IDSEL, RO#, SPDIFO, and PCREQ#). Otherwise, pin 2 may only be used for IDSEL.
RST#	86	I	PCI reset input.
INT#	87	O	Interrupt request output.
PCICLK	88	I	PCI bus clock input.
GNT#	91	I	Bus master grant input.
REQ#	92	O	Bus master request output.

ORDERING INFORMATION

Part Number	Description	Package
ES1988S	PCI Audio-Modem Accelerator	100-pin LQFP

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