A Cirrus Logic Company

CS4237B

Advanced Audio System with 3D Sound

- Integrated SRS® 3D Sound Technology
- Compatible with Sound Blaster®, Sound Blaster Pro™, and Windows Sound System™
- Advanced MPC3-Compliant Input and Output Mixer
- Enhanced Stereo Full Duplex Operation
- Dual Type-F DMA Support
- Industry Leading Delta-Sigma Data Converters
- Fully Plug-and-Play ISA Compatible
- 3.3V or 5V ISA Bus Operation
- Programmable Power Management
- Hardware Master Volume Control
- Enhanced Digital Gameport
- CS9236 Wavetable Digital Audio Interface
- MPU-401 MIDI Interface
- Consumer IEC-958 Digital Output (S/PDIF)
- CS4236/CS4232/CS4231 Register Compatible

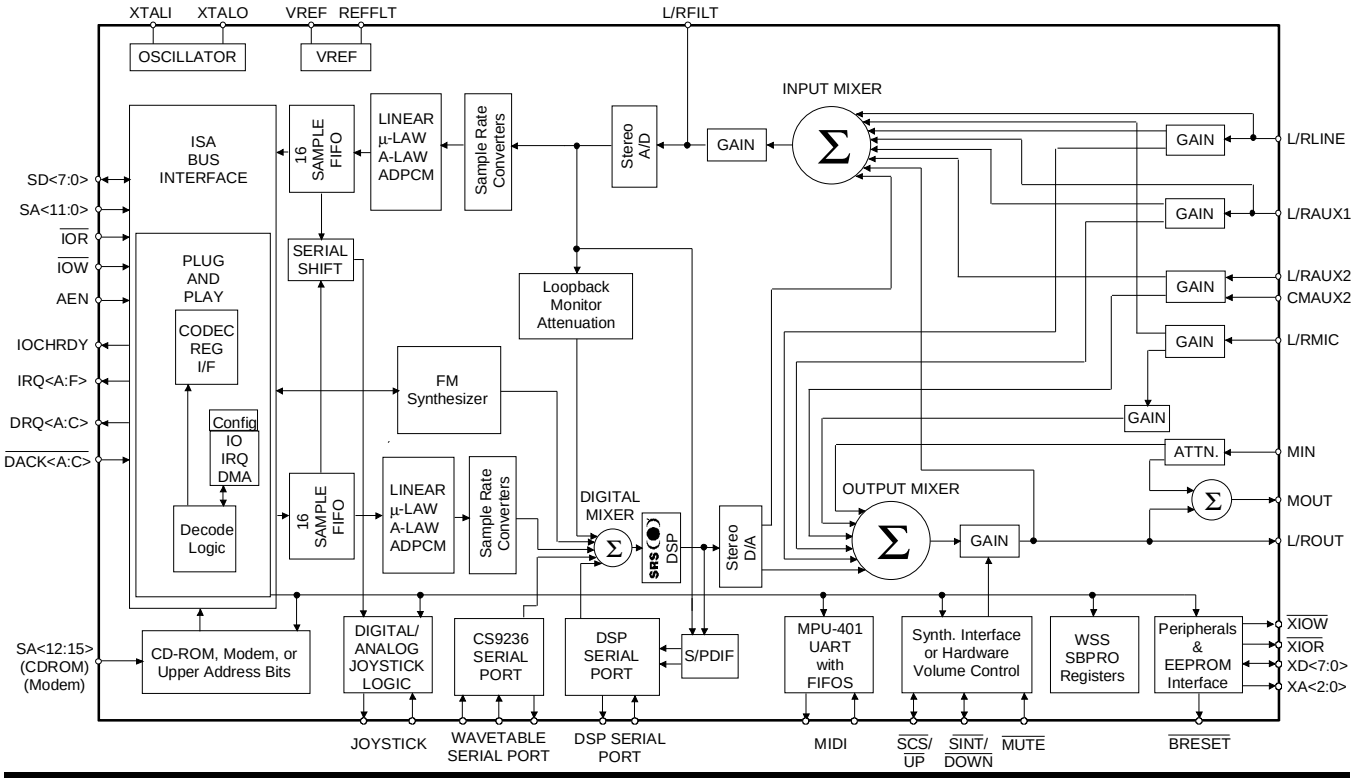
General Description

The CS4237B is a single chip multimedia audio system that provides compatibility with the Microsoft Windows Sound System standard and will run software written to the Sound Blaster and Sound Blaster Pro interfaces. The CS4237B is fully compliant with Microsoft's PC' 97 and WHQL audio requirements. The product includes an internal FM synthesizer and Plug-and-Play external interfaces for Wavetable, CD-ROM, and modem devices. In addition, the CS4237B includes hardware master volume control pins as well as extensive power management and SRS 3D sound technology.

SRS *everything else is only stereo™*

ORDERING INFORMATION:

CS4237B-KQ 100 pin TQFP, 14x14x1.4mm



Advanced Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581
http://www.crystal.com

ANALOG CHARACTERISTICS

T_A = 25 °C; VA, VD1, VDF1-VDF4 = +5V
Input Levels: Logic 0 = 0V, Logic 1 = VD1; 1 kHz Input Sine wave; Sample Frequency, Fs = 44.1 kHz;
Measurement Bandwidth is 20 Hz to 20 kHz - unweighted, 16-bit linear coding.)

Parameter*		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum Gain Setting (0dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16			Bits
ADC Differential Nonlinearity	(Note 1)				±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	85 79		dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD		0.006 0.01	0.02 0.025	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2			80 80 90 90		dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs				±0.5 ±0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5		dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain			±10	±100	LSB
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2, MIN Inputs		0.26 2.6 2.6	0.28 2.8 2.8		V_{pp} V_{pp} V_{pp}
Gain Drift				±100		ppm/°C
Input Resistance (Note 1)	Mic Inputs Other Inputs		8 20	11 23		kΩ kΩ
Input Capacitance	(Note 1)				15	pF

Notes: 1. This specification is guaranteed by characterization, no production testing.
2. MGE = 1 (see WSS Indirect Reg I0, I1).

*Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0dB); unless otherwise specified.							
DAC Resolution		(Note 1)		16			Bits
DAC Differential Nonlinearity		(Note 1)				±0.5	LSB
Dynamic Range	-Total -Instantaneous	All Outputs	TDR IDR	 80	95 85		dB dB
Total Harmonic Distortion		(Note 3)	THD		0.01	0.02	%
Interchannel Isolation	Line Out	(Note 3)			95		dB
Interchannel Gain Mismatch		Line Out			±0.1	±0.5	dB
Voltage Reference Output - VREF				2.0	2.2	2.5	V
Voltage Reference Output Current - VREF		(Notes 1,4)			100	400	µA
DAC Programmable Attenuation Span				100	106.5		dB
DAC Attenuation Step Size		+12 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage					±1	±10	mV
Full Scale Output Voltage:	OUT, MOUT	(Notes 3)		2.6	2.8	3.2	Vpp
Gain Drift					100		ppm/°C
Deviation from Linear Phase	(Passband)	(Note 1)				1	Degree
External Load Impedance		(Note 1)		10			kΩ
Mute Attenuation				80			dB
Total Out-of-Band Energy	0.6xFs to 100 kHz	(Note 1)				-45	dB
Audible Out-of-Band Energy	0.6xFs to 22 kHz	(Fs=8kHz) (Note 1)				-70	dB
Power Supply							
Power Supply Current		Digital, Operating Analog, Operating Total Operating Total Power Down			80 25 105 100	91 31 122 400	mA mA mA µA
Power Supply Rejection	1 kHz	(Note 1)		40			dB

Notes: 3. 10 kΩ, 100 pF load.

4. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.

MIXERS (T_A = 25 °C; VA, VD1, VDF1-VDF4 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD1; 1 kHz Input Sine wave, Measurement Bandwidth is 20 Hz to 20 kHz - unweighted.

Parameter		Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	LINE, AUX1, AUX2		45	46.5		dB
	MIC, MIN		42	45		dB
	Hardware Master		44	48		dB
(Digital)	Wavetable, Monitor, PC Wave, DSP, FM		90	94.4		dB
Step Size	MIC, LINE, AUX1, AUX2		1.3	1.5	1.7	dB
	MIN		2.3	3.0	3.7	dB
	Hardware Master		1.6	2.0	2.4	dB
(Digital)	Wavetable, Monitor, PC Wave, DSP, FM		0.9	1.5	2.0	dB
Dynamic Range	-Total			94.5		dB
(Analog Mixers)	-Instantaneous			91		dB
Total Harmonic Distortion (Analog Mixers)	(Note 3)			0.002		%

ABSOLUTE MAXIMUM RATINGS (AGND, DGND, SGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital	VD1	-0.3	6.0	V
		VDF1-VDF4	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Total Power Dissipation	(Supplies, Inputs, Outputs)			1	W
Input Current per Pin	(Except Supply Pins)		-10.0	+10.0	mA
Output Current per Pin	(Except Supply Pins)		-50	+50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage:	SA<11:0>, IOR, IOW, AEN SD<7:0>, DACK<A:C>		-0.3	VD1+0.3	V
	All other digital inputs		-0.3	VDF+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, SGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD1	4.75	5.0	5.25	V
	(Note 5)		3.0	3.3	3.6	V
	Digital Filtered	VDF1-VDF4	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	0	25	70	°C

Note 5. When VD1 is powered from 3.3 Volts, all ISA bus input pins, except DRQA, must also be 3.3 Volts. DRQA is internally powered from the VDF supply and must have a 5 Volt interface. To use DRQA in a 3.3 Volt application, a level translator is needed.

DIGITAL FILTER CHARACTERISTICS (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
Passband			0		0.40xFs	Hz
Frequency Response			-1.0		+0.5	dB
Passband Ripple	(0-0.40xFs)				±0.1	dB
Transition Band			0.40xFs		0.60xFs	Hz
Stop Band			0.60xFs			Hz
Stop Band Rejection			74			dB
Group Delay	8- and 16-bit formats Stereo ADPCM format Mono ADPCM format				10/Fs 14/Fs 18/Fs	s s s
Group Delay Variation vs. Frequency	ADCs DACs				0.0 0.1/Fs	µs µs

DIGITAL CHARACTERISTICS (T_A = 25°C; VA, VDF1-VDF4 = 5V, VD1 = 5V/3V; AGND, DGND1, SGND1-SGND4 = 0V.)

Parameter			Symbol	Min	Max	Units
High-level Input Voltage	Digital Inputs XTALI		V_{IH}	2.0 VD-1.0		V V
Low-level Input Voltage			V_{IL}		0.8	V
High-level Output Voltage:						
ISA Bus Pins (except DRQA)		I_0 = -24.0 mA	V_{OH}	2.4	VD1	V
DRQA		I_0 = -24.0 mA		2.4	VDF	V
IOCHRDY, SDA/XD0 (Note 6)				2.4	VDF	V
All Others		I_0 = -1.0 mA		2.4	VDF	V
Low-level Output Voltage:	ISA Bus Pins	I_0 = 24.0 mA	V_{OL}		0.55	V
		I_0 = 18.0 mA			0.4	V
	IOCHRDY	I_0 = 8.0 mA			0.4	V
	All Others	I_0 = 4.0 mA			0.4	V
Input Leakage Current	(Digital Inputs)			-10	10	µA
Output Leakage Current	(High-Z Digital Outputs)			-10	10	µA

Note 6. Open Collector pins. High level output voltage dependent on external pull up (required) used and number of peripherals (gates) attached.

GENERAL DESCRIPTION

This device is comprised of six physical devices along with Plug-and-Play support for two additional external devices. The internal devices are:

- Windows Sound System Codec
- Sound Blaster Pro Compatible Interface
- Game Port (Joystick)
- Control
- MPU-401
- FM Synthesizer

The two external devices are:

- IDE CDROM
- Modem

A full ISA interface with Plug and Play compatibility and an External Peripheral Port for interfacing to external devices (i.e. Wave-Table Synthesizer, CDROM, and Modem) is included. Since the Wave-Table Synthesizer and CDROM analog inputs are external, mapping as shown in Figure 5, on page 58, must be used to maintain Sound Blaster compatibility, i.e. CDROM analog must be connected to the AUX2 analog inputs of the mixer.

On power up, this part requires a RESDRV signal to initialize the internal configuration. When initially powered up, the part is isolated from the bus, and each device supported by the part must be activated via software. Once activated, each device responds to the resources given (Address, IRQ, and DMA channels). The eight devices listed above are grouped into six logical devices, as shown in Figure 1 (bracketed features are supported, but typically not used). The six logical devices are:

LOGICAL DEVICE 0:
- Windows Sound System Codec (WSS Codec)
- Adlib/Sound Blaster-compatible Synthesizer
- Sound Blaster Pro Compatible Interface

LOGICAL DEVICE 1: Game Port

LOGICAL DEVICE 2: Control

LOGICAL DEVICE 3: MPU401

LOGICAL DEVICE 4: CDROM

LOGICAL DEVICE 5: Modem

Logical Device 0 consists of three physical devices. The WSS Codec and the Synthesizer are grouped together since the original Windows Sound System board expected an FM synthesizer if the codec was present. The Sound Blaster Pro Compatible interface, SBPro, is also grouped to allow the WSS Codec and the SBPro to share Interrupts and DMA channels. The Synthesizer device could be the internal FM synthesizer, or a synthesizer externally located on the Peripheral Port. The external synthesizer interface supports both FM and wavetable synthesizers such as the CS9233. The WSS Codec, FM synthesizer, and the SBPro compatible devices are internal to the part.

Logical Device 1 is the Game Port that supports up to two joystick devices.

Logical Device 2 is the Control device that supports global features of the part. This device uses I/O locations to control power management, joystick rate, and PnP resource data loading.

Logical Device 3 is the MPU-401 interface. The MPU-401 MIDI interface includes a 16-byte FIFO for data transmitted out the MIDOUT pin and a 16-byte FIFO for data received from the MIDIN pin.

Logical Device 4 supports an IDE CDROM connected to the peripheral port. This interface, on the external peripheral port, can support CDROMs with up to 8 I/O locations and supports both the base address and the alternate base address, an interrupt, and a DMA channel. Although this logical device is listed as a CDROM, any external device that fits within the resources listed above may be substituted.

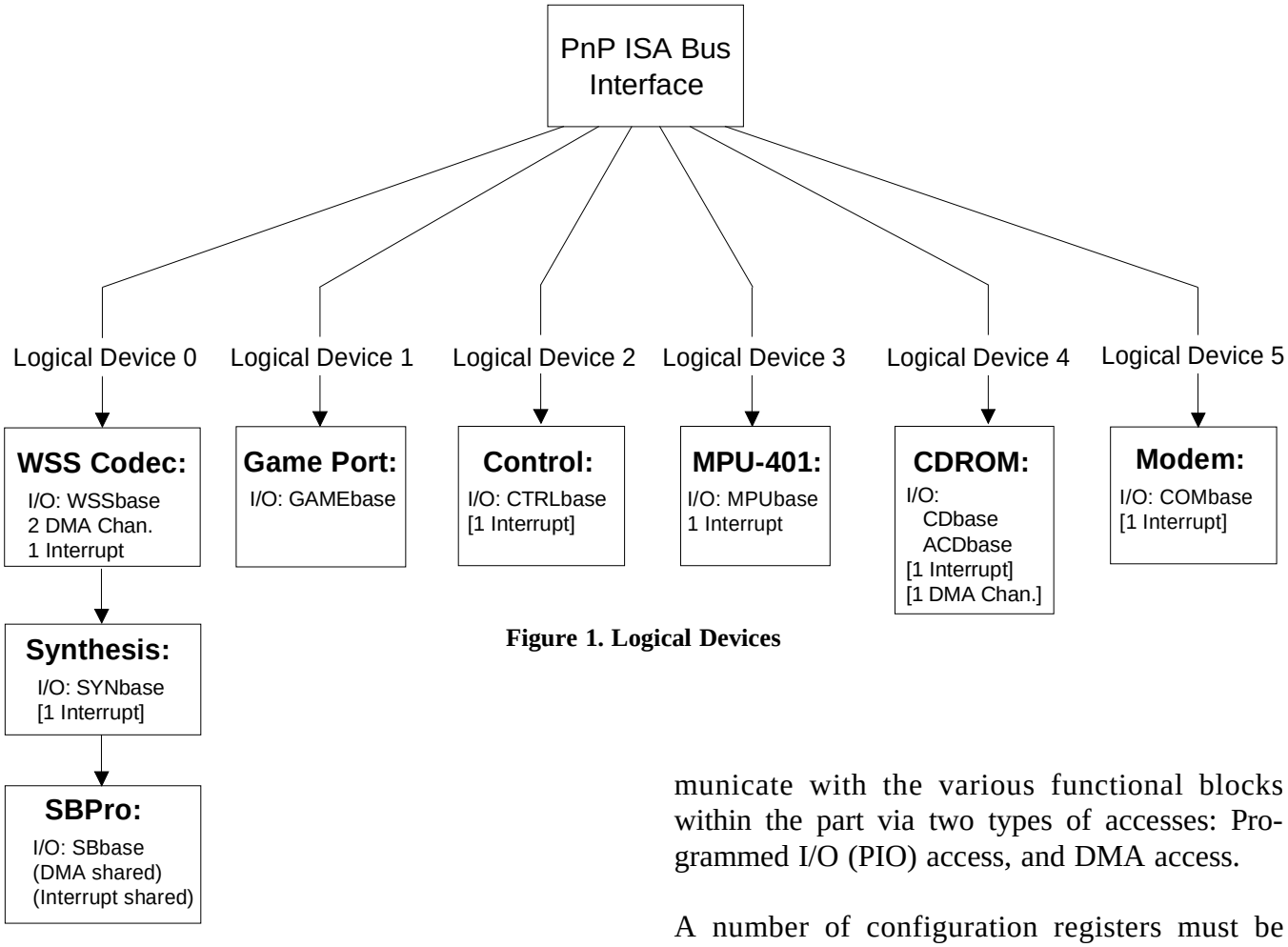


Figure 1. Logical Devices

Logical Device 5 supports a modem connected to the peripheral port. This interface, on the external peripheral port, supports modems with 2 to 256 I/O locations (only SA2-SA0 are buffered through the part) and supports a base address and an interrupt. Although this logical device is listed as a modem, any external device that fits within the resources listed above may be substituted.

ISA Bus Interface

The 8-bit parallel I/O and 8-bit parallel DMA ports provide an interface which is compatible with the Industry Standard Architecture (ISA) bus. The ISA Interface enables the host to communicate with the various functional blocks within the part via two types of accesses: Programmed I/O (PIO) access, and DMA access.

A number of configuration registers must be programmed prior to any accesses by the host computer. The configuration registers are programmed via a Plug-and-Play configuration sequence or via configuration software provided by Crystal Semiconductor.

I/O CYCLES

Every device that is enabled, requires I/O space. An I/O cycle begins when the part decodes a valid address on the bus while the DMA acknowledge signals are inactive and AEN is low. The $\overline{IOR}$ and $\overline{IOW}$ signals determine the direction of the data transfer. For read cycles, the part will drive data on the SD<7:0> lines while the host asserts the $\overline{IOR}$ strobe. Write cycles require the host to assert data on the SD<7:0> lines and strobe the $\overline{IOW}$ signal. Data is latched on the rising edge of the $\overline{IOW}$ strobe.

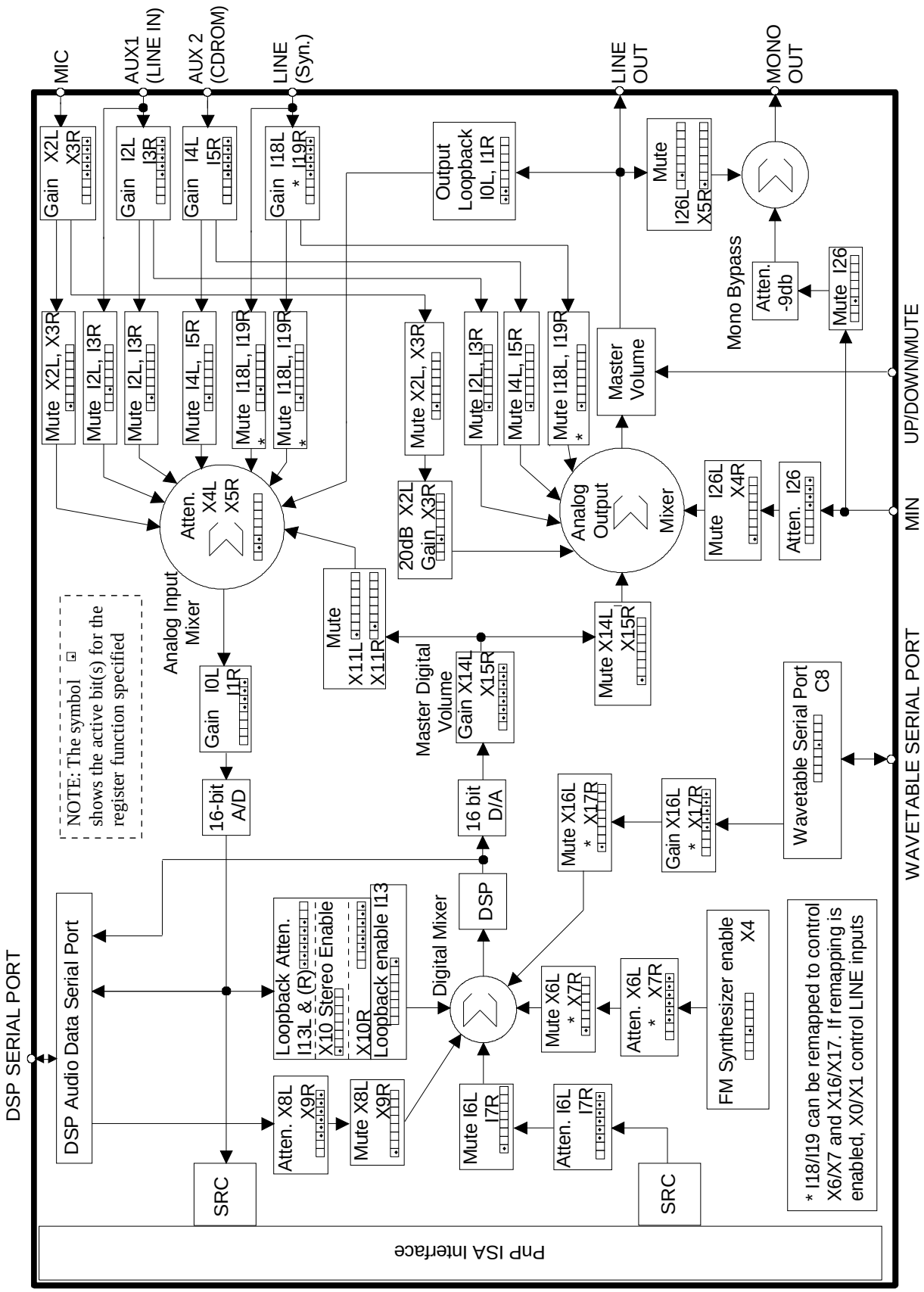
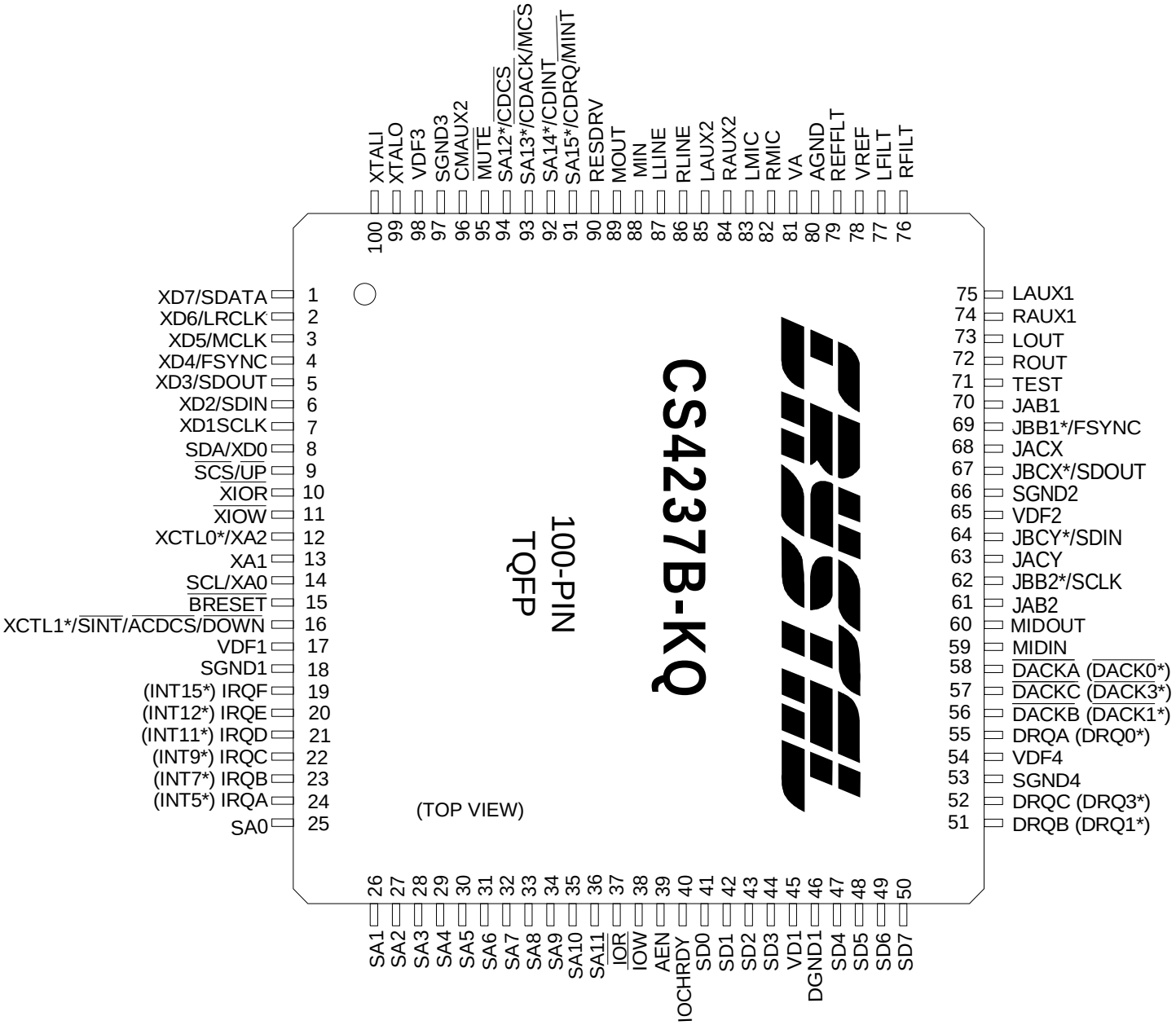


Figure 4. MODE 3 Mixer (assumes IFM or WTEN is set)

PIN DESCRIPTIONS



* **Defaults** - See individual pin descriptions for more details