Designed for Microsoft® Windows®2000 Professional Windows® NT Workstation 4.0 Windows® 98

ACPI CardBus Controller

FEATURES

- ACPI-PCI Bus Power Management Interface Specification Rev 1.1 Compliant
- Supports OnNow LAN wakeup, OnNow Ring Indicate, PCI CLKRUN#, PME#, and CardBus CCLKRUN#
- Compliant with PCI specification v2.2, 2000 PC Card Standard 7.1
- Yenta™ PCI to PCMCIA CardBus Bridge register compatible
- ExCA (Exchangeable Card Architecture) compatible registers mappable in memory and I/O space
- Intel™ 82365SL PCIC Register Compatible
- Supports PCMCIA_ATA Specification
- Supports 5V/3.3V PC Cards and 3.3V CardBus cards
- Supports two PC Card or CardBus slots with hot insertion and removal
- Supports multiple FIFOs for PCI/CardBus data transfer
- Supports Direct Memory Access for PC/PCI and PCI/Way on PC Card socket
- Programmable interrupt protocol: PCI, PCI+ISA, PCI/Way, or PC/PCI interrupt signaling modes
- Win'98 IRQ and PC-98/99 compliant
- Supports parallel or serial interface for socket power control including devices from Micrel and TI
- Zoomed Video Support; Zoomed Video Buffer Enable Pins
- $D3_{cold}$ state PME# wakeup support
- 3.3Vaux Power Support
- Integrated PC 98/99 -Subsystem Vendor ID support, with auto lock bit
- LED Activity Pins

ORDERING INFORMATION

OZ6933T – 208 pin TQFP
OZ6933B – 208 pin Mini-BGA

GENERAL DESCRIPTION

The OZ6933 is an ACPI and PC98/99 logo certified, high performance, dual slot PC Card controller with a synchronous 32-bit bus master/target PCI interface. This PC Card to PCI bridge host controller is compliant with the 2000 PC Card Standard. This standard incorporates the new 32-bit CardBus while retaining the 16-bit PC Card specification as defined by PCMCIA release 2.1. CardBus is intended to support "temporal" add-in functions on PC Cards, such as Memory cards, Network interfaces, FAX/Modems and other wireless communication cards, etc. The high performance and capability of the CardBus interface will enable the new development of many new functions and applications.

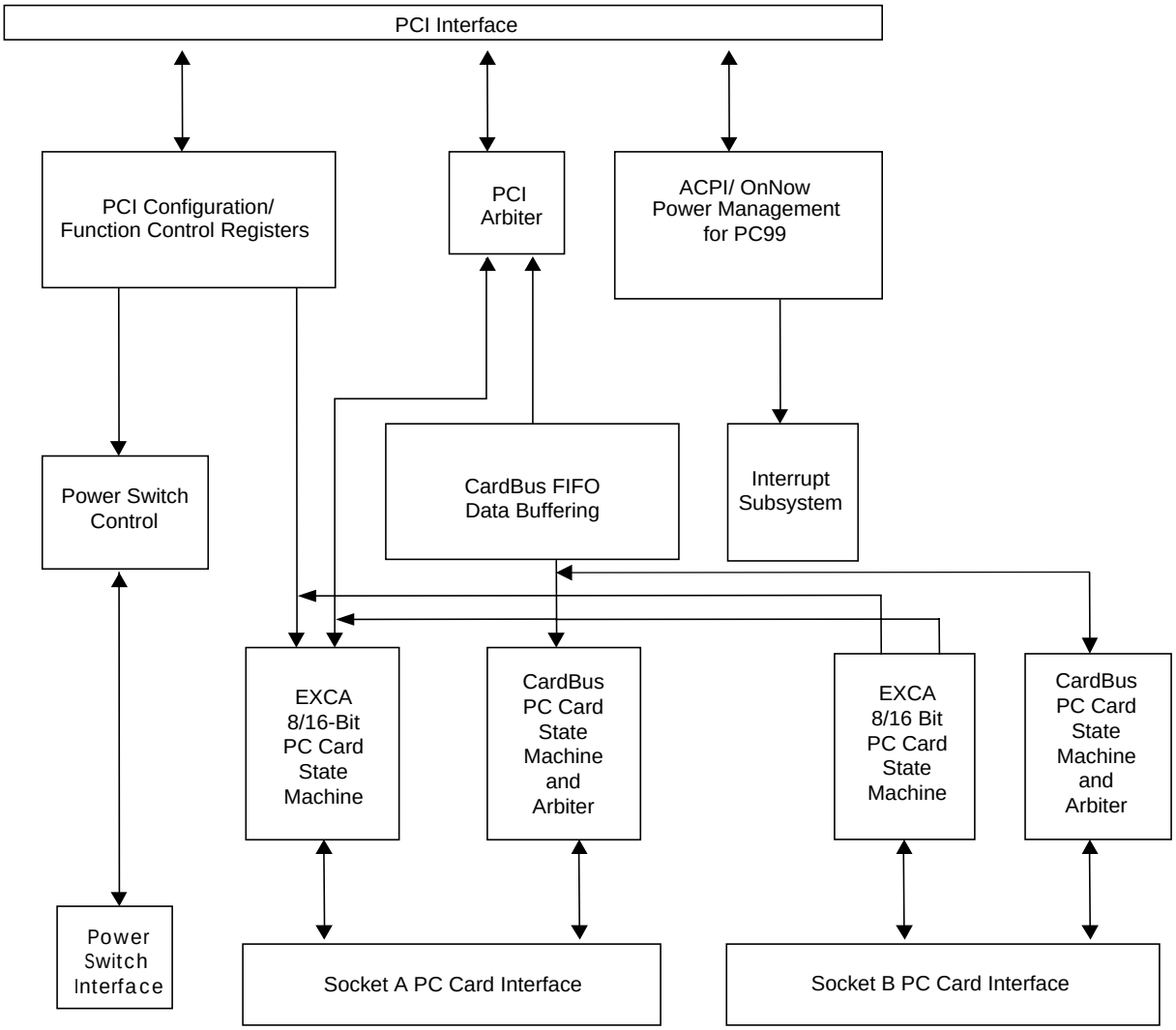
The OZ6933 CardBus controller is compliant with the latest ACPI-PCI Bus Power Management Interface Specification. It supports all four power states and the PME# function for maximum power savings and ACPI compliance. Additional compliance to OnNow Power Management includes $D3_{cold}$ state support, paving the way for low sleep state power consumption and minimized resume times. To allow host software to reduce power consumption further, the OZ6933 provides a power-down mode in which internal clock distribution and the PC Card socket clocks are stopped. An advanced CMOS process is also used to minimize system power consumption.

The OZ6933 dual PCMCIA socket supports two 3.3V/5V 8/16-bit PC Card R2 cards or 32-bit CardBus R3 cards. The R2 card support is compatible with the Intel 82365SL PCIC controller, and the R3 card support is fully compliant with the 2000 PC Card Standard CardBus specification. The OZ6933 is a stand alone device, which means that it does not require an additional buffer chip for the PC Card socket interface. In addition, the OZ6933 supports dynamic PC Card hot insertion and removal, with auto configuration capabilities.

The OZ6933 is fully compliant with the 33Mhz PCI Bus specification, v2.2. It supports a master device with internal CardBus direct data transfer. The OZ6933 implements a FIFO data buffer architecture between the PCI bus and CardBus socket interface to enhance data transfers to CardBus devices. The bi-directional FIFO buffer permits the OZ6933 to accept data from a target bus (PCI or CardBus interface) while simultaneously transferring data. This architecture not only speeds up data transfers but also prevents system deadlocks.

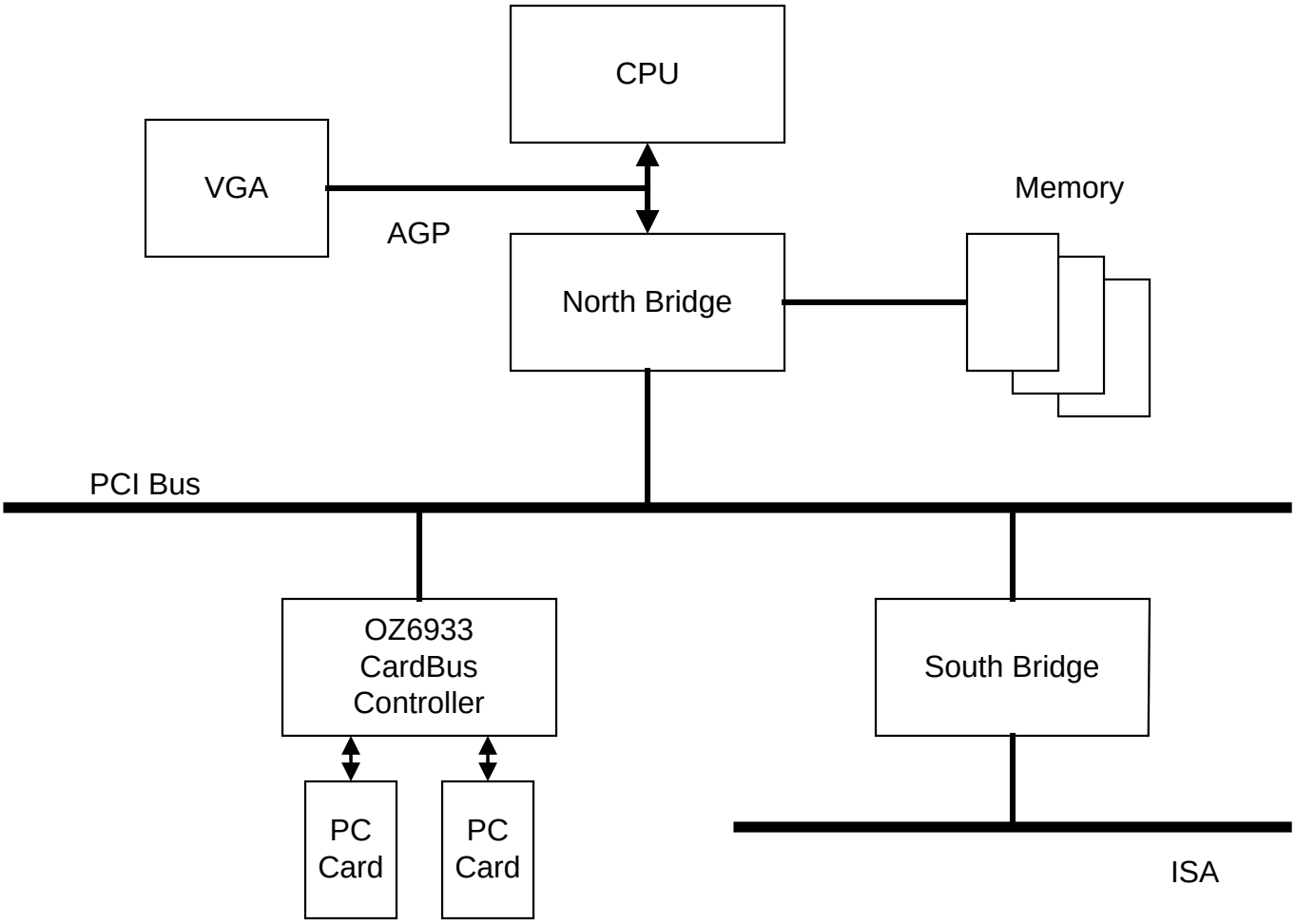
The OZ6933 is a PCMCIA R2/CardBus controller, providing the most advanced design flexibility for PC Cards that interface with advanced notebook designs.

FUNCTIONAL BLOCK DIAGRAM

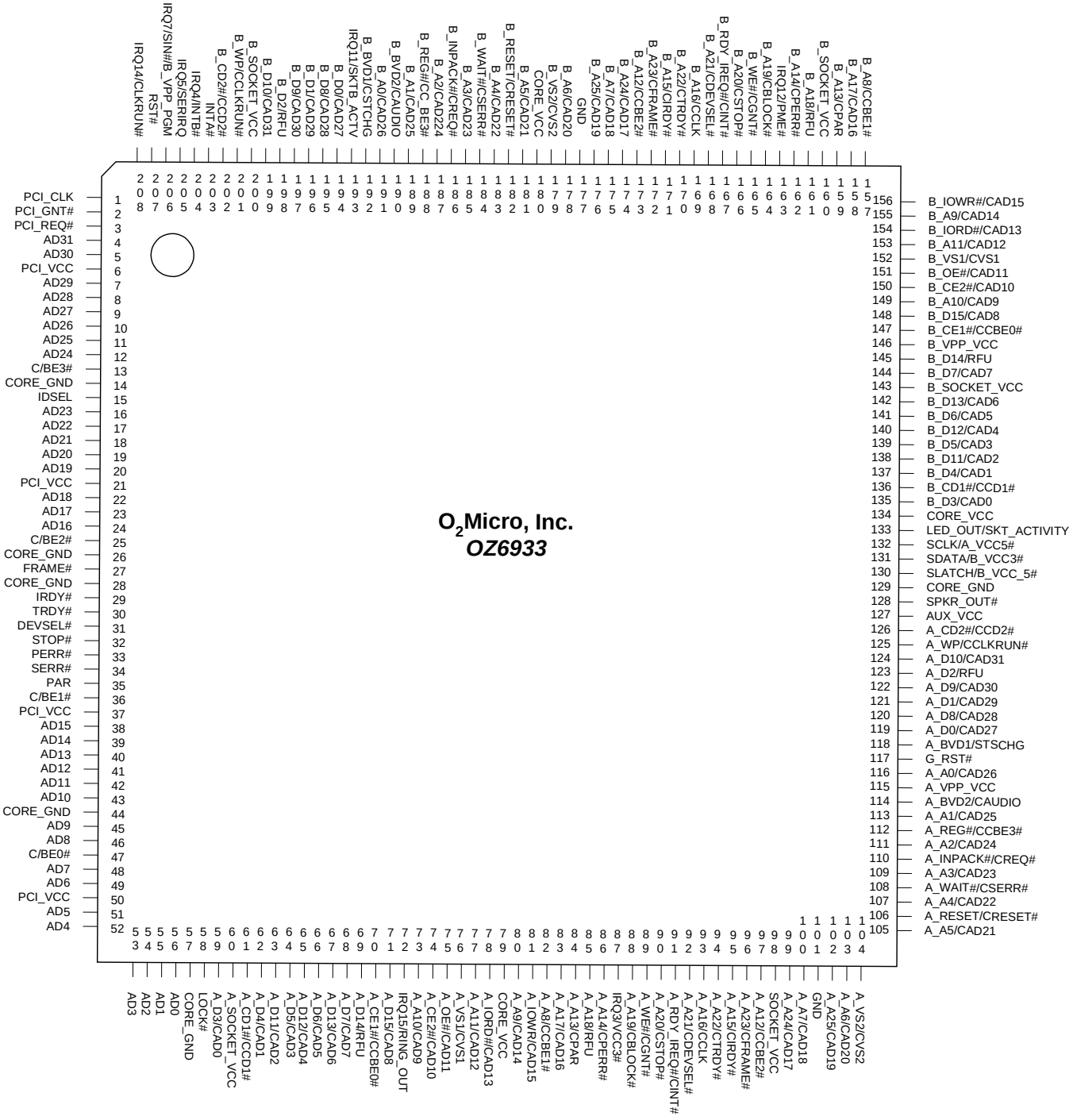


SYSTEM BLOCK DIAGRAM

The following diagram is a typical system block diagram utilizing the OZ6933 ACPI CardBus controller with other related chipsets.



PIN DIAGRAM - 208 PIN TQFP



PIN LIST

Bold Text = Normal Default Pin Name

PCI Bus Interface Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
AD[31:0]	**PCI Bus Address Input/Data:** These pins connect to PCI bus signals AD[31:0]. A Bus transaction consists of an address phase followed by one or more data phases.	4-5, 7-12, 16-20, 22-24, 38-43, 45-46, 48-49, 51-56	E1, E2, F3, F1, G5, H6, G3, G2, H2, H1, J1, J2, J3, J6, K1, K2, M5, N2, N1, N3, N6, P1, P3, N5, P6, R2, R3, T1, W4, R6, U5, P7	TTL	I/O	4	PCI Spec
C/BE[3:0]#	**PCI Bus Command/Byte Enable:** The command signaling and byte enables are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# are interpreted as the bus commands. During the data phase, C/BE[3:0]# are interpreted as byte enables. The byte enables are to be valid for the entirety of each data phase, and they indicate which bytes in the 32-bit data path are to carry meaningful data for the current data phase.	13, 25, 36, 47	G1, K3, M3, R1	TTL	I/O	4	-
FRAME#	**Cycle Frame:** This input indicates to the OZ6933 that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in its final phases.	27	K6	TTL	I/O	4	-
IRDY#	**Initiator Ready:** This input indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.	29	L1	TTL	I/O	4	-
TRDY#	**Target Ready:** This output indicates target Agent's the OZ6933's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.	30	L2	TTL	I/O	4	PCI Spec
STOP#	**Stop:** This output indicates the current target is requesting the master to stop the current transaction.	32	L5	TTL	I/O	4	PCI Spec
IDSEL	**Initialization Device Select:** This input is used as chip select during configuration read and write transactions. This is a point-to-point signal. IDSEL can be used as a chip select during configuration read and write transactions.	15	H5	TTL	I	4	-
DEVSEL#	**Device Select:** This output is driven active LOW when the PCI address is recognized as supported, thereby acting as the target for the current PCI cycle. The Target must respond before timeout occurs or the cycle will terminate.	31	L3	TTL	I/O	4	PCI Spec
PERR#	**Parity Error:** The output is driven active LOW when a data parity error is detected during a write phase.	33	L6	-	TO	4	PCI Spec

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
SERR#	**System Error:** This output is driven active LOW to indicate an address parity error.	34	M1	-	TO	4	PCI Spec
PAR	**Parity:** This pin generates PCI parity and ensures even parity across AD[31:0] and C/BE[3:0]#. During the address phase, PAR is valid after one clock. With data phases, PAR is stable one clock after a write or read transaction.	35	M2	TTL	I/O	4	PCI Spec
PCI_CLK	**PCI Clock:** This input provides timing for all transactions on the PCI bus to and from the OZ6933. All PCI bus signals, except RST#, are sampled and driven on the rising edge of PCI_CLK. This input can be operated at frequencies from 0 to 33MHz.	1	E3	TTL	I	4	-
RST#	**Device Reset**: This input is used to initialize all registers and internal logic to their reset states and place most OZ6933 pins in a HIGH-impedance state.	207	D1	TTL	I	1	-
RI_OUT	**Ring Indicate Out**: This pin is Ring Indicate when the following occurs while O_2 Mode Control B Register (index 2Eh) bit 7 is set to 1: 1) Power Control (Index+02h) bit 7 set to 1 2) Interrupt and General Control (Index+03h) bit 7 set to 1 3) PCI O_2Micro Control 2 (Offset: D4h) bit X = 0	72	V9	-	TO	1	6mA
CLKRUN#	**PCI Clock Run Request:** This signal is used by the central resource to request permission to stop the PCI clock or to slow it down, and the OZ6933 responds accordingly. To enable the CLKRUN# signal, you need to enable ExCA register 3B bit[3:2].	208	A4	TTL	I/O	4	PCI Spec
PME#	**Power Management Event:** A power management event is the process by which the OZ6933 can request a change of its power consumption state. Usually, a PME occurs during a request to change from a power saving state to the fully operational state.	163	B14	-	TO	1	6mA
SKTB_ACTV	**Socket B Activity:** This signal indicates that there is any activity on the socket B read/write access. Refer to PCI Configuration Register 90h.	193	E8	-	TO	1	6mA
INTA#	**PCI Bus Interrupt A:** This output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6933 to the system, a common use is to connect this pin to the system PCI bus INTA# signal.	203	B5	-	TO	4	PCI Spec

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
INTB#	**PCI Bus Interrupt B: T**his output indicates a programmable interrupt request generated from any of a number of card actions. Although there is no specific mapping requirement for connecting interrupt lines from the OZ6933 to the system, a common use is to connect this pin to the system PCI bus INTB# signal.	204	F6	-	TO	4	PCI Spec
IRQSER/ SOUT#/ IRQ5	**IRQSER/SOUT#/IRQ5:** In PC/PCI Serial Interrupt Signaling mode, this pin is the serial interrupt output, SOUT#. In PC/Way mode, this pin is the IRQ serializer pin to the interrupt controller. In the parallel ISA mode, this pin is the ISA IRQ5	205	C5	TTL	I/O	4	PCI Spec
IRQ7/SIN#/ B_VPP_PGM	**IRQ7/SIN#/B_VPP_PGM:** In PC/PCI Serial Input Signaling mode, this pin is the serial interrupt input, SIN#. In the parallel ISA mode, this pin is the ISA IRQ7. This pin also can be configured as parallel power control pin B_VPP_PGM	206	E6	TTL	I/O	1	6mA
GNT#	**Grant:** This signal indicates that access to the bus has been granted.	2	F5	TTL	I	4	PCI Spec
REQ#	**Request:** This signal indicates to the arbiter that the OZ6933 requests use of the bus.	3	G6	N/A	TO	4	PCI Spec
LOCK#	**PCI LOCK#:** This signal is used by a PCI master to perform a locked transaction to a target memory. LOCK# is used to prevent more than one master from using a particular system resource.	58	V5	TTL	I/O	4	PCI Spec
PCI_VCC	**PCI Bus VCC:** These pins must be connected to a 3.3-volt power supply. The PCI bus interface pin outputs listed in this table (Table 2-1) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6933 pin groups.	6, 21, 37, 50	F2, J5, M6, P5	-	PWR	-	-

PCMCIA Sockets Interface Pins

Socket A pin number --- Socket B pin number

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
-REG#/ CCBE3#	**Register Access:** During PCMCIA memory cycles, this output chooses between attribute and common memory. During I/O cycles for non-DMA transfers, this signal is active (low). During ATA mode, this signal is always inactive. For DMA cycles on the OZ6933 to a DMA-capable card, -REG is inactive during I/O cycles to indicate DACK to the PCMCIA card. **CardBus Command Byte Enable:** In CardBus mode, this pin is the CCBE3#.	112	N15	188	F9	1	I/O	2 or 3	CardBus spec.
A[25:24]/ CAD[19, 17]	PCMCIA socket address 25:24 outputs. **CardBus Address/Data:** CardBus mode, these pins are the CAD bits 19 and 17.	102, 99	U15, W15	176, 174	C11, A11	2	I/O	2 or 3	CardBus spec.
A23/ CFRAME#	PCMCIA socket address 23 output. **CardBus Frame:** In CardBus mode, this pin is the CFRAME# signal.	96	U14	172	B12	1	I/O	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
A22/ CTRDY#	PCMCIA socket address 22 output. **CardBus Target Ready:** In CardBus mode, this pin is the CTRDY# signal.	94	W14	170	A13	1	I/O-PU	2 or 3	CardBus spec.
A21/ CDEVSEL#	PCMCIA socket address 21 output. **CardBus Device Select:** In CardBus mode, this pin is the CDEVSEL# signal.	92	U13	168	B13	1	I/O-PU	2 or 3	CardBus spec.
A20/ CSTOP#	PCMCIA socket address 20 output. **CardBus Stop:** In CardBus mode, this pin is the CSTOP# signal.	90	W13	166	C13	1	I/O-PU	2 or 3	CardBus spec.
A19/ CBLOCK#	PCMCIA socket address 19 output. **CardBus Lock:** In CardBus mode, this signal is the CBLOCK# signal used for locked transactions.	88	U12	164	A14	1	I/O-PU	2 or 3	CardBus spec.
A18/ RFU	PCMCIA socket address 18 output. **Reserved:** In CardBus mode, this pin is reserved for future use.	85	D11	161	C14	1	TO	2 or 3	CardBus spec.
A17/ CAD16	PCMCIA socket address 17 output. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 16.	83	U11	158	E14	1	I/O	2 or 3	CardBus spec.
A16/ CCLK#	PCMCIA socket address 16 output. **CardBus Clock:** In CardBus mode, this pin supplies the clock to the inserted card.	93	V13	169	E12	1	I/O	2 or 3	CardBus spec.
A15/ CIRDY#	PCMCIA socket address 15 output. **CardBus Initiator Ready:** In CardBus mode, this pin is the CIRDY# signal.	95	P13	171	C12	1	I/O-PU	2 or 3	CardBus spec.
A14/ CPERR#	PCMCIA socket address 14 output. **CardBus Parity Error:** CardBus mode, this pin is the CPERR# signal.	86	V12	162	A15	1	I/O-PU	2 or 3	CardBus spec.
A13/ CPAR	PCMCIA socket address 13 output. **CardBus Parity:b** In CardBus mode, this pin is the CPAR signal.	84	R11	159	C15	1	I/O	2 or 3	CardBus spec.
A12/ CCBE2#	PCMCIA socket address 12 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE2# signal.	97	V14	173	A12	1	I/O	2 or 3	CardBus spec.
A[11:9]/ CAD[12, 9, 14]	PCMCIA socket address 11:9 output. **CardBus Address/Data:** In CardBus mode, these pin are the CAD bits 12, 9 and 14.	77, 73, 80	V10, U9, W11	153, 149, 155	F14, F18, F15	3	I/O	2 or 3	CardBus spec.
A8/ CCBE1#	PCMCIA socket address 8 output. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBE1# signal.	82	V11	157	A16	1	I/O	2 or 3	CardBus spec.
A[7:0]/ CAD[18, 20-26]	PCMCIA socket address 7:0 outputs. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 18 and 20:26.	100, 103, 105, 107, 109, 111, 113, 116	P14, R14, T19, R17, N14, R19, P18, N17	175, 178, 181, 183, 185, 187, 189, 191	B11, F11, E10, F10, B9, E9, A8, B8	8	I/O	2 or 3	CardBus spec.
D15/ CAD8	PCMCIA socket data/0 bit 15. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 8.	71	W9	148	F17	1	I/O	2 or 3	CardBus spec.
D14/ RFU	PCMCIA socket data I/0 bit 14. **Reserved:** In CardBus mode, this pin is reserved for future use.	69	V8	145	G17	1	I/O	2 or 3	2 mA

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
D[13:3]/ CAD[6, 4, 2, 31, 30, 28, 7, 5, 3, 1, 0]	PCMCIA socket data I/0 bits 13:3. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 6 4, 2, 31, 30, 28, 7, 5, 3, 1, and 0, respectively.	67, 65, 63, 124, 122, 120, 68, 66, 64, 62, 59	P8, V7, W6, L18, M19, M15, U8, W7, U7, P8, U6	142, 140, 138, 199, 197, 195, 144, 141, 139, 137, 135	H15, H17, H19, B6, A6, C7, G18, H14, H18, J14, J17	11	I/O	2 or 3	CardBus spec.
D2/ RFU	PCMCIA socket data I/O bit 2. **Reserved:** In CardBus mode, this pin is reserved for future use.	123	L19	198	F7	1	I/O	2 or 3	CardBus spec.
D[1:0]/ CAD[29,27]	PCMCIA socket data I/O bits 1:0. **CardBus Address/Data:** In CardBus mode, these pins are the CAD bits 29 and 27, respectively.	121, 119	M18, M17	196, 194	B7, A7	2	I/O	2 or 3	CardBus spec.
-OE/ CAD11	**Output Enable**: This output goes active (low) to indicate a memory read from the PCMCIA socket to the OZ6933. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 11.	75	P9	151	G15	1	I/O	2 or 3	CardBus spec.
-WE/ CGNT#	**Write Enable**: This output goes active (low) to indicate a memory write from the OZ6933 to the PCMCIA socket. **CardBus Grant:** In CardBus mode, this pin is the CGNT# signal.	89	R12	165	E13	1	TO	2 or 3	CardBus spec.
-IORD/ CAD13	**I/O Read**: This output goes active (low) for I/O reads from the socket to the OZ6933. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 13.	78	U10	154	E17	1	I/O	2 or 3	CardBus spec.
-IOWR/ CAD15	**I/O Write**: This output goes active (low) for I/O writes from the OZ6933 to the socket. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 15.	81	P10	156	D19	1	I/O	2 or 3	CardBus spec.
WP/ -IOIS16/ CCLKRUN#	**Write Protect/ I/O Is 16-Bit**: In Memory Card Interface mode, this inputs is interpreted as the status of the write protect switch on the PCMCIA card. In I/O Card Interface mode, this input indicates the size of the I/O data at the current address on the PCMCIA card. **CardBus Clock Run:** In CardBus mode, this pin is the CCLKRUN# signal, which starts and stops the CardBus CCLK. To enable the CLKRUN# signal, ExCA register 3Bh/7Bh bit[3:2] must be enabled.	125	L17	201	A5	1	I/O-PU	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
-INPACK/ CREQ#	**Input Acknowledge**: The -INPACK function is not applicable in PCI bus environments. However, for compatibility with other Cirrus Logic products, this pin should be connected to the PCMCIA socket's -INPACK pin. **CardBus Request:** In CardBus mode, this pin is the CREQ# signal.	110	P17	186	C9	1	I-PU	2 or 3	CardBus spec.
RDY/ -IREQ/ CINT#	**Ready/Interrupt Request**: In Memory Card Interface mode, this input indicates to the OZ6933 that the card is either ready or busy. In I/O Card Interface mode, this input indicates a card interrupt request. **CardBus Interrupt:** In CardBus mode, this pin is the CINT# signal. This signal is active-low and level-sensitive.	91	P12	167	F12	1	I-PU	2 or 3	CardBus spec.
-WAIT/ CSERR#	**Wait**: This input indicates a request by the card to the OZ6933 to halt the cycle in progress until this signal is deactivated. **CardBus System Error:** In CardBus mode, this pin is the CSERR# signal.	108	R18	184	A9	1	I-PU	2 or 3	CardBus spec.
CD[2:1]/ CCD[2:1]#	**Card Detect**: These inputs indicate to the OZ6933 that a card is in the socket. They are internally pulled high to the voltage of the AuxVCC power pin. **CardBus Card Detect:** In CardBus mode, these inputs are used with CVS[2:1] to detect presence and type of card.	126, 61	L14, V6	202, 136	C6, J15	2	I-PU-Schmitt	1	CardBus spec.
-CE2/ CAD10	**Card Enable** pin is driven low by the OZ6933 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. **CardBus Address/Data:** In CardBus mode, this pin is the CAD bit 10.	74	R9	150	E19	1	I/O	2 or 3	CardBus spec.
-CE1/ CCBE0#	**Card Enable** pin is driven low by the OZ6933 during card access cycles to control byte/word card access. -CE1 enables even-numbered address bytes, and -CE2 enables odd-numbered address bytes. When configured for 8-bit cards, only -CE1 is active and A0 is used to indicate access of odd- or even-numbered bytes. **CardBus Command/Byte Enable:** In CardBus mode, this pin is the CCBEO# signal.	70	W8	147	G14	1	I/O	2 or 3	CardBus spec.
RESET/ CRST#	**Card Reset**: This output is low for normal operation and goes high to reset the card. To prevent reset glitches to a card, this signal is high-impedance unless a card is seated in the socket, card power is applied, and the card's interface signals are enabled. **CardBus Reset:** In CardBus mode, this pin is the CRST# output.	106	P15	182	C10	1	TO	2 or 3	CardBus spec.

Name[1]	Description[2]	Pin Number				Qty	I/O	Pwr	Drive
		Socket A		Socket B					
		TQFP	BGA	TQFP	BGA				
BVD2/ -SPKR/ -LED/ CAUDIO	**Battery Voltage Detect 2/Speaker/ LED**: In Memory Card Interface mode, this input serves as the BVD2 (battery warning status) input. In I/O Card Interface mode, this input can be configured as a card's -SPKR binary audio input. For ATA or non-ATA (SFF-68) disk-drive support, this input can also be configured as a drive-status LED input. **CardBus Audio:** In CardBus mode, this pin is the CAUDIO input.	114	M14	190	C8	1	I-PU	2 or 3	-
BVD1/ -STSCHG/ -RI/ CSTSCHG	**Battery Voltage Detect 1/Status Change/Ring Indicate**: In Memory Card Interface mode, this input serves as the BVD1 (battery-dead status) input. In I/O Card Interface mode, this input is the -STSCHG input, which indicates to the OZ6933 that the card's internal status has changed. If bit 7 of the **Interrupt and General Control** register is set to `1`, this pin serves as the ring indicate input for wakeup-on-ring system power management support. **CardBus Status Change:** In CardBus mode, this pin is the CSTSCHG. This pin can be used to generate PME#.	118	N19	192	F8	1	I-PU	2 or 3	-
VS2/ CVS2	**Voltage Sense 2:** This pin is used in conjunction with VS1 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the AuxVCC power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 57. **CardBus Voltage Sense:** In CardBus mode, these pins are the CVS2 pins.	104	W16	179	A10	1	I/O-PU	1	CB-spec
VS1/ CVS1	**Voltage Sense 1:** This pin is used in conjunction with VS2 to determine the operating voltage of the card. This pin is internally pulled high to the voltage of the AuxVCC power pin under the combined control of the external data write bits and the CD pull up control bits. This pin connects to PCMCIA socket pin 43. **CardBus Voltage Sense:** In CardBus mode, these pins are the CVS1 pins.	76	W10	152	E18	1	I/O-PU	1	CB-spec
SOCKET_VCC	Connect these pins to the Vcc supply of the socket (pins 17 and 51 of the respective PCMCIA socket). These pins can be 0, 3.3, or 5 V, depending on card presence, card type, and system configuration. The socket interface outputs (listed in this table, Table 2-2) will operate at the voltage applied to these pins, independent of the voltage applied to other OZ6933 pin groups.	60, 198	R7, R13	200, 160, 143	E7, F13, G19	2, 3	PWR	-	-

[1]To differentiate the sockets in the pin diagram, all socket- specific pins have either A_ or B_ prefixes to the pin names indicated. For example, A_A[25:0] and B_A[25:0] are the independent address buses to the sockets.
[2]When a socket is configured as an ATA drive interface, socket interface pin functions change.

Power Control and General Interface Pins

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
SPKR_OUT	**Speaker Output:** This output can be used as a digital output to a speaker to allow a system to support PC Card fax/modem/voice and audio sound output. This output is enabled by setting the socket's **Misc Control 1** register bit 4 to "1" (for the socket whose speaker signal is to be directed from BVD2/-SPKR/-Led to this pin).	128	K19	TTL	I/O	1	6mA
LED_OUT/ SKTA_ACTV	**LED Output/SKTA_ACTV:** This output can be used as an LED driver to indicate disk activity when a socket's BVD2/-SPKR/-LED pin has been programmed for LED support. In the O2 Mode(Index 3B/7B bit 5) , this pin indicates the socket A activity. The socket B activity refers to PCI Configuration Register offset 90h (Mux Control register)	133	J19	TTL	I/O	1	6mA
CPWRCLK/ A_VCC5#	**Card Power Clock:** This input is used as a reference clock (10-100 kHz, usually 32 kHz) to control the serial interface of the socket power control chips. A_VCC5#: This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of A_VCC3#.	132	K14	TTL	I/O	1	6mA
CPWRDATA/ B_VCC3#	**Card Power Serial Data:** This pin serves as output DATA pin when used with the serial interface of Texas Instruments' TPS2206IDF & Micrel 2564 socket power control chip. B_VCC3#: This active-LOW output controls the 3.3-volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of B_VCC5#.	131	K15	TTL	I/O	1	6mA
CPWRLATC/ B_VCC5#	**Card Power Serial Latch:** This pin serves as output LATCH pin when used with the serial interface of Texas Instruments' TPS2206IDF & Micrel 2564 socket power control chip. B_VCC5#: This active-LOW output controls the 5 -volt supply to the A socket's VCC pins. The active-LOW level of this output is mutually exclusive with that of B_VCC3#.	130	K17	N/A	I/O	1	6mA

Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
IRQ3/ A_VCC3#	**A_VCC3#/IRQ3**: This active-LOW output controls of the 3.3-volt supply to the socket's VCC pins. The active-LOW level of this output is mutually exclusive with of VCC_5#. **This mode active only in SktPwr Parallel mode enabled.** This pin can be IRQ3 in parallel IRQ mode.	87	W12	N/A	TO	1	6mA
IRQ9/ A_VPP_VCC	**VPP_VCC/IRQ9:** This active-HIGH output controls the socket A VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled** This pin can be configured as IRQ9 in parallel IRQ mode.	115	P19	N/A	TO	1	6mA
IRQ10/ B_VPP_VCC	**VPP_VCC/IRQ10:** This active-HIGH output controls the socket B VCC supply to the socket's VPP1 and VPP2 pins. The active-HIGH level of this output is mutually exclusive with that of VPP_PGM. **This mode active only in SktPwr Parallel mode enabled.** This pin can be configured as IRQ10 in parallel IRQ mode.	146	F19	N/A	TO	1	6mA
G_RST#	**Global_Reset#:** This signal can be connected to either PCI reset or ACPI reset depending on system implementation. If the D3 cold state is implemented, this signal should be connected to the ACPI reset, otherwise, connect to PCI reset. This signal can reset the PME content under the D3 cold state if AUX_VCC is provided	117	N18	TTL	I	1	-

Power, Ground, and Reserved Pins

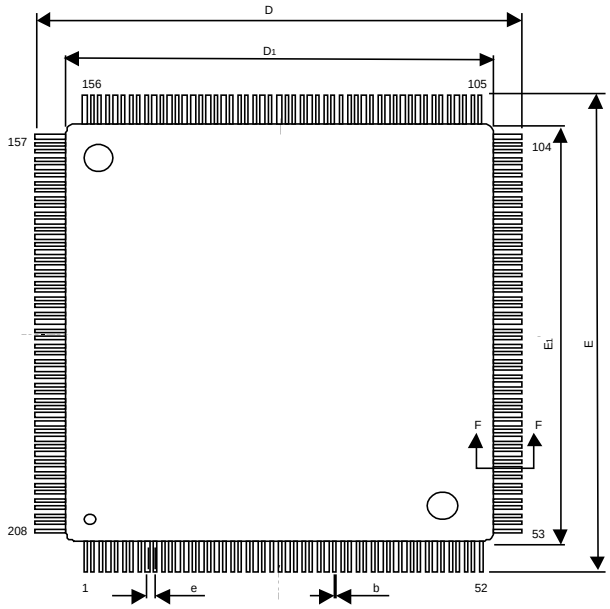
Pin Name	Description	Pin Number		Input	Type	Power Rail	Drive
		TQFP	BGA				
AUX_VCC	This pin must be connected to the system's 3.3-volt supply.	127	L15	N/A	PWR	-	-
CORE_VCC	This pin provides power to the core circuitry of the OZ6933. It must be connected to a 3.3 power supply.	180, 134, 79	B10, J18, R10	N/A	PWR	-	-
GND	All OZ6933 ground pins must be connected to system ground.	14, 26, 28, 44, 57, 101, 129, 177	H3, K5, K5, P2, W5, V15, K18, E11	N/A	GND	-	-

Legend

I/O Type	Description
I	Input Pin
I-PU	Input pin with internal pull-up
O	Output
OD	Open-drain
TO	Tri-state output
TO-PU	Tri-state output with internal pull-up
OD-PU	Open-drain output with internal pull-up
PW	Power pin

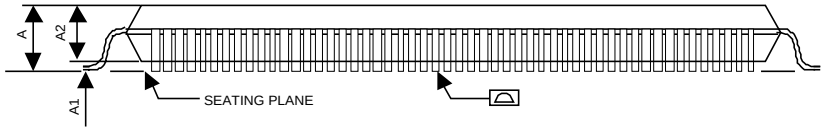
Power Rail	Source of Output's Power
1	AUX_VCC: outputs powered from AUX_VCC
2	A_SLOT_VCC: outputs powered from the socket A
3	B_SLOT_VCC: outputs powered from the socket B
4	PCI_VCC: outputs powered from PCI bus power supply
5	CORE_VCC: outputs powered from the CORE_VCC

PACKAGE SPECIFICATIONS

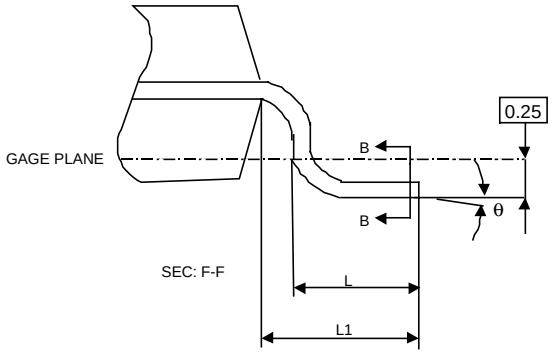


OZ6933 208-PIN TQFP

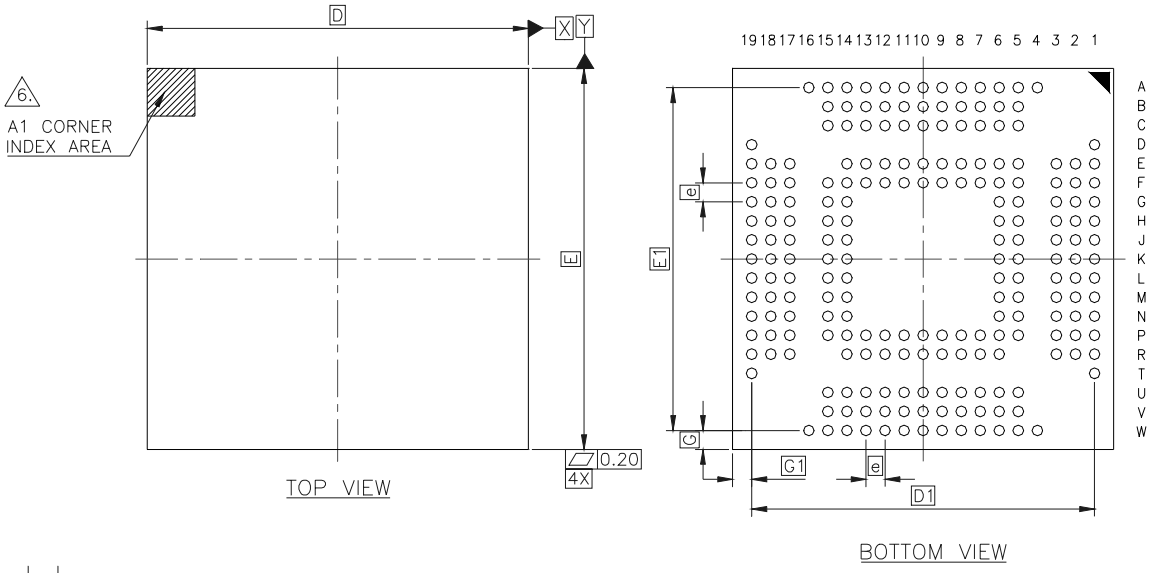
O_2MICRO, INC.

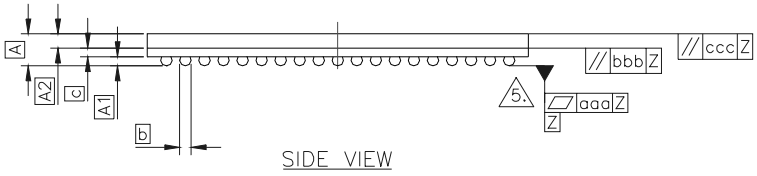


Symbol	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.063	-	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D		1.181			30.00 BSC.	
D_1		1.102			28.00 BSC.	
E		1.181			30.00 BSC.	
E_1		1.102			28.00 BSC.	
e		0.020 BSC.			0.50 BSC.	
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039 REF			1.00 REF	
θ	0°	3.5°	7°	0°	3.5°	7°



208 PIN – BGA





PACKAGE SPECIFICATION			
SYMBOL	MIN	NOM	MAX
D	15.90	16.00	16.10
E	15.90	16.00	16.10
D1		14.40	
E1		14.40	
e		0.80	
A	1.24	1.34	1.44
A1	0.33	0.38	0.43
A2	0.55	0.60	0.65
c	0.32	0.36	0.40
b	0.43	0.48	0.53
G		0.80	
G1		0.80	
aaa		0.12	
bbb		0.10	
ccc		0.10	
M1		19	
M2		19	
N		361	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
3. "N" REPRESENTS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE M1 AND M2.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW AND PARALLEL TO PRIMARY DATUM Z, THE ORIGINAL SOLDER BALL DIAMETER IS 0.45 mm.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. A1 CORNER MUST BE IDENTIFIED BY INK MARK, METALLIZED MARKINGS, IDENTATION OR OTHER FEATURE OF PACKAGE BODY, LID OR INTEGRAL HEATSLUG, ON THE TOP SURFACE OF THE PACKAGE.
7. SOLDER BALL DEPOPULATION IS ALLOWED. DEPOPULATION IS THE OMISSION OF BALLS FROM A FULL MATRIX (M1 OR M2).
8. BALL PAD A1 CORNER INDICATOR (NC) SOLDER BALL