PCI Bus Operation

A guide for the uninformed by the slightly less uninformed!

E. Hazen - 09/17/99

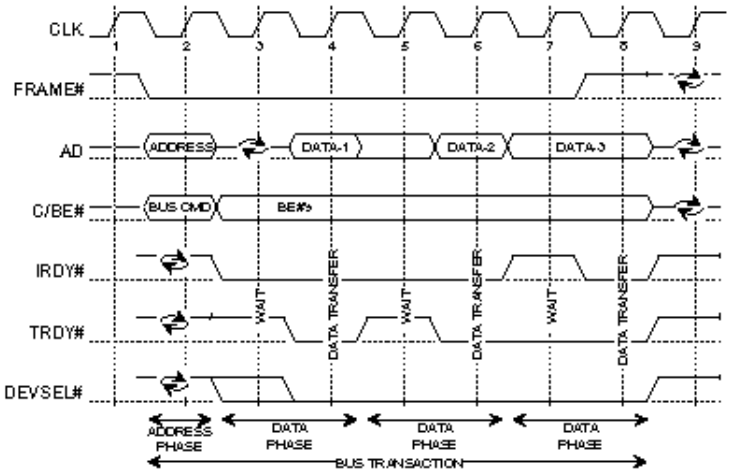
PCI Fundamentals

The PCI bus is the de-facto standard bus for current-generation personal computers. The main advantages for embedded applications like the STT are:

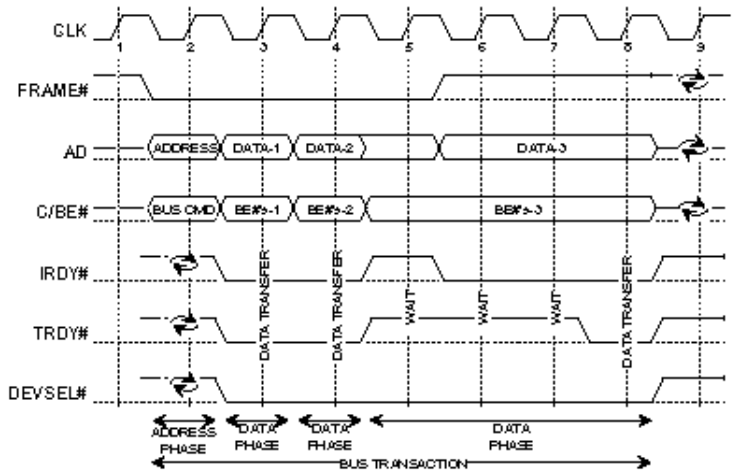
- direct implementation in FPGAs (no data buffers or glue chips)
- efficient protocol ("data burst" is the standard transfer)
- ready availability of development hardware (PC motherboards or VME carriers)

The PCI bus is a 32- or 64-bit wide bus with multiplexed address and data lines. The bus requires about 47 lines for a complete (32-bit) implementation. The standard operating speed is 33MHz, and data can be transferred continuously at this rate for large bursts.

The basic transfer mechanism is a burst, composed of an address phase and one or more data phases. Typical read and write transfers are illustrated below:



PCI Read Cycle. Note that the first data phase is delayed by the target, the second is not delayed (full speed) and the third is delayed by the master.



PCI Write Cycle. The first two data phases run at full speed, while the second is delayed first by the master, then by the target.

Required PCI Bus Signals

All required PCI bus signals is shown in the table below with explanations.

Signal Name	Driven by	Description
CLK	Master	Bus Clock (normally 33MHz; DC okay)
FRAME#	Master	Indicates start of a bus cycle
AD[31:0]	Master/Target	Address/Data bus (multiplexed)
C/BE#[3:0]	Master	Bus command (address phase) Byte enables (data phases)
IRDY#	Master	Ready signal from master
TRDY#	Target	Ready signal from target
DEVSEL#	Target	Address recognized
RST#	Master	System Reset
PAR	Master/Target	Parity on AD, C/BE#
STOP#	Target	Request to stop transaction
IDSEL		Chip select during initialization transactions
PERR#	Receiver	Parity Error
SERR#	Any	Catestrophic system error

PCI vs PMC vs PC-MIP

Confused by all those acronyms? Me, too!

PCI is the basic bus standard. It defines the electrical characteristics, protocol, and the

standard plug-in card format which is used in PCS.
PMC (PCI Mezzanine Card) is the mezzanine card format I propose for the logic boards. It is electrically compatible with the standard PCI bus. PMC modules are widely used in physics and industry.
PC-MIP is another, smaller mezzanine card format which is also electrically compatible with PCI. It is also an industrial standard, typically used for I/O.

Sources of Additional Information

- **PCI SIG** - the keeper of the PCI bus specification (available from their web site for $50). They also have a brief Introduction to the PCI bus.
- Altera PCI and Bus Interfaces page.
-

PCI Development Options

PCI Bus Interfaces

Complete Chips (PLX, AMCC, Intel, others)

Stand-alone solution; easy to get working
Working examples we can steal from (CMS groups)

FPGA and CPLD "cores"

Altera, Xilinx, Cypress and others provide "ready-to-compile" blocks
Some are expensive (Altera = $15k!), some are free (Cypress)
Efficient use of board space (can put other stuff in FPGA)

Development Platforms

PC Motherboard with adapter cards

Can buy adapters of various types for PMC and PC-MIP coards
PCI bus is built-in to all modern PC motherboards
Can build a "development system" for < $500
Lots of experience at CERN and other places with this option

VME Carrier Boards

Various "Intelligent" (with CPU) and "non-Intelligent" boards exist
Need working VME system
Expensive to get started (VME crate plus $3-$5k for modules)
...but, we ultimately need VME

D0 STT Meeting

E. Hazen - 24 September 99

Test Fixtures Needed

Testing FRC:

- CFT/CTT Simulator (G-Link Tx + memory) — Ed Barsotti?
- SCL Simulator (????)
- STC Simulator (LVDS Rx on PCI bus) — Develop Ourselves
- Receiver for J3 aux bus buffering signals (wire-wrap thing?)

Testing STC:

- FRC Road Simulator (LVDS Tx on PCI bus) — Develop Ourselves
- FRC J3 buffer signals simulator (????)
- SMT data source (SVX simulator + Sequencer + crate?)
  (or another G-Link transmitter from Ed Barsotti)
- TFC Simulator (LVDS Rx on PCI bus) — Develop Ourselves

Testing TFC/ZVC:

- STC Simulator (LVDS Tx on PCI bus) — Develop Ourselves
- FRC J3 buffer signals simulator (????)

Other Common Test Fixtures:

- VIPA Crate (with power supplies)
- VBD
- VME CPU board
- VME extender
- VME display/switch module
- Test software (some OS for CPU)