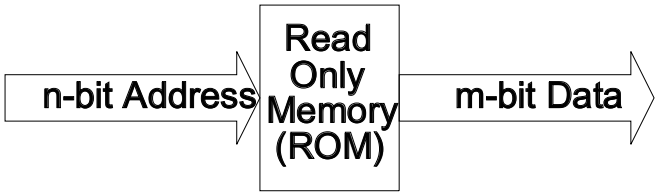
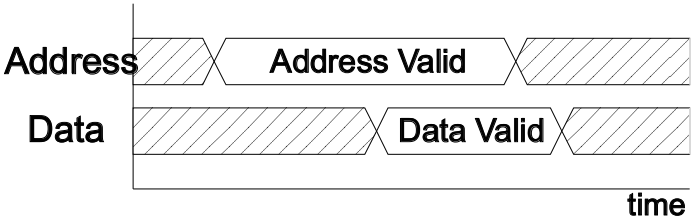
The ISA Bus:

Communicating With The Outside World

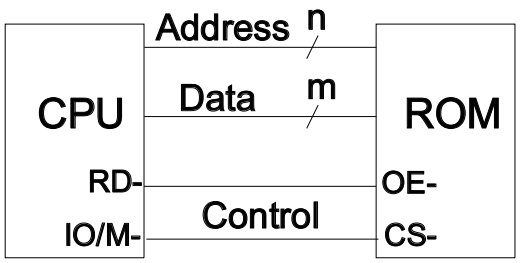
A Simple Example Of Memory System Timing

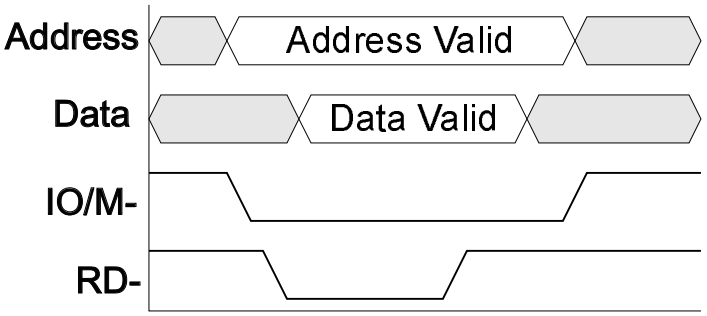
A typical memory system has an n-bit address bus and an m-bit data bus along with several other control signals. The time between applying an address to the memory and receiving data in return is called the access time of the memory.





In a real microprocessor system, the timing relationships between the signals on the bus determine what the system does. In this example, a memory read instruction has been issued by the processor. (How do I know that?)





Ok, But Where Do These Signals Come From?

Good question.

The fact is, a real microprocessor system is really pretty complicated. Not because any one thing is difficult to understand, but because there are so many things going on at the same time. Also, there are many ways to do things.

For now, remember our onion. Shortly, we'll apply the "onion principle" to microprocessor signals.

Also, remember our lowly flip-flop. We saw that this simple logic element had a lot of the same interface signals (**data, address, and control**) that we see in a microprocessor system.

Next, keep in mind that the **microprocessor is the boss**. Except in very, very special circumstances it is the microprocessor that controls everything that happens in the system.

Last, think about what the signals **do** and **why**. Names of signals change for different processors. Timing specifications change. But all processors end up doing things just about the same way.

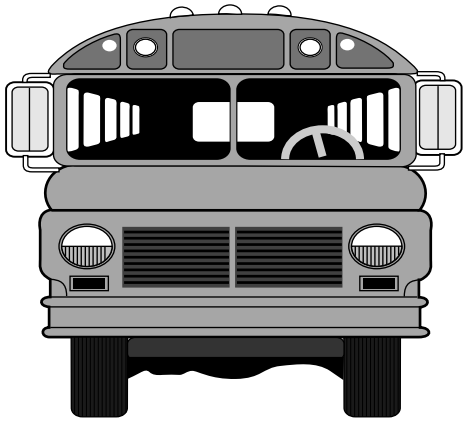
On with the show!

The Basic Idea Of A Bus

Question:

What is a bus???

Answer:



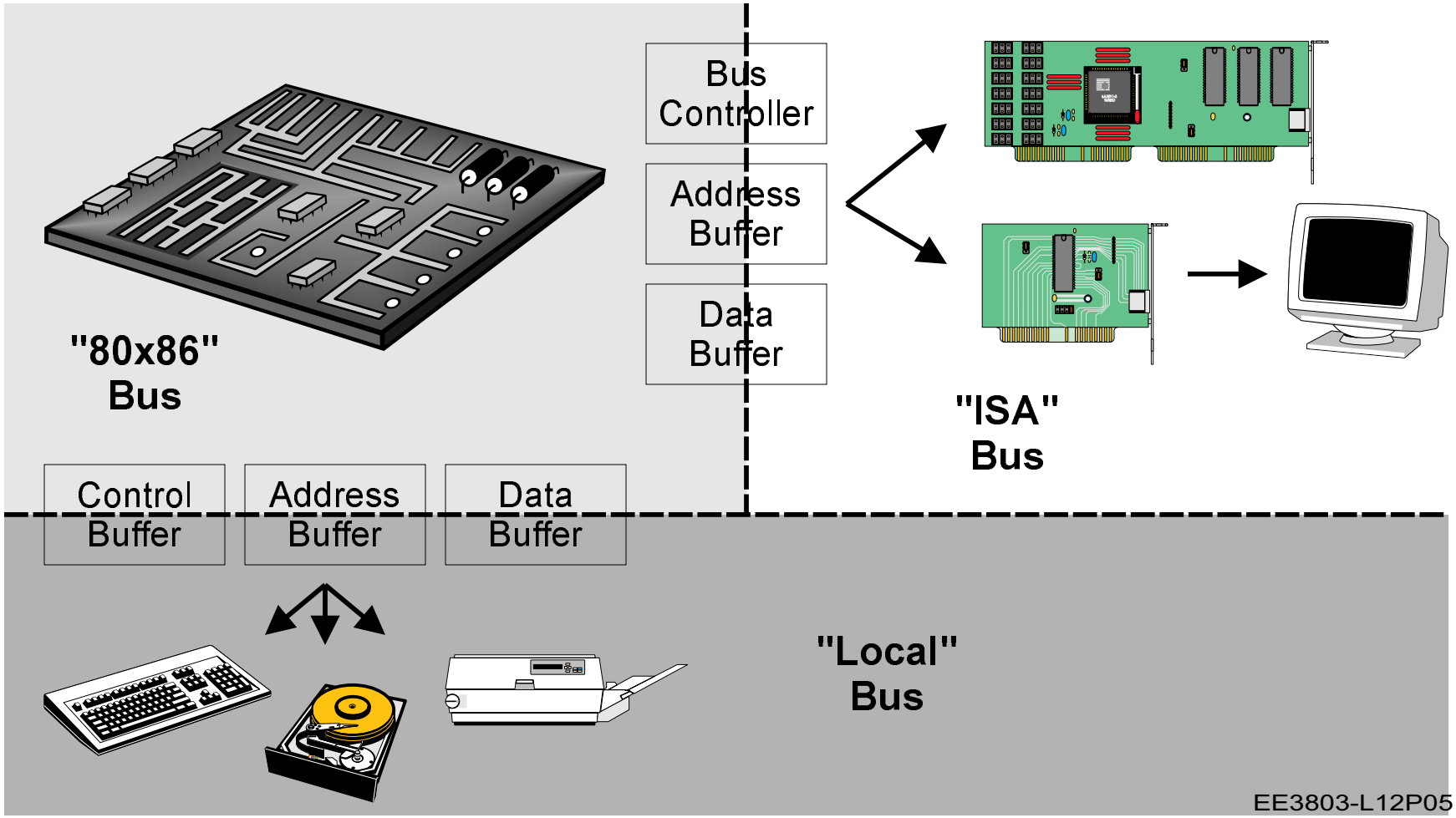
A bit silly? Perhaps. But let's look at the analogy.

A Bus:

- Carries multiple things with a common purpose.
- Can have different drivers at different times.
- Can travel in multiple directions.
- Is subject to collisions (which should be avoided at all times).
- May require you to transfer from one bus to another to get where you want to go.
- May look different than another, but fulfills the same basic purpose.

Microprocessor Buses

Like our software model of the PC, the bus structure of the PC has a couple of different levels. The ISA, or Industry Standard Architecture bus lies at the top level and the actual processor bus lies at the bottom.



The ISA Bus "Cycles"

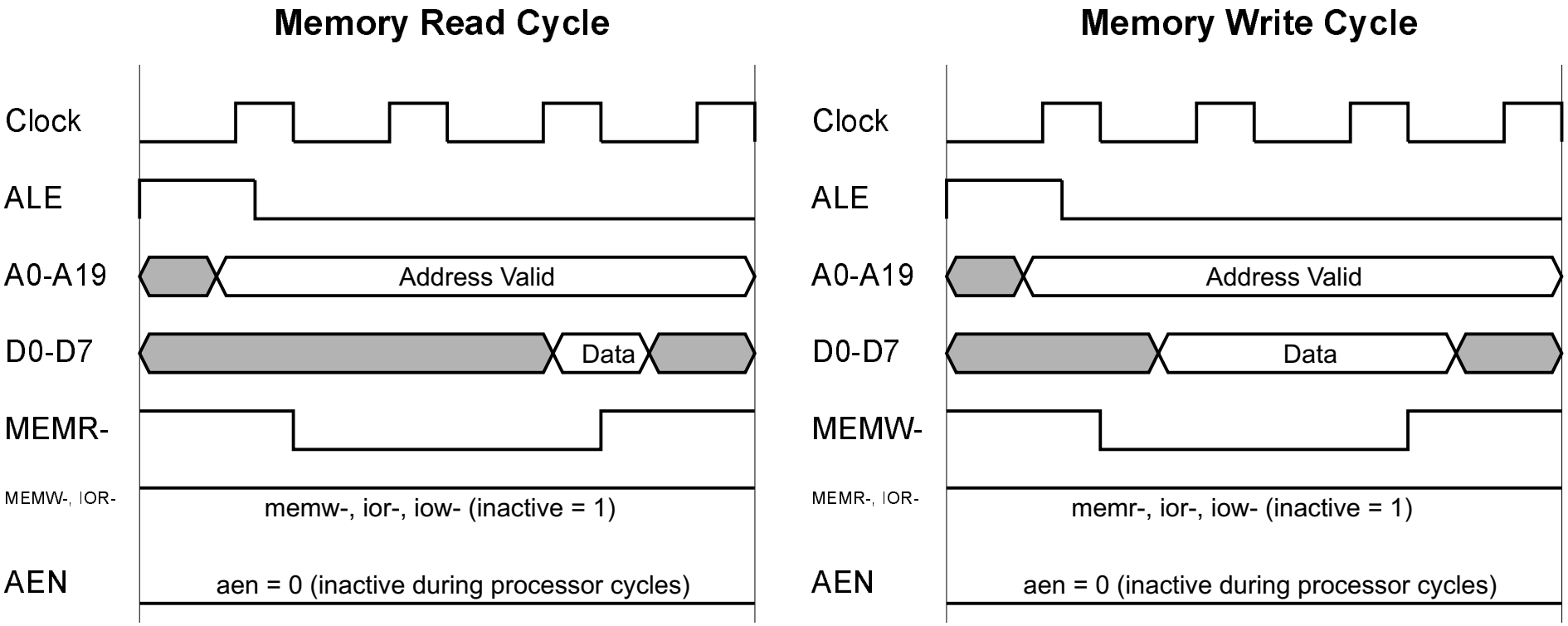
When computer engineers talk buses, they talk in terms of "bus cycles." A bus cycle refers to the type of transfer that is taking place on the bus and to the signals that are important in making that transfer take place.

On the ISA bus there are four bus cycles in which the 80x86 drive the bus and two when another device (called the DMA controller) drives the bus.

The cycles where the 80x86 is in control are:

Bus Cycle	Purpose	Data Flow
Memory Read	The processor is fetching data or instructions.	From memory to the 80x86.
Memory Write	The processor is writing data.	From processor to memory.
I/O Read	Data is being fetched from I/O.	From I/O port to 80x86.
I/O Write	Data is being written from I/O.	From processor to I/O port.

The Memory Read and Write Cycles



The I/O Port Read and Write Cycles