Design with Microprocessors

Year III Computer Sci. English
1-st Semester

Lecture 11:
Direct Memory Access (DMA)
&
DMA Controlled I/O

Direct memory access

Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.

DMA is for **high-speed data transfer** from/to mass storage peripherals, e.g. hard-disk drive,CD-ROM, and sometimes video controllers.

The basic idea of **DMA** is to transfer *blocks of data* directly between memory and peripherals. The data don't go through the microprocessor but the system data bus is occupied.

"Normal" transfer of one data byte takes up to 29 clock cycles. The DMA transfer requires only 5 clock cycles.

Nowadays, DMA can transfer data as fast as 60 MB per second or more. The transfer rate is limited by the speed of memory and peripheral devices.

Basic process of DMA

For 8088/8086 in minimum mode:

The HOLD and HLDA pins are used to receive and acknowledge the hold request respectively.

Normally the CPU has full control of the system bus. In a DMA operation, the peripheral takes over bus control temporarily.

Sequence of events of a typical DMA process

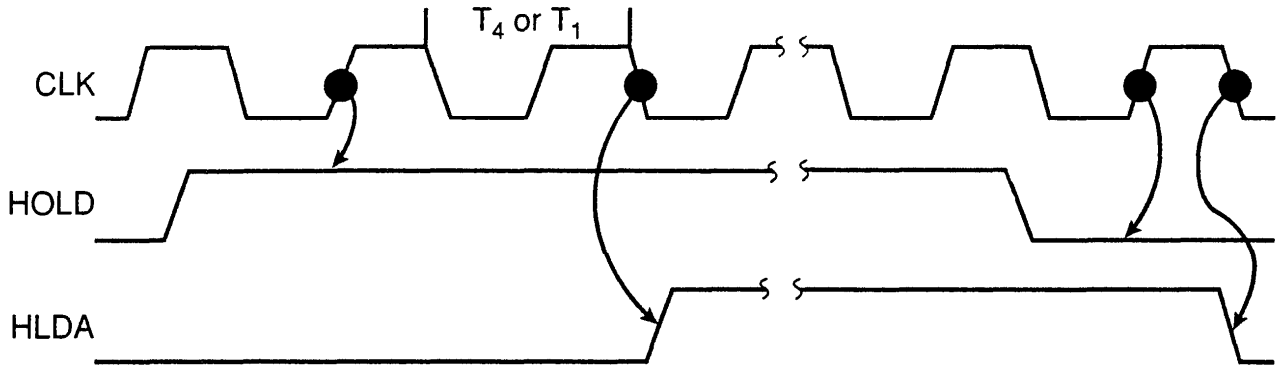
1) DMA controller asserts the request on the HOLD pin

2) 8086 completes its current bus cycle and enters into a HOLD state

3) 8086 grants the right of bus control by asserting a grant signal via the HOLDA pin. 8086 pins (Address, Data, C-trol $\Rightarrow$ 3-rd state)

4) DMA operation starts

5) Upon completion of the DMA operation, the DMA controller asserts low the request/grant pin again to relinquish bus control.



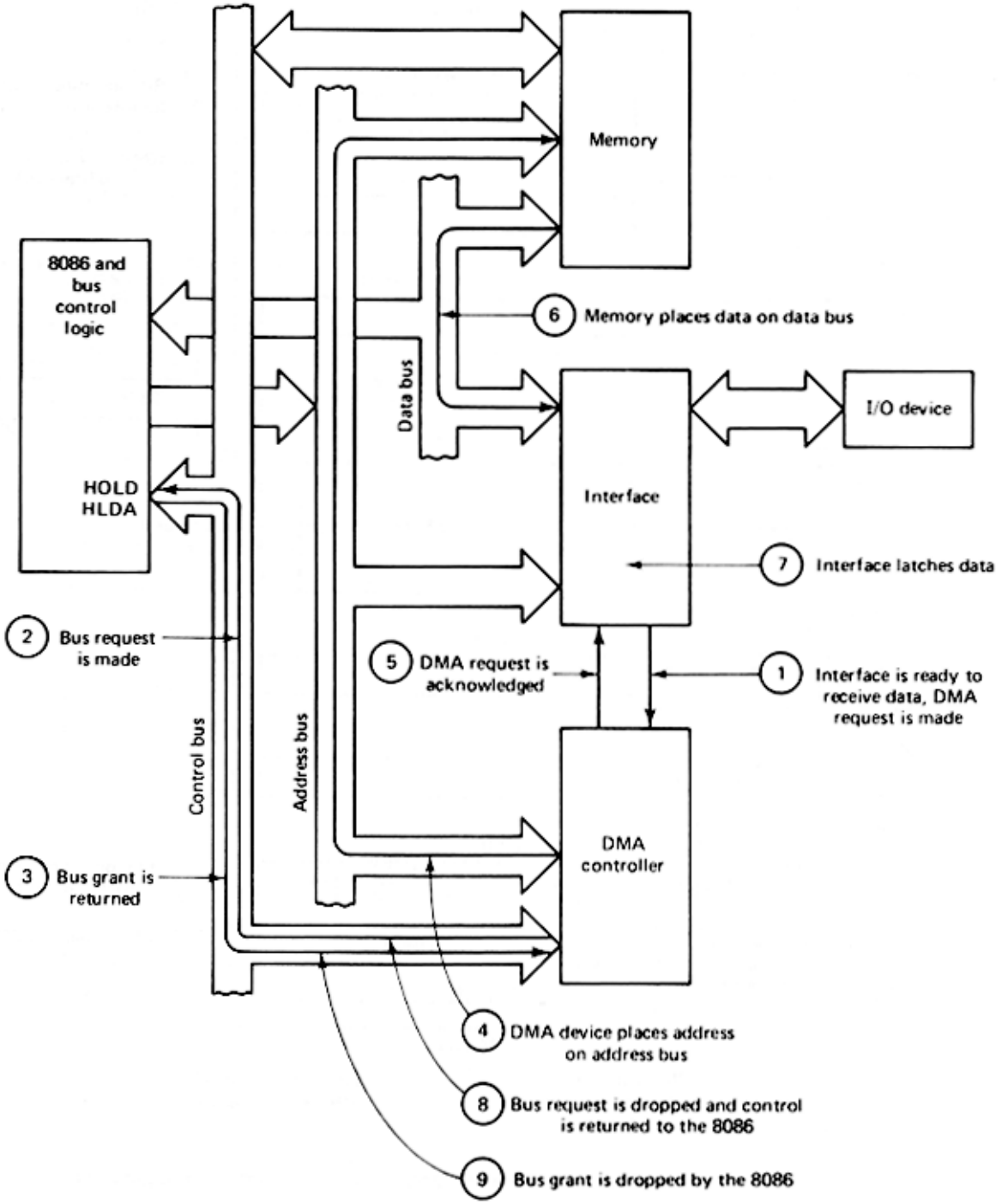
Basic process of DMA

For 8088/8086 in maximum mode:

The RQ/GT1 and RQ/GT0 pins are used to issue DMA request and receive acknowledge signals.

Sequence of events of a typical DMA process

1) DMA controller asserts one of the request pins, e.g. RQ/GT1 or RQ/GT0 (RQ/GT0 has higher priority)
2) 8086 completes its current bus cycle and enters into a HOLD state
3) 8086 grants the right of bus control by asserting a grant signal via the same pin as the request signal.
4) DMA operation starts
5) Upon completion of the DMA operation, the DMA controller asserts the request/grant pin again to relinquish bus control.


Memory
8086 and bus control logic
HOLD
HLDA
6 Memory places data on data bus
Data bus
I/O device
Interface
7 Interface latches data
2 Bus request is made
5 DMA request is acknowledged
1 Interface is ready to receive data, DMA request is made
Control bus
Address bus
DMA controller
3 Bus grant is returned
4 DMA device places address on address bus
8 Bus request is dropped and control is returned to the 8086
9 Bus grant is dropped by the 8086

General organization of the DMA controller

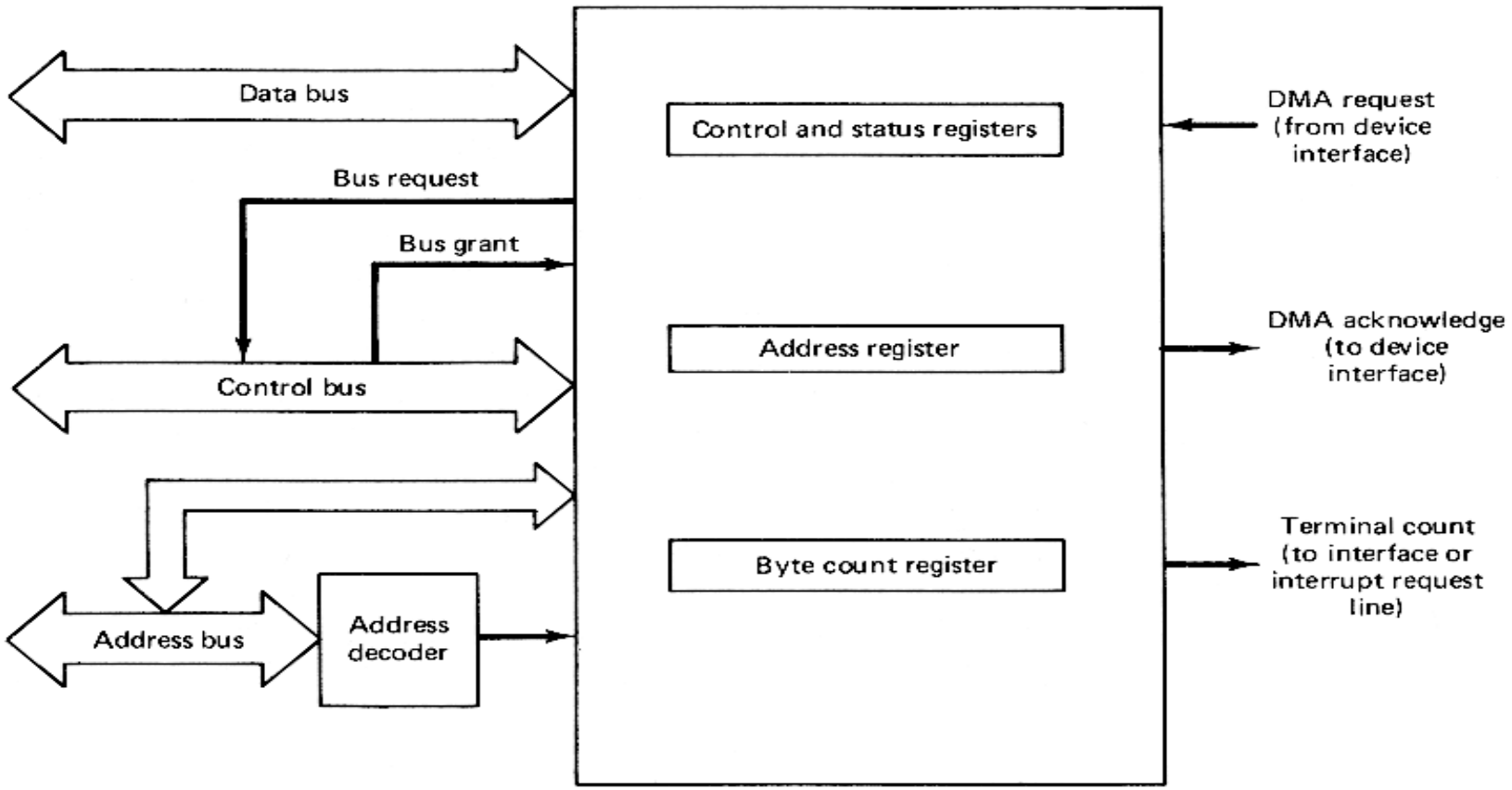
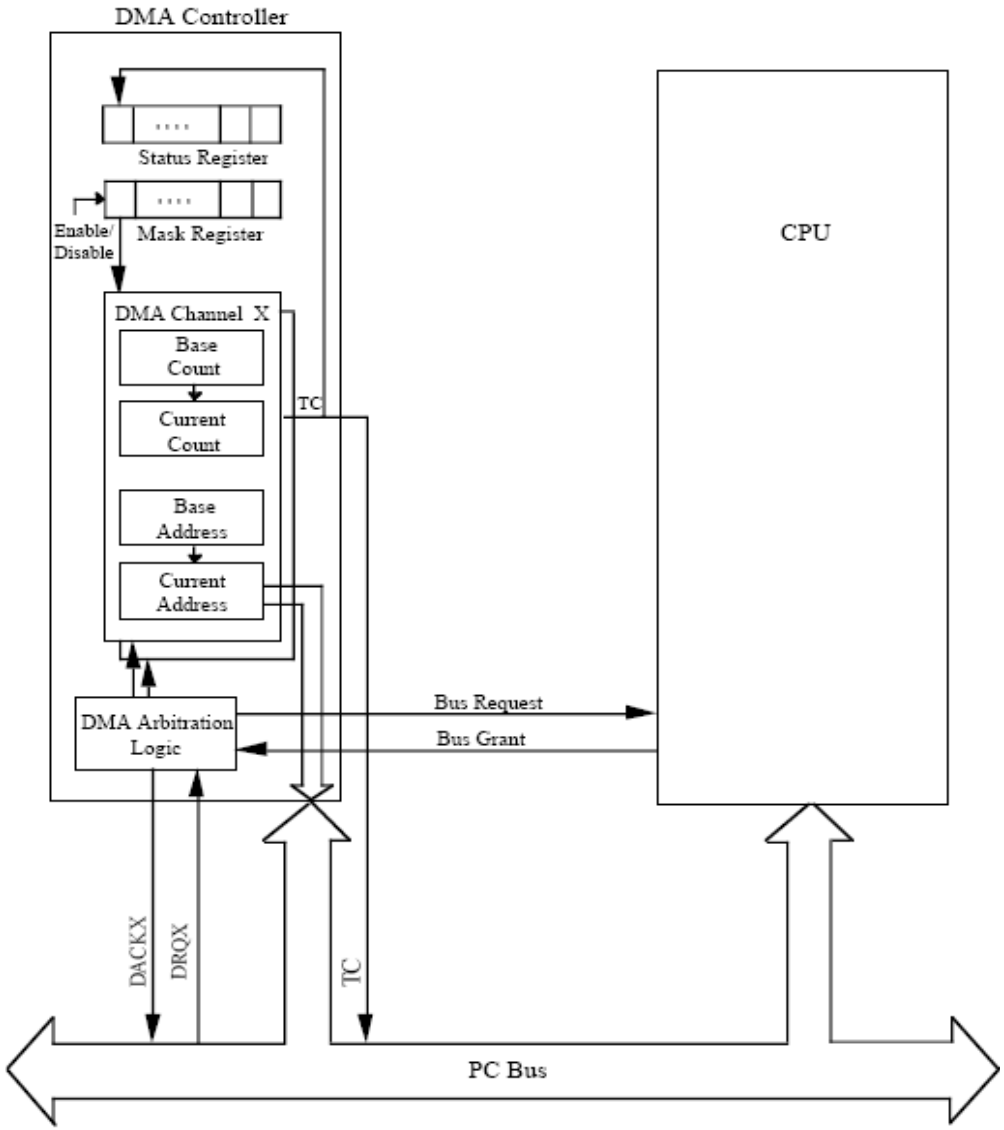
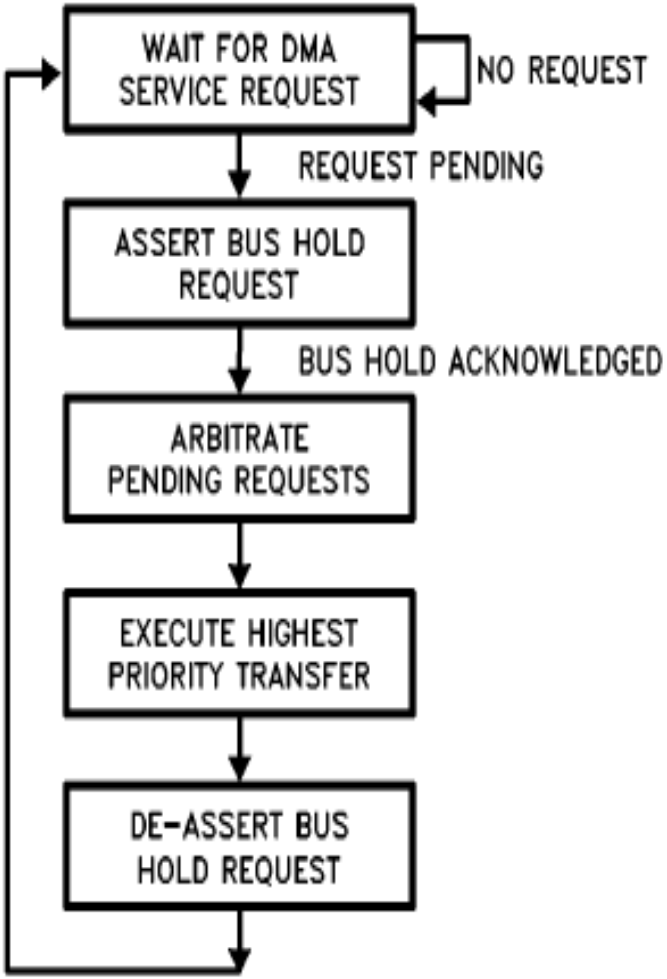


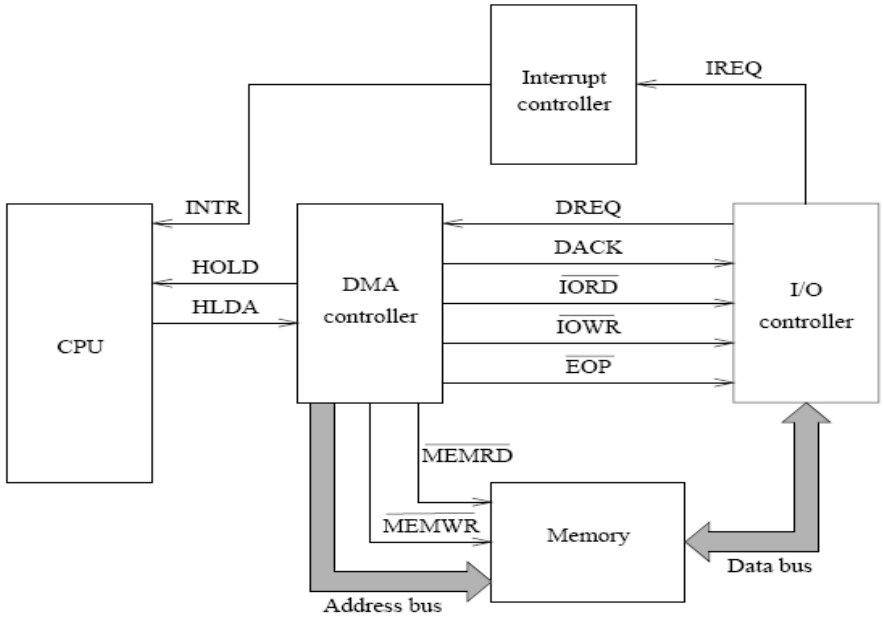
Figure 9-36 General organization of a DMA controller.

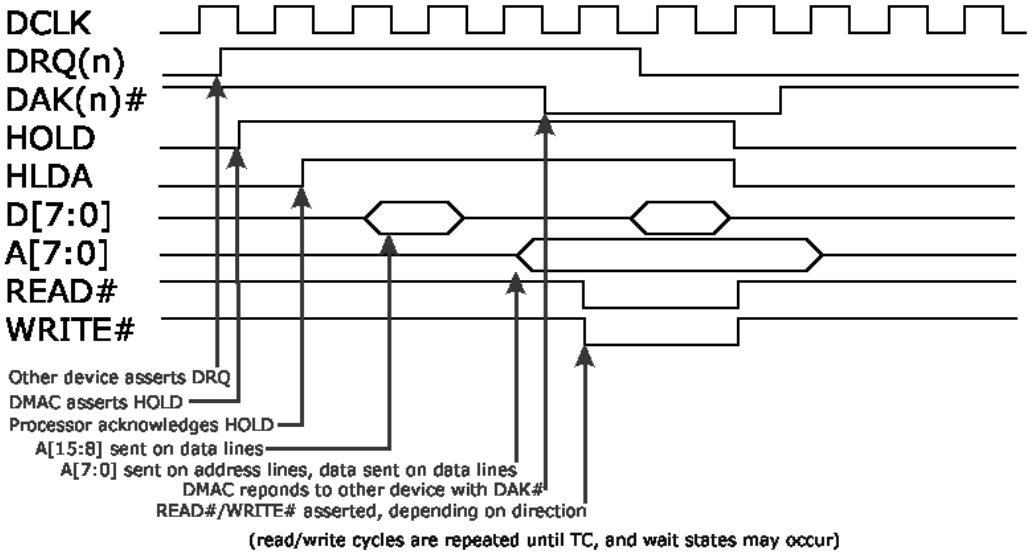
DMA transfer





DMA transfer - signals





DMA transfer types

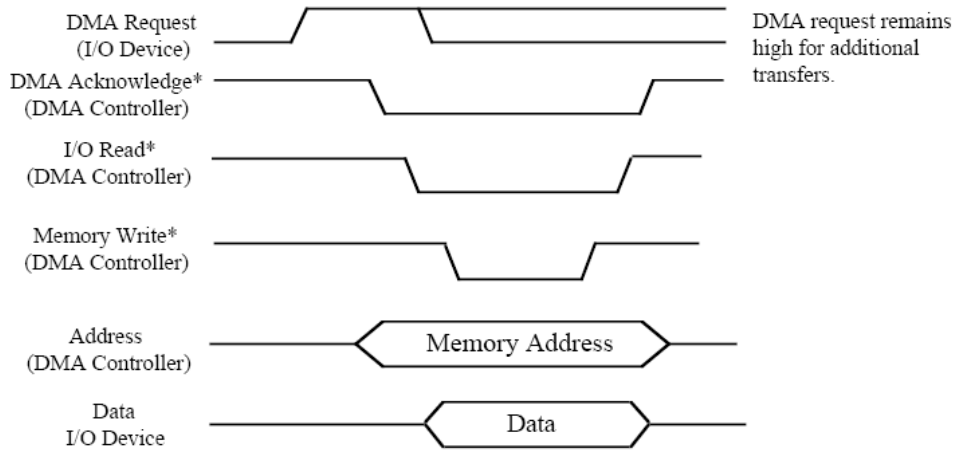
Fly-by DMA Transfer

-Data don't pass through the DMA controller

-1 bys-cycle / transfer

- Mem ↔ I/O

- Simultaneous control signals

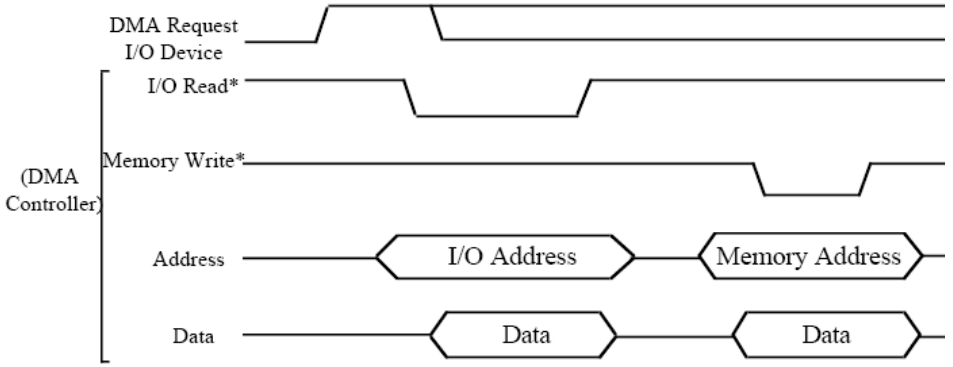


Flow-through DMA Transfer

- Data pass through controller

- Fetch-and-Deposit DMA Transfer: 2 cycles/transfer

- Mem ↔ Mem, I/O ↔ I/O, Mem ↔ I/O



DMA controller

A DMA controller interfaces with several peripherals that may request DMA.

The controller decides the priority of simultaneous DMA requests communicates with the peripheral and the CPU, and provides memory addresses for data transfer.

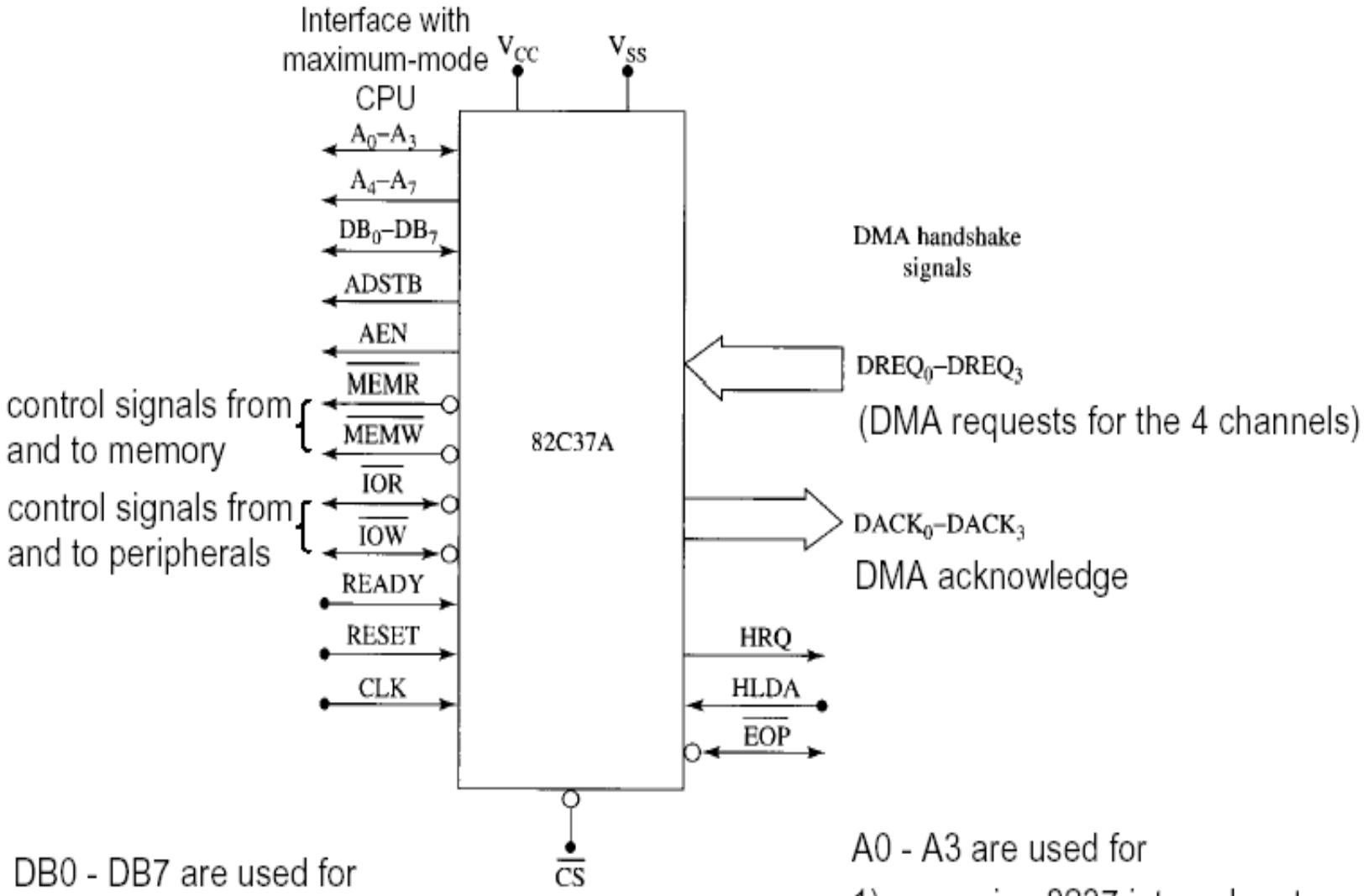
DMA controller commonly used with 8088/8086 is the

8237 programmable device.

The 8237 is in fact a special-purpose microprocessor.
Normally it appears as part of the system controller chip-sets.

The 8237 is a 4-channel device. Each channel is dedicated to a specific peripheral device and capable of addressing a 64 K bytes section of memory.

8237 DMA controller



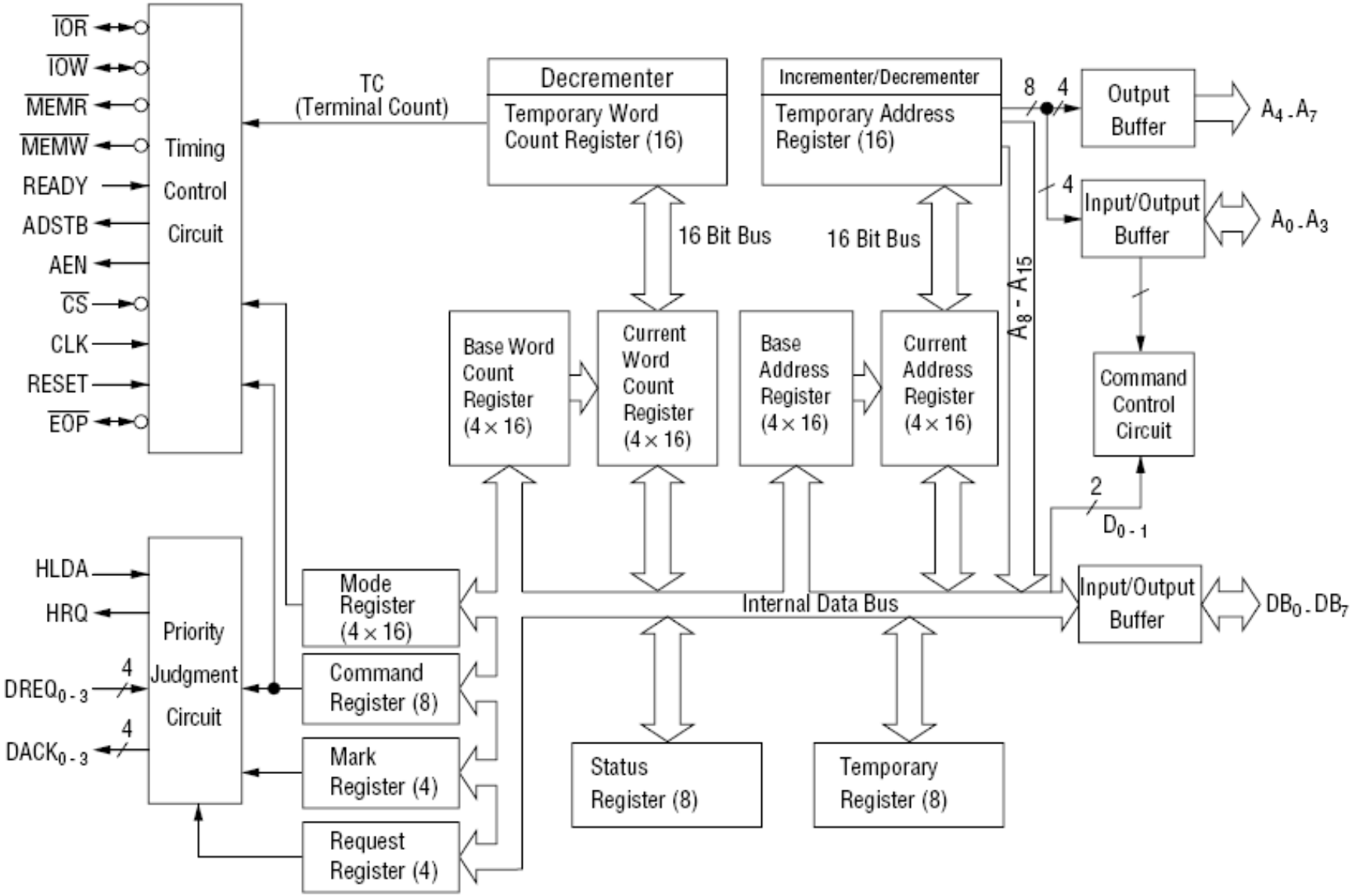
DB0 - DB7 are used for

1) transfer of data
2) 8237 programming

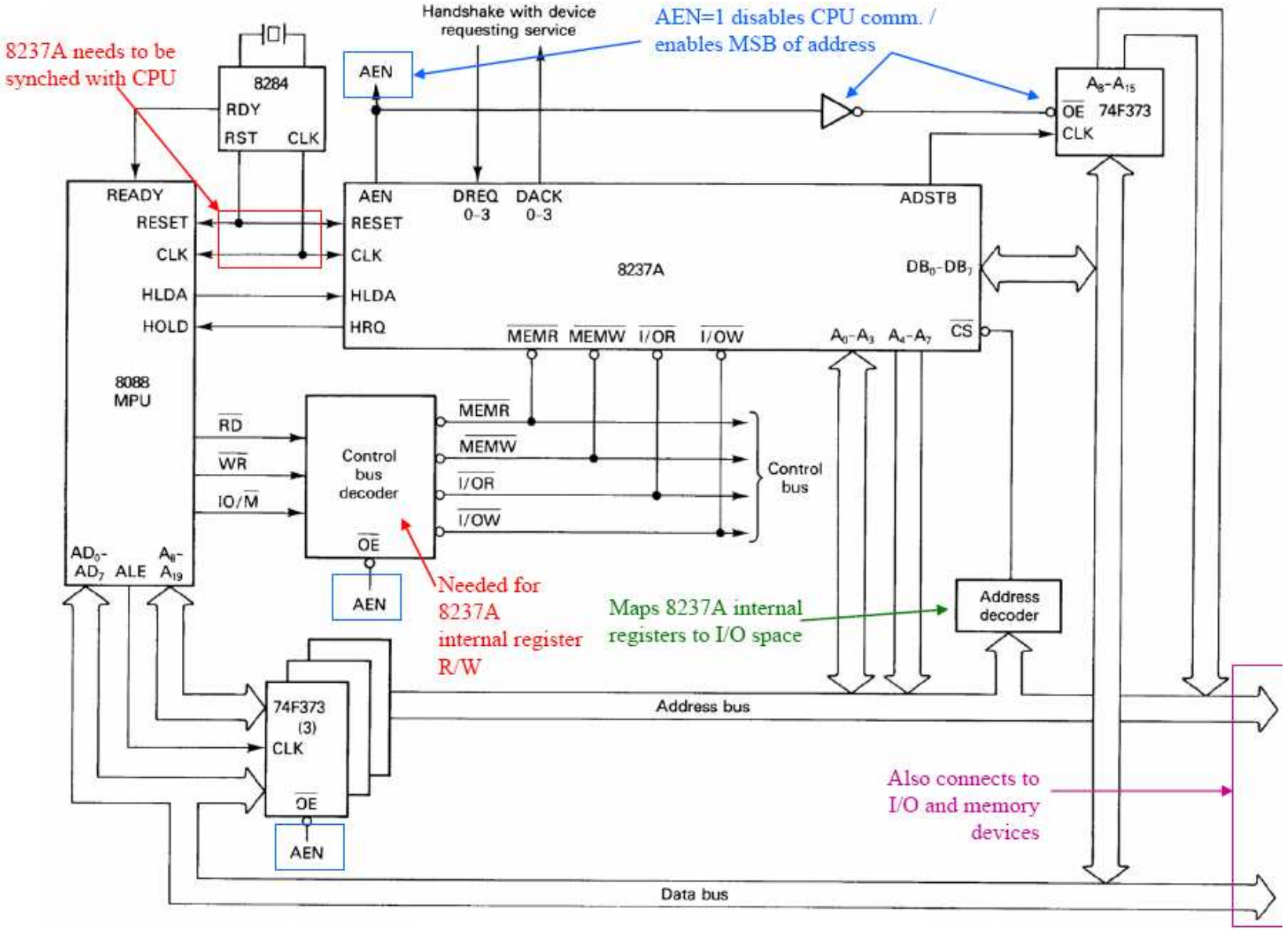
A0 - A3 are used for

1) accessing 8237 internal ports
2) carrying memory address in DMA read and write operations

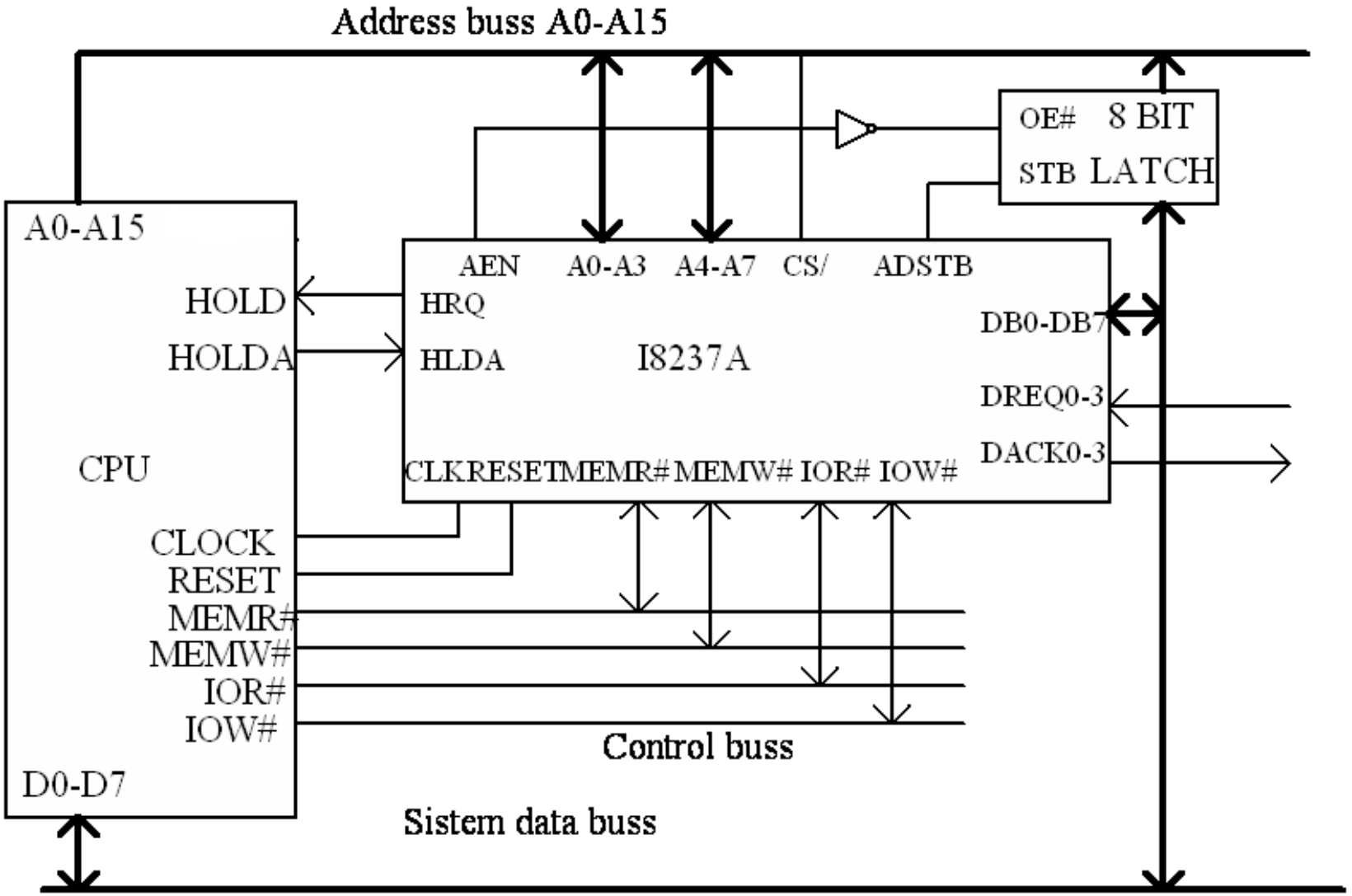
i8237A – Block diagram



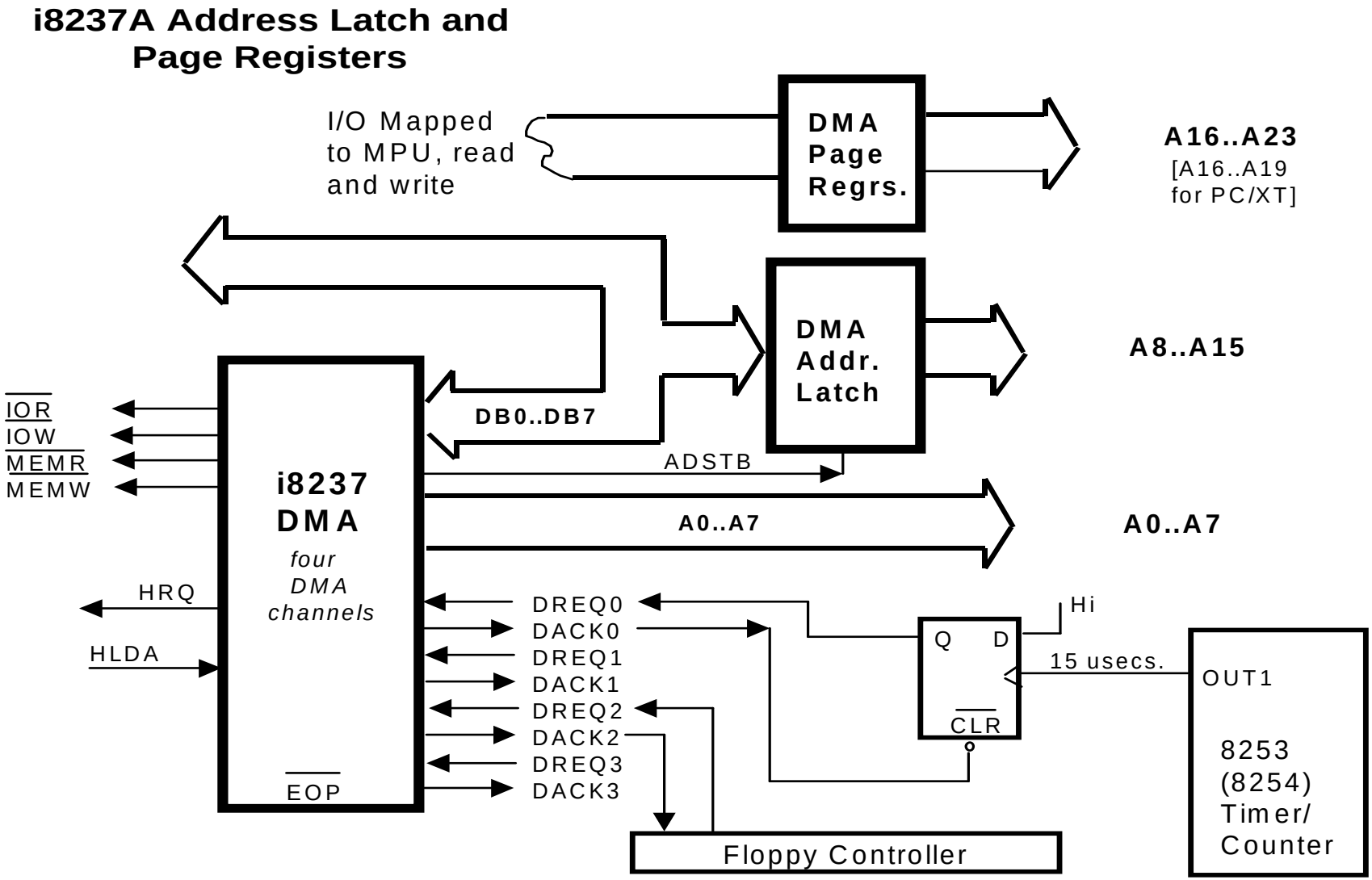
8088 + i8237A


8237A needs to be synched with CPU
Handshake with device requesting service
AEN=1 disables CPU comm. / enables MSB of address
8284
RDY
RST
CLK
AEN
A8-A15
OE 74F373
CLK
READY
RESET
CLK
HLDA
HOLD
8088 MPU
AEN
DREQ 0-3
DACK 0-3
RESET
CLK
HLDA
HRQ
8237A
ADSTB
DB0-DB7
MEMR MEMW I/OR I/OW
A0-A3
A4-A7
CS
RD
WR
IO/M
Control bus decoder
OE
MEMR
MEMW
I/OR
I/OW
Control bus
AD0-AD7
ALE
A8-A19
AEN
Needed for 8237A internal register R/W
Maps 8237A internal registers to I/O space
Address decoder
74F373 (3)
CLK
OE
AEN
Address bus
Also connects to I/O and memory devices
Data bus

Generating 16 bit addresses



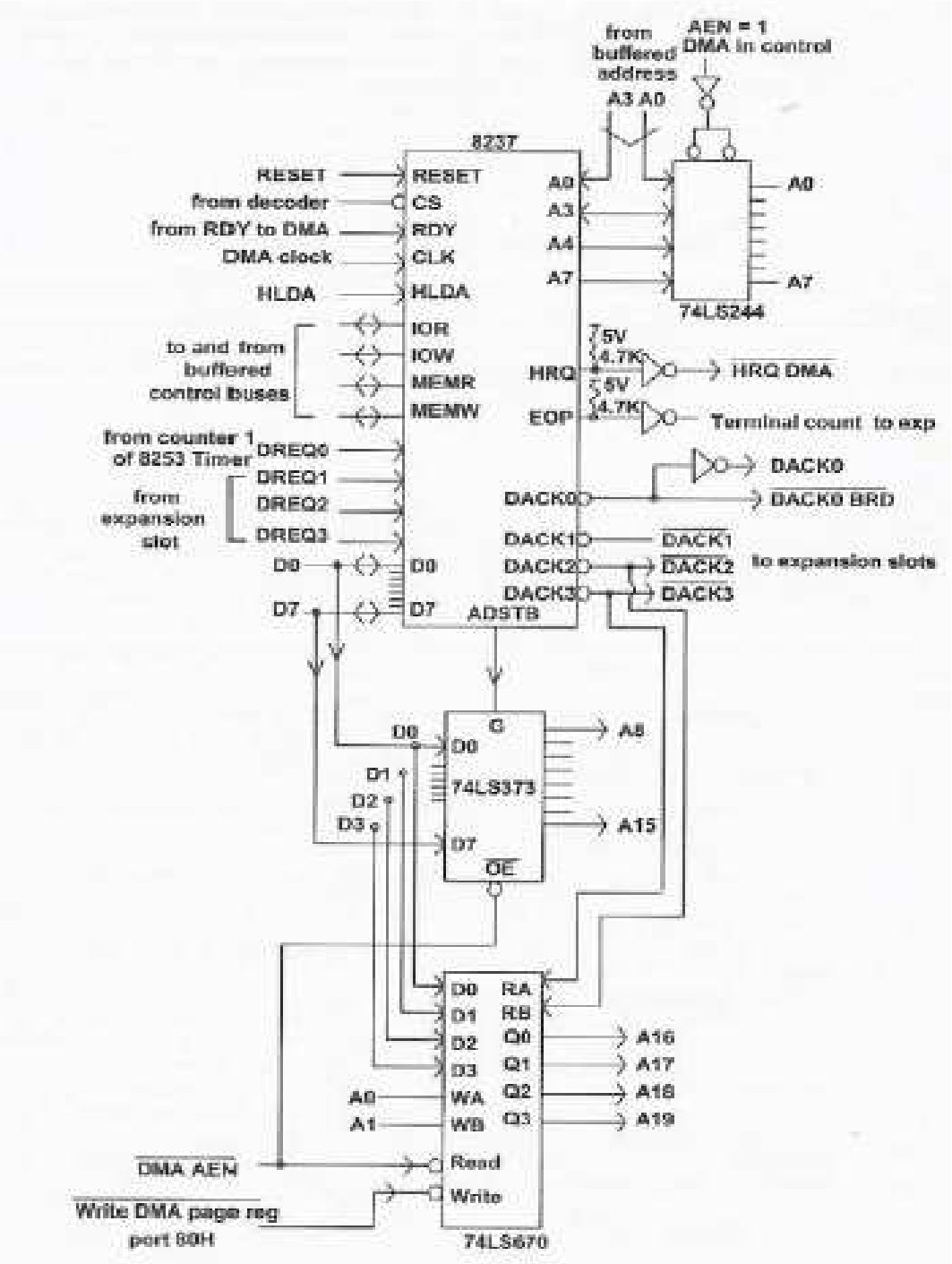
Generating addresses > 16 bits



DMA for PC/XT:

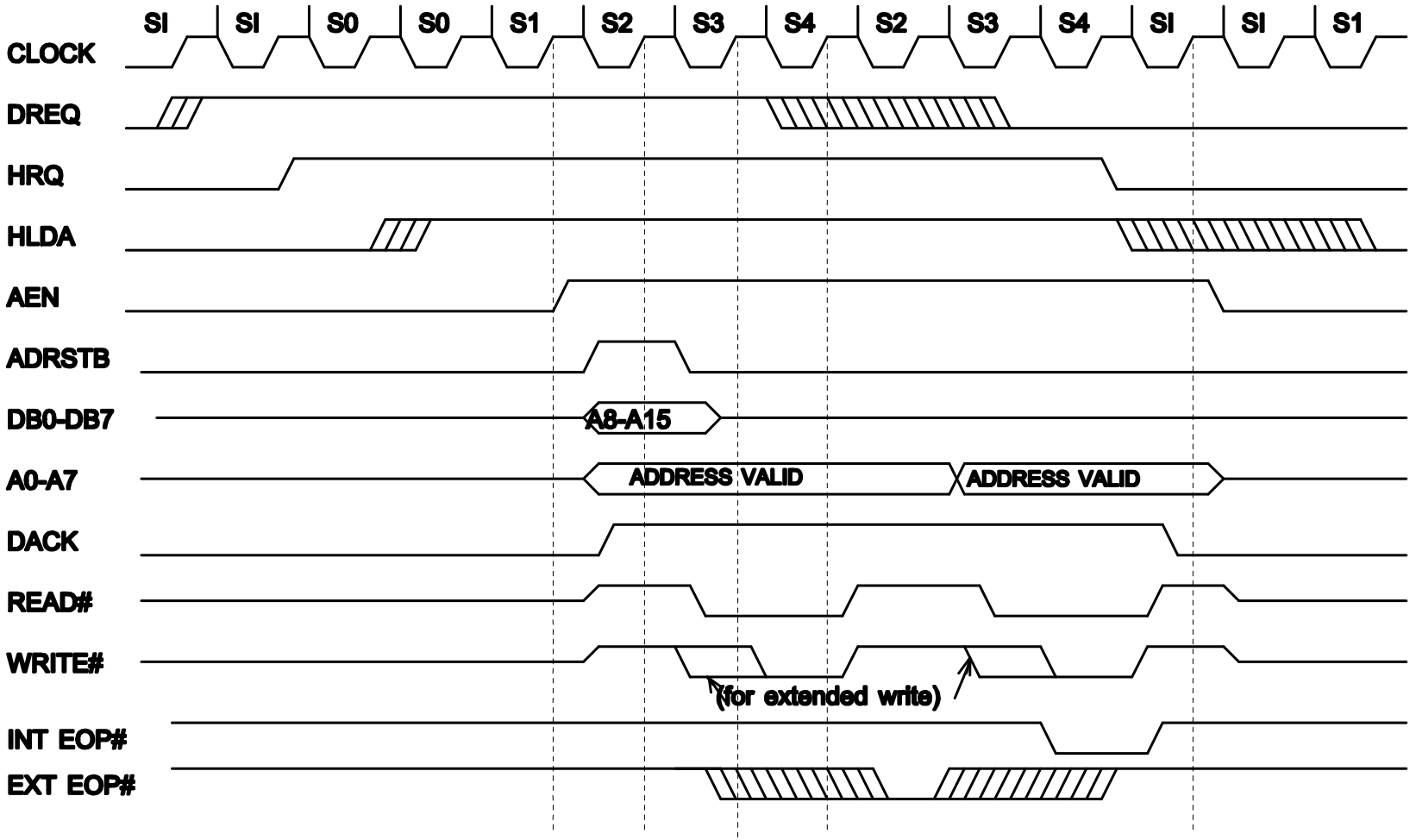
Address latch – 74LS373 (A8-15)

Page register – 74LS670 (A16-19)

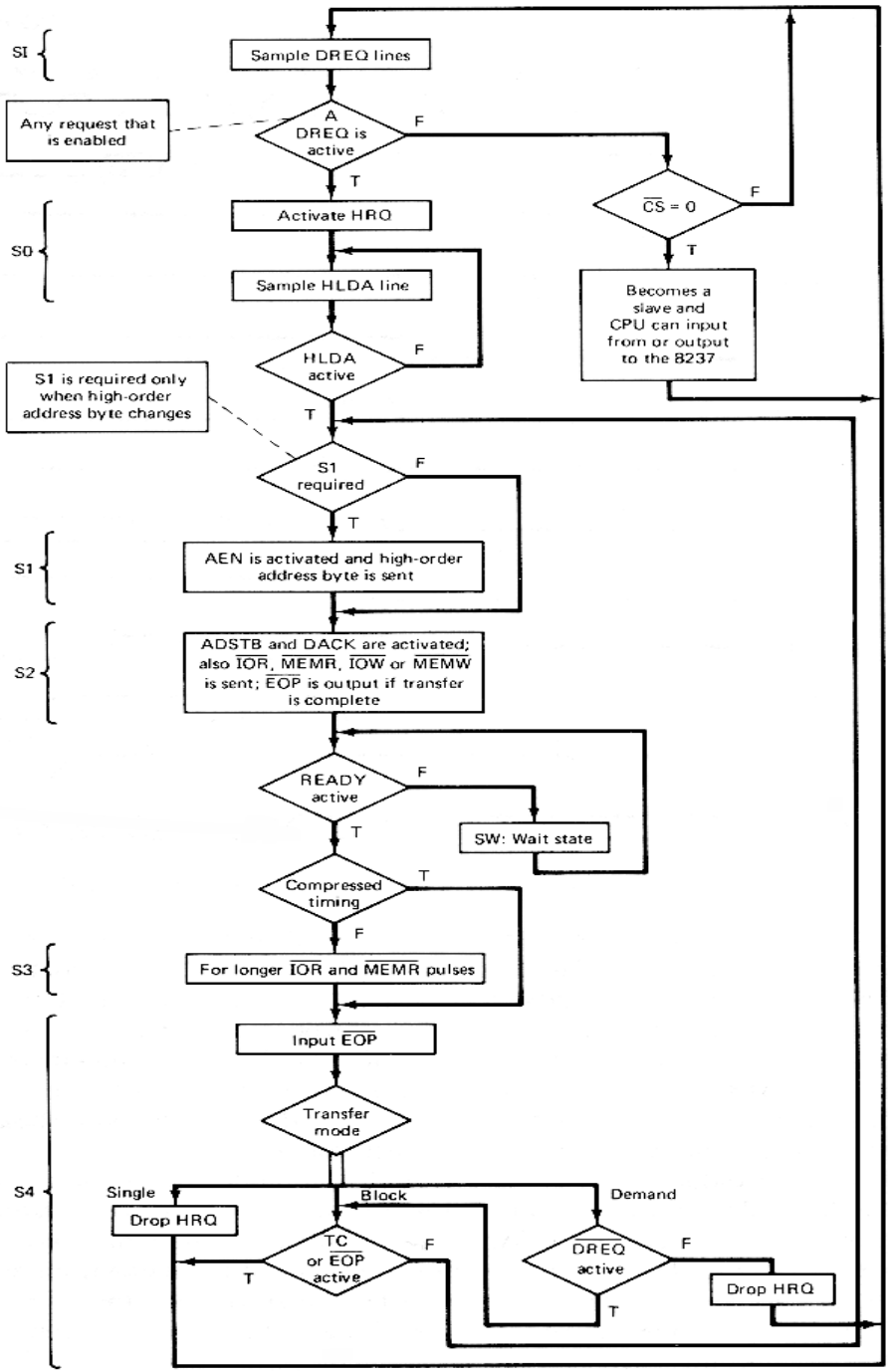


DMA transfer cycle

(memory to I/O or IO to memory)



Compressed timing : S2 (change address) + S4 (read/write)


SI
Sample DREQ lines
Any request that is enabled
A DREQ is active
F
T
$\overline{CS}$ = 0
F
T
Becomes a slave and CPU can input from or output to the 8237
S0
Activate HRQ
Sample HLDA line
HLDA active
F
T
S1 is required only when high-order address byte changes
S1 required
F
T
S1
AEN is activated and high-order address byte is sent
S2
ADSTB and DACK are activated; also $\overline{IOR}$, $\overline{MEMR}$, $\overline{IOW}$ or $\overline{MEMW}$ is sent; $\overline{EOP}$ is output if transfer is complete
READY active
F
T
SW: Wait state
Compressed timing
T
F
S3
For longer $\overline{IOR}$ and $\overline{MEMR}$ pulses
S4
Input $\overline{EOP}$
Transfer mode
Single
Block
Demand
Drop HRQ
TC or $\overline{EOP}$ active
F
T
DREQ active
F
T
Drop HRQ

Functioning modes

Idle (slave)

– programmed (#CS=0, HOLDA=0)

- DREQ sampled on the falling edge of the Clk

- If DREQ on an un-masked channel or software request (mem-to-mem transfer) ⇒ Active

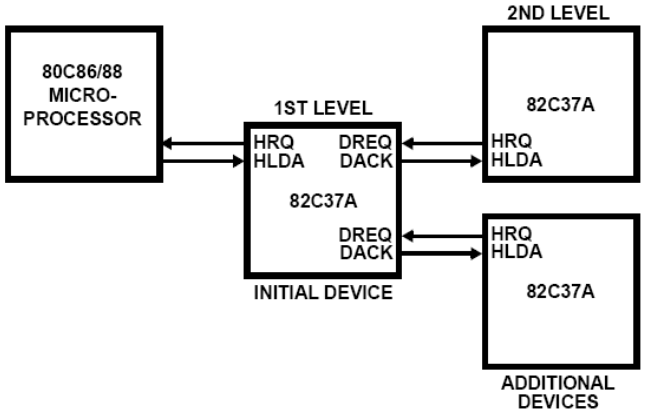
Active (master) – DMA transfer:

Single transfer Mode - release HOLD after each byte transferred. If DREQ is held active HOLD is issued again.

Bloc transfer Mode – transfers a block of size specified in the count register (DREQ need not to be held active).

Demand Transfer Mode – transfers data until external #EOP is received or until DREQ becomes inactive

Cascade Mode -



Transfer Types

Write transfers move data from an I/O device to the memory by activating MEMW and IOR.

Read transfers move data from memory to an I/O device by activating MEMR and IOW.

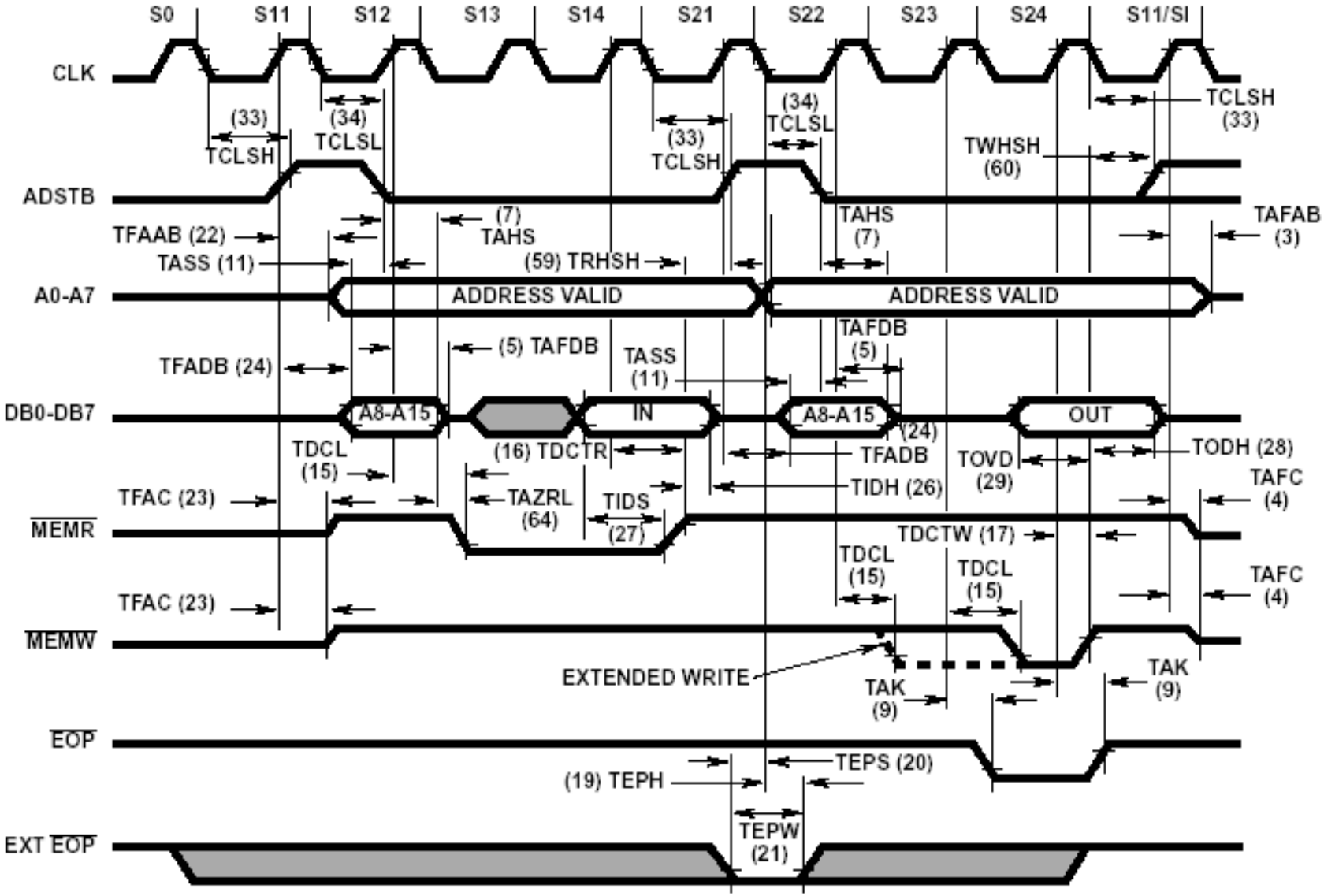
Verify transfers are pseudo-transfers. The 82C37A operates as in Read or Write transfers generating addresses and responding to EOP, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation.

Memory-to-memory

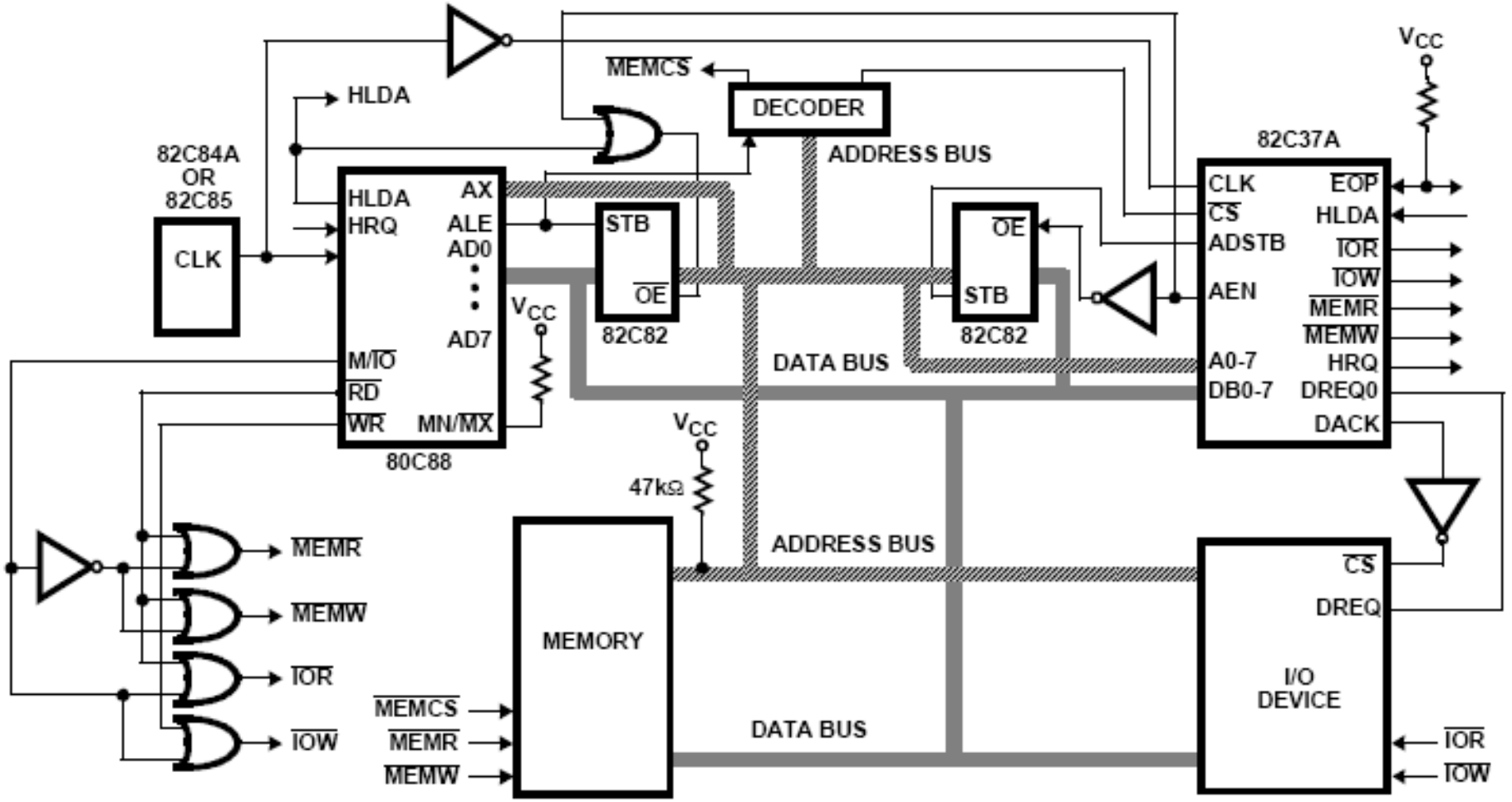
- Channel 0 – source address & counter
- Channel 1 – destination address & counter
- The data byte read from the memory is stored in the 82C37A internal Temporary register
- The transfer is initiated by setting the software or hardware DREQ for channel 0. The 82C37A requests a DMA service in the normal manner.

Autoinitialize – a channel may be set up as an Autoinitialize channel. During

Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of the channel following EOP. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.



Memory-to-memory



NOTE: The address lines need pull-up resistors.

FIGURE 6. APPLICATION FOR DMA SYSTEM

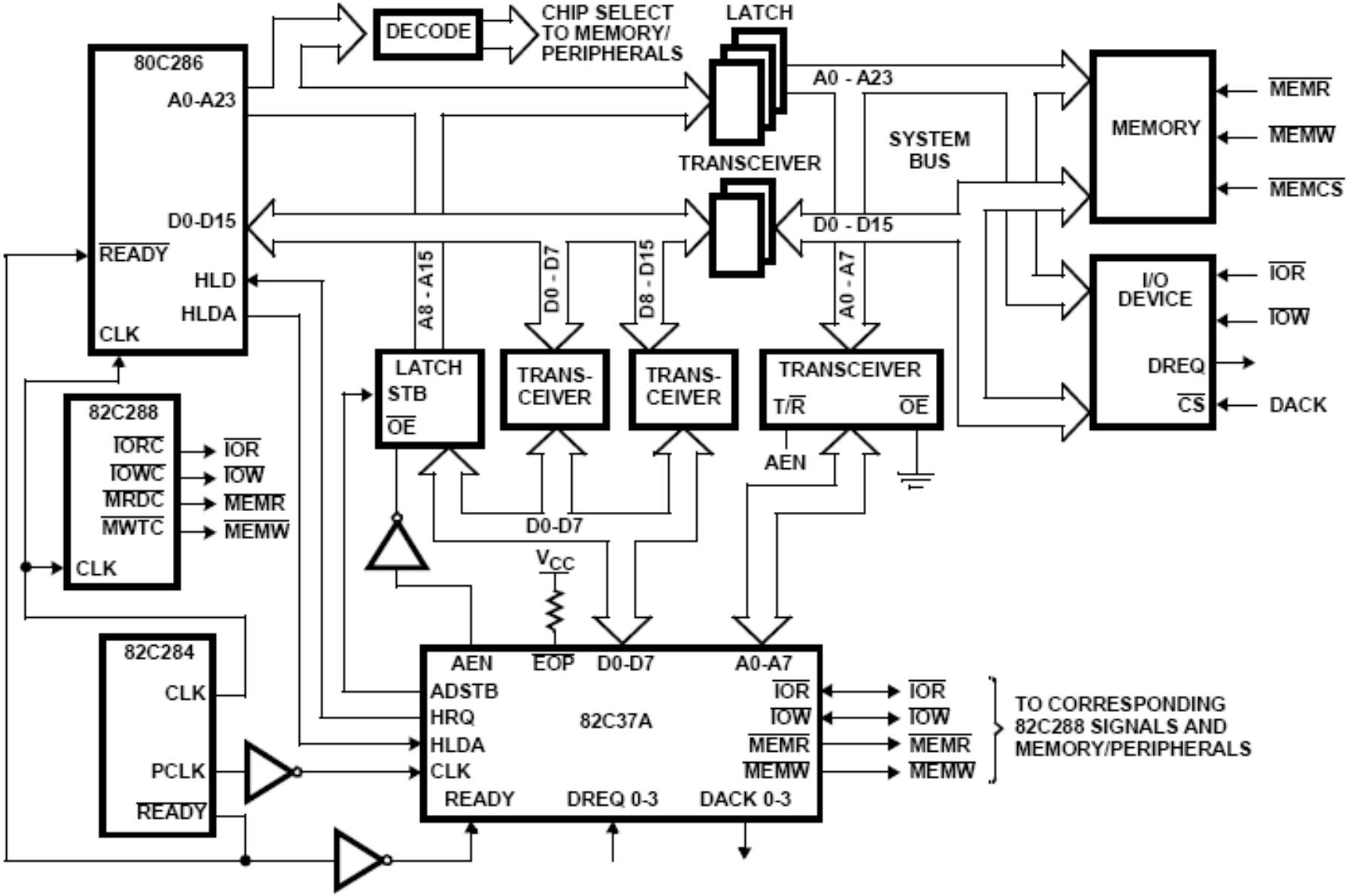
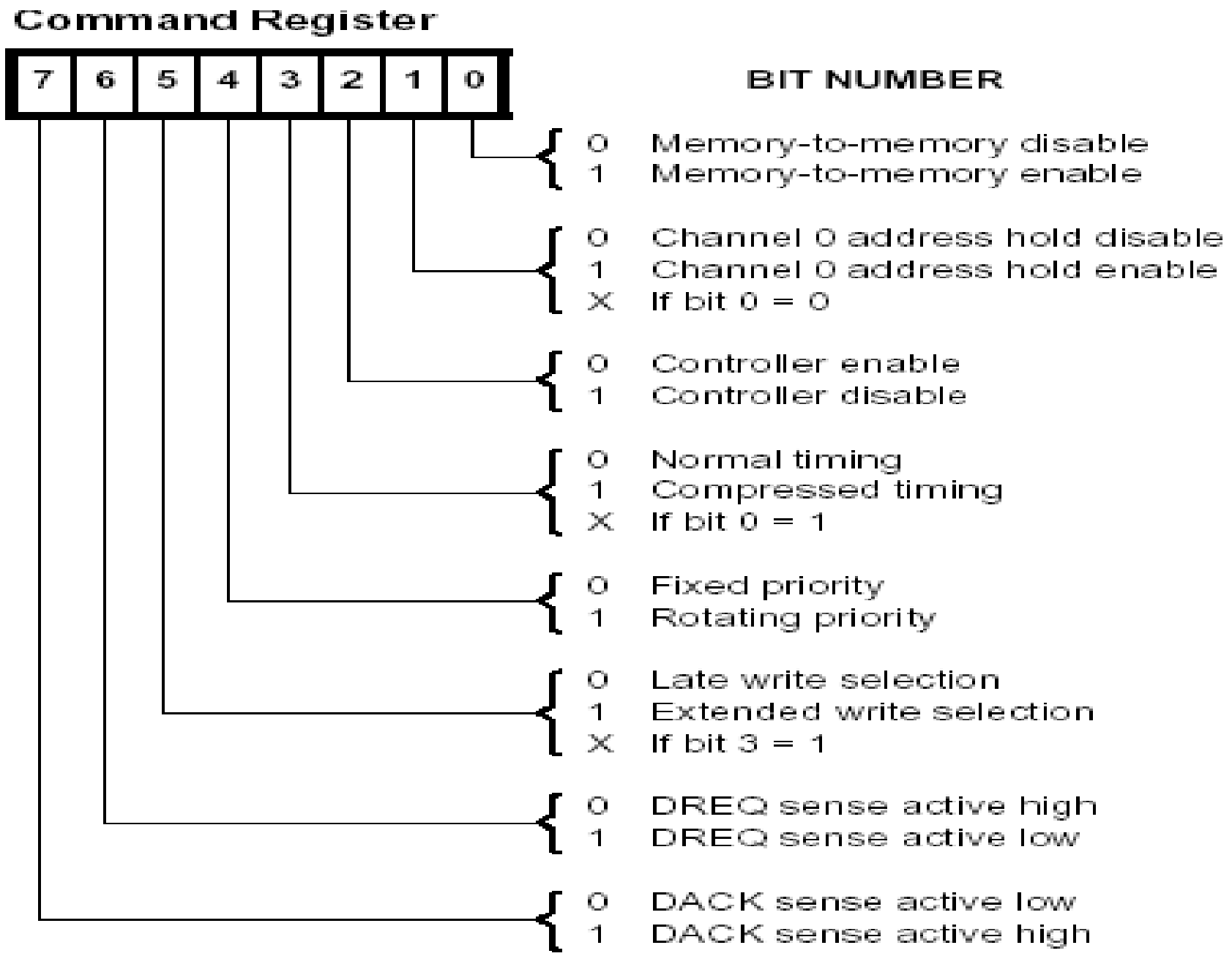
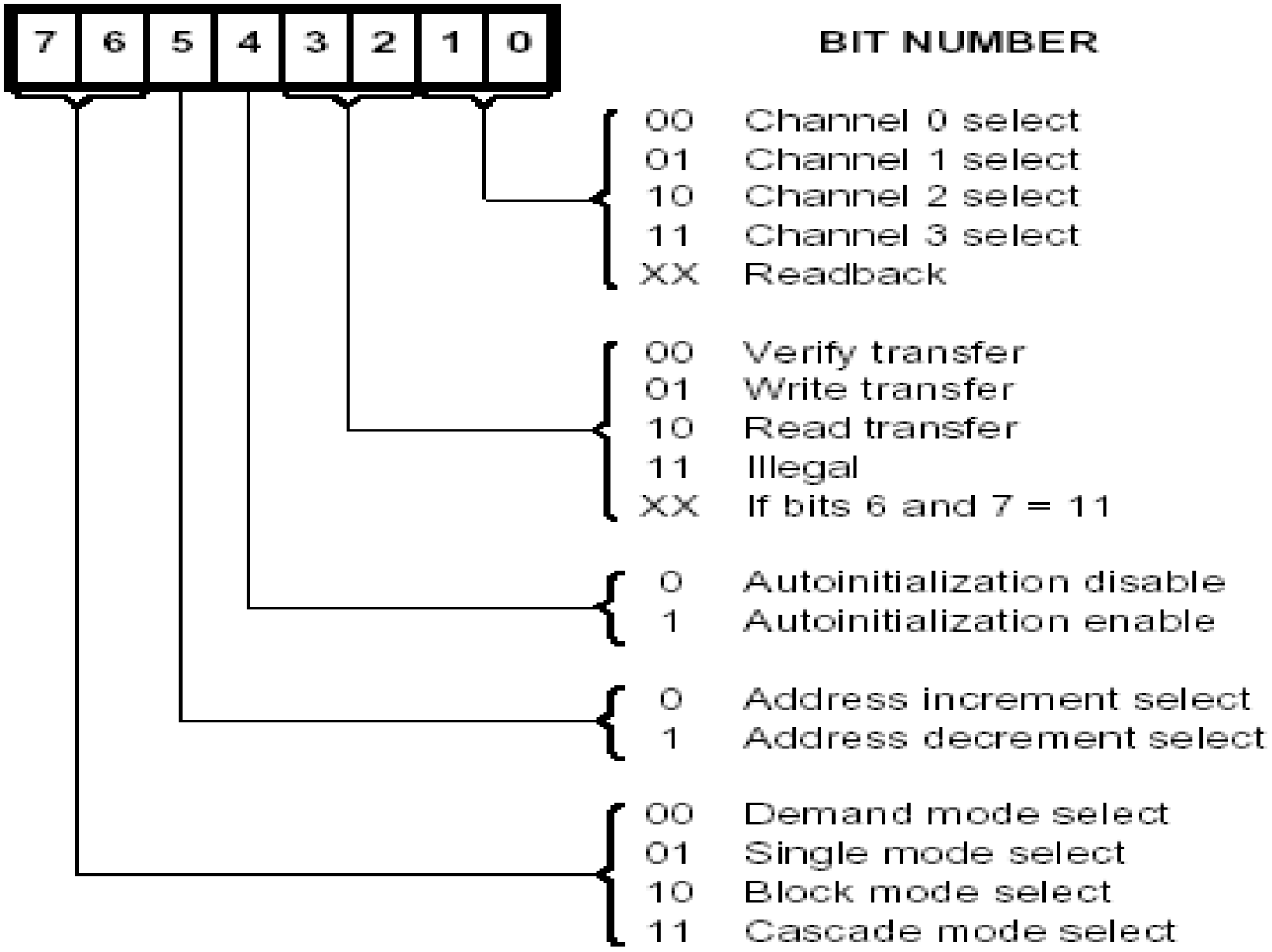


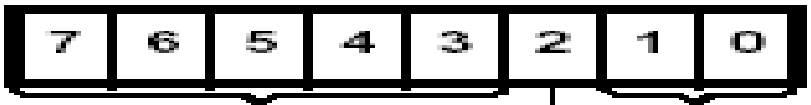
FIGURE 7. 80C286 DMA APPLICATION


Command Register
7
6
5
4
3
2
1
0
BIT NUMBER
0 Memory-to-memory disable
1 Memory-to-memory enable
0 Channel 0 address hold disable
1 Channel 0 address hold enable
X If bit 0 = 0
0 Controller enable
1 Controller disable
0 Normal timing
1 Compressed timing
X If bit 0 = 1
0 Fixed priority
1 Rotating priority
0 Late write selection
1 Extended write selection
X If bit 3 = 1
0 DREQ sense active high
1 DREQ sense active low
0 DACK sense active low
1 DACK sense active high

Mode Register



Request Register



Don't Care, Write Bits 4-7 All Ones. Read

BIT NUMBER

00	Select Channel 0
01	Select Channel 1
10	Select Channel 2
11	Select Channel 3

0	Reset request bit
1	Set request bit

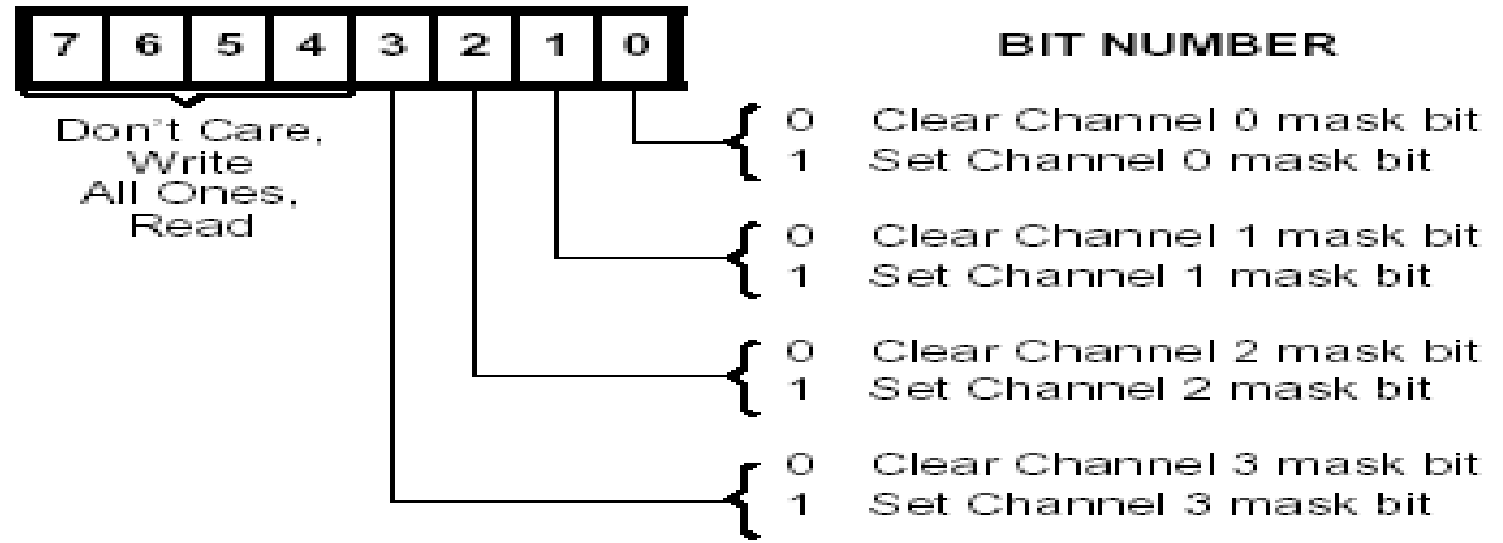
Mask Register

Don't Care

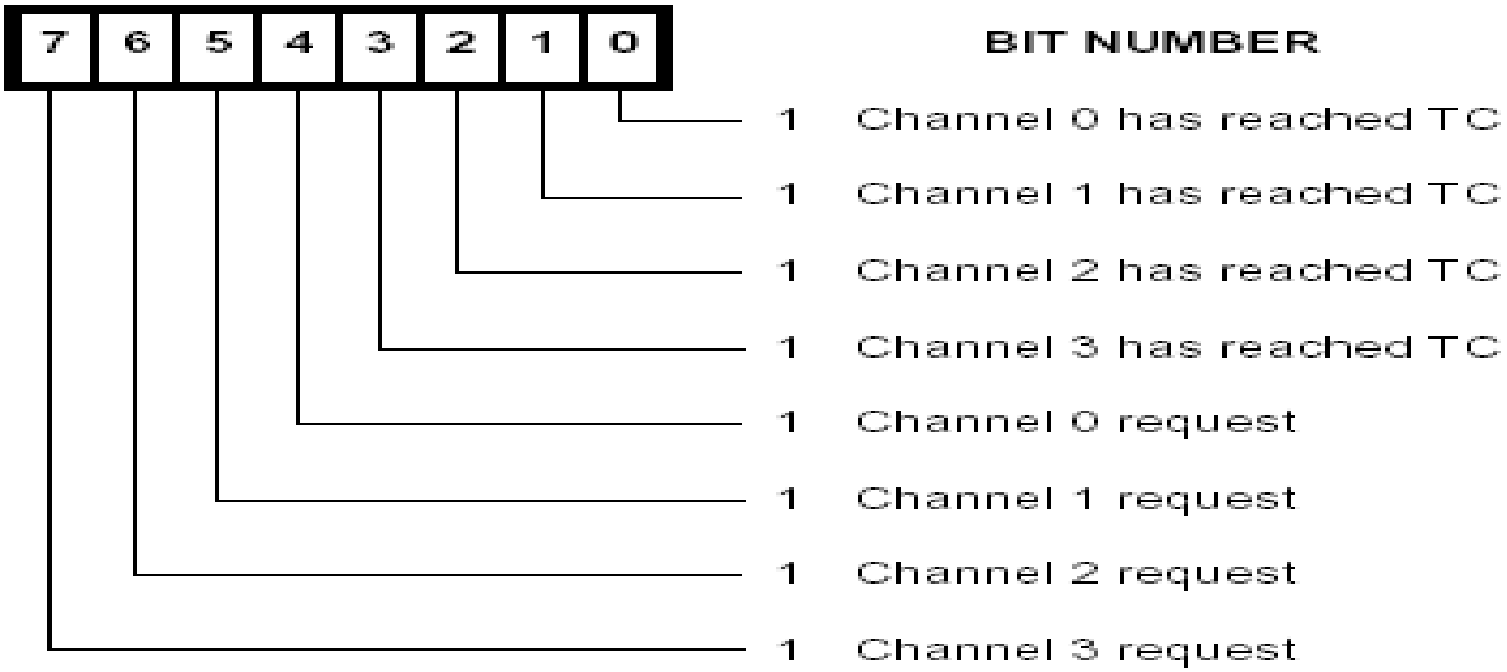
BIT NUMBER

00	Select Channel 0 mask bit
01	Select Channel 1 mask bit
10	Select Channel 2 mask bit
11	Select Channel 3 mask bit

0	Clear mask bit
1	Set mask bit



Status Register



OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set First/Last F/F	1	1	0	0	0	1
Clear First/Last F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

CHANNEL	REGISTER	OPERATION	SIGNALS							FIRST/LAST FLIP-FLOP STATE	DATA BUS DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15