CHAPTER 13
Direct Memory Access and DMA-Controlled I/O

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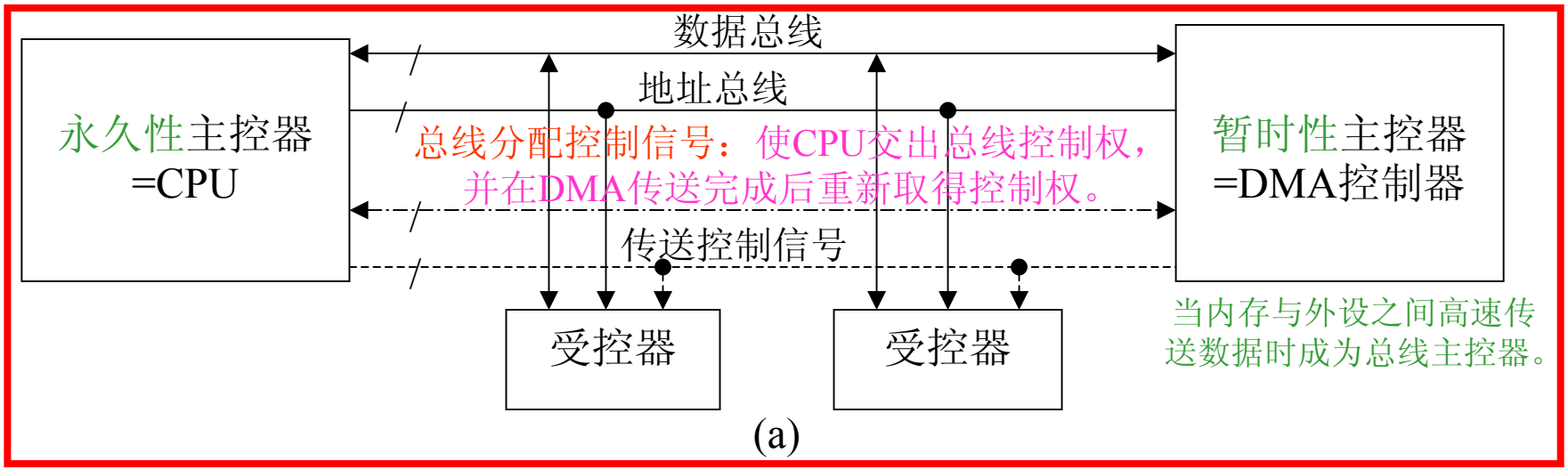
§ 13-1 BASIC DMA OPERATION

What is DMA?

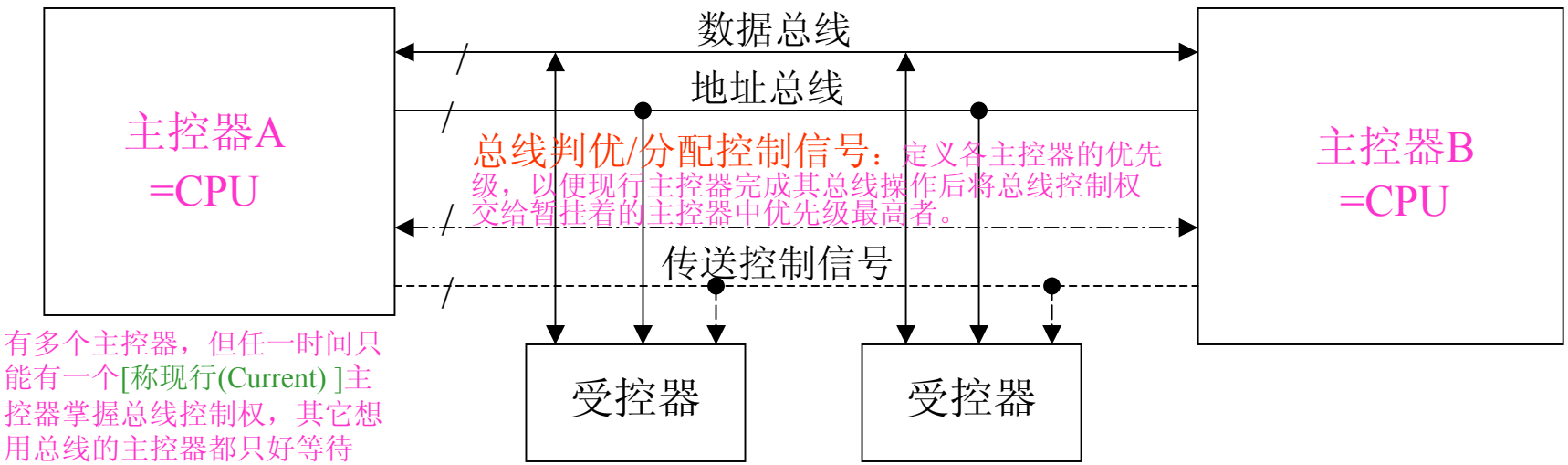
- An ***alternative*** to the *basic* and *interrupt-driven* I/O discussed previously
- DMA can transfer ***large blocks of data*** from memory to device *or* from device to memory
  - Uses same Address/Data lines on system bus
  - Controls the system bus *instead of* the processor ("bus master")
  - Does *not require the processor* for data transfer
- Common DMA operations:
  - DRAM refresh
  - Video refresh
  - Disk-memory system reads and writes.

回忆：复用信息类型的选择

有不止一个主控器

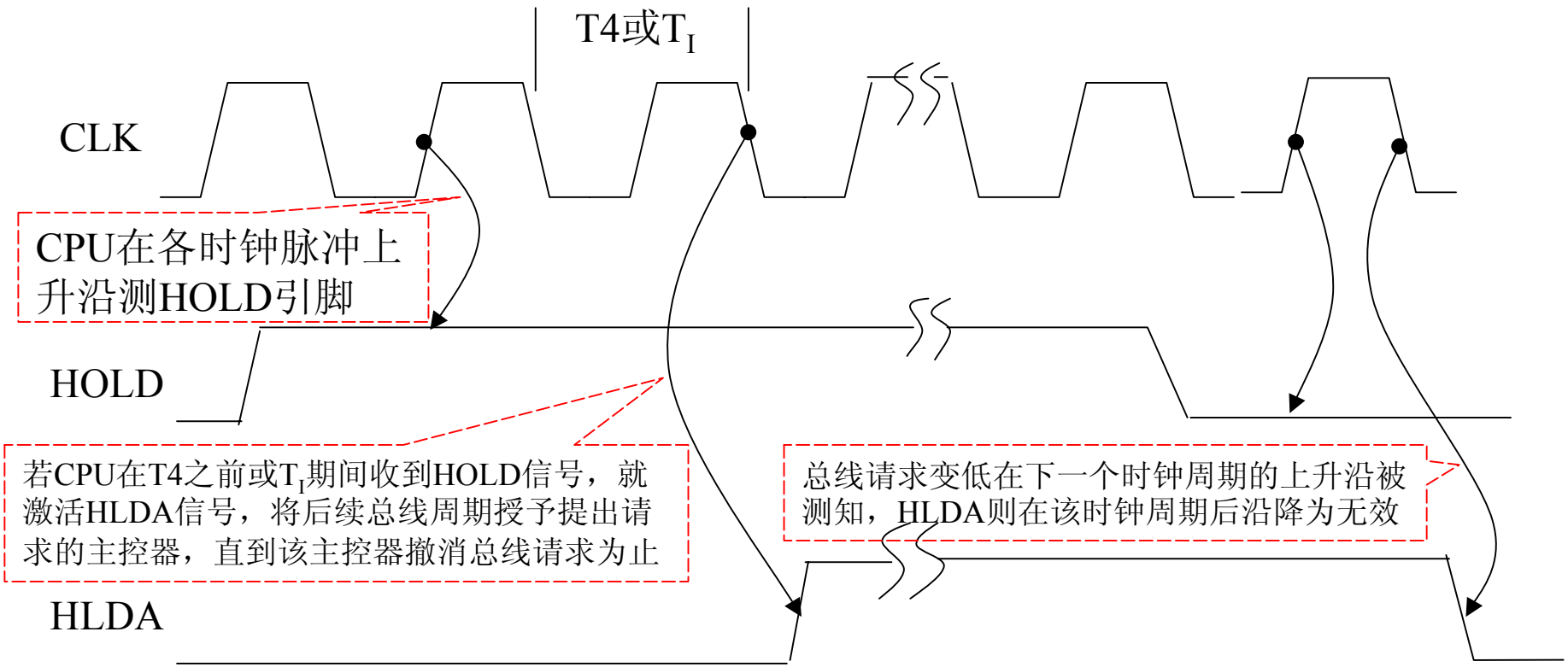


(a)



(b)多微处理器系统

回忆：最小模式 总线请求和总线授予



- 当HLDA为1时：
  - CPU的所有三态输出都进入高阻态。
  - 已在指令队列中的指令将继续执行，直到有指令需用总线时为止。例如：指令 MOV AX,BX 能执行完；MOV AX,NUMBER 只能执行到必须从NUMBER单元中取数时为止。

Request/Ack a DMA Transfer

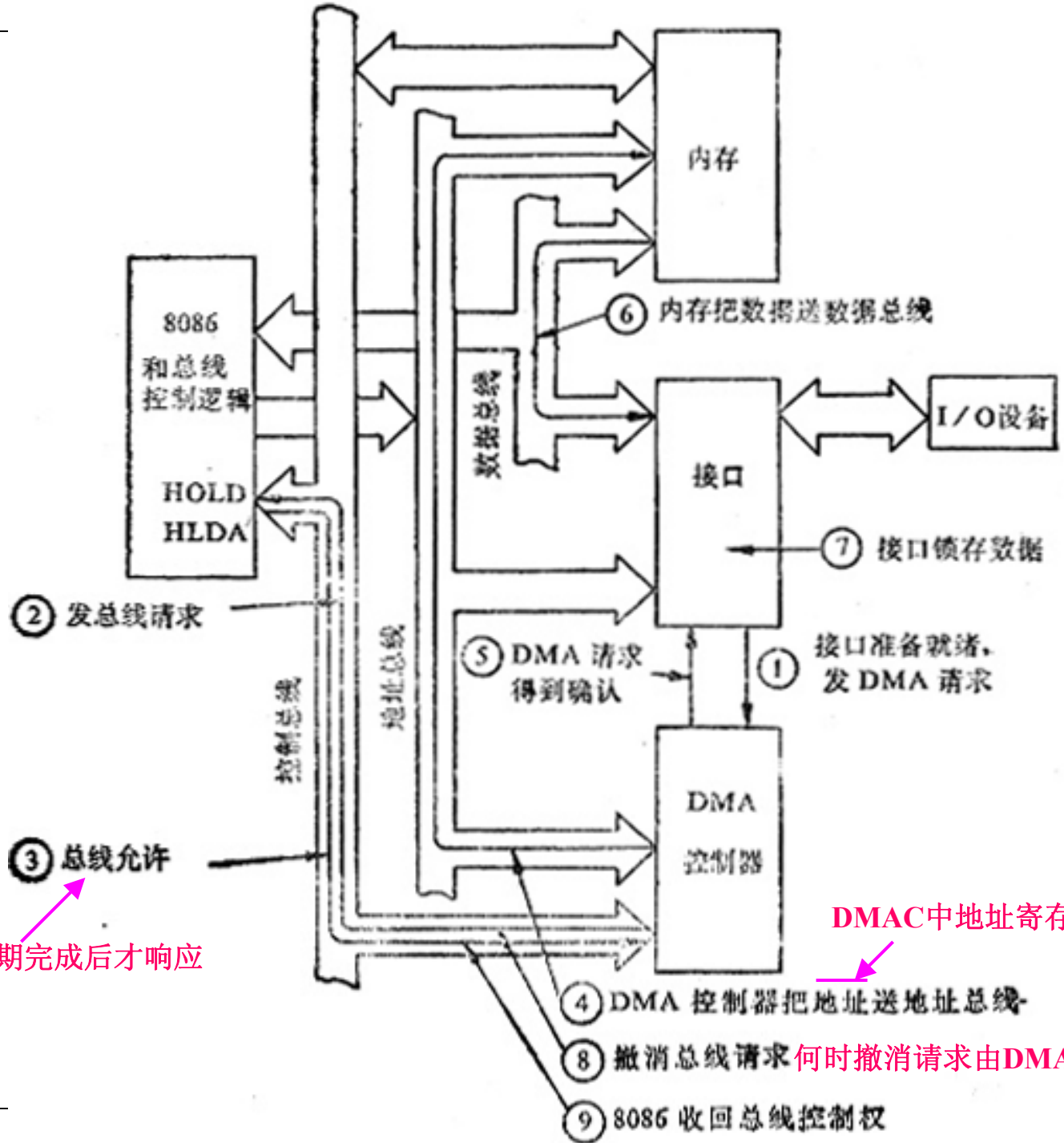
- Two **signals** are used to request/ack a DMA transfer:
  - **HOLD** is *an input to the microprocessor* that requests a DMA action
  - **HLDA** is *an output from the microprocessor* granting the DMA action
- The **microprocessor** responds
  - by suspending the execution of the program *and*
  - by placing its address, data and control bus in high-impedance states

Data Transfer

- ***DMA "reads"*** refer to transfers from memory to an I/O device and involves the use of *MRDC and *IOWC.
- ***DMA "writes"*** refer to transfers from an I/O device to memory and involves the use of *MWTC and *IORC.

- The data transfer rate is determined by the speed of memory or the DMA controller (usually the latter = § 13-2).

DMA输出单个数据

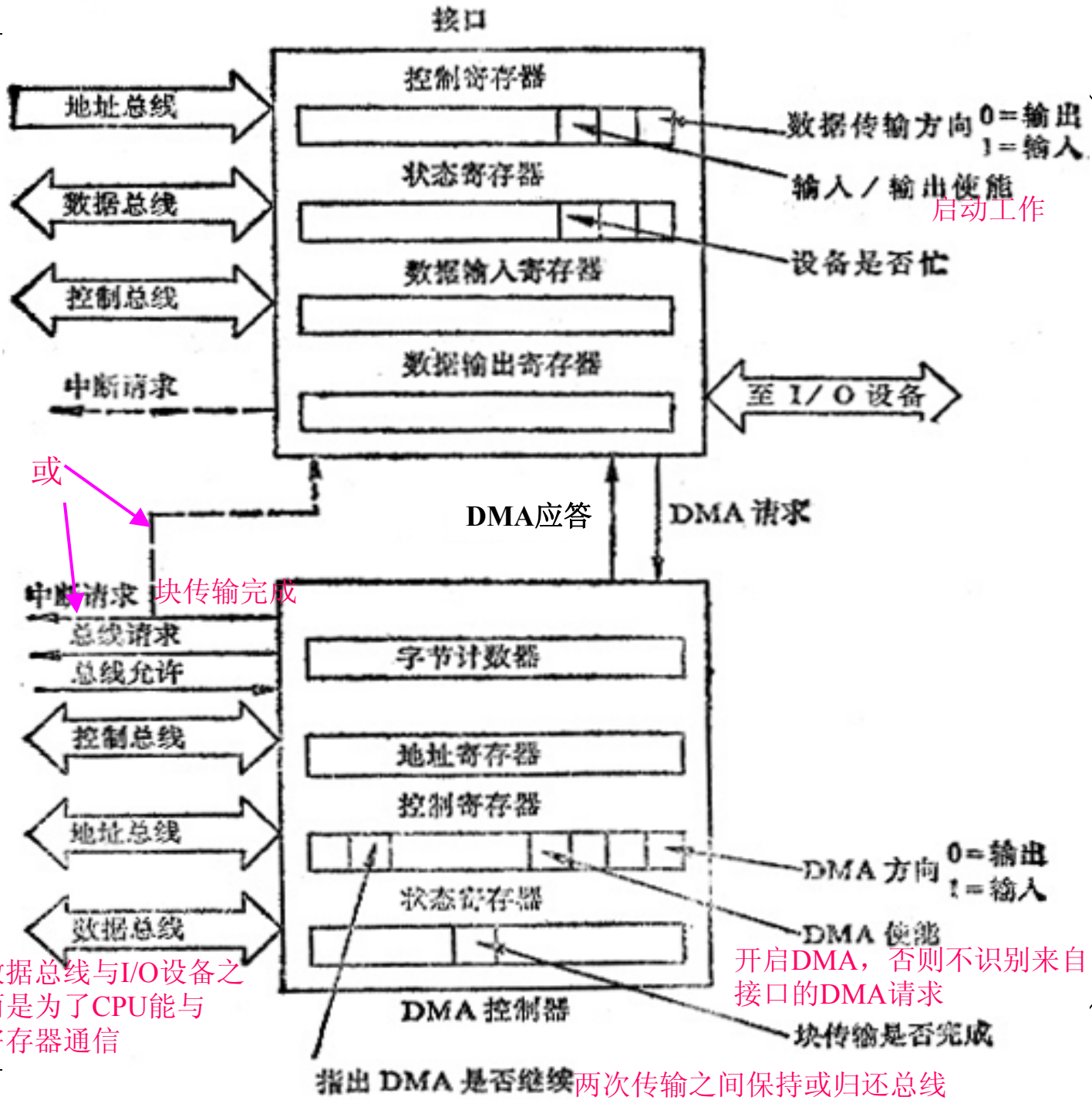


现行总线周期完成后才响应

DMAC中地址寄存器的内容

何时撤消请求由DMAC决定

最小的DMAC/接口配置



不是为了在数据总线与I/O设备之间传数据，而是为了CPU能与DMAC中的寄存器通信

开启DMA，否则不识别来自接口的DMA请求

两次传输之间保持或归还总线

启动DMA传送的典型程序段

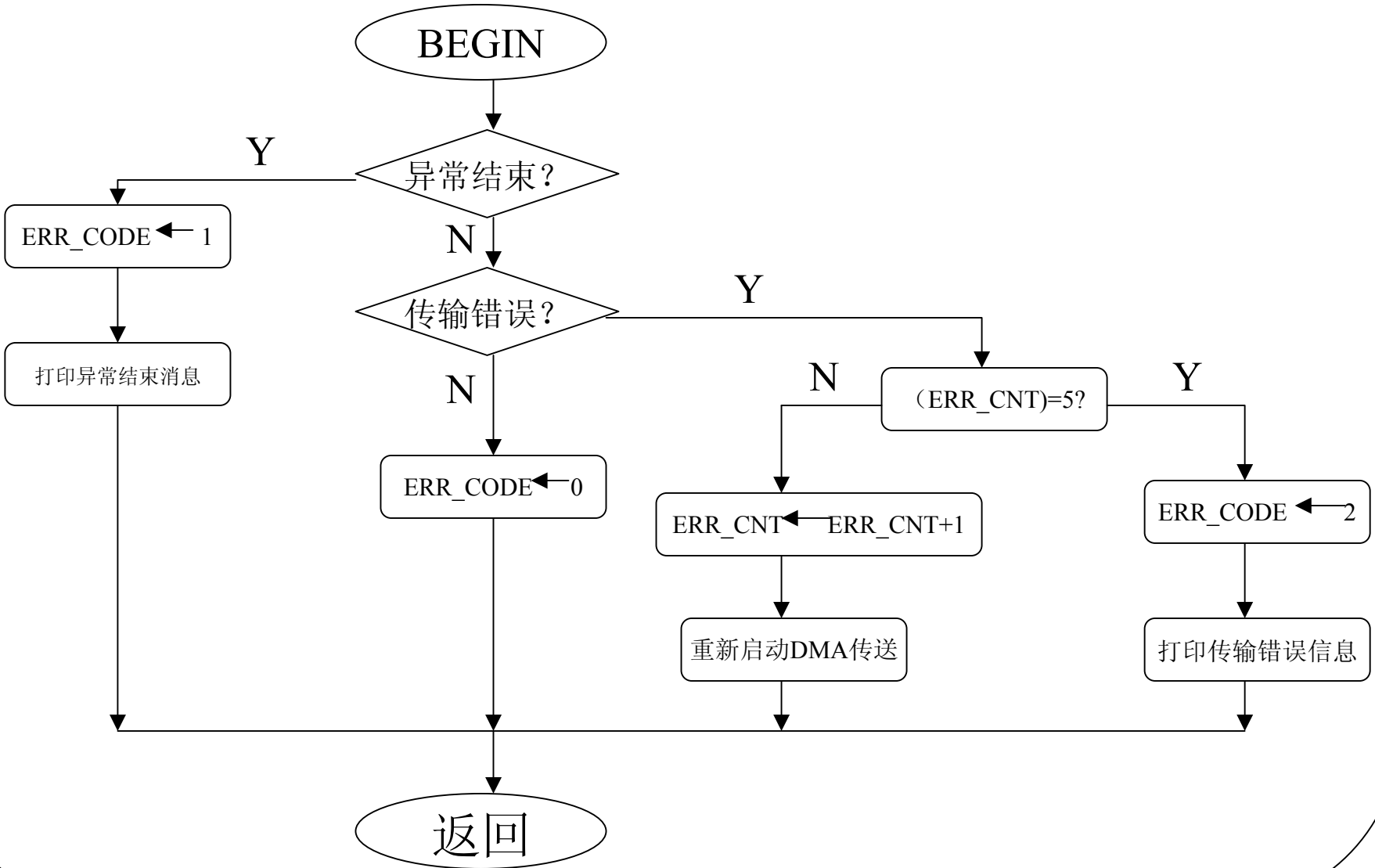
```
IDLE:   IN      AL, INTSTAT          ; 接口状态
        TEST    AL, 00000100B
        JNZ     IDLE                 ; 忙则等

        MOV     AX, BYTE_COUNT       ; 数据块长度
        OUT     BC_REG, AX           ; 置入DMAC字节计数寄存器
        LEA     AX, BUFFER           ; 数据块起始地址
        OUT     ADDR_REG, AX         ; 置入DMAC流水地址寄存器
        MOV     AL, DMAC控制字[注]
        OR      AL, 00001001B        ; 开放DMA，输入
        OUT     DMA_CON，AL          ; 置入DMAC控制寄存器

        MOV     AL，接口控制字[注]
        OR      AL，00000101B        ; 接口工作，输入
        OUT     INT_CON，AL          ; 置入接口控制寄存器
```

[注] DMAC控制字和接口控制字预先存在内存中

传送结束和结束例程


BEGIN
异常结束？
Y
N
ERR_CODE ← 1
打印异常结束消息
传输错误？
Y
N
ERR_CODE ← 0
（ERR_CNT)=5?
N
Y
ERR_CNT ← ERR_CNT+1
重新启动DMA传送
ERR_CODE ← 2
打印传输错误信息
返回

§ 13-2 THE 8237 PROGRAMMABLE DMA CONTROLLER

Features

- DMA controller provides memory with the address and select the appropriate I/O device (via *DACK)
- Address Increment or Decrement
- Four Independent DMA Channels
- Enable/Disable Control of Individual DMA Requests
- Directly Expandable to *Any Number* of Channels
- Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5

Other Features

- ***Memory-to-Memory*** Transfers
- Memory Block ***Initialization***
- ***End of Process*** ***Input*** for Terminating Transfers
- Software DMA Requests
- Independent ***Polarity*** Control for DREQ and DACK Signals

pp.499-501 *Pin Definition (1/10)*

Symbol	Type	Name and Function
V_{CC}		POWER: +5V supply.
V_{SS}		GROUND: Ground.
CLK	I	CLOCK INPUT: Clock Input controls the ***internal operations*** of the8237A and its ***rate of data transfers***. •The input may be driven at up to 5 MHz for the 8237A-5.

Pin Definition (2/10)

Symbol	Type	NAME and Function
$\overline{CS}$	I	CHIP SELECT: Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	RESET: Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip-flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	READY: Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices, i.e.,allows memory and I/O to insert wait states into the 8237.

Pin Definition (3/10)

Symbol	Type	NAME and Function
HLDA	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0 - DREQ3	I	DMA REQUEST: The DMA Request lines are individual *asynchronous* channel request inputs used by peripheral circuits to obtain DMA service. –A request is generated by activating the DREQ line of a channel. –DACK will acknowledge the recognition of DREQ signal. –DREQ must be maintained until the corresponding DACK goes active. ●Polarity of DREQ is programmable. –Reset initializes these lines to active high. ●In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority.

Pin Definition (4/10)

Symbol	Type	NAME and Function
DB0- DB7	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. ●The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. ●The outputs are disabled and the inputs are enabled during an I/O Write cycle when the CPU is programming the 8237A control registers. ●During DMA cycles the ***most significant 8 bits of the address*** are output to be strobed into an external latch by ADSTB. ●In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.

Pin Definition (5/10)

Symbol	Type	NAME and Function
$\overline{\text{IOR}}$	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. •In the Idle cycle, it is an *input* control signal used by the CPU to read the control registers. •In the Active cycle, it is an *output* control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{\text{IOW}}$	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. •In the Idle cycle, it is an *input* control signal used by the CPU to load information into the 8237A. •In the Active cycle, it is an *output* control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

Pin Definition (6/10)

Symbol	Type	NAME and Function
$\overline{\text{EOP}}$	I/O	END OF PROCESS: is an active low bidirectional signal. •Information concerning the completion of DMA services is available at the bidirectional EOP pin. –The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the EOP input low with an external EOP signal. –The 8237A also generates a pulse when the *terminal count (TC)* for any channel is reached. This generates an EOP signal which is output through the EOP line. •The reception of EOP, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if *autoinitialize* is enabled, to write the base registers to the current registers of that channel. –The mask bit will be set for the currently active channel by EOP unless the channel is programmed for autoinitialize. In that case, the mask bit remains unchanged. •During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs.

Pin Definition (7/10)

Symbol	Type	NAME and Function
A0-A3	I/O	ADDRESS: The four least significant address lines are bidirectional three-state signals. •In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. •In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4-A7	O	ADDRESS: The four most significant address lines are three-state outputs and provide 4 bits of address. •These lines are enabled *only* during the DMA service.

Pin Definition (8/10)

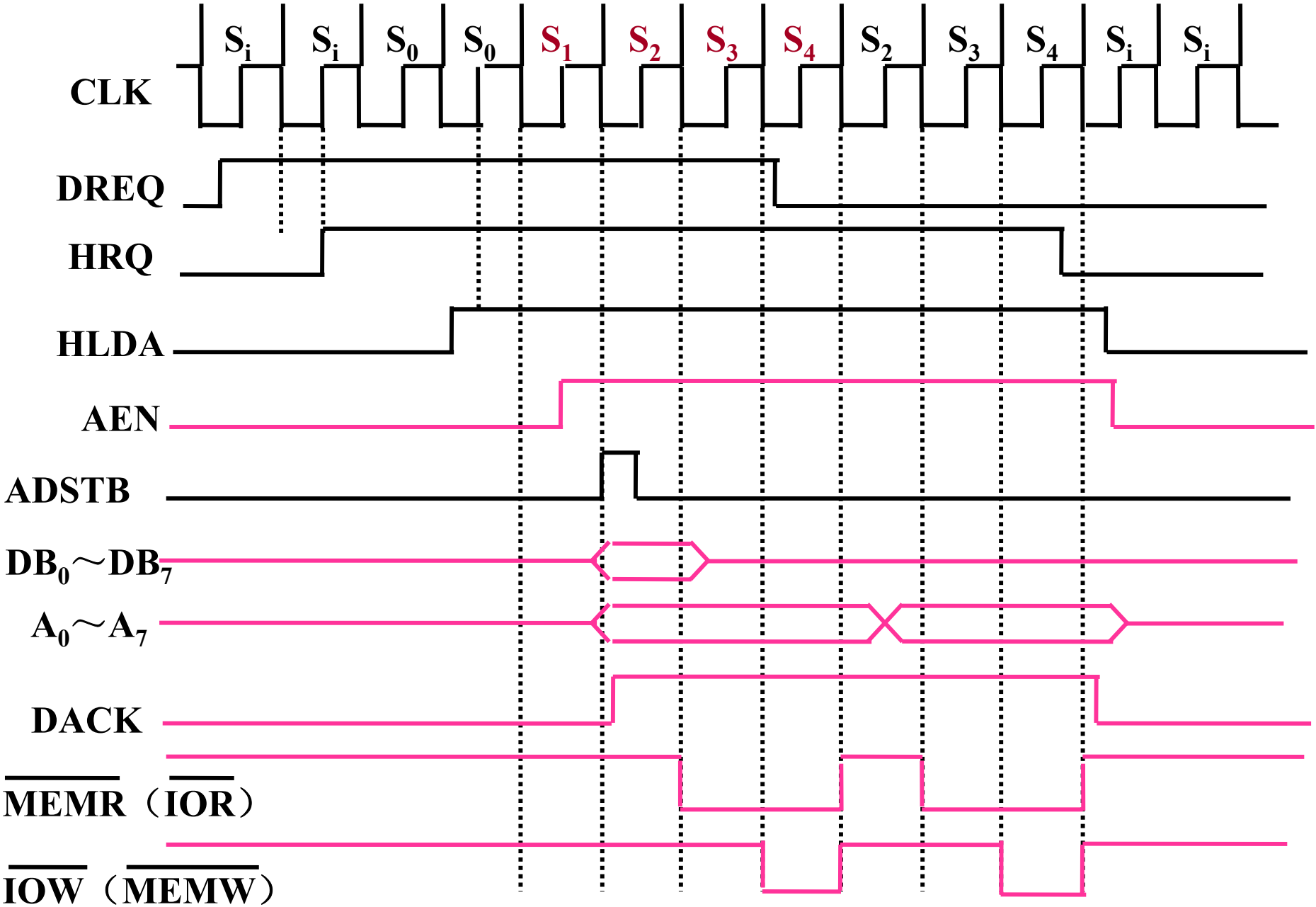
Symbol	Type	NAME and Function
HRQ	O	HOLD REQUEST: This is the Hold Request *to* the CPU and is used to request control of the system bus. •If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.
DACK0 - DACK3	O	DMA ACKNOWLEDGE: DMA Acknowledge is used *to notify* the individual peripherals when one has been granted a DMA cycle. •The sense of these lines is programmable. –Reset initializes them to active low.

Pin Definition (9/10)

Symbol	Type	NAME and Function
AEN	O	ADDRESS ENABLE: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	ADDRESS STROBE: The active high, Address Strobe is used to strobe the upper address byte into an external latch.

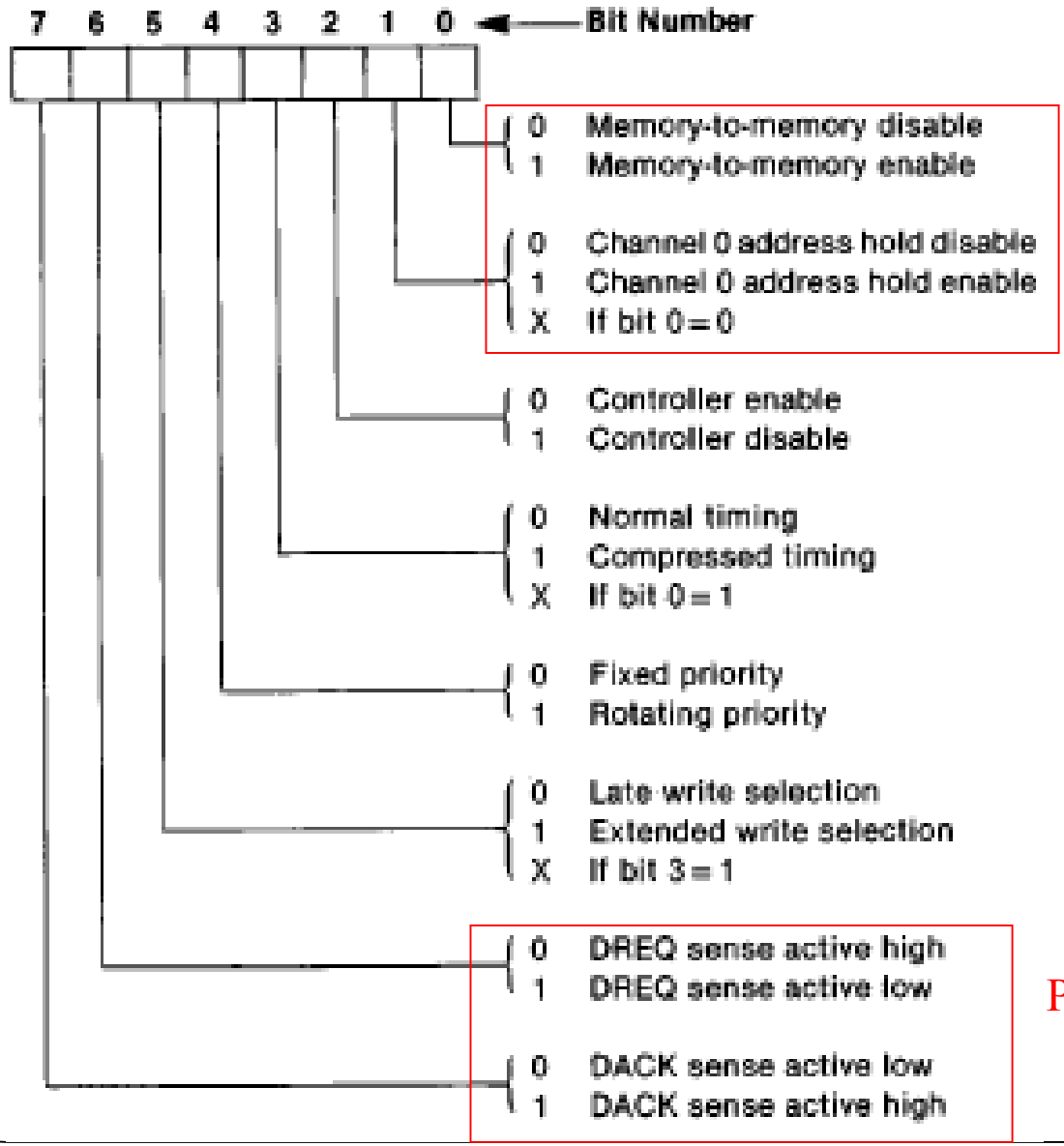
Pin Definition (10/10)

Symbol	Type	NAME and Function
$\overline{\text{MEMR}}$	O	MEMORY READ: The Memory Read signal is an active low three-state output used to access data from *the selected memory location* during a DMA Read or a memory-to-memory transfer.
$\overline{\text{MEMW}}$	O	MEMORY WRITE: The Memory Write is an active low three-state output used to write data to *the selected memory location* during a DMA Write or a memory-to-memory transfer.


Si Si S0 S0 S1 S2 S3 S4 S2 S3 S4 Si Si
CLK
DREQ
HRQ
HLDA
AEN
ADSTB
DB0～DB7
A0～A7
DACK
MEMR（IOR）
IOW（MEMW）

pp.501-504 *Internal Registers*

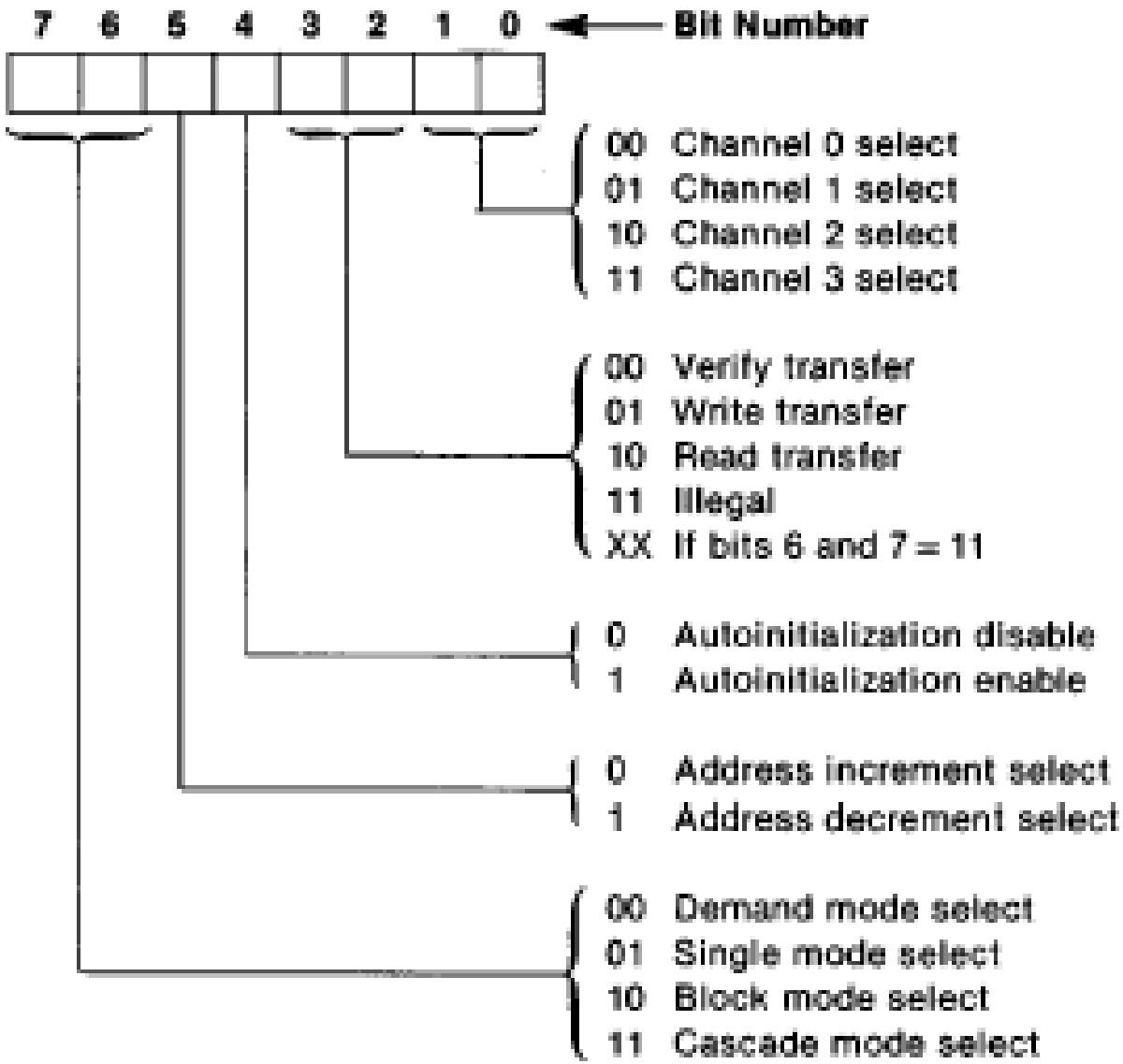
Command Register



Memory-to-Memory Transfer

Polarity

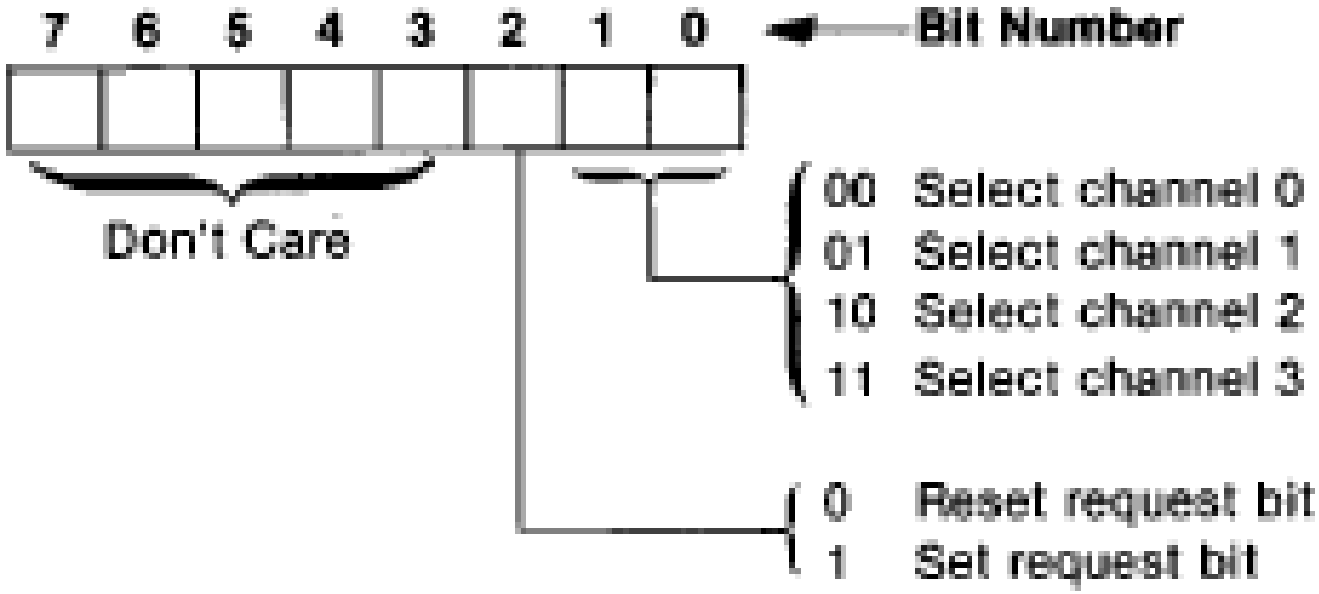
Mode Register



8237 Modes

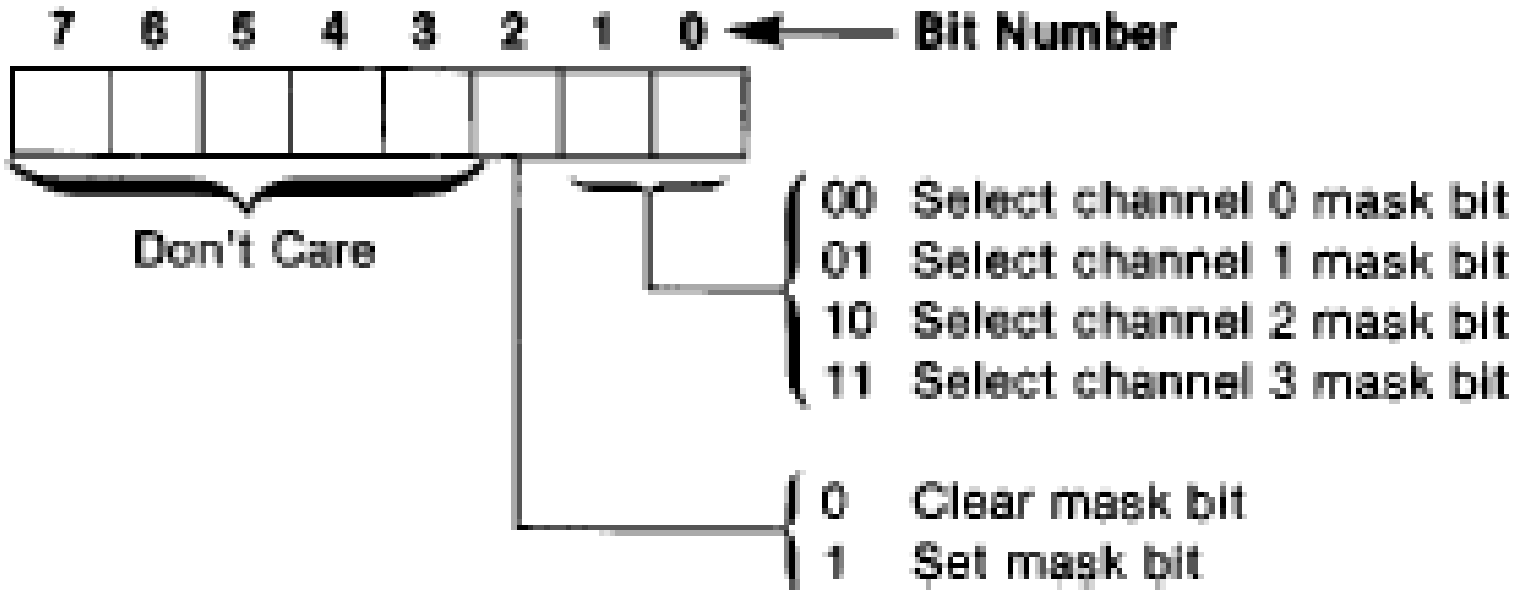
- Intel 8237 can be set to four different style of transfer:
  - Single - One transfer at a time, allow processor access to the bus between transfers
  - Block - Transfer all data, do not allow processor access to the bus (may cause problems with memory refresh!)
  - Demand - Keep transferring as long as target keeps DRQ asserted
  - Cascade - allow a slave controller use of the DMAC
- In addition, the DMA controller can be set to make continuous transfers
  - known as auto-initialized DMA
  - normal DMA is known as "single-cycle"

Request Register



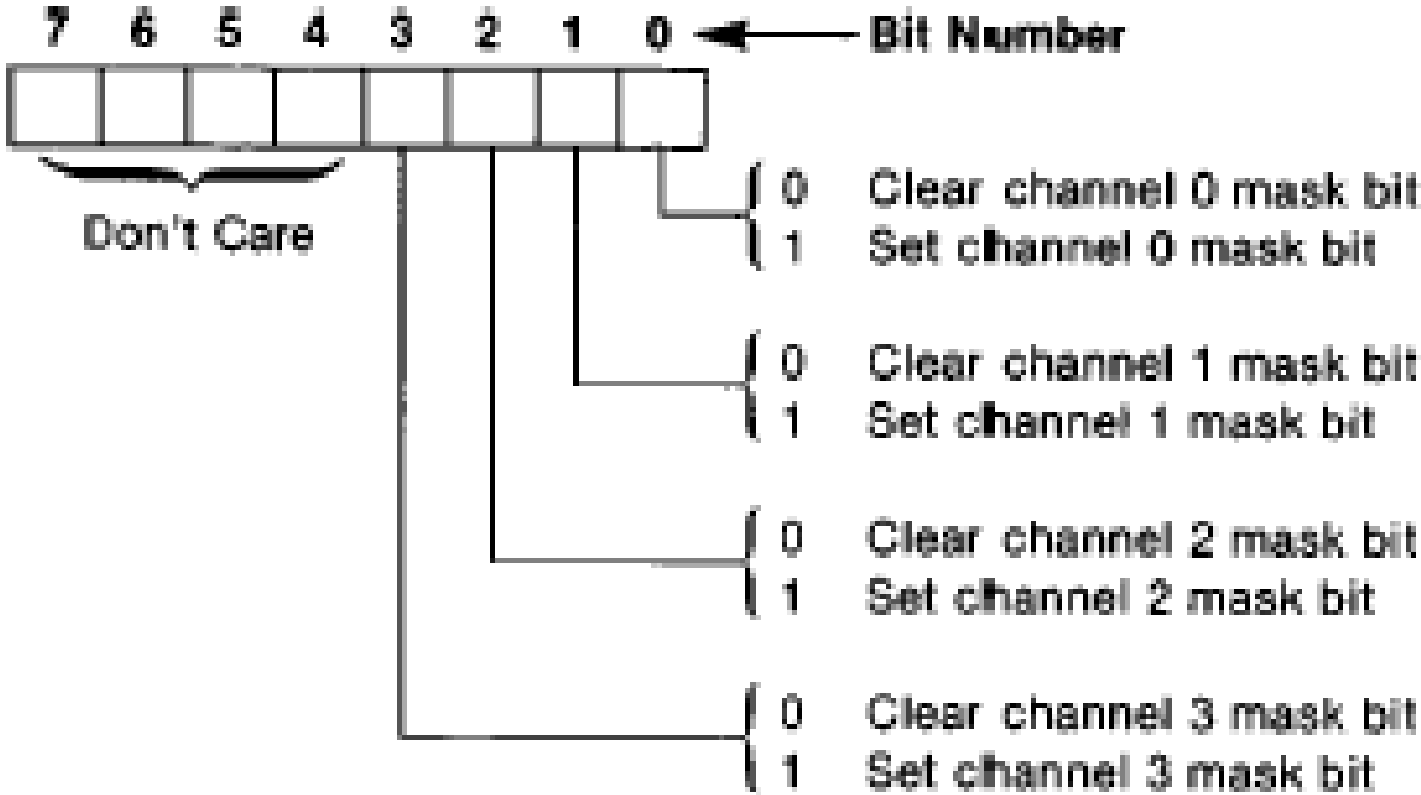
- The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ.
  - Each channel has a request bit associated with it in the 4-bit Request register.
  - These are non-maskable

Mask Register Set / Reset

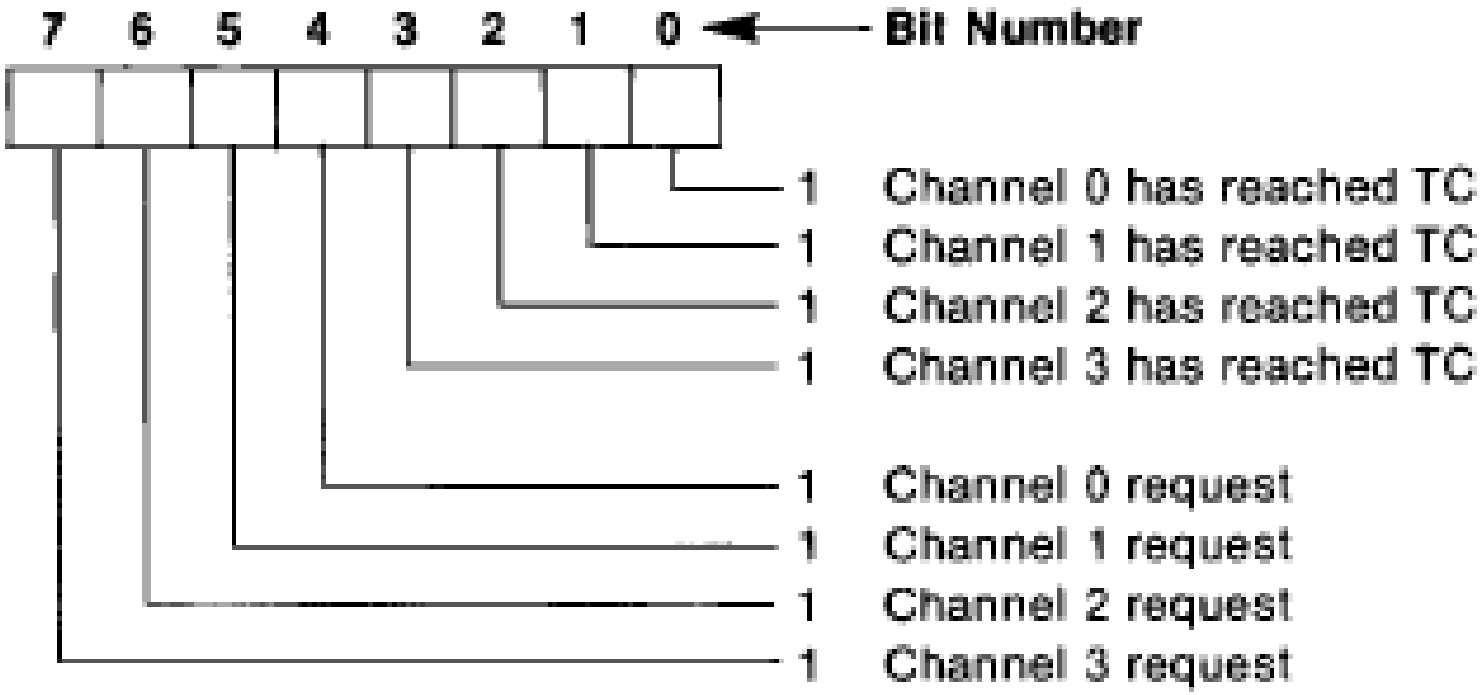


Mask Register

- All four bits of the Mask register may also be written with a single command:



Status Register



- Bits 0-3 are set every time a TC (Terminal Count) is reached by that channel or an external $\overline{EOP}$ is applied.
  - -These bits are cleared upon Reset and on each Status Read.
- Bits 4-7 are set whenever their corresponding channel is requesting service.

Definition of Register Codes

Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

p.504 Software Commands

- These are additional special software commands which can be executed in the Program Condition.
  - ❑They do not depend on any specific bit pattern on the data bus.
- The three software commands are:

1.Clear First/Last Flip-Flop:

- ➢Must be executed prior to writing or reading new address or word count information to the 8237A
- ➢Initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

2.Master Clear:

- ➢Has the same effect as the hardware RESET.

3.Clear Mask Register:

- ▪Clears the mask bits of all four channels, enabling them to accept DMA requests.

p.504 FIGURE 13-10
8237A-5 Command and Control Port Assignments

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

= p.504 Software Command

pp.504-505 Programming the Address and Count Register

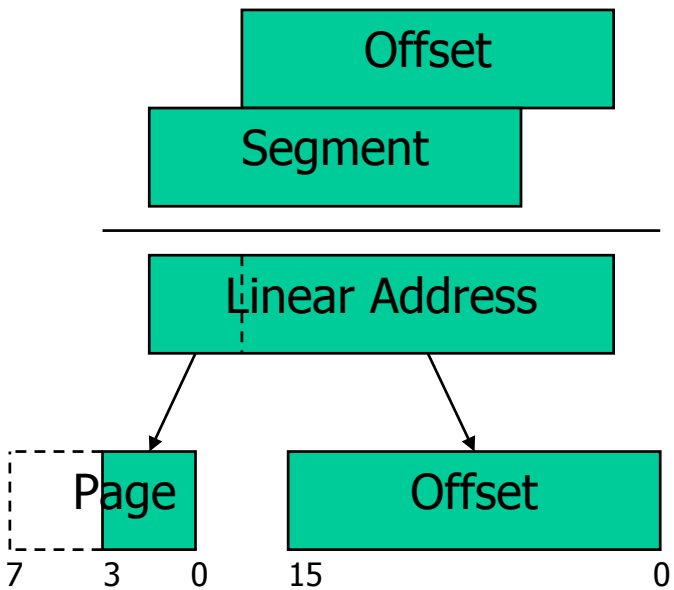
Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0–A7
			0	1	0	0	0	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0–A7
			0	0	1	0	0	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0–W7
			0	1	0	0	0	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0–W7
			0	0	1	0	0	0	1	1	W8–W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0–A7
			0	1	0	0	0	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0–A7
			0	0	1	0	0	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0–W7
			0	1	0	0	0	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0–W7
			0	0	1	0	0	1	1	1	W8–W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0–A7
			0	1	0	0	1	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0–A7
			0	0	1	0	1	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0–W7
			0	1	0	0	1	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0–W7
			0	0	1	0	1	0	1	1	W8–W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0–A7
			0	1	0	0	1	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0–A7
			0	0	1	0	1	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0–W7
			0	1	0	0	1	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0–W7
			0	0	1	0	1	1	1	1	W8–W15

Coding DMA Transfers

1. Find the Page and Page Offset of the memory block you wish to transfer
2. Turn off the DMA channel (so it will not accept requests while you reprogram it)
3. Clear the byte pointer flip/flop
4. Write the transfer mode to the mode register
5. Write the page offset to the address register
6. Write the length (-1 byte/word) to the count register
   (0=1 byte, 65535=64Kbytes)
7. Write the page # to the *page register*
8. Re-enable the DMA channel
9. Set up target device

Page Register

- Because the range of the 8237 is 64K bytes (or 64K words), each channel has a page register to extend the address to 24-bits
- If use real mode, only use 4 bits of the page register
- To get the page #, calculate linear (absolute) address. The upper 4 bits are the page:



Find the Page and Page Offset

```
; Code to convert segment:offset to
; page:page_offset
; SI contains offset, DX contains segment
   mov ax,dx
   mov cl,4
   shl ax,cl          ; shift segment left 4
   shr dx,cl
   add si,ax          ; add shifted segment to offset
   adc dh,0
; Now SI contains the offset within the page,
; the low 4-bits of DH contain the page #
```

Coding DMA Transfers (Cont'd)

```
; Clear byte ptr F/F
   out BYTEREG,al       ; any value to reset

; write mode to mode register
   mov al, mode
   out MODEREG,al

; write page offset to address reg.
   mov ax,si            ; get offset in ax
   out ADDRREG,al       ; write LSB of DMA offset
   mov al,ah
   out ADDRREG,al       ; write MSB of DMA offset
```

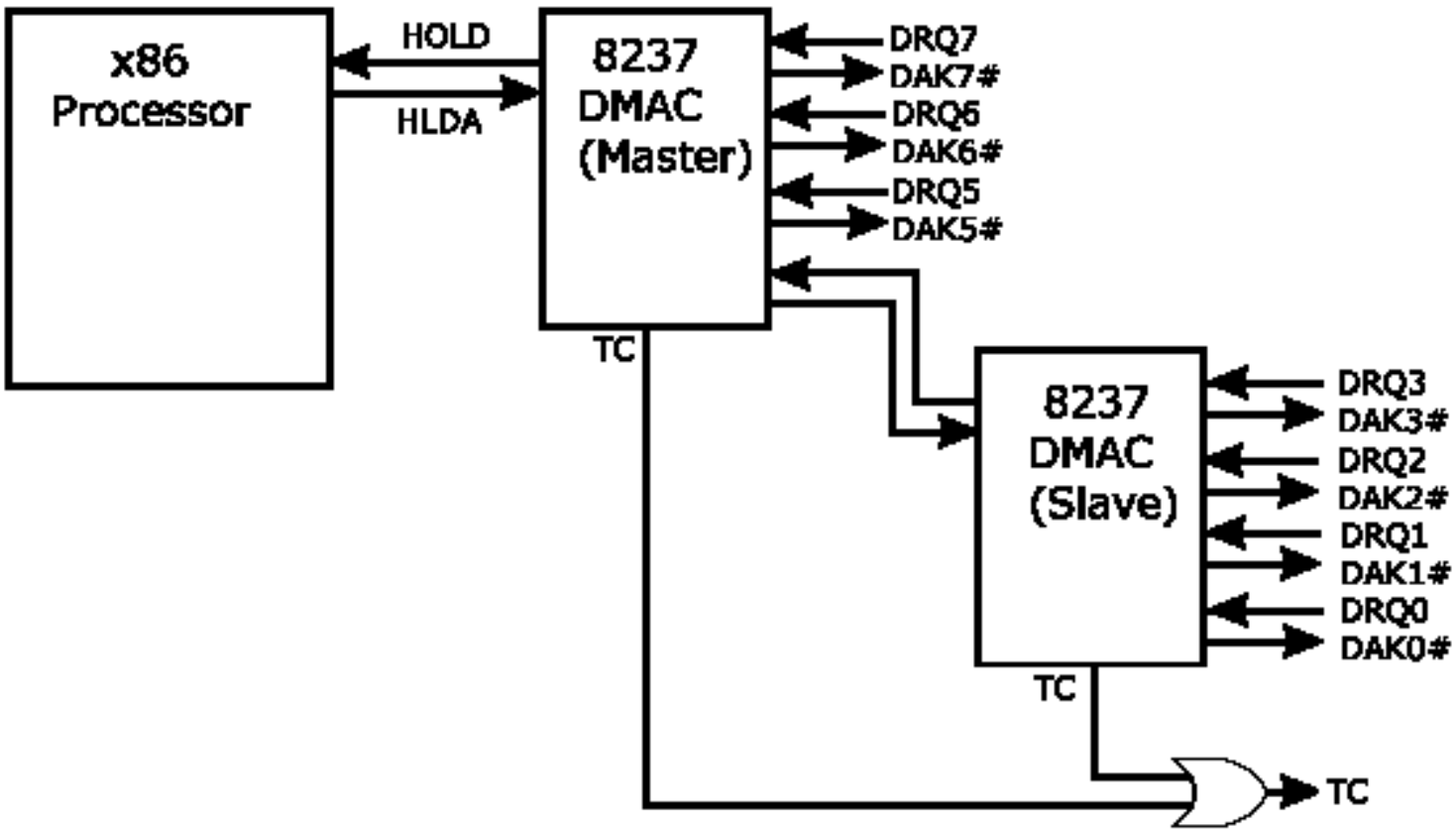
Coding DMA Transfers (Cont'd)

```
; write length (-1) to count reg.
   mov ax,length                ; ax=length-1
   dec ax
   out COUNTREG,al              ; write LSB of size
   mov al,ah
   out COUNTREG,al              ; write MSB of size

; write page# to page register
   mov      al,dh
   out      PAGEREG,al          ; write page
```

DMA Hardware on PC

- The PC has two 8237 DMA Controllers, arranged in a Master/Slave organization:

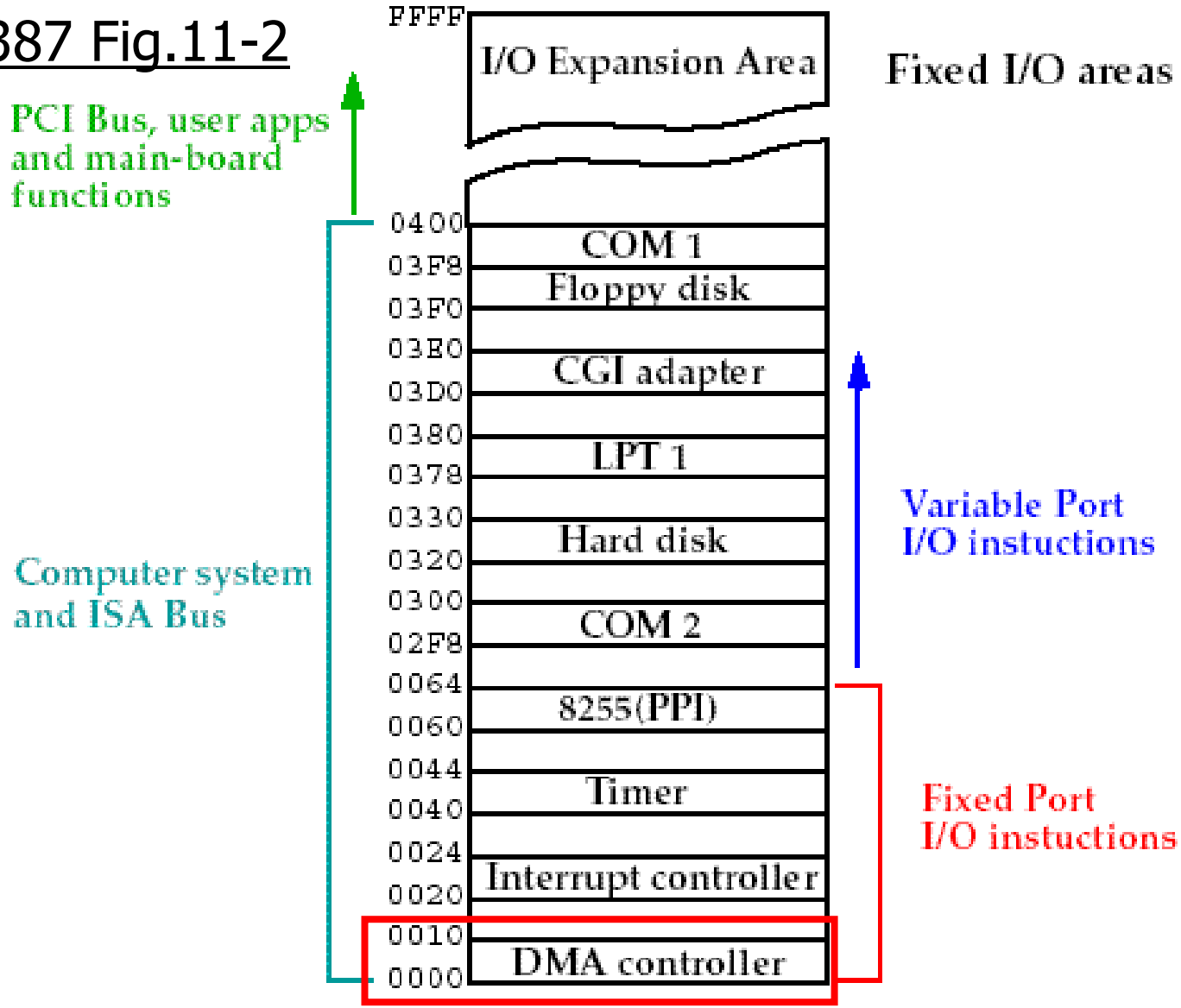


DMA Hardware on PC (Cont'd)

- Processor has HOLD/HOLD Acknowledge lines to interact with 8237
  - DMAC can gain control of ISA bus by asserting HOLD
  - Processor acknowledges with HLDA
- DRQ4 services slave controller
- Priorities are set as fixed
  - DRQ0 highest, DRQ7 lowest
  - Can be reprogrammed for rotating priority

Personal Computer I/O Map

See p.387 Fig.11-2



DMA Hardware on PC (Cont'd)

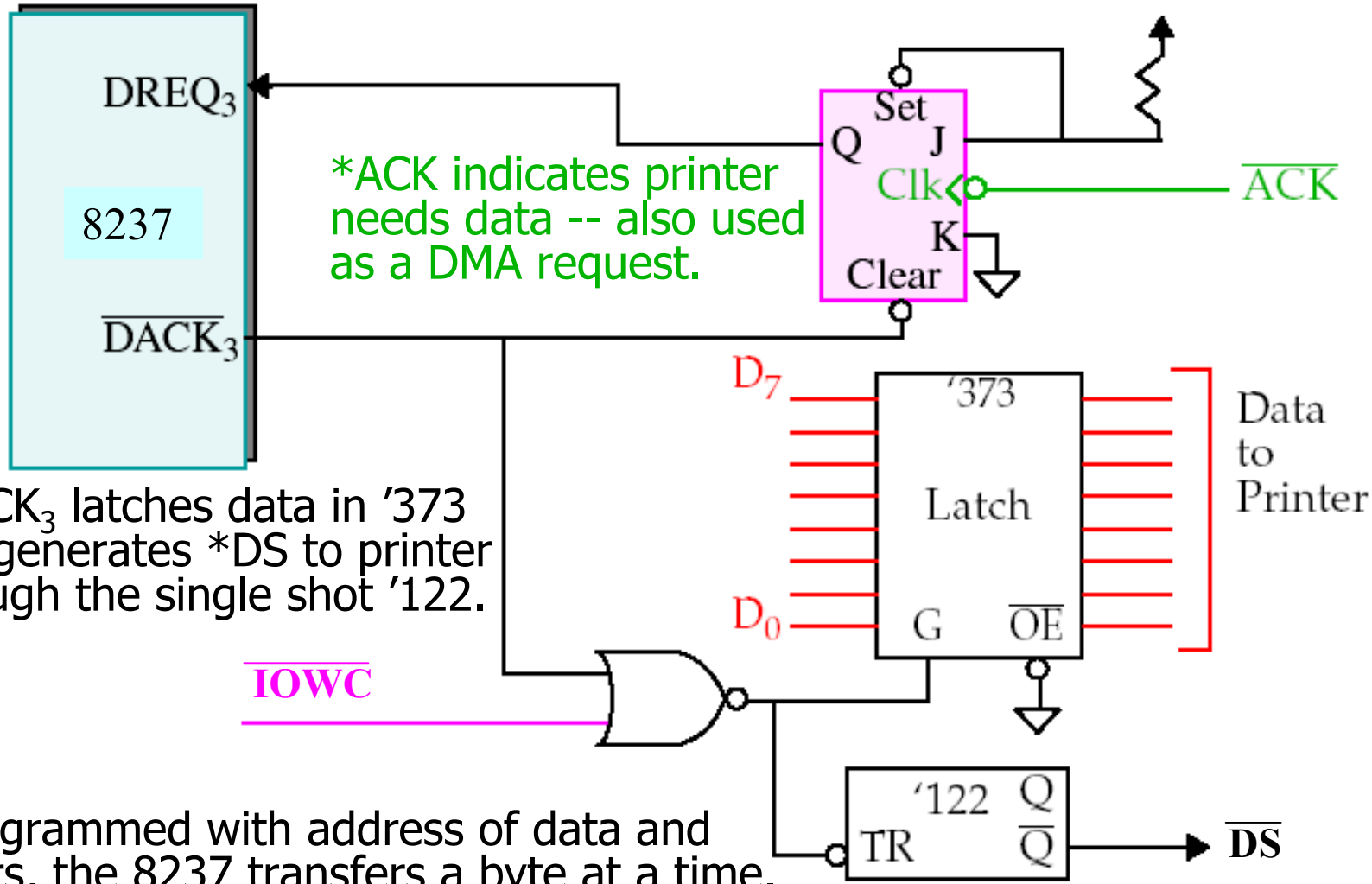
- ISA address/data/control lines are also connected (not shown)
  - Can access internal registers through ports
  - Each channel has a page register associated with it

DMA Controller	Slave				Master			
DRQ#	0	1	2	3	4	5	6	7
Memory Address Register I/O Address	00h	02h	04h	06h	C0h	C4h	C8h	CCh
Page Register	87h	83h	81h	82h	(none)	8Bh	89h	8Ah
Count Register I/O Address	01h	03h	05h	07h	(none)	C6h	CAh	CEh

DMA Hardware on PC (Cont'd)

DMA Controller	Slave	Master
Control Register I/O Address	08h	D0h
Mode Register I/O Address	0Bh	D6h
Mask Register I/O Address	0Ah	D4h
Clear Byte F/F I/O Address	0Ch	D8h

DMA-Processed Printer Interface



Once programmed with address of data and # of chars, the 8237 transfers a byte at a time.

- Note that the I/O device is NOT selected by decoding the address bus, but rather by *DACK, since address bus contains a memory address.
- See code in book and example of 8237 connected to an 8088. (pp. 506-507).

Homework

1. Page 546 Problem 7
2. Page 546 Problem 11
3. Page 546 Problem 13
4. Page 546 Problem 15