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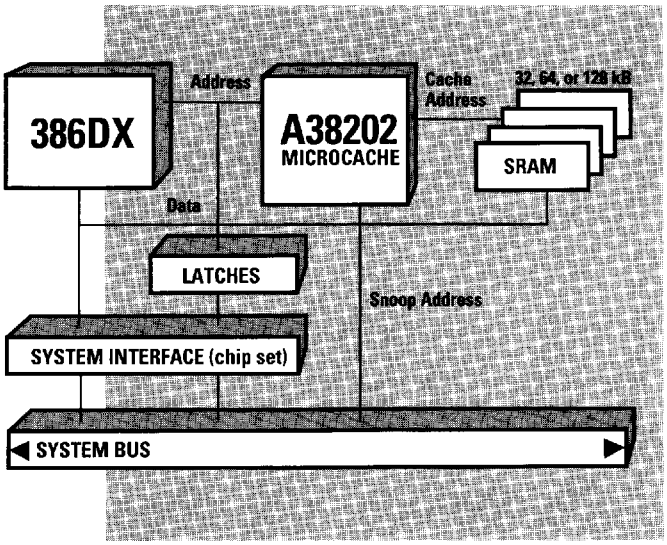
MICROCACHE® HIGH PERFORMANCE

Cache memory increases performance over 30% in a 386DX system. Austek's A38202 cache memory controller maximizes cache performance, allows product differentiation, and can be optimally configured for DOS, Windows, OS/2, UNIX and networking environments.



386DX

A38202 MICROCACHE FOR 386DX SYSTEMS

The A38202 controls cache sizes of 32-KBytes, 64-kBytes and 128-kBytes at 25 MHz, 33 MHz and 40 MHz. The cache may be configured as direct mapped for lowest cost or two-way set associative for highest performance. The controller is easily incorporated into a design with the 386DX microprocessor and a chip set to interface to the AT, EISA or MCA bus. A complete cache AT system can be built with about 20 integrated circuits.

The A38202 has on-chip tag SRAMS, eliminating the need for external high speed tag SRAMS. It provides zero wait states on read hits and buffered writes. Three on-chip programmable non-cache regions can be programmed for individual system configurations. The device allows caching of BIOS and ROM code, which can provide over 30% performance improvement for ROM-intensive routines such as video. A separate clock reset, which synchronizes but does not flush the cache on reset, improves performance with Windows, OS/2 and network operating systems. Performance in systems with alternate bus masters such as network and SCSI cards is improved by using a snoop bus to maintain coherency; this allows the 386DX to continue execution during DMA operations.

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A38202 MICROCACHE FOR 386DX SYSTEMS

Key Features

- Directly interfaces to 386DX microprocessor and 386DX chip sets
- Configuration options programmable by BIOS
- Supports three cache sizes - *32-kByte, 64-kByte and 128-kByte*
  - *System may be populated with minimum cache and easily expanded to larger sizes and associativity by the end user*
- Caches full 386DX address space
- Two-way set associative or direct mapped
  - *Two-way set associative cache can exceed the performance of a direct mapped cache of twice the size*
- Write-through memory update policy
- Least recently used (LRU) replacement algorithm
- On-chip high speed tag SRAMs
- Direct interface to x4, x8 and x16 cache data SRAMs - requires no interface latches

Cache Data SRAM Options

(35ns at 25-MHz/25ns at 33-MHz/20ns at 40-MHz)

	Direct Mapped	Two-way set associative
32-kbyte cache	*2 8Kx16* *4 8Kx8*	*2 8Kx16*
64-kByte cache	*2 16Kx16* *4 8Kx16* *8 8Kx8* *8 16Kx4*	*2 16Kx16* *4 8Kx16* *8 8Kx8*
128-kByte cache	*4 32Kx8* *4 16Kx16* *8 8Kx16*	*4 16Kx16* *8 8Kx16* *16 8Kx8*

- Three on-chip noncachable regions
  - *One region of any multiple of 4-kByte size locatable on any 4-kByte boundary*
  - *Two regions of any multiple of 64-kByte size locatable on any 64-kByte boundary*
  - *Each region may be noncached for reads and writes or writes only*
- Noncache input provides for additional noncache regions
- On-chip programmable write buffer control for zero wait state writes
  - *I/O write buffering may be turned on/off*
- Separate functional (PWRGOOD) and clock (RESET) reset inputs - RESET synchronizes, but does not flush the cache, this increases performance in Windows, OS/2 and network operating systems
- Asynchronous snoop bus to maintain cache coherency
  - *Increases system performance by allowing the processor to continue execution during DMA, refresh and other bus master activity*
  - *No synchronizing logic required*
- Burst read from DRAM - up to 60% wait state reduction on a miss
- GATEA20 input
- Internal decoding for 387 and Weitek 3167 coprocessors
- Caches memory on the processor bus and the AT/EISA/MCA bus
- On-chip diagnostic mode to test cache data SRAM
- On-chip fault detection to help system debug
- 25 MHz, 33 MHz and 40 MHz
- Low power CMOS
- 160 lead plastic quad flat pack (EIAJ)

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