



# Intel® Itanium® Processor Family System Abstraction Layer Specification Update

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*June 2004*

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## Revision History

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Date	Version	Description
June 2004	002	Added Specification Change 1; added Documentation Changes 1 - 4.

# Preface

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This document is an update to the specifications contained in the Affected Documents/Related Documents table. This document is a compilation of documentation errata, specification clarifications, and changes. It is intended for hardware system manufacturers and firmware/software developers.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents/Related Documents

Title	Document #
December 2003 release of the <i>Intel® Itanium® Processor Family System Abstraction Layer Specification</i>	245359-007

## Nomenclature

**Specification Changes** are modifications to the current published specifications in the Affected Documents list and should be considered a part of those documents. These changes will be incorporated in the next release of the specifications.

**Specification Clarifications** describe a specification in greater detail or further explain a specification's interpretation. These clarifications will be incorporated in the next release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the documents listed above.

# Summary of Changes

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The following tables indicate the specification changes, specification clarifications, or documentation changes that apply to the December 2003 release of the *Intel® Itanium® Processor Family System Abstraction Layer Specification*.

## Specification Changes

No.	Page	SPECIFICATION CHANGES
1	8	Platform Features ITC bit field

## Specification Clarifications

No.	Page	SPECIFICATION CLARIFICATIONS
		None for this revision of the Specification Update

## Documentation Changes

No.	Page	DOCUMENTATION CHANGES
1	10	MOD_REQUESTOR_IDENTIFIER field in MOD_ERROR_INFO_STRUCT
2	10	SAL_MC_RENDEZ description clarification
3	10	Error Record Header minor revision number increment
4	11	Clarification to Platform PCI Component Error Info Error Record Section

# Specification Changes

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## 1. Platform Features ITC bit field

The Platform Features Descriptor Entry described in Section 3.2.6.2, must be replaced with the following, reflecting the addition of bit 3 to the Platform Feature List.

Offset (in Bytes)	Length (in Bytes)	Description
0	1	Entry type = 2 denoting Platform Features type.
1	1	Platform Feature List: Bit 0: 1 if Bus Lock is implemented on the processor as well as the platform. Bit 1: 1 if the chipset supports redirection hint for interrupt messages originating from the platform (lowest priority interrupt). Bit 2: 1 if the chipset supports redirection hint for IPI messages originating from the processors. Bit 3: 1 if the processor Interval Timer Counter and Match Registers (ITC) in the system may drift from each other. 0 if processor ITCs will not drift once synchronized. Bits 4-7 = Reserved.
2	14	Reserved.



## ***Specification Clarifications***

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There are no Specification Clarifications for this revision of the *Intel® Itanium® Processor Family System Abstraction Layer Specification Update*.

# Documentation Changes

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## 1. MOD\_REQUESTOR\_IDENTIFIER field in MOD\_ERROR\_INFO\_STRUCT

The MOD\_REQUESTOR\_IDENTIFIER and MOD\_RESPONDER\_IDENTIFIER fields are reversed in MOD\_ERROR\_INFO\_STRUCT. The definition of MOD\_ERROR\_INFO\_STRUCT (page B-5/6) must be replaced with the following:

```

struct{
    VALID_FIELD_BITS                48 bytes4 (Mod)
    CHECK_INFO_VALID_BIT           8 bytes
    REQUESTOR_IDENTIFIER_VALID_BIT Bit 0
    RESPONDER_IDENTIFIER_VALID_BIT Bit 1
    TARGET_IDENTIFIER_VALID_BIT    Bit 2
    PRECISE_IP_VALID_BIT           Bit 3
    RESERVED_VALID_BIT             Bit 4
    MOD_CHECK_INFO                 Bit 5-63
    MOD_REQUESTOR_IDENTIFIER       8 bytes
    MOD_RESPONDER_IDENTIFIER       8 bytes
    MOD_TARGET_IDENTIFIER          8 bytes
    MOD_PRECISE_IP                 8 bytes
} MOD1_ERROR_INFO_STRUCT

```

## 2. SAL\_MC\_RENDEZ description clarification

The second paragraph of the description of the SAL\_MC\_RENDEZ procedure on page 93 must be replaced with:

Once SAL has determined that a machine check is in progress, this procedure is invoked on non-monarch processors. This procedure will disable interrupts and set an implementation-specific check-in flag within the SAL data area to indicate to the monarch processor that the non-monarch processor has reached SAL. Next, it will call the PAL\_MC\_DRAIN procedure to complete all outstanding transactions within the processor. The non-monarch processor will then go into a spin loop awaiting a wakeup signal from the monarch processor. The wakeup mechanism may be an external interrupt or a memory variable as set up by the SAL\_MC\_SET\_PARAMS procedure. SAL will return an error if a wakeup mechanism has not been registered.

## 3. Error Record Header minor revision number increment

Clarifications were made to the interpretation of Error Record Section headers in December 2003 release of the *Intel® Itanium® Processor Family System Abstraction Layer Specification*. This requires a minor revision number update in the Error Record Header. The Revision field of the Record Header in Section B.2.1 must be replaced with the following:

8	2 bytes	REVISION	2-byte Major and Minor revision number of the Record in BCD format: Byte0 – Minor (0x04) Byte1 – Major (0x00)
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#### 4. Clarification to Platform PCI Component Error Info Error Record Section

In the Platform PCI Component Error Info Error Record Section of B.2.4.3, replace the PCI\_COMP\_REGS\_DATA\_PAIR and PCI\_COM\_OEM\_DATA\_STRUCT fields with the following clarification:

40	2 x 8 x M bytes	PCI_COMP_REGS_DATA_PAIR	An array of address/data pair values. The data may be 8 bytes in length. M = PCI_COMP_MEM_NUM + PCI_COMP_IO_NUM
40+2x8xN	N bytes	PCI_COMP_OEM_DATA_STRUCT	OEM specific data of variable length. See <a href="#">Table B-2</a> for the format of this structure. If PCI_COMP_OEM_DATA_STRUCT_VALID_BIT is not set, N = 0.

