

Opcode	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AND<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	0	0	0	0	0	0	S	Rn	Rd	shift #	0	shift	0	Rm													
AND<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	0	0	0	0	0	S	Rn	Rd	Rs	0	shift	1	Rm														
MUL<cond><S> Rd, Rm, Rs	cond	0	0	0	0	0	0	0	0	0	S	Rd	SBZ	Rs	1	0	0	1	Rm													
STR<cond>H Rd, <address>	cond	0	0	0	0	P	U	1	W	0		Rn	Rd	addr_mode	1	0	1	1	addr_mode													
LDR<cond>H Rd, <address>	cond	0	0	0	0	P	U	1	W	1		Rn	Rd	addr_mode	1	0	1	1	addr_mode													
Undefined Instruction	cond	0	0	0	0	x	x	x	x	0		x	x	x	x	x	x	x	x	1	1	0	1	0	x	x	x	x				
LDR<cond>SB Rd, <address>	cond	0	0	0	0	P	U	1	W	1		Rn	Rd	addr_mode	1	1	0	1	addr_mode													
Undefined Instruction	cond	0	0	0	0	x	x	x	x	0		x	x	x	x	x	x	x	x	1	1	1	1	0	x	x	x	x				
LDR<cond>SH Rd, <address>	cond	0	0	0	0	P	U	1	W	1		Rn	Rd	addr_mode	1	1	1	1	addr_mode													
EOR<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	0	0	0	1	S	Rn	Rd	shift #	0	shift	0	Rm															
EOR<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	0	0	0	1	S	Rn	Rd	Rs	0	shift	1	Rm															
MLA<cond><S> Rd, Rm, Rs, Rn	cond	0	0	0	0	0	0	1	S	Rd	Rn	Rs	1	0	0	1	Rm															
SUB<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	0	0	1	S	Rn	Rd	shift #	0	shift	0	Rm																
SUB<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	0	0	1	S	Rn	Rd	Rs	0	shift	1	Rm																
RSB<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	0	0	1	S	Rn	Rd	shift #	0	shift	0	Rm																
RSB<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	0	0	1	S	Rn	Rd	Rs	0	shift	1	Rm																
ADD<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	0	1	0	S	Rn	Rd	shift #	0	shift	0	Rm																
ADD<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	0	1	0	S	Rn	Rd	Rs	0	shift	1	Rm																
UMULL<cond><S> RdLo, RdHi, Rm, Rs	cond	0	0	0	0	1	0	0	S	RdHi	RdLo	Rs	1	0	0	1	Rm															
ADC<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	1	0	1	S	Rn	Rd	shift #	0	shift	0	Rm																
ADC<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	1	0	1	S	Rn	Rd	Rs	0	shift	1	Rm																
UMLAL<cond><S> RdLo, RdHi, Rm, Rs	cond	0	0	0	0	1	0	1	S	RdHi	RdLo	Rs	1	0	0	1	Rm															
SBC<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	1	1	0	S	Rn	Rd	shift #	0	shift	0	Rm																
SBC<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	1	1	0	S	Rn	Rd	Rs	0	shift	1	Rm																
SMULL<cond><S> RdLo, RdHi, Rm, Rs	cond	0	0	0	0	1	1	0	S	RdHi	RdLo	Rs	1	0	0	1	Rm															
RSC<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	0	1	1	1	S	Rn	Rd	shift #	0	shift	0	Rm																
RSC<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	0	1	1	1	S	Rn	Rd	Rs	0	shift	1	Rm																
SMALAL<cond><S> RdLo, RdHi, Rm, Rs	cond	0	0	0	0	1	1	1	S	RdHi	RdLo	Rs	1	0	0	1	Rm															
TST<cond> Rn, Rm OP #	cond	0	0	0	1	0	0	0	1	Rn	SBZ	shift #	0	shift	0	Rm																
TST<cond> Rn, Rm OP Rs	cond	0	0	0	1	0	0	0	1	Rn	SBZ	Rs	0	shift	1	Rm																
MRS<cond> Rd, CPSR	cond	0	0	0	1	0	0	0	0	SBO	Rd	SBZ																				
SWP<cond> Rd, Rm, [Rn]	cond	0	0	0	1	0	0	0	0	SBZ	Rn	Rd	SBZ	1	0	0	1	Rm														
TEQ<cond> Rn, Rm OP #	cond	0	0	0	1	0	0	1	1	Rn	SBZ	shift #	0	shift	0	Rm																
TEQ<cond> Rn, Rm OP Rs	cond	0	0	0	1	0	0	1	1	Rn	SBZ	Rs	0	shift	1	Rm																
MSR<cond> CPSR <fields>, Rm	cond	0	0	0	1	0	0	1	0	field_mask	SBO	SBZ																				
EX<cond> Rm	cond	0	0	0	1	0	0	1	0	SBO	SBO	SBO	0	0	0	1	Rm															
CMP<cond> Rn, Rm OP #	cond	0	0	0	1	0	1	0	1	Rn	SBZ	shift #	0	shift	0	Rm																
CMP<cond> Rn, Rm OP Rs	cond	0	0	0	1	0	1	0	1	Rn	SBZ	Rs	0	shift	1	Rm																
MRS<cond> Rd, SPSPR	cond	0	0	0	1	0	1	0	0	SBO	Rd	SBZ																				
SWP<cond>B Rd, Rm, [Rn]	cond	0	0	0	1	0	1	0	1	SBZ	Rn	Rd	SBZ	1	0	0	1	Rm														
CMN<cond> Rn, Rm OP #	cond	0	0	0	1	0	1	1	1	Rn	SBZ	shift #	0	shift	0	Rm																
CMN<cond> Rn, Rm OP Rs	cond	0	0	0	1	0	1	1	1	Rn	SBZ	Rs	0	shift	1	Rm																
MSR<cond> SPSPR <fields>, Rm	cond	0	0	0	1	0	1	1	0	field_mask	SBO	SBZ																				
ORR<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	1	1	0	0	1	S	Rn	Rd	shift #	0	shift	0	Rm															
ORR<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	1	1	0	0	1	S	Rn	Rd	Rs	0	shift	1	Rm															
MOV<cond><S> Rd, Rm OP #	cond	0	0	0	1	1	0	1	0	S	SBZ	Rd	shift #	0	shift	0	Rm															
MOV<cond><S> Rd, Rm OP Rs	cond	0	0	0	1	1	0	1	0	S	SBZ	Rd	Rs	0	shift	1	Rm															
BIC<cond><S> Rd, Rn, Rm OP #	cond	0	0	0	1	1	1	0	1	S	Rn	Rd	shift #	0	shift	0	Rm															
BIC<cond><S> Rd, Rn, Rm OP Rs	cond	0	0	0	1	1	1	0	1	S	Rn	Rd	Rs	0	shift	1	Rm															
MVN<cond><S> Rd, Rm OP #	cond	0	0	0	1	1	1	1	0	S	SBZ	Rd	shift #	0	shift	0	Rm															
MVN<cond><S> Rd, Rm OP Rs	cond	0	0	0	1	1	1	1	0	S	SBZ	Rd	Rs	0	shift	1	Rm															
AND<cond><S> Rd, Rn, #	cond	0	0	1	0	0	0	0	S	Rn	Rd	rotate																				
EOR<cond><S> Rd, Rn, #	cond	0	0	1	0	0	0	1	S	Rn	Rd	rotate																				
SUB<cond><S> Rd, Rn, #	cond	0	0	1	0	0	1	0	S	Rn	Rd	rotate																				
RSB<cond><S> Rd, Rn, #	cond	0	0	1	0	0	1	1	S	Rn	Rd	rotate																				
ADD<cond><S> Rd, Rn, #	cond	0	0	1	0	1	0	0	S	Rn	Rd	rotate																				
ADC<cond><S> Rd, Rn, #	cond	0	0	1	0	1	0	1	S	Rn	Rd	rotate																				
SBC<cond><S> Rd, Rn, #	cond	0	0	1	0	1	1	0	S	Rn	Rd	rotate																				
RSC<cond><S> Rd, Rn, #	cond	0	0	1	0	1	1	1	S	Rn	Rd	rotate																				
TST<cond> Rn, #	cond	0	0	1	1	0	0	0	1	Rn	SBZ	rotate																				
TEQ<cond> Rn, #	cond	0	0	1	1	0	0	1	1	Rn	SBZ	rotate																				
MSR<cond> CPSR f, #	cond	0	0	1	1	0	0	1	0	field_mask	SBO	rotate																				
CMP<cond> Rn, #	cond	0	0	1	1	0	1	0	1	Rn	SBZ	rotate																				
CMN<cond> Rn, #	cond	0	0	1	1	0	1	1	1	Rn	SBZ	rotate																				
MSR<cond> SPSPR f, #	cond	0	0	1	1	0	1	1	0	field_mask	SBO	rotate																				
ORR<cond><S> Rd, Rn, #	cond	0	0	1	1	1	0	0	1	S	Rn	Rd	rotate																			
MOV<cond><S> Rd, #	cond	0	0	1	1	1	0	1																								

Data Processing Opcode	Flag	Description
Load/Store Opcode	Z	Zero Flag
Branching Opcode	C	Carry Flag
Multiplication Opcode	N	Negative Flag
Other Opcodes	V	Overflow Flag
CoProcessor Opcodes		

rE Ejected
ARM Reference
<http://www.agbdev.net/re-eject/>

STR<<cond> Rd, Rn, #	cond	0	1	0	P	U	0	W	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond> Rd, Rn, #	cond	0	1	1	P	U	0	W	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond>B Rd, Rn, #	cond	0	1	0	P	U	1	W	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond>B Rd, Rn, #	cond	0	1	1	P	U	1	W	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond>BT Rd, Rn, #	cond	0	1	0	0	U	1	1	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond>BT Rd, Rn, #	cond	0	1	1	0	U	1	1	0	Rn	Rd	shift #	shift	0	Rm			
STR<<cond>H Rd, <address>	cond	0	0	0	0	P	U	1	W	0	Rn	Rd	adrr mode	1	0	1	1	adrr mode