Video Electronics Standards Association

19-inch Wide Standard Panel

860 Hillview Court, Suite 150
Milpitas, CA 95035

Phone: 408-957-9270
Fax: 408-957-9277

Proposed VESA Monitor Standard Panel

19-inch Wide

Version 1

December 4, 2007

Purpose

This specification defines the requirements to standardize the mechanical dimensions and selected electrical interface elements of 19-inch wide format panels intended for use as LCD monitors.

This standard will help LCD manufacturers and panel consumers to better control panel supply and demand cycles.

The intent of this standard is that panels built to this specification are interchangeable without requiring alterations to tooling or drive electronics.

Summary

This proposal describes the mechanical dimensions, electrical interfaces and data formatting for 19.0-inch wide monitor panels.

Table of Contents

Tables

Figures

Preface

Intellectual Property

While every precaution has been taken in the preparation of this standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

Trademarks

All trademarks used within this document are the property of their respective owners. VESA is a registered trademark of the Video Electronics Standards Association.

Patents

VESA draws attention to the fact that it is claimed that compliance with this specification may involve the use of a patent or other intellectual property right (collectively, "*IPR*") concerning items in this proposal. VESA takes no position concerning the evidence, validity, and scope of this *IPR.*

The following holders of this *IPR* have assured VESA that they are willing to license the *IPR* on *RAND* terms. The statement of the holder of this *IPR* is registered with VESA.

Holder Name	Contact Information	Claims Known
JAE	Mark Saubert (saubertm@jae.com)	EXHIBIT C-1 OF JAE ELECTRONICS, INC. (aka JAPAN AVIATION ELECTRONICS INDUSTRIES, LTD) IDENTIFICATION OF NECESSARY CLAIM Issued United States Patents: Please note that the identification of claims for the issued patents is limited to the independent claims. JAE has not attempted to identify each and every dependent claim that may also be considered a necessary claim. 6,315,616 claims 8, 9, and 11 Pending United States Patent Applications: The below identified patent applications (and others) may result in patents issuing that include necessary claims: 10/287,925 Note 1: JAE also has (or will have) foreign patents and/or patent applications corresponding to each of the identified patents and patent applications.

Attention is drawn to the possibility that some of the elements of this VESA Specification may be the subject of *IPR* other than those identified above. VESA shall not be held responsible for identifying any or all such *IPR*, and has made no inquiry into the possible existence of any such *IPR*.

THIS SPECIFICATION IS BEING OFFERED WITHOUT ANY WARRANTY WHATSOEVER, AND IN PARTICULAR, ANY WARRANTY OF NON-INFRINGEMENT IS EXPRESSLY DISCLAIMED. ANY IMPLEMENTATION OF THIS SPECIFICATION SHALL BE MADE ENTIRELY AT THE IMPLEMENTER'S OWN RISK, AND NEITHER VESA, NOR ANY OF ITS MEMBERS OR SUBMITTERS, SHALL HAVE ANY LIABILITY WHATSOEVER TO ANY IMPLEMENTER OR THIRD PARTY FOR ANY DAMAGES OF ANY NATURE WHATSOEVER DIRECTLY OR INDIRECTLY ARISING FROM THE IMPLEMENTATION OF THIS SPECIFICATION.

Support

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates 19-inch Wide Standard Panel, ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. Submit all comments or reported errors in writing to VESA using one of the following methods.

- Fax 408- 957- 9277, *direct this fax to Technical Support at VESA*
- E-mail support@vesa.org
- Mail Technical Support
  Video Electronics Standards Association
  860 Hillview Court, Suite 150
  Milpitas, CA 95035

Acknowledgements

This document would not have been possible without the efforts of the VESA Display Device Standards Committee's Monitor Task Group. In particular, the following individuals and their companies contributed significant time and knowledge.

Main Contributors

Name	Company	Contribution
Joe Goodart	Dell	Task Group Chair
Jeff Frankel	Genesis Microchip	Task Group Vice-chair
Louis Liu	Hannstar	
David Braun	Hewlett-Packard	
Karl Kwiat	Hirose	
Toshio Shimoyama	JAE	
Brian Kim	LG.Philips LCD	
H.J. So	LG.Philips LCD	
Brian Berkeley	Samsung	
Mark Son	Samsung	
Doron Lapidot	Tyco Electronics	
Alain d'Hautecourt	ViewSonic	

Revision History

Dec. 4, 2007 Initial release of the standard

1. OVERVIEW

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for industry compatible panels sized 19.0W for notebook and similar applications.

1.2 Standard Objectives

This document establishes common panels for the 19-inch wide display sizes so that a standard panel can be mounted in any notebook case designed to accept the maximum defined size. The dimensioning allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms.

1.3 Reference Documents

The following documents forms a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the correct versions of these referenced standards:

Table 1-1: Reference Documents

Document	Version/Revision	Date
VESA Policy 200B Intellectual Property Rights	Version B	Feb. 2005
VESA Glossary of Terms (www.vesa.org)	Current	
VESA Enhanced Display Data Channel Standard (E-DDC)	Version 1.1	March 24, 2004
ANSI/TIA/EIA-644-A-2001, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits	Version A	Feb 1, 2001

2. System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: a LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 16:10 image format and square pixels (e.g. 1280 x 800). Figure 2-1 shows the pixel formatting for the active display surface.

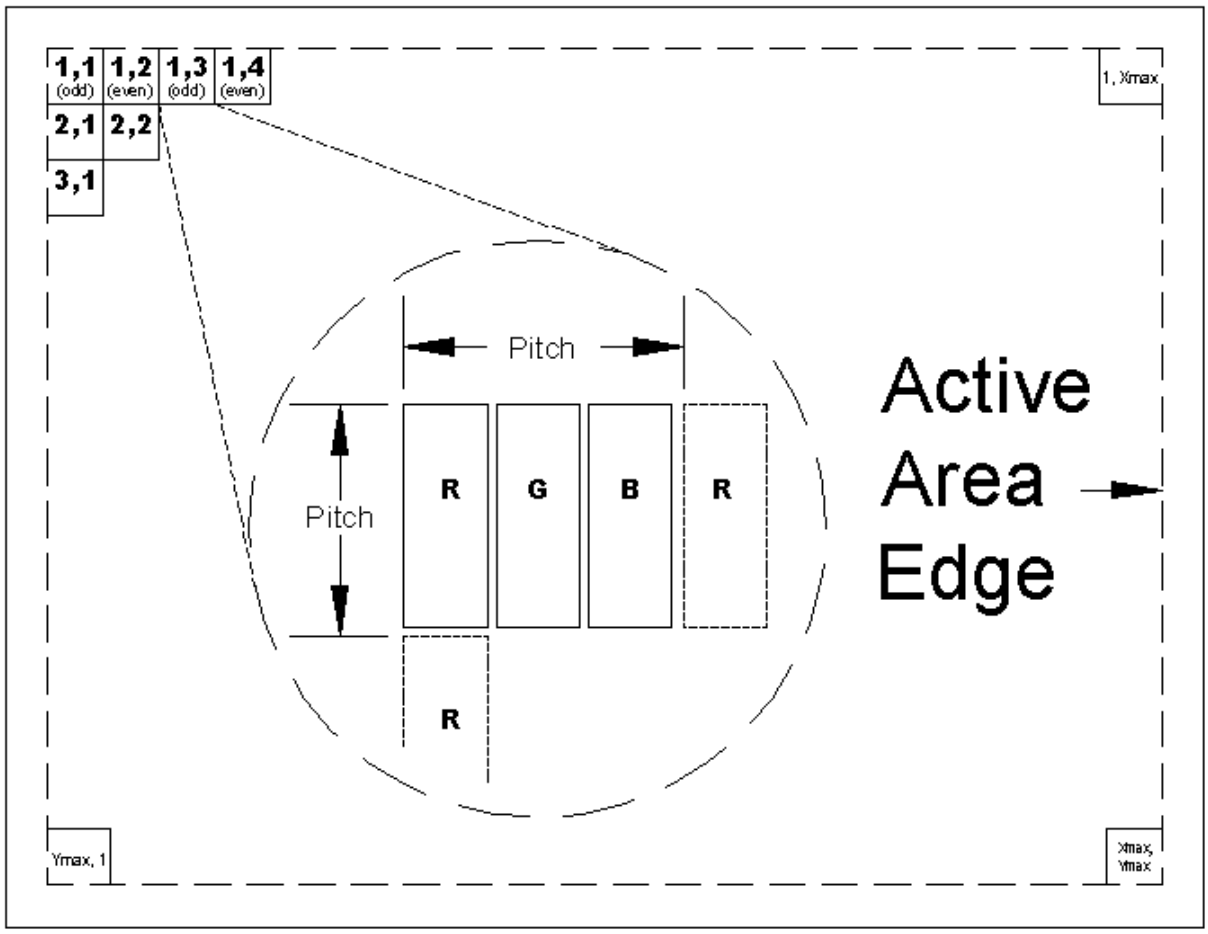


Figure 2-1: Active Area Pixel Layout

2.1 LVDS Interfaced

2.1.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area shall be designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector keying relative to pin-one designation shall be as shown on Figure 2-7. Connector location shall be as shown on Figure 2-8.

2.1.2 LVDS Interface Signal Definition

The panel LVDS signal interface shall be terminated to a JAE FI-XB30SSRL-HF16 or equivalent connector. The interface connector pin assignments are listed in Table 2-1.

Table 2-1: LVDS Interface Cable Pin Assignments

Pin No.	Symbol	Function	
1	FR0M	Minus signal of odd channel 0 (LVDS)	First Data
2	FR0P	Plus signal of odd channel 0 (LVDS)	
3	FR1M	Minus signal of odd channel 1 (LVDS)	
4	FR1P	Plus signal of odd channel 1 (LVDS)	
5	FR2M	Minus signal of odd channel 2 (LVDS)	
6	FR2P	Plus signal of odd channel 2 (LVDS)	
7	GND	Ground	
8	FCLKINM	Minus signal of odd clock channel (LVDS)	
9	FCLKINP	Plus signal of odd clock channel (LVDS)	
10	FR3M	Minus signal of odd channel 3 (LVDS)	
11	FR3P	Plus signal of odd channel 3 (LVDS)	
12	SR0M	Minus signal of even channel 0 (LVDS)	Second Data
13	SR0P	Plus signal of even channel 0 (LVDS)	
14	GND	Ground	
15	SR1M	Minus signal of even channel 1 (LVDS)	
16	SR1P	Plus signal of even channel 1 (LVDS)	
17	GND	Ground	
18	SR2M	Minus signal of even channel 2 (LVDS)	
19	SR2P	Plus signal of even channel 2 (LVDS)	
20	SCLKINM	Minus signal of even clock channel (LVDS)	
21	SCLKINP	Plus signal of even clock channel (LVDS)	
22	SR3M	Minus signal of even channel 3 (LVDS)	
23	SR3P	Plus signal of even channel 3 (LVDS)	
24	GND	Ground	
25	NC	No Connection	
26	NC	No Connection	
27	NC	No Connection	
28	VLCD	Power Supply +5.0V	
29	VLCD	Power Supply +5.0V	
30	VLCD	Power Supply +5.0V	

2.1.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data/control signal sequencing of Figure 2-2 and 2-3.

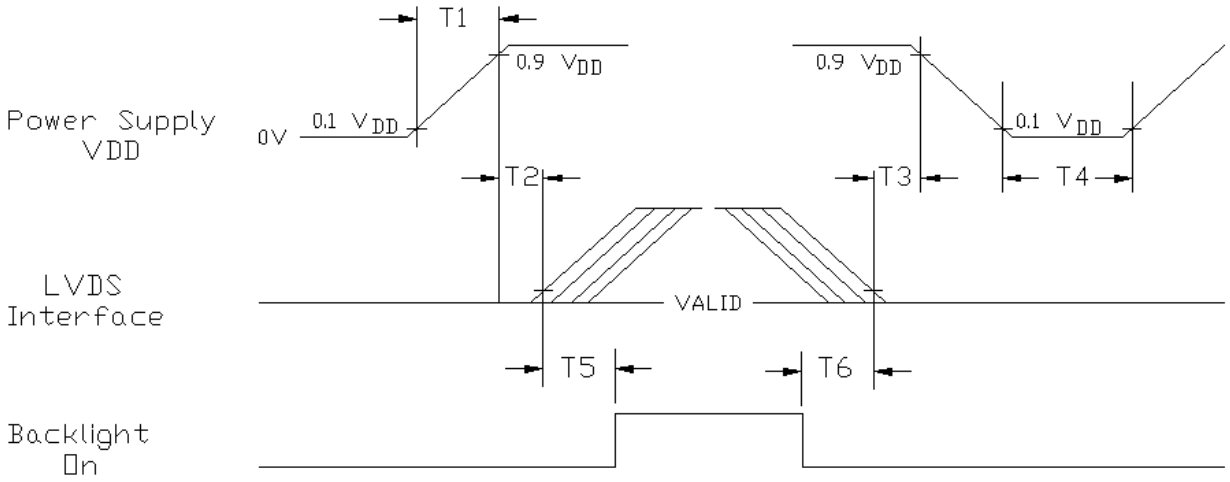


Figure 2-2: Logic Power and LVDS Signals Sequencing Diagram

0.5 ms < T1 < 10 ms 0 < t2 < 50 ms 0 < t3 < 50 ms 1000 ms < T4 500 ms < T5 200 ms < T6

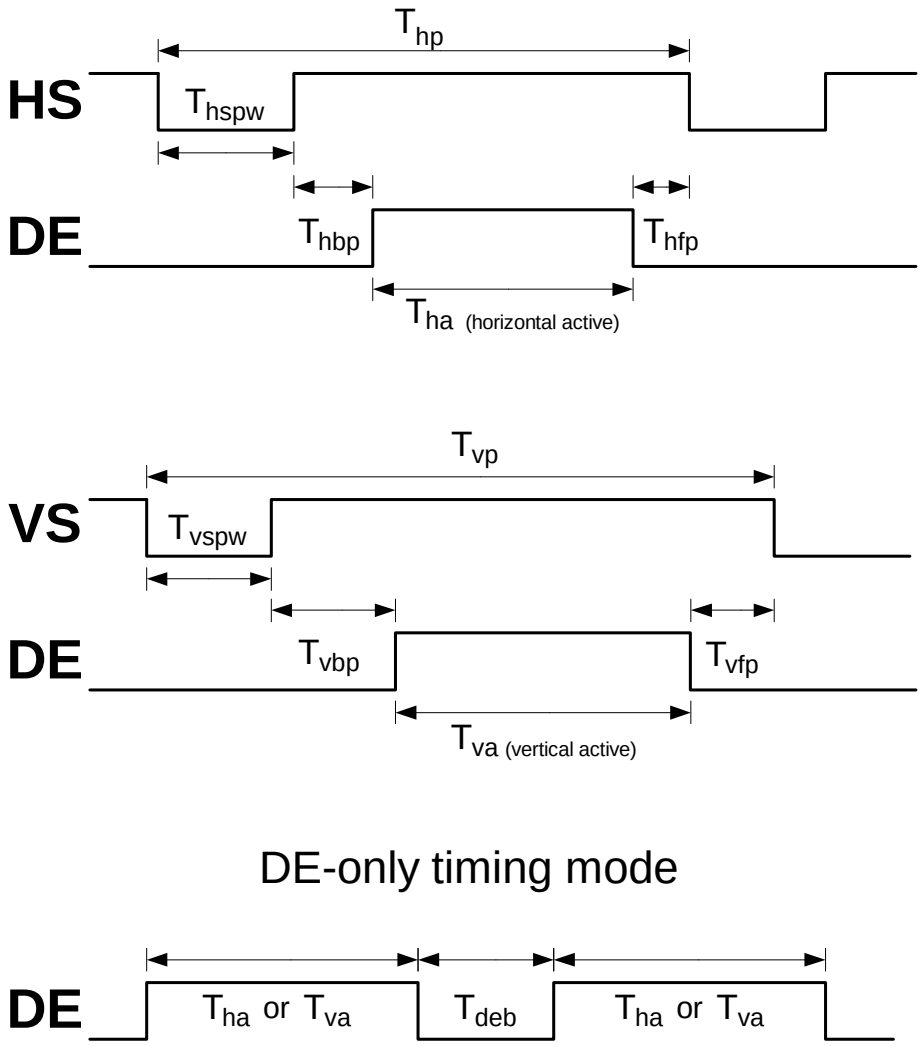


Figure 2-3: Data Enable Timing Parameters

2.1.4 LVDS Data and Control Signal Interface

The modules LVDS signals interface shall meet requirements of ANSI/TIA/EIA-644. Figure 2-4, Figure 2-5 and Figure 2-6 show the data mapping diagram of each LVDS channel. The LVDS differential signals line-to-line termination impedance, Z_T, shall be 100 ±10 ohms.

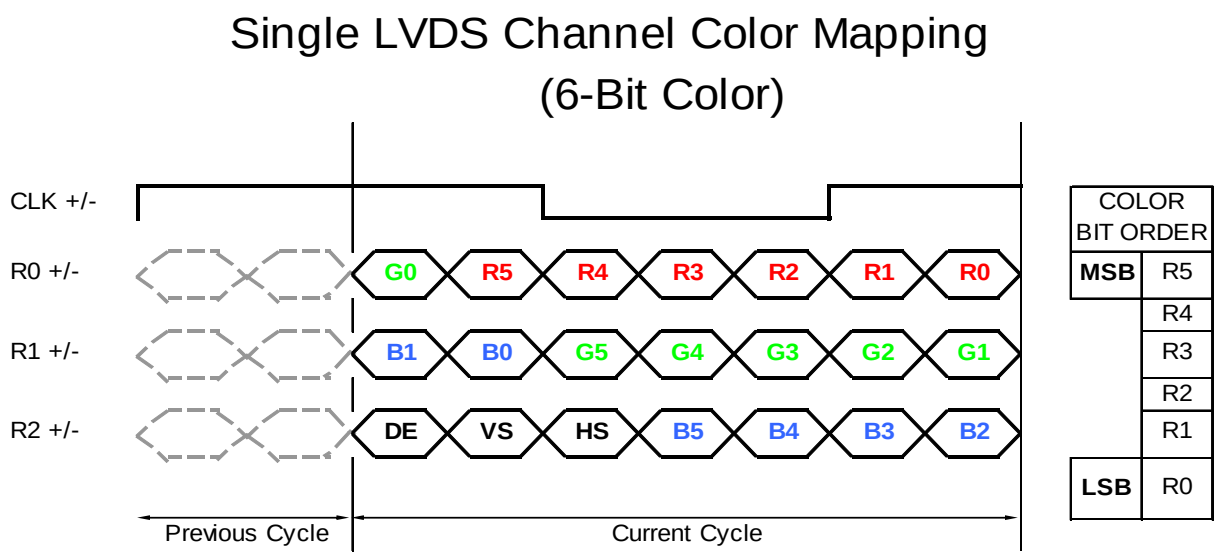


Figure 2-4: Single LVDS Channel Interface Data Mapping Diagram (6 Bit Color)

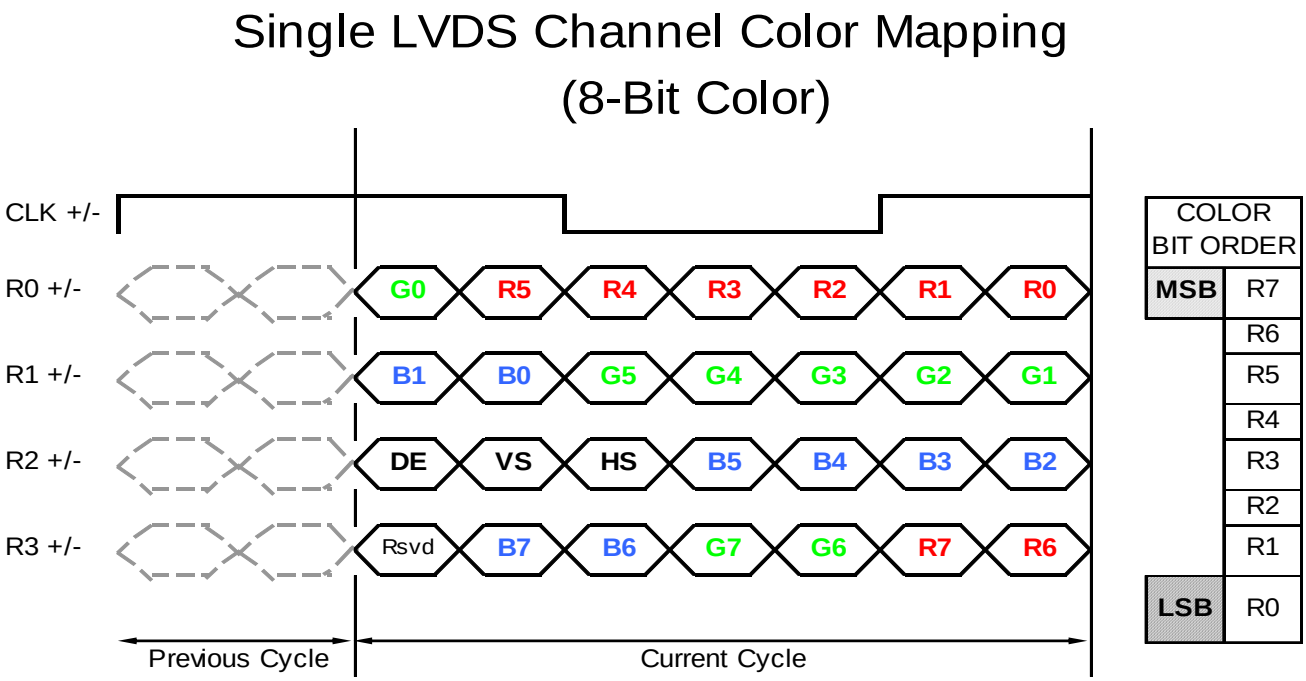
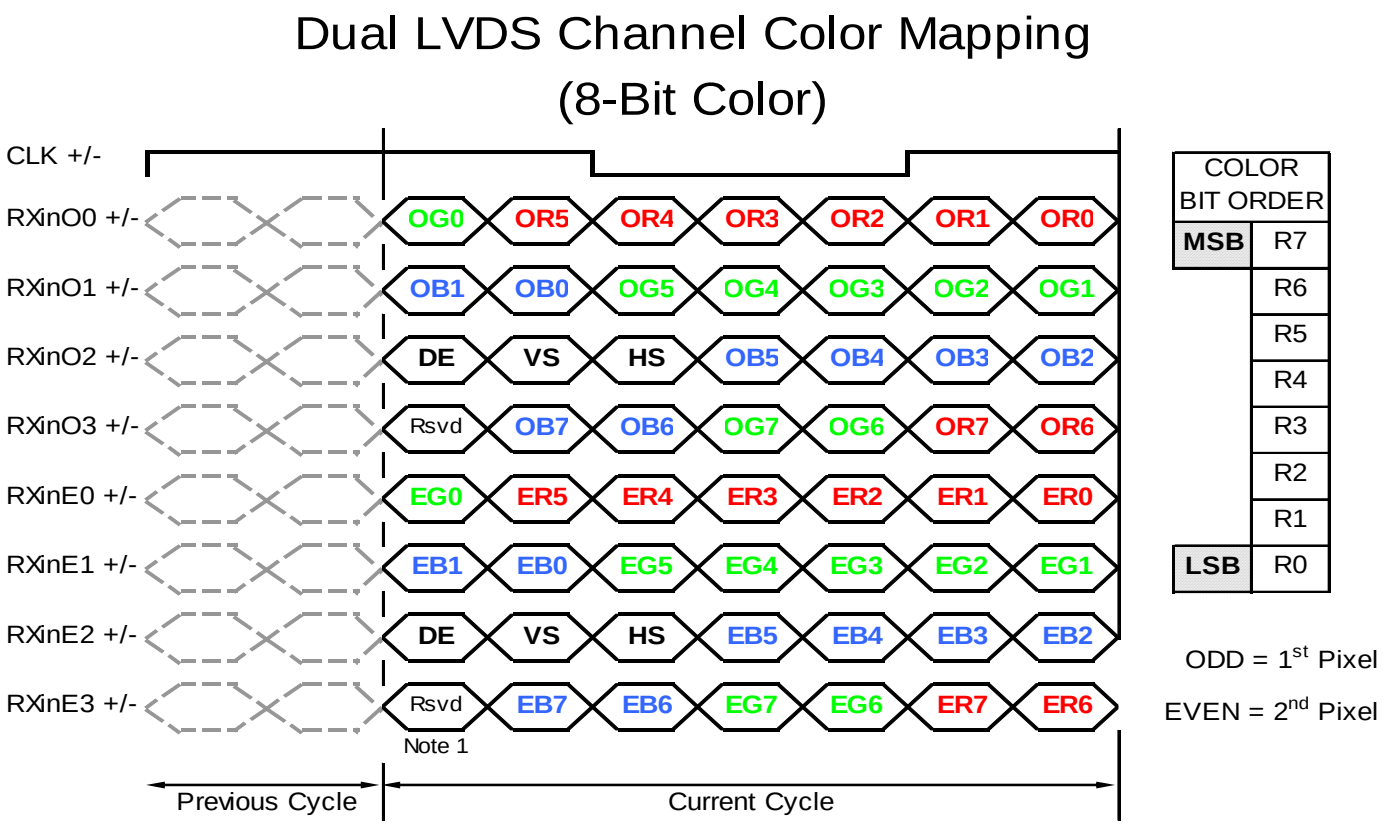


Figure 2-5: Single LVDS Channel Interface Data Mapping Diagram (8 Bit Color)



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Figure 2-6: Dual LVDS Channel Interface Data Mapping Diagram (8 Bit Color)

2.1.5 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into a Yeonho 35001HS-02LD or equivalent connector. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 2-2.

Table 2-2: Backlight Electrical Interface

Pin No.	Signal	Level	Function
1	V_{CCFL}	AC	Power Supply for CCFL
2	Gnd Rtn	Ground	Power Return for CCFL

2.1.6 Mechanical Interface Requirements

Figure 2-7 shows the critical exterior dimensions; Figure 2-8 show the locations of connectors.

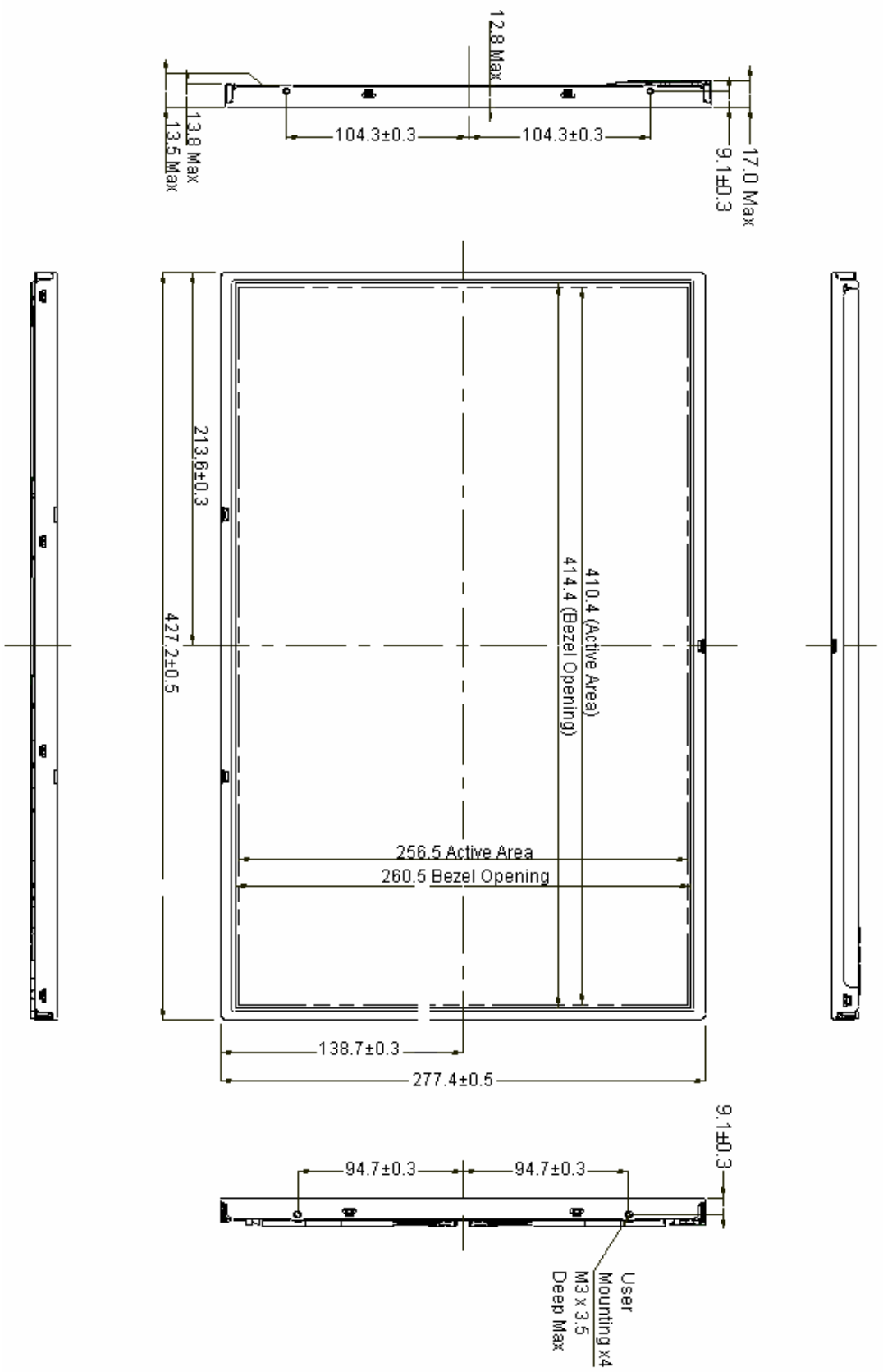
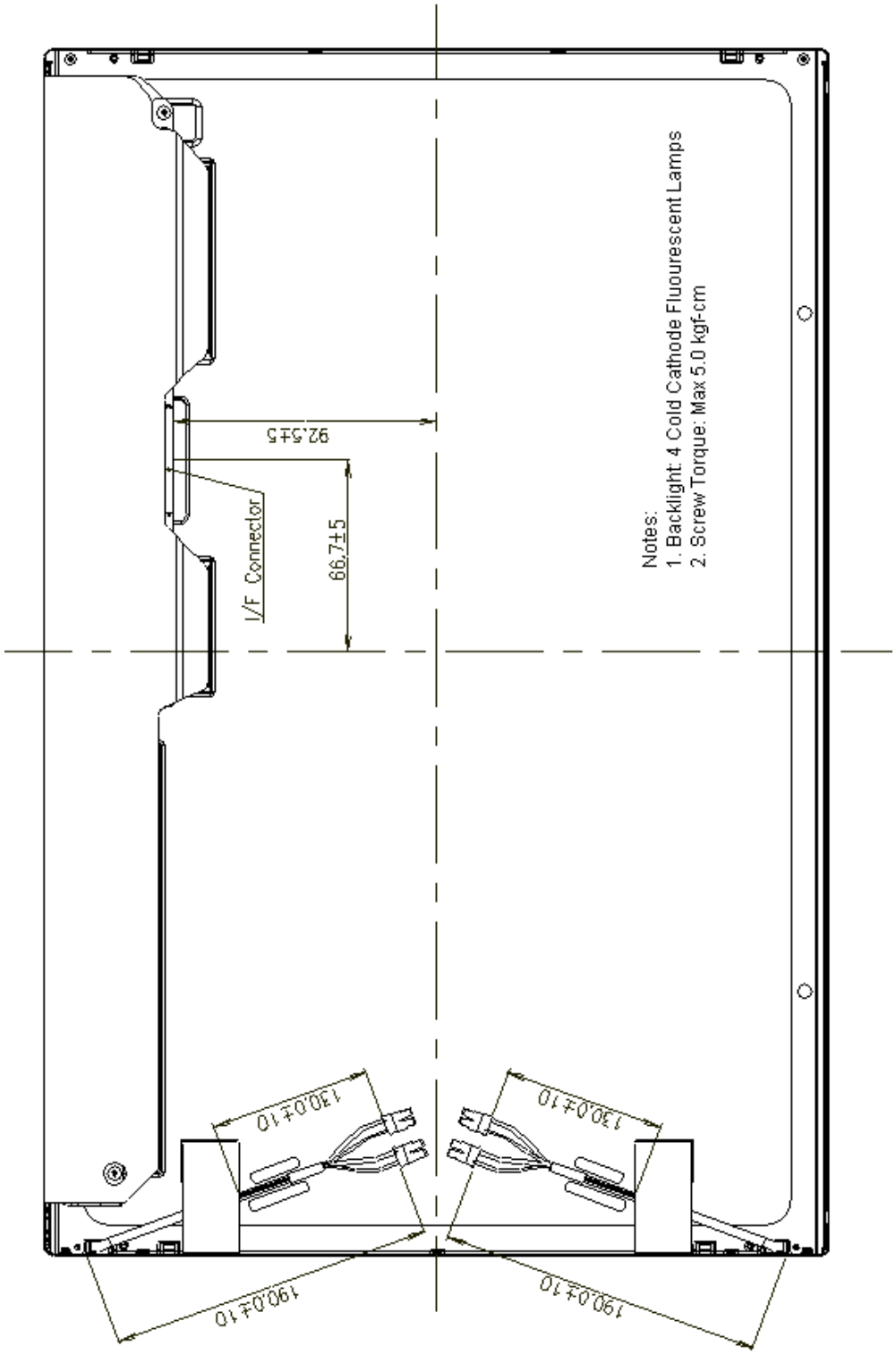


Figure 2-7: Mechanical Dimensions - Panel A

Note: All



dimensions in mm.

Figure 2-8: Connector Location - Panel A

Note: All dimensions in mm.

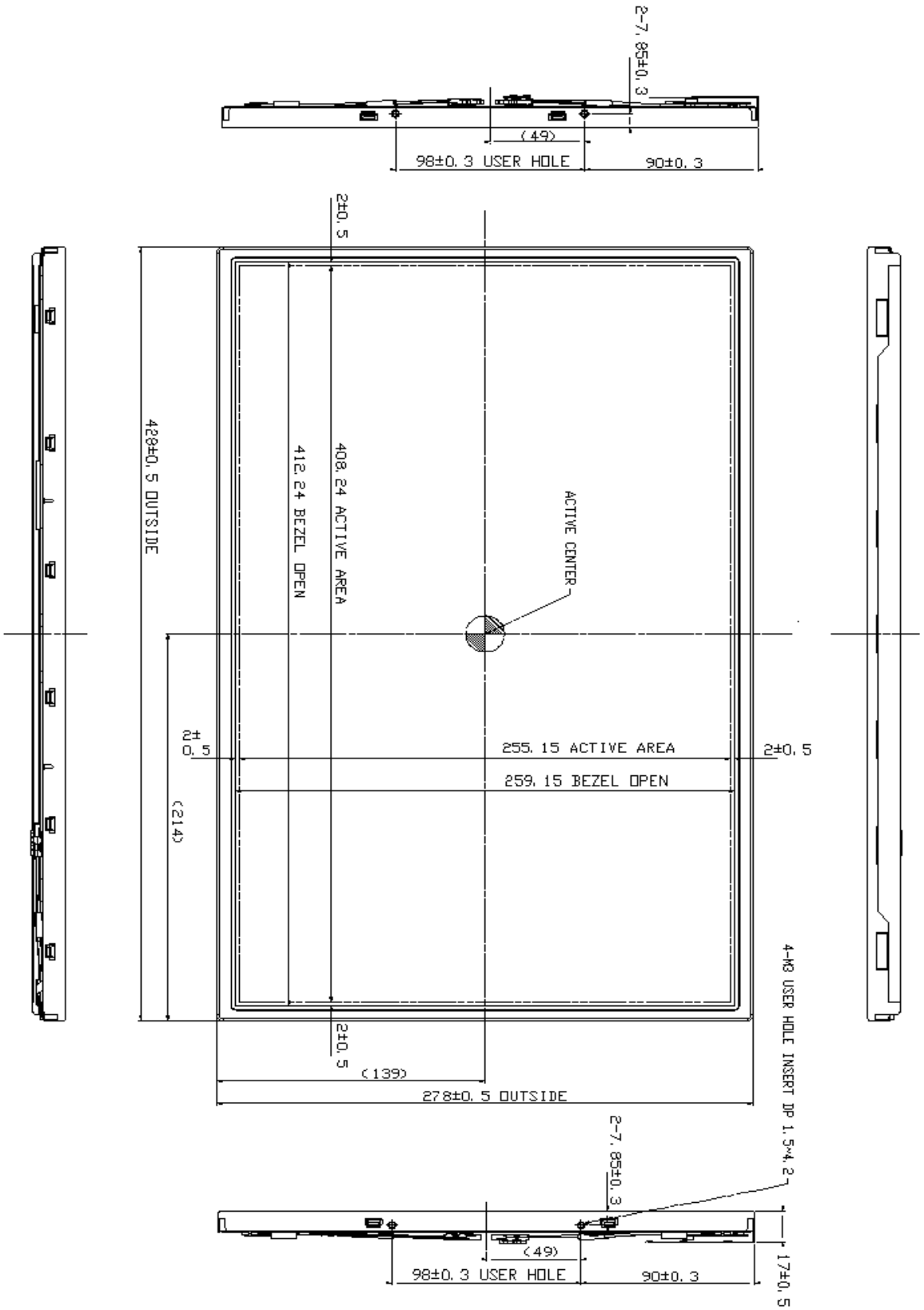


Figure 2-9: Mechanical Dimensions - Panel B

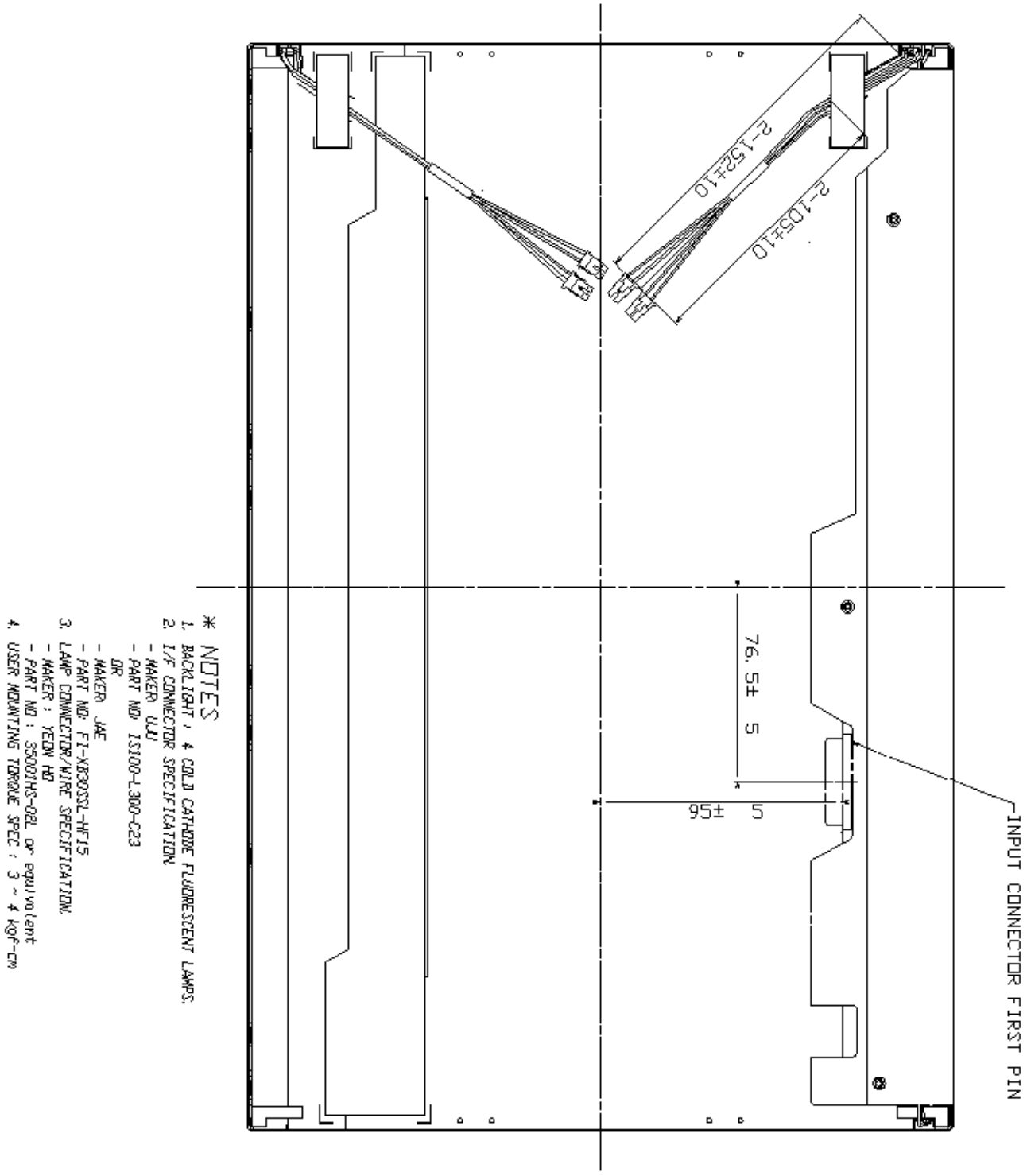


Figure 2-10: Connector Location - Panel B

3. Glossary of Terms

Abbreviation	Explanation
CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
LVDS	Low Voltage Differential Signaling
TDEB	Time – Display Enable Blanking
THA	Time – Horizontal Active
THBP	Time – Horizontal Back Porch
THFP	Time – Horizontal Front Porch
THP	Time – Horizontal Period
THSPW	Time – Horizontal Sync Pulse Width
TVA	Time – Vertical Active
TVBP	Time – Vertical Back Porch
TVFP	Time – Vertical Front Porch
TVSPW	Time – Vertical Sync Pulse Width
VCCFL	Voltage for CCFL
VS	Vertical Sync