Video Electronics Standards Association

24-inch Wide Panel Standard (12-volt)

860 Hillview Court, Suite 150
Milpitas, California 95035

Phone: 408-957-9270
Fax: 408-957-9277
www.vesa.org

VESA 24-inch Wide Panel Standard (12-volt)

Version 1
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Purpose

This specification defines the requirements to standardize the mechanical dimensions and selected electrical interface elements of 24-inch wide format panels intended for use as LCD monitors. This panel is designed to operate from a 12-volt source.

This standard will help LCD manufacturers and panel consumers to better control panel supply and demand cycles.

The intent of this standard is that panels built to this specification are interchangeable without requiring alterations to tooling or drive electronics.

Summary

This proposal describes the mechanical dimensions, electrical interfaces and data formatting for 24-inch wide monitor panels.

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Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Table 1 - Reference Documents

Source	Name	Version / Date
TIA/EIA-644	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	March 1, 1996

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

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mail: Technical Support
Video Electronics Standards Association
860 Hillview Court, Suite 150
Milpitas, CA 95035

Acknowledgements

This document would not have been possible without the efforts of the VESA Display Device Standards Committee's Monitor Panel Standards Task Group. In particular, the following individuals and their companies contributed significant time and knowledge to this version of the standard.

Table 2 - Acknowledgements

Name	Company Name	Contribution
Ted Wang	AU Optronics, Inc.	
Emily Hwei	Chi Mei Optoelectronics	
Anny Yuan	Chi Mei Optoelectronics	
C.J. Lin	Chi Mei Optoelectronics	
Alex Wong	Chunghwa Picture Tubes	
Ryan Huang	Chunghwa Picture Tubes	
Ronald Chung	Chunghwa Picture Tubes	
Billy Leong	Dell	
Thomas Chung	Dell	
Sim Tiak Hooy	Dell	
Joe Goodart	Dell	Task Group Chair
Jeff Frankel	Genesis Microchip	Task Group Secretary & Editor
David Braun	Hewlett-Packard	
Karl Kwiat	Hirose Electronics	
Sue Wood	JAE	
Hunter Ryu	LG.Philips LCD	
Ian Miller	Samsung	
Moo-Kyung (Mark) Son	Samsung	
Pablo Temprano	Samsung	
Alain d'Hautecourt	ViewSonic	

Revision History - Initial Release of the Standard, May 1, 2006

1 Overview

1.1 Summary

This document defines the electrical interface requirements and mechanical dimensions for industry compatible 24-inch wide LCD panels.

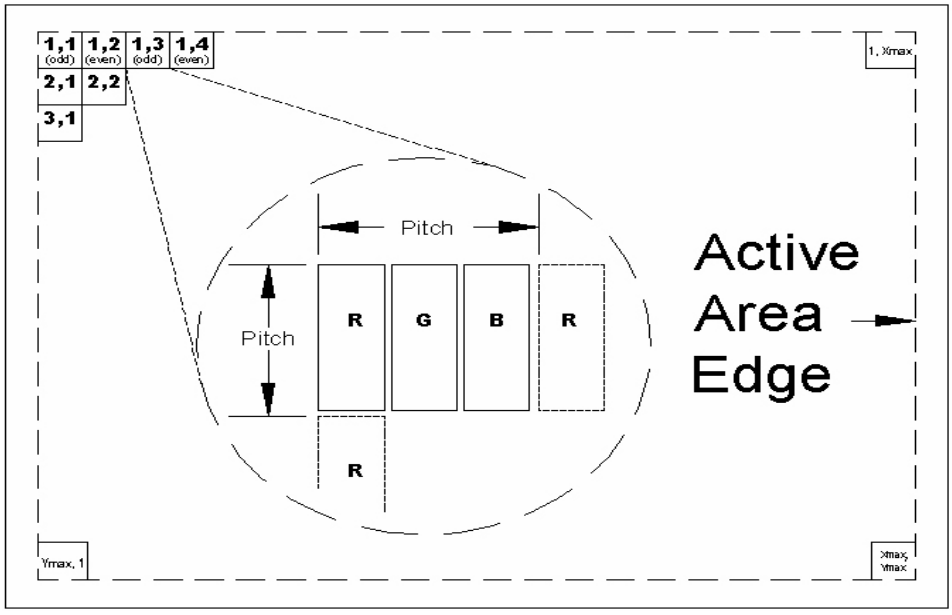
1.2 Standard Objectives

This document establishes a common specification for 24-inch wide monitor LCD panels with the intent of creating standardization among these panels such that panels meeting this specification are interchangeable with respect to mechanical fit, electrical requirements, signal definitions and data formats.

2 System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: an LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 16:10 image format supporting a pixel format of 1,920 pixels horizontally by 1,200 pixels vertically.

Figure 1 – Active Area Pixel Layout



2.1 LVDS Interface

2.1.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area is designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector

orientation relative to pin-one designation shall be as shown in Figure 8 – 24-inch Standard Panel Mechanical Dimensions.

2.1.2 LVDS Interface Signal Definition

The LVDS signal interface cable shall be terminated to a FI-X30SSL-HF or equivalent connector. This connector is a locking type. The interface connector pin assignments are listed below.

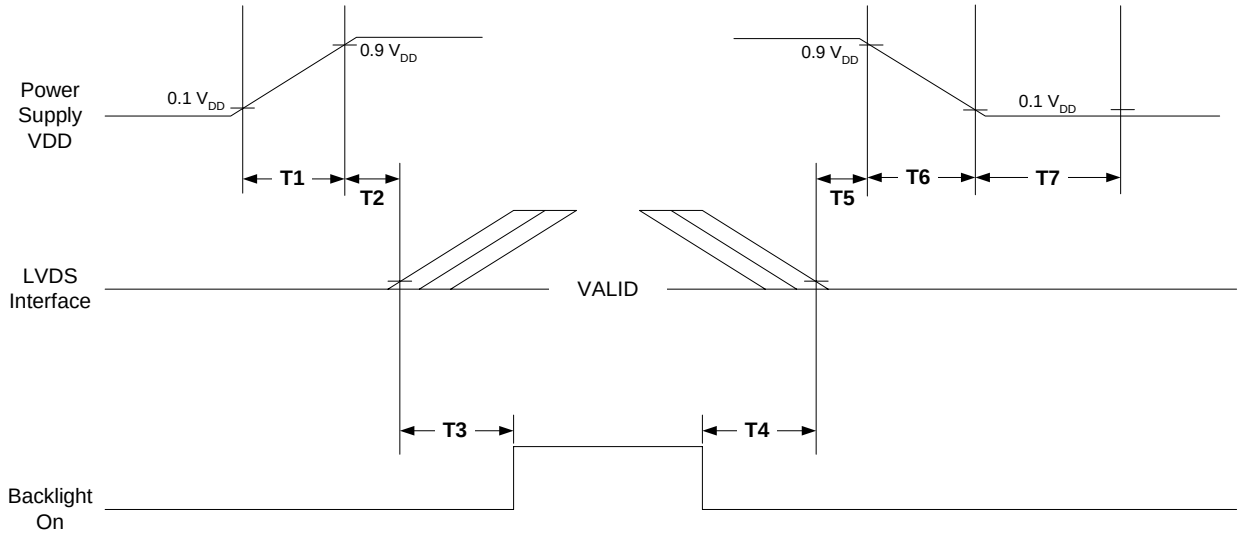
Table 3 – LVDS Connector Pin Assignments

Pin No.	Symbol	Function
Frame		Ground
1	RxO0-	- LVDS differential data input, Chan 0-Odd
2	RxO0+	+ LVDS differential data input, Chan 0-Odd
3	RxO1-	- LVDS differential data input, Chan 1-Odd
4	RxO1+	+ LVDS differential data input, Chan 1-Odd
5	RxO2-	- LVDS differential data input, Chan 2-Odd
6	RxO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RxOC-	- LVDS Differential Clock input (Odd)
9	RxOC+	+ LVDS Differential Clock input (Odd)
10	RxO3-	- LVDS differential data input, Chan 3-Odd
11	RxO3+	+ LVDS differential data input, Chan 3-Odd
12	RxE0-	- LVDS differential data input, Chan 0-Even
13	RxE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RxE1-	- LVDS differential data input, Chan 1-Even
16	RxE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RxE2-	- LVDS differential data input, Chan 2-Even
19	RxE2+	+ LVDS differential data input, Chan 2-Even
20	RxEC-	- LVDS Differential Clock input (Even)
21	RxEC+	+ LVDS Differential Clock input (Even)
22	RxE3-	- LVDS differential data input, Chan 3-Even
23	RxE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	NC	No Connection
26	NC	No Connection
27	NC	No Connection
28	Vcc	+ 12 Volts
29	Vcc	+ 12 Volts
30	Vcc	+ 12 Volts
Frame		Ground

2.1.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data/control signal sequencing of Figures 2, 3 and 4.

Figure 2 - Logic Power and LVDS Signals Sequencing Diagram



	Minimum time (ms)	Maximum time (ms)
T1	0.5	10
T2	0.0	50
T3	1000	-
T4	200	-
T5	0.0	50
T6	0.01	10
T7	1000	-

Figure 3 – Data Enable Timing

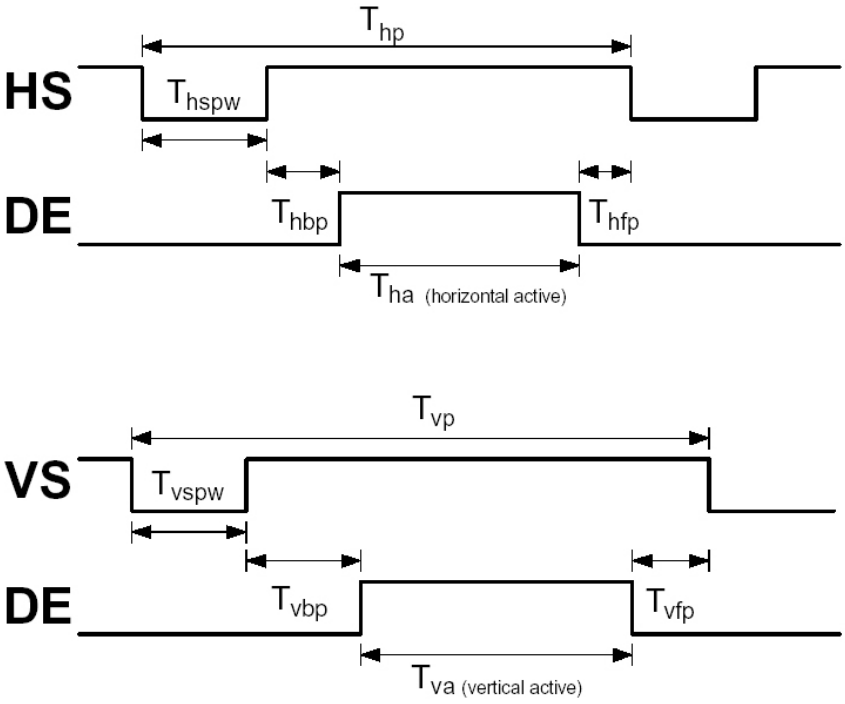
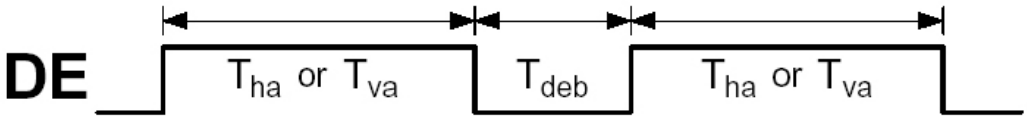


Figure 4 – DE Only Timing Mode



2.1.4 LVDS Data and Control Signal Interface

The module's LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 5 shows the data mapping diagram of each LVDS channel when 8-bit color is used, Figure 6 shows the data mapping diagram of each LVDS channel when 6-bit color is used. The LVDS differential signals line-to-line termination impedance, ZT, shall be 100 ± 10 ohms.

Figure 5 – Dual LVDS Channel Color Mapping (8-bit)

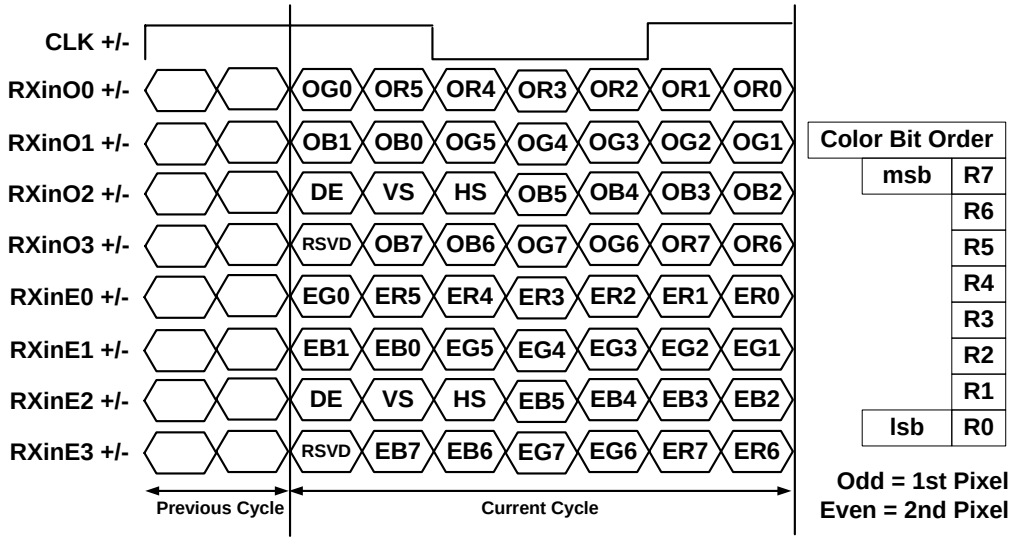
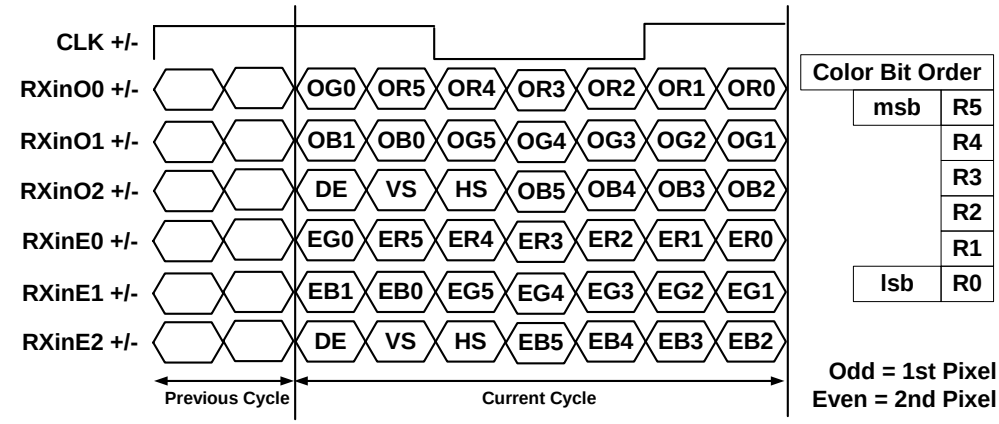


Figure 6 – Dual LVDS Channel Color Mapping (6-bit)



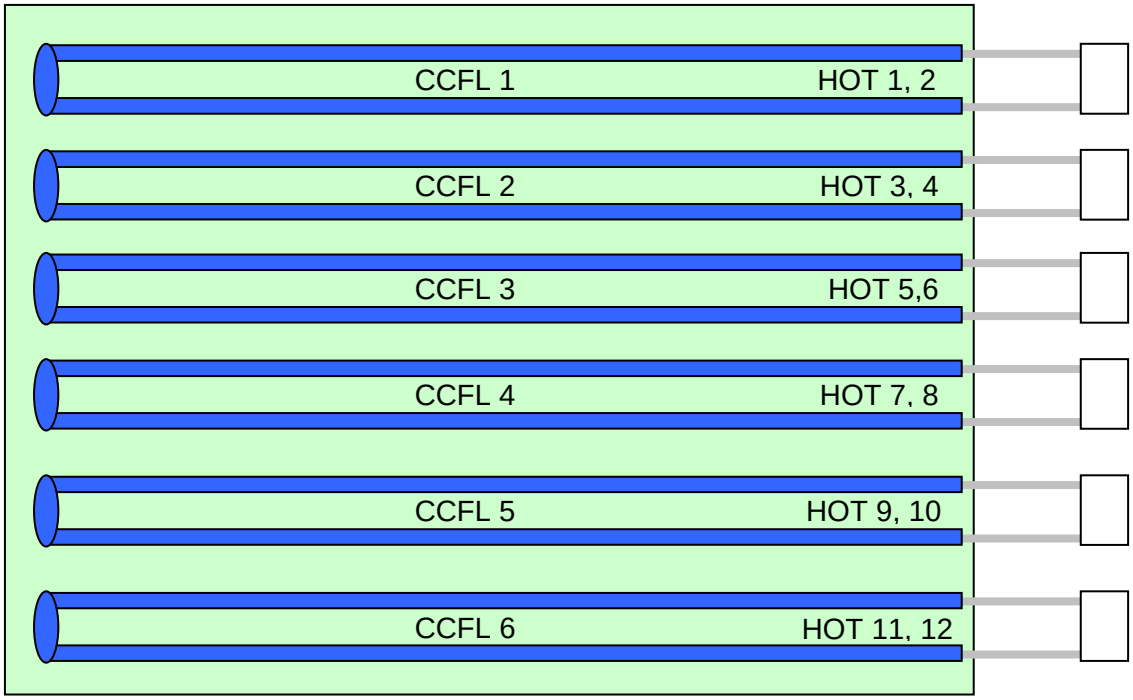
2.2 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into JST BHR-04VS-1 or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in the table below.

Table 4 - Backlight Connector

Connector	Pin No	Function
1	1	High Voltage
	2	High Voltage
2	3	High Voltage
	4	High Voltage
3	5	High Voltage
	6	High Voltage
4	7	High Voltage
	8	High Voltage
5	9	High Voltage
	10	High Voltage
6	11	High Voltage
	12	High Voltage

Figure 7 – Lamp Connector Configuration



3 Mechanical Interface Requirements

Figure 6 shows the critical exterior dimensions and connector location.

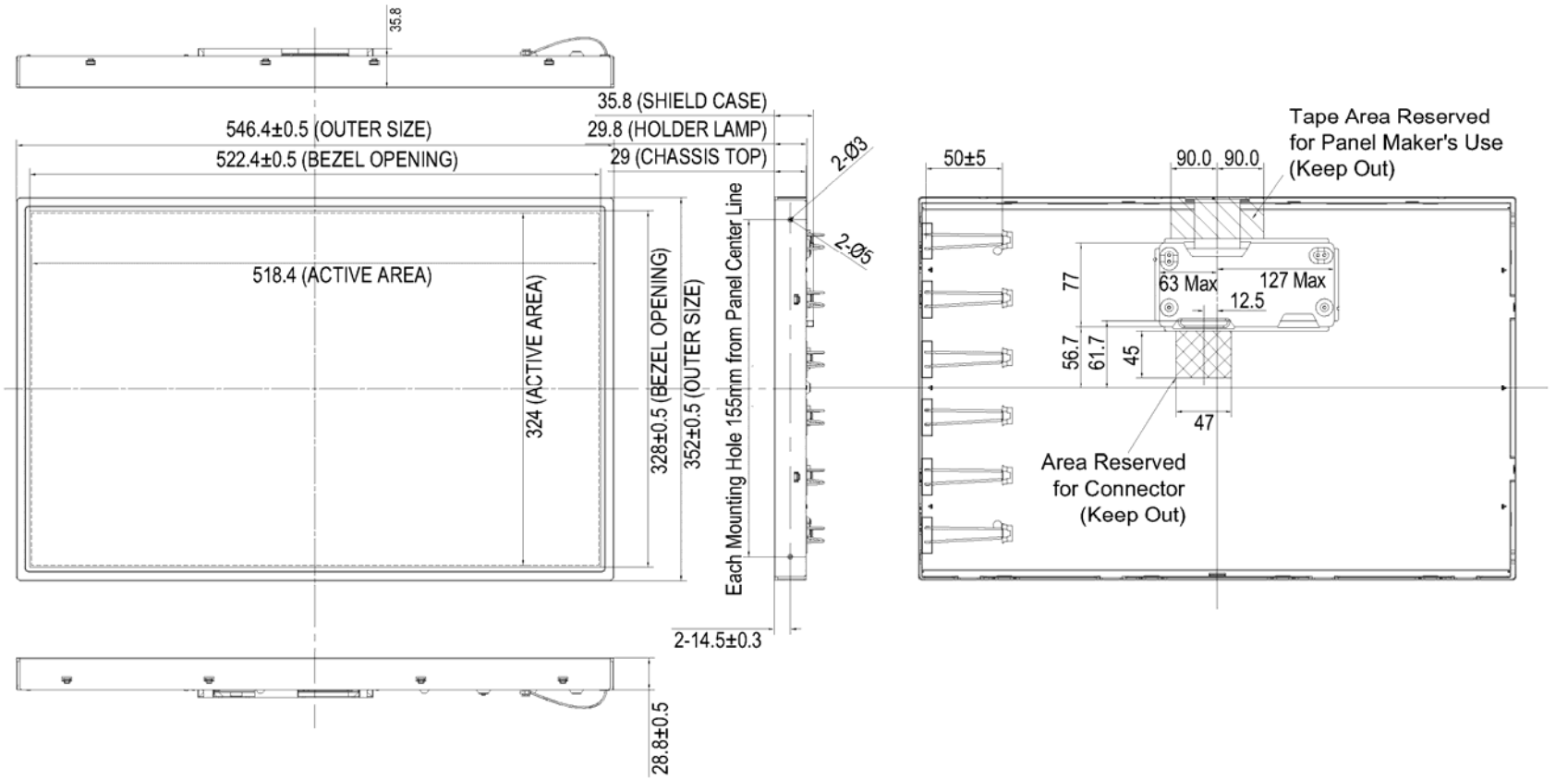


Figure 8 – 24-inch Standard Panel Mechanical Dimensions

4 Drawing Notes

NOTE:
1. BACKLIGHT: 6 COLD CATHODE FLUORESCENT LAMPS.
2. LAMP WIRE SPEC.
   - HOT 1: UL3239 AWG24 DC6kV, C1.74
   - HOT 2: UL3239 AWG24 DC6kV, C1.74
3. CONNECTOR SPEC.
   A) CCFL LAMP CONNECTOR
      - MAKER: JST OR EQUIVALENT
      - PART NO.: JST BHR-04VS-1 OR EQUIVALENT
   B) DATA CONNECTOR
      - MAKER: JAE
      - PART NO.: FI-XB30SSL-HF15 OR EQUIVALENT
4. UNSPECIFIED TOLERANCE TO BE %%P1.0
5. ALLOWED DEPTH OF SCREW INSERTION IN MOUNTING HOLES IS 5.0mm MAX
6. WEIGHT: Max 3.5kg
7. SCREW TORQUE SPEC.
   M2.6: MIN 3 kgfcm (5 TIMES)
   M3.0: MIN 7 kgfcm (5 TIMES)

Glossary of Terms

Abbreviation	Meaning
CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
lsb	Least Significant Bit
LVDS	Low Voltage Differential Signaling: TIA/EIA-644
msb	Most Significant Bit
NC	No Connection
T_{deb}	Time - Display Enable Blanking
T_{ha}	Time - Horizontal Active
T_{hbp}	Time - Horizontal Back Porch
T_{hfp}	Time - Horizontal Front Porch
T_{hp}	Time - Total Horizontal Period
T_{hspw}	Time - Horizontal Sync Pulse Width
T_{va}	Time - Vertical Active
T_{vbp}	Time - Vertical Back Porch
T_{vfp}	Time - Vertical Front Porch
T_{vp}	Time - Total Vertical Period
T_{vspw}	Time - Vertical Sync Pulse Width
VBR	Backlight Brightness
VIN	Backlight Power
VON/OFF	Backlight On / Off
VS	Vertical Sync