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VESA 20.1-inch Wide Monitor Panel Standard (12-volt Panels)

**Version 1
November 29, 2005**

Purpose

This document will define requirements for the standardization of mechanical dimensions and selected electrical interface requirements of 20.1-inch wide format panels intended for use as LCD monitors. This panel is designed to operate from a 12-volt source. This standard should help LCD manufacturers and panel consumers to better control panel supply and demand cycles. The intent is that panels built to this specification will be able to be used interchangeably without requiring alterations in product tooling or the display module.

Summary

This standard describes the mechanical dimensions, electrical interfaces and data formatting for 20.1-inch wide monitor panels.

Table of Contents

PREFACE

<i>Intellectual Property Statement</i>	3
<i>Trademarks</i>	3
<i>Patents</i>	3
<i>Other Documents Referenced</i>	3
<i>Support For This Standard</i>	3

LIST OF FIGURES2

1 OVERVIEW	5
1.1 Summary	5
1.2 Standard Objectives	5
2 SYSTEM ELECTRICAL INTERFACE REQUIREMENTS	5
2.1 LVDS Interface	6
2.2 Backlight Electrical Interface	6
3 MECHANICAL INTERFACE REQUIREMENTS	11
4 GLOSSARY OF TERMS	12
APPENDIX A – REPRESENTATIVE LVDS CONNECTOR DRAWING	13

List of Tables & Figures

Table 1 – Reference Documents	3
Table 2 - Acknowledgements	4
Figure 2-1 – Active Area Pixel Layout	5
Table 3 – LVDS Connector Pin Assignments	6
Figure 2-2 - Logic Power and LVDS Signals Sequencing Diagram	7
Figure 2-3 – Data Enable Timing	8
Figure 2-4 – DE Only Timing Mode	8
Figure 2-5 – Dual LVDS Channel Color Mapping (8-bit)	9
Figure 2-6 – Dual LVDS Channel Color Mapping (6-bit)	9
Figure 2-7 – Lamp Connector Configuration	10
Figure 3-1 – 20.1-inch Wide Monitor Panel Standard Mechanical Dimensions	11
Figure A-1 – LVDS Connector	13

Intellectual Property

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Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Source	Name	Version / Date
TIA/EIA-644	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	March 1, 1996

Table 1 - Reference Documents

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product which incorporates this standard, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

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Table 2 – Acknowledgements

Revision History

November 29, 2005 –Initial release of the standard

1 Overview

1.1 Summary

This document defines the electrical interface requirements and mechanical dimensions for industry compatible 20.1-inch wide LCD panels.

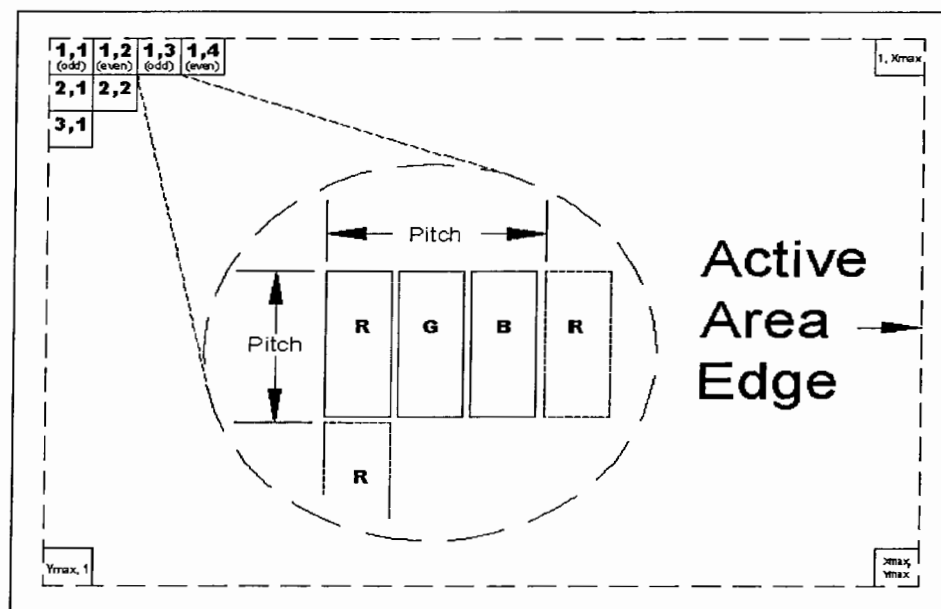
1.2 Standard Objectives

This document establishes a common specification for 20.1-inch wide LCD panels with the intent of creating standardization among these panels such that panels meeting this specification are interchangeable with respect to mechanical fit, electrical requirements, signal definitions and data formats.

2 System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: an LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 16:10 image format supporting a pixel format of 1,680 pixels horizontally by 1,050 pixels vertically.

Figure 2-1 – Active Area Pixel Layout



2.1 LVDS Interface

2.1.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area shall be designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector keying relative to pin-one designation shall be as shown on Figure 3-1 – 20.1-inch Wide Monitor Panel Std. Mechanical Dimensions.

2.1.2 LVDS Interface Signal Definition

The LVDS signal interface cable shall be terminated into a JAE FI-X30SSL-HF or mechanical interface equivalent connector. This connector is to be locking type. The interface connector pin assignments are listed below.

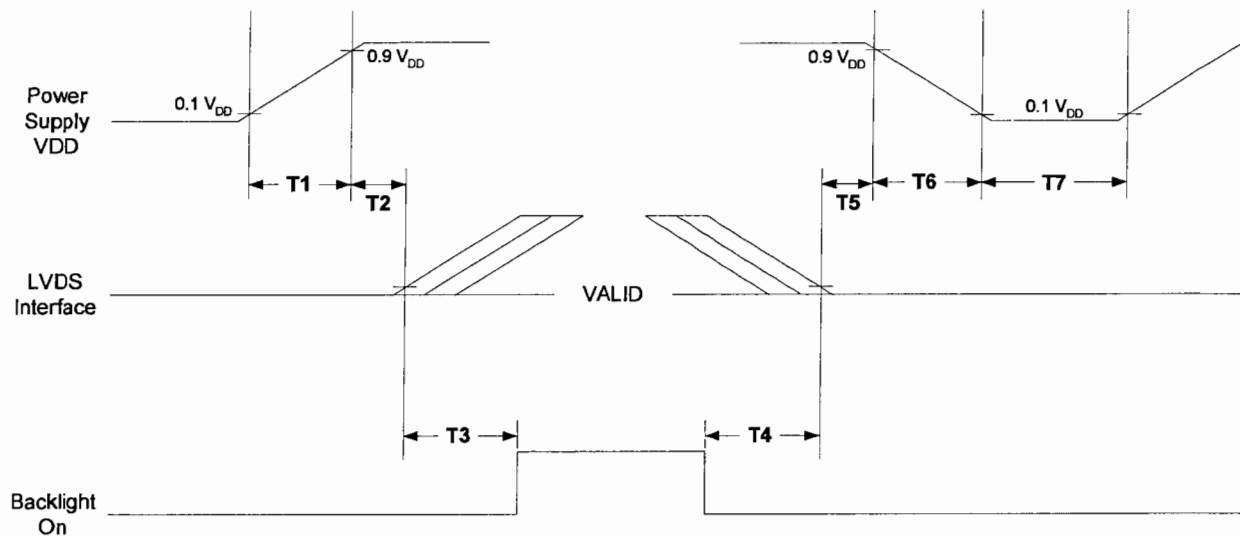
Table 3 – LVDS Connector Pin Assignments

Pin No.	Symbol	Function
Frame	Vss	Ground
1	RxO0-	- LVDS differential data input, Chan 0-Odd
2	RxO0+	+ LVDS differential data input, Chan 0-Odd
3	RxO1-	- LVDS differential data input, Chan 1-Odd
4	RxO1+	+ LVDS differential data input, Chan 1-Odd
5	RxO2-	- LVDS differential data input, Chan 2-Odd
6	RxO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RxOC-	- LVDS Differential Clock input (Odd)
9	RxOC+	+ LVDS Differential Clock input (Odd)
10	RxO3-	- LVDS differential data input, Chan 3-Odd
11	RxO3+	+ LVDS differential data input, Chan 3-Odd
12	RxE0-	- LVDS differential data input, Chan 0-Even
13	RxE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RxE1-	- LVDS differential data input, Chan 1-Even
16	RxE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RxE2-	- LVDS differential data input, Chan 2-Even
19	RxE2+	+ LVDS differential data input, Chan 2-Even
20	RxEC-	- LVDS Differential Clock input (Even)
21	RxEC+	+ LVDS Differential Clock input (Even)
22	RxE3-	- LVDS differential data input, Chan 3-Even
23	RxE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	Vss	No Connection
26	NC	No Connection
27	Vss	No Connection
28	Vcc	+ 12 Volts
29	Vcc	+ 12 Volts
30	Vcc	+ 12 Volts
Frame	Vss	Ground

2.1.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data / control signal sequencing of Figures 3 and 4.

Figure 2-2 - Logic Power and LVDS Signals Sequencing Diagram



$0.5 \text{ ms} < T1 < 10 \text{ ms}$
$0 < T2 < 50 \text{ ms}$
$T3 > 250 \text{ ms}$
$200 \text{ ms} < T4$

$0 < T5 < 50 \text{ ms}$
$0.01 \text{ ms} < T6 < 10 \text{ ms}$
$1,000 \text{ ms} < T7$

Figure 2-3 – Data Enable Timing

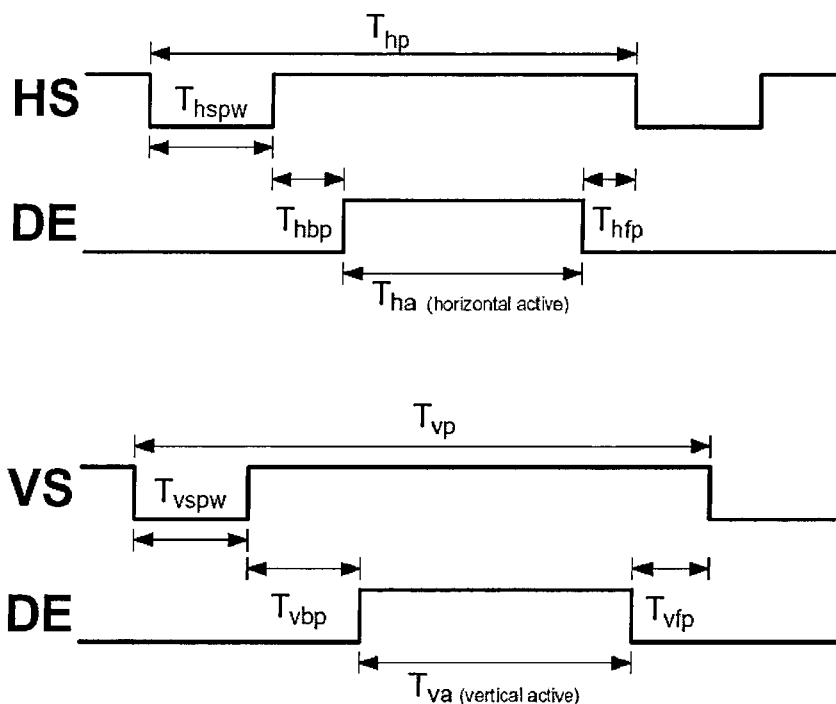
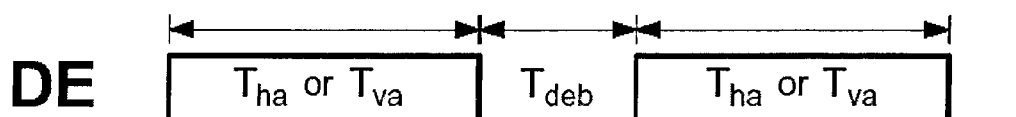


Figure 2-4 – DE Only Timing Mode



2.1.4 LVDS Data and Control Signal Interface

The module's LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 4 shows the data mapping diagram of each LVDS channel when 6-bit color is used, Figure 5 shows the data mapping diagram of each LVDS channel when 8-bit color is used. The LVDS differential signals line-to-line termination impedance, Z_T , shall be 100 ± 10 ohms.

Figure 2-5 – Dual LVDS Channel Color Mapping (8-bit)

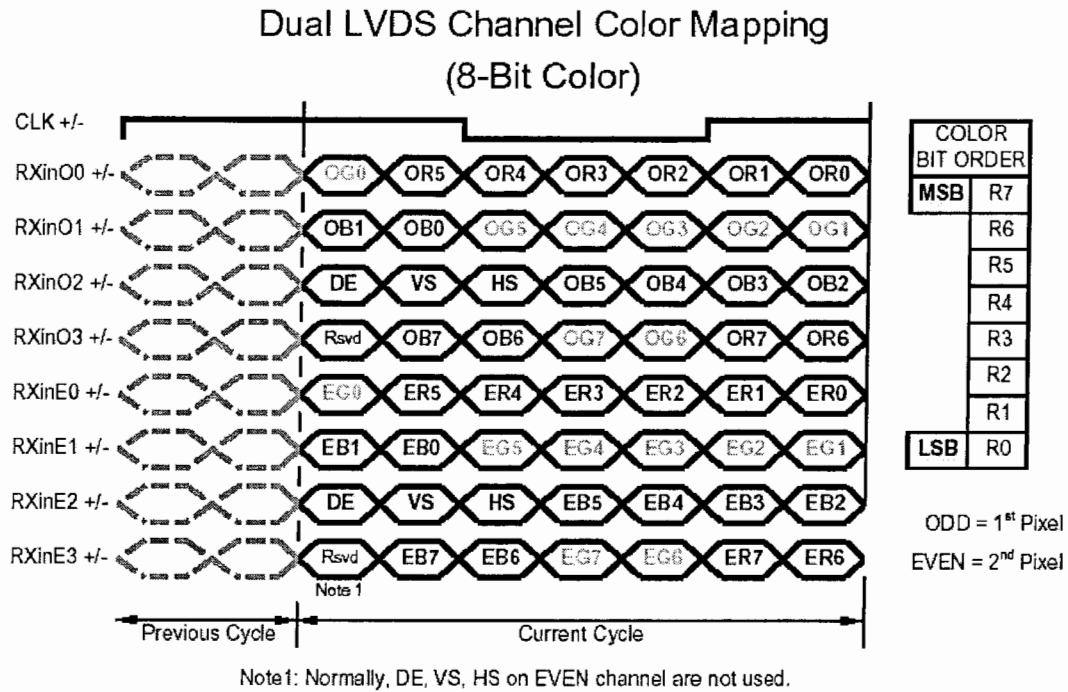
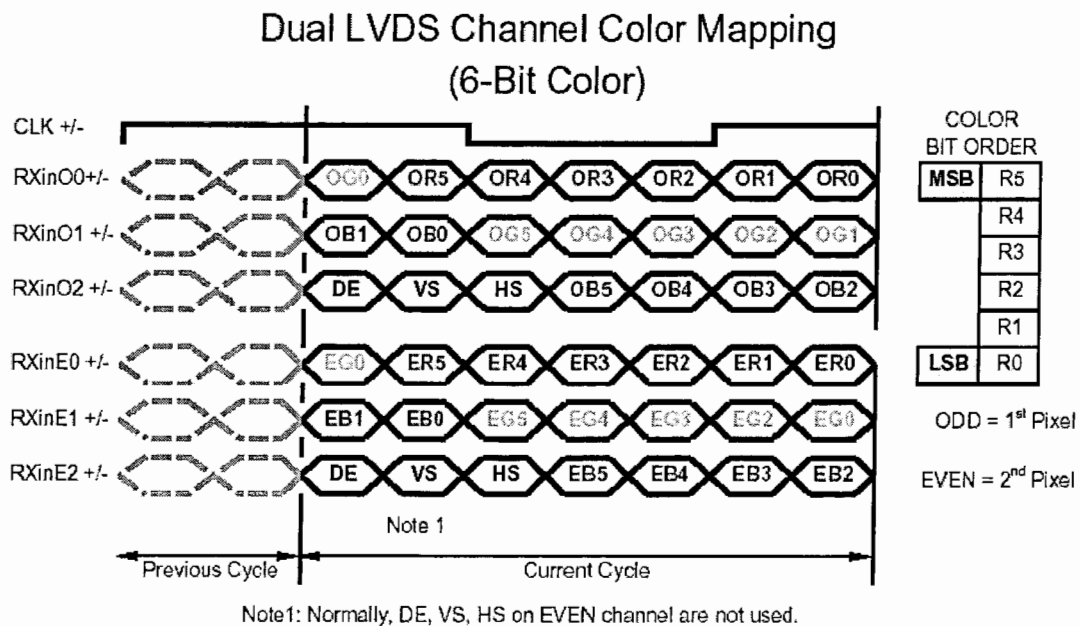


Figure 2-6 – Dual LVDS Channel Color Mapping (6-bit)

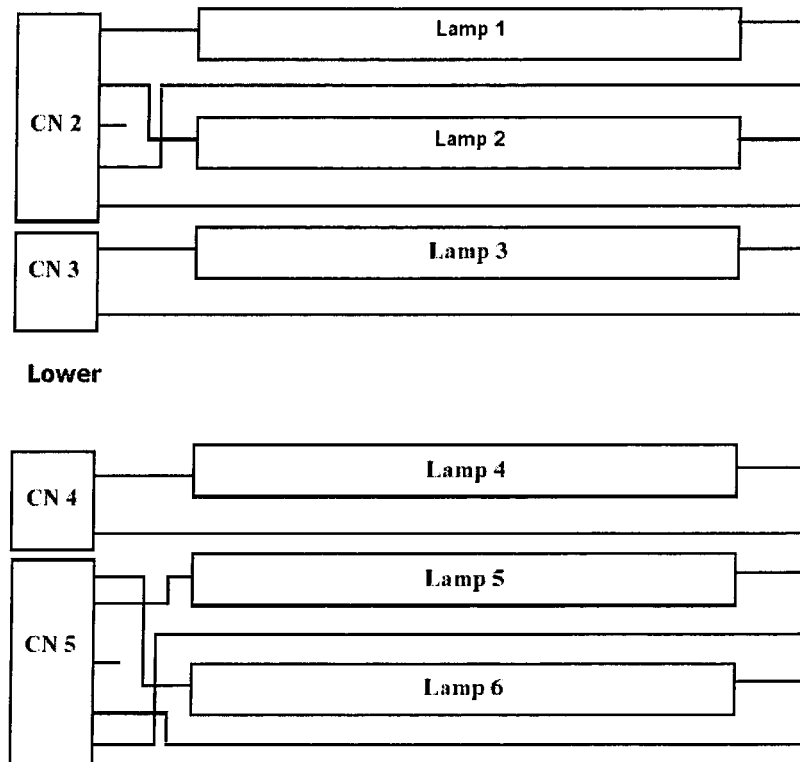


2.2 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into JST BHSR-02VS-1 (CN3/CN4) and BHR-05VS-1 (CN2/CN5) or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in the table below.

	Connector No#	Pin No.	Function
Upper	CN2	1	High Voltage (Lamp 1)
		2	High Voltage (Lamp 2)
		3	N/C
		4	Low Voltage (Lamp 1)
		5	Low Voltage (Lamp 2)
Lower	CN3	1	High Voltage (Lamp 3)
		2	Low Voltage (Lamp 3)
	CN4	1	High Voltage (Lamp 4)
		2	Low Voltage (Lamp 4)
	CN5	1	High Voltage (Lamp 6)
		2	High Voltage (Lamp 5)
		3	N/C
		4	Low Voltage (Lamp 6)
		5	Low Voltage (Lamp 5)

Figure 2-7 – Lamp Connector Configuration



3 Mechanical Interface Requirements

Figure 3.1 shows the critical exterior dimensions and connector location.

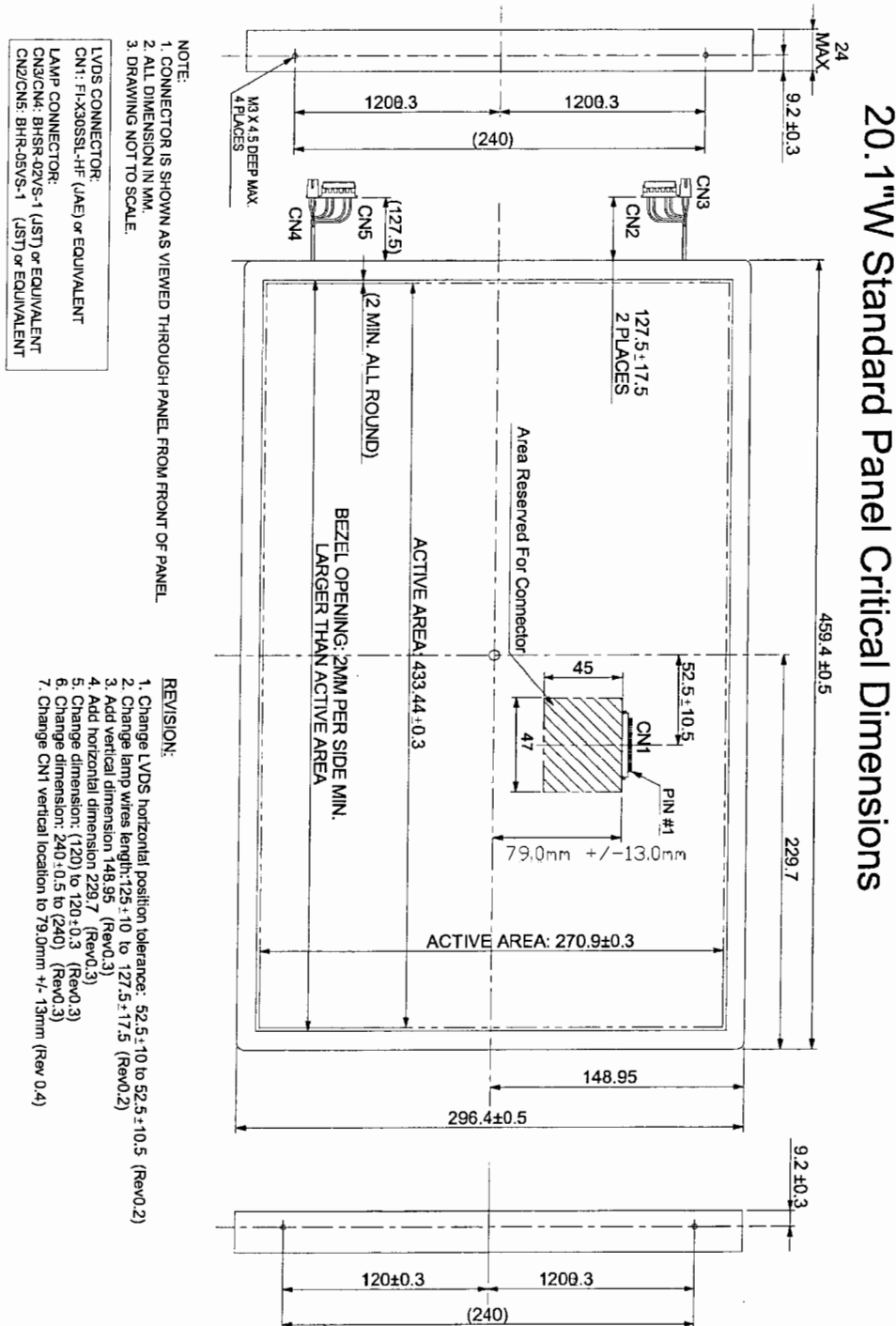


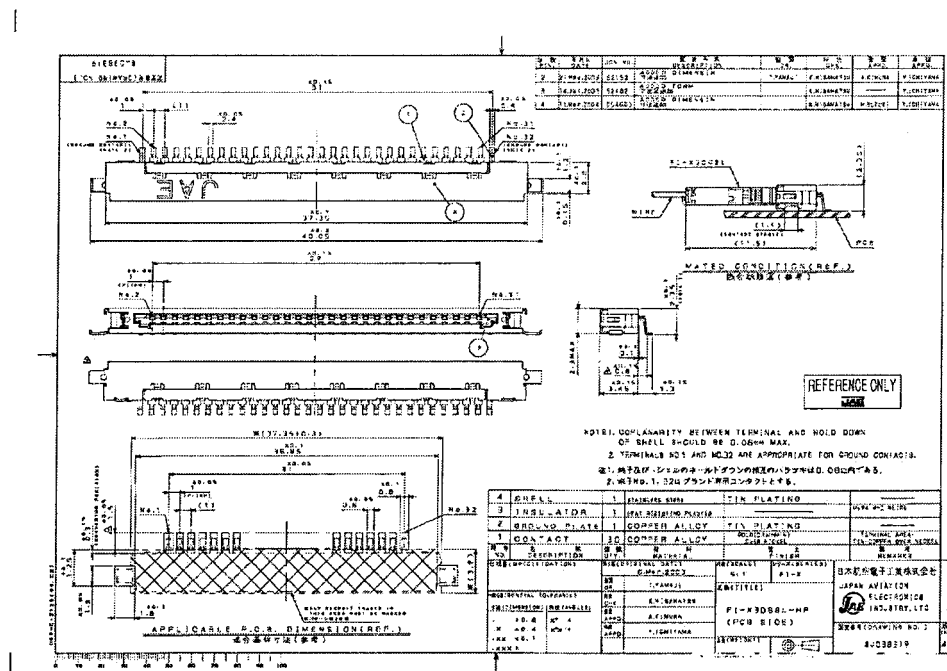
Figure 3-1 – 20.1-inch Wide Monitor Panel Std. Mechanical Dimensions

4 Glossary of Terms

Abbreviation	Meaning
CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
LVDS	Low Voltage Differential Signaling
TDEB	Time - Display Enable Blanking
THA	Time - Horizontal Active
THBP	Time - Horizontal Back Porch
THFP	Time - Horizontal Front Porch
THP	Total - Horizontal Period
THSPW	Time - Horizontal Sync Pulse Width
TVA	Time - Vertical Active
TVBP	Time - Vertical Back Porch
TVFP	Time - Vertical Front Porch
Tvspw	Time - Vertical Sync Pulse Width
VCCFL	Voltage for CCFL
VS	Vertical Sync

Appendix A – Representative LVDS Connector Drawing

Figure A-1 – LVDS Connector



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