Video Electronics Standards Association

20.1-inch Wide, 4-lamp Panel Standard

860 Hillview Court, Suite 150
Milpitas, CA 95035

Phone: 408-957-9270
Fax: 408-957-9277

VESA 20.1-inch Wide, 4-lamp Panel Standard

Version 1

October 22, 2007

Purpose

This specification defines the requirements to standardize the mechanical dimensions and selected electrical interface elements of a 20.1-inch wide format panels intended for use as LCD monitors. This will help LCD manufacturers and panel consumers to better control panel supply and demand cycles.

The intent of this standard is that panels built to this specification are interchangeable without requiring alterations to tooling or drive electronics.

Summary

This proposal describes the mechanical dimensions, electrical interfaces and data formatting for 20.1-inch wide, 4 lamp monitor panels.

Preface

Intellectual Property

While every precaution has been taken in the preparation of this standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

Trademarks

All trademarks used within this document are the property of their respective owners. VESA is a registered trademark of the Video Electronics Standards Association.

Patents

VESA draws attention to the fact that it is claimed that compliance with this specification may involve the use of a patent or other intellectual property right (collectively, "*IPR*") concerning items in this proposal. VESA takes no position concerning the evidence, validity, and scope of this *IPR.*

The following holders of this *IPR* have assured VESA that they are willing to license the *IPR* on *RAND* terms. The statement of the holder of this *IPR* is registered with VESA.

Holder Name	**Contact Information**	**Claims Known**
JAE Electronics, Inc. 142 Technology Dr, Suite 100 Irvine, CA 92618	Ph: 949-753-2600 Mark Saubert (saubertm@jae.com)	

Attention is drawn to the possibility that some of the elements of this VESA Specification may be the subject of *IPR* other than those identified above. VESA shall not be held responsible for identifying any or all such *IPR*, and has made no inquiry into the possible existence of any such *IPR.*

THIS SPECIFICATION IS BEING OFFERED WITHOUT ANY WARRANTY WHATSOEVER, AND IN PARTICULAR, ANY WARRANTY OF NON-INFRINGEMENT IS EXPRESSLY DISCLAIMED. ANY IMPLEMENTATION OF THIS SPECIFICATION SHALL BE MADE ENTIRELY AT THE IMPLEMENTER'S OWN RISK, AND NEITHER VESA, NOR ANY OF ITS MEMBERS OR SUBMITTERS, SHALL HAVE ANY LIABILITY WHATSOEVER TO ANY IMPLEMENTER OR THIRD PARTY FOR ANY DAMAGES OF ANY NATURE WHATSOEVER DIRECTLY OR INDIRECTLY ARISING FROM THE IMPLEMENTATION OF THIS SPECIFICATION.

Support

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates 20.1-inch Wide, 4-Lamp Standard Panel, ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. Submit all comments or reported errors in writing to VESA using one of the following methods.

- Fax 408- 957- 9277, *direct this fax to Technical Support at VESA*
- E-mail support@vesa.org
- Mail Technical Support
  Video Electronics Standards Association
  860 Hillview Court, Suite 150
  Milpitas, CA 95035

Acknowledgements

This document would not have been possible without the efforts of the VESA Display Device Standards Committee and the Monitor Panel Standards Task Group. In particular, the following individuals and their companies contributed significant time and knowledge to this version of the standard.

Name	Company Name	Contribution
Emily Hwei	Chi Mei Optoelectronics	
C.J. Lin	Chi Mei Optoelectronics	
Alex Wong	Chunghwa Picture Tubes	
Billy Leong	Dell	
Thomas Chung	Dell	
Sim Tiak Hooy	Dell	
Joe Goodart	Dell	Task Group Chair & Editor
Jeff Frankel	Genesis Microchip	Task Group Co-editor
David Braun	Hewlett-Packard	
Hunter Ryu	LG.Philips LCD	
Moo-Kyung (Mark) Son	Samsung	
Choing Choi	Samsung	
Alain d'Hautecourt	ViewSonic	

Revision History

October 22, 2007	Initial release of the 20.1-inch, 4-lamp Panel Standard

Table of Contents

Tables

Figures

1. OVERVIEW

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for industry compatible panels sized 20.1W for notebook and similar applications.

1.2 Standard Objectives

This document establishes common panels for the 20.1-inch wide display sizes so that a standard panel can be mounted in any notebook case designed to accept the maximum defined size. The dimensioning allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms.

1.3 Reference Documents

The following documents forms a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the correct versions of these referenced standards:

Table 1-1: Reference Documents

Document	Version/Revision	Date
VESA Policy 200B Intellectual Property Rights	Version B	December 2004
VESA Glossary of Terms (www.vesa.org)	Current	Current
VESA Enhanced Display Data Channel Standard (E-DDC)	Version 1.1	March 24, 2004
ANSI/TIA/EIA-644-A-2001, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits	Version A	Feb 1, 2001

2. System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: an LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 16:10 image format supporting a pixel format of 1,680 pixels horizontally by 1,050 pixels vertically.

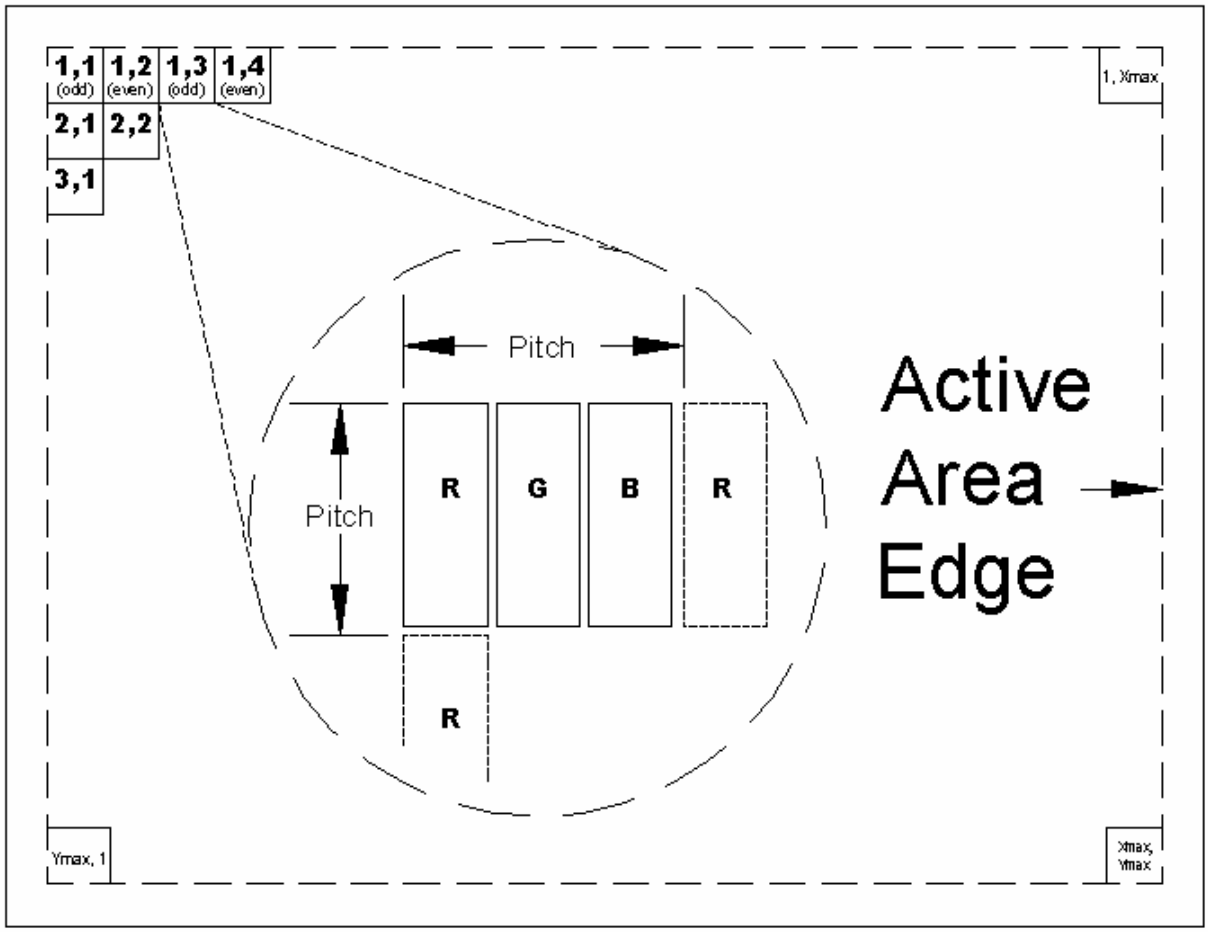


Figure 2-1: Active Area Pixel Layout

2.1 DisplayPort Interface

The DisplayPort Interface connector is described in a separate VESA standard

2.2 LVDS Interface

2.2.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area is designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector location and keying relative to pin-one designation shall be as shown in Figure 2-8.

2.2.2 LVDS Interface Signal Definition

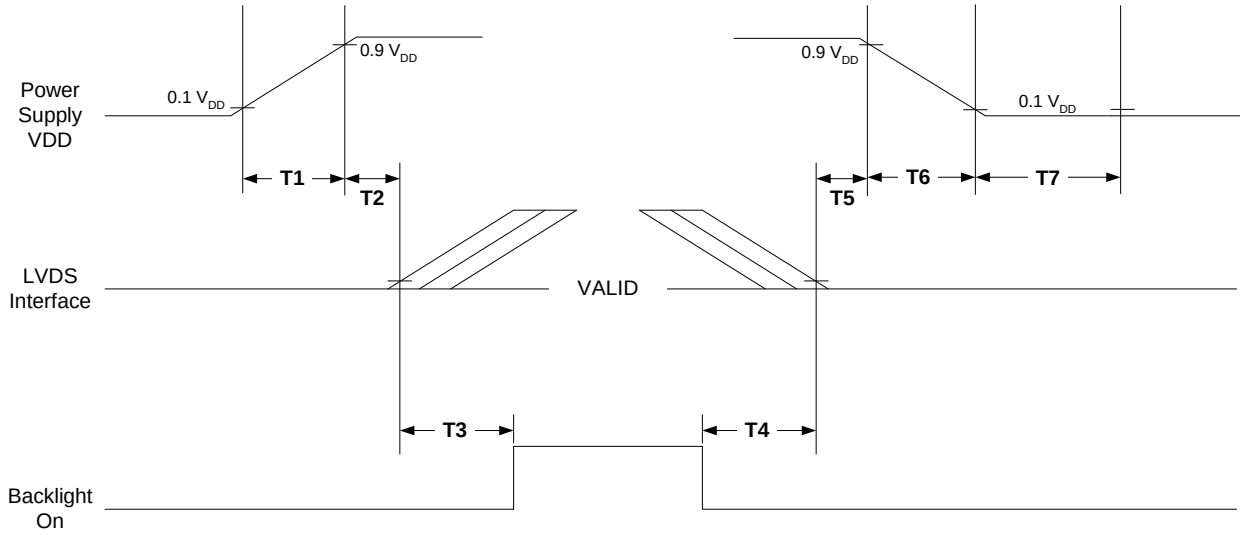
The LVDS signal interface cable shall be terminated to a JAE FI X30SSL-HF, FI-XB30SRL-HF11 or locking type equivalent connector. The interface connector pin assignments are listed in Table 2-1.

Table 2-1: LVDS Interface Cable Pin Assignments

Pin No.	Symbol	Function
Frame		Ground
1	RxO0-	- LVDS differential data input, Chan 0-Odd
2	RxO0+	+ LVDS differential data input, Chan 0-Odd
3	RxO1-	- LVDS differential data input, Chan 1-Odd
4	RxO1+	+ LVDS differential data input, Chan 1-Odd
5	RxO2-	- LVDS differential data input, Chan 2-Odd
6	RxO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RxOC-	- LVDS Differential Clock input (Odd)
9	RxOC+	+ LVDS Differential Clock input (Odd)
10	RxO3-	- LVDS differential data input, Chan 3-Odd
11	RxO3+	+ LVDS differential data input, Chan 3-Odd
12	RxE0-	- LVDS differential data input, Chan 0-Even
13	RxE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RxE1-	- LVDS differential data input, Chan 1-Even
16	RxE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RxE2-	- LVDS differential data input, Chan 2-Even
19	RxE2+	+ LVDS differential data input, Chan 2-Even
20	RxEC-	- LVDS Differential Clock input (Even)
21	RxEC+	+ LVDS Differential Clock input (Even)
22	RxE3-	- LVDS differential data input, Chan 3-Even
23	RxE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	NC	No Connection
26	NC	No Connection
27	NC	No Connection
28	Vcc	+ 5 Volts
29	Vcc	+ 5 Volts
30	Vcc	+ 5 Volts

2.2.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data/control signal sequencing of Figure 2-2, Figure 2-3 and Figure 2-4.



	Minimum time (ms)	Maximum time (ms)
T1	0.5	10
T2	0	50
T3	1000	-
T4	200	-
T5	0	50
T6	0.01	1000
T7	1000	-

Figure 2-2: Logic Power and LVDS Signals Sequencing Diagram

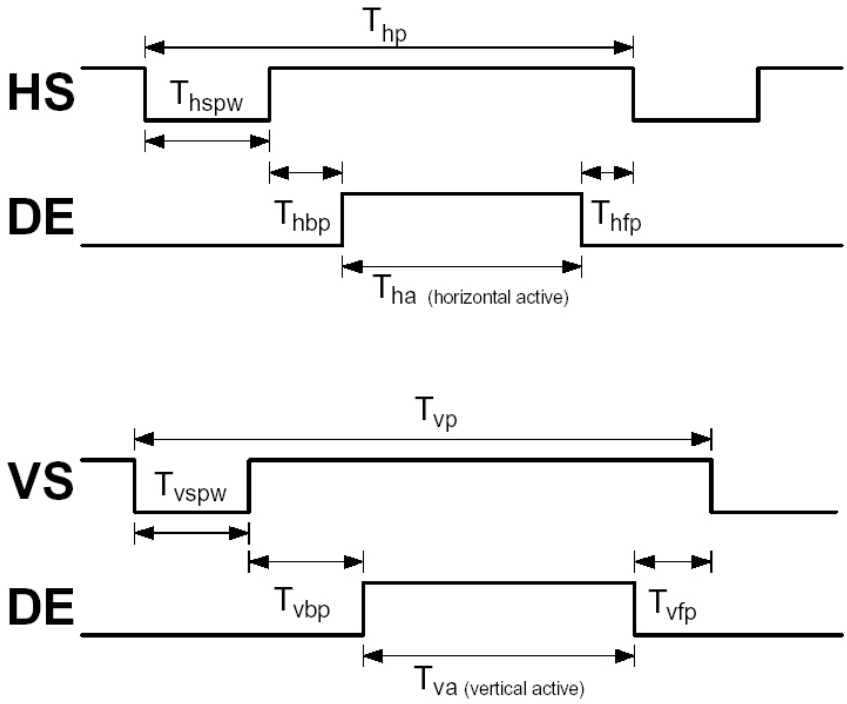


Figure 2-3: Data Enable Timing Parameters

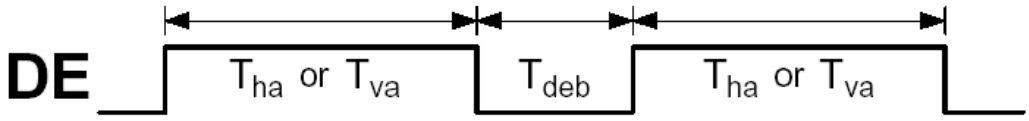


Figure 2-4: DE Only Timing Mode

2.2.4 LVDS Data and Control Signal Interface

The module's LVDS signals interface shall meet requirements of ANSI/TIA/EIA-644A. Figures 2-5 and 2-6 show the data mapping diagram of each LVDS channel. The LVDS differential signals line-to-line termination impedance, Z_T, shall be 100 ± 10 ohms.

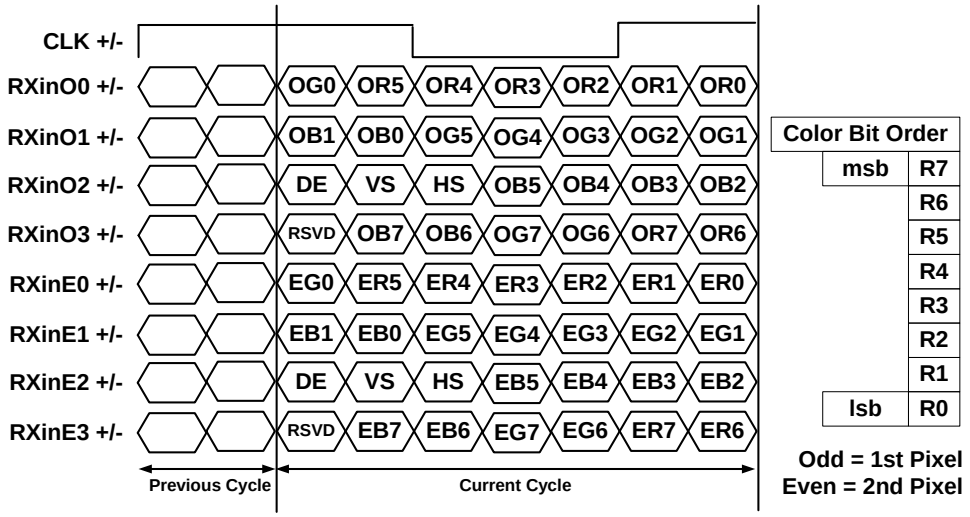


Figure 2-5: Dual LVDS Color Channel Mapping (8-Bit)

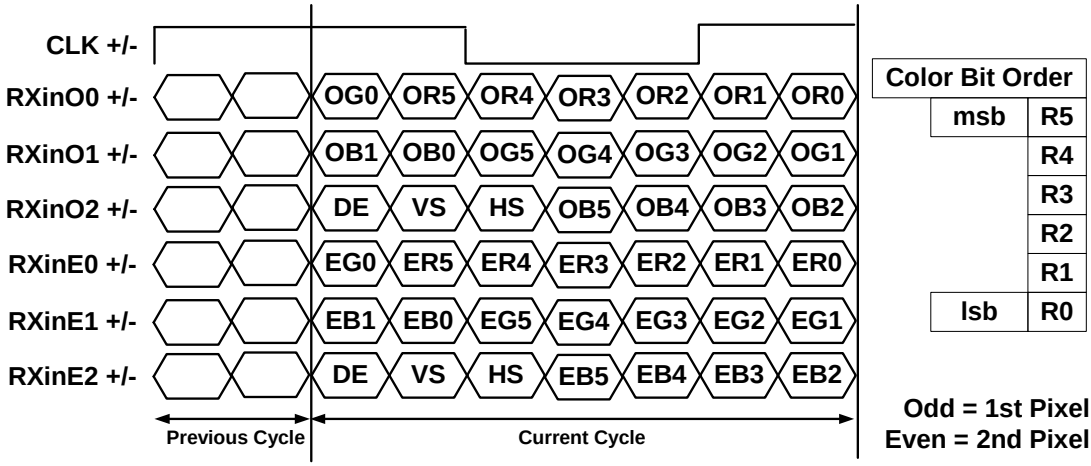


Figure 2-6: Dual LVDS Color Channel Mapping (6-Bit)

2.2.5 Backlight Electrical Interface

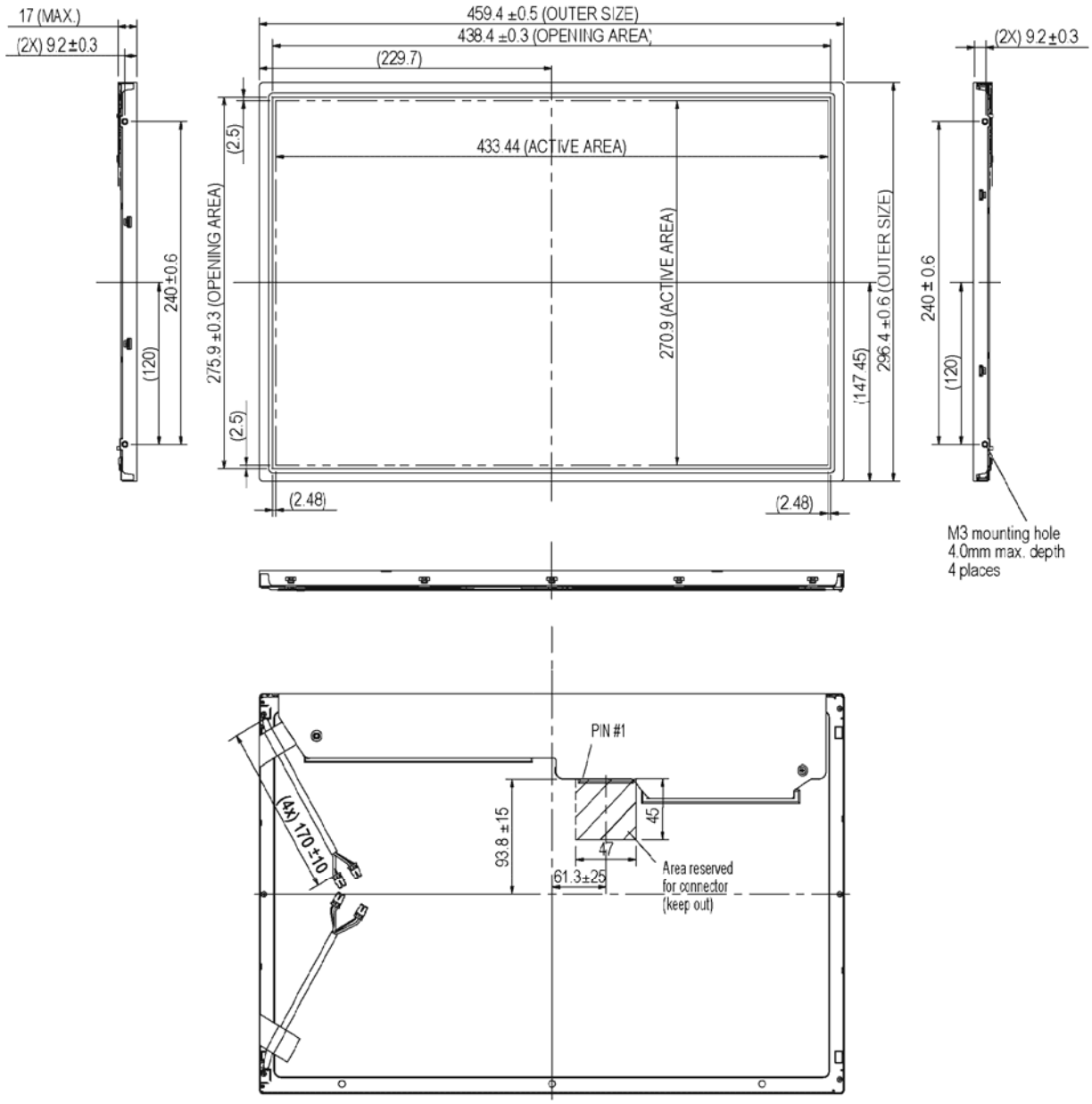
The panel-side backlight interface cable shall be terminated into JST BHR-02VS-1,2 or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Figure 2-7.

Figure 2-7: Lamp Connector Configuration

Pin	Symbol	Description	Remark
1	HV	High Voltage	Pink
2	LV	Low Voltage	White
1	HV	High Voltage	Blue
2	LV	Low Voltage	Black
1	HV	High Voltage	Pink
2	LV	Low Voltage	White
1	HV	High Voltage	Blue
2	LV	Low Voltage	Black

2.2.6 Mechanical Interface Requirements

Figure 2.8 shows the critical exterior dimensions and the locations of connectors.



NOTE
1. All dimension in mm.
2. Drawing not to scale
3. Interface connector: FI-XB30SRL-HF11 (JAE) or equivalent.
4. Lamp connector: 35001HS-02LD (Yeonho) or equivalent.
5. Torque for mounting hole: 3.0~4.0 kgf-cm.
6. Panel weight: 2200g ± 200g

Figure 2-8: Dimensions

3. Glossary of Terms

Abbreviation	Meaning
CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
lsb	Least Significant Bit
LVDS	Low Voltage Differential Signaling: TIA/EIA-644
msb	Most Significant Bit
NC	No Connection
T_{deb}	Time - Display Enable Blanking
T_{ha}	Time - Horizontal Active
T_{hbp}	Time - Horizontal Back Porch
T_{hfp}	Time - Horizontal Front Porch
T_{hp}	Time - Total Horizontal Period
T_{hspw}	Time - Horizontal Sync Pulse Width
T_{va}	Time - Vertical Active
T_{vbp}	Time - Vertical Back Porch
T_{vfp}	Time - Vertical Front Porch
T_{vp}	Time - Total Vertical Period
T_{vspw}	Time - Vertical Sync Pulse Width
VBR	Backlight Brightness
VIN	Backlight Power
VON/OFF	Backlight On / Off
VS	Vertical Sync