VESA®

19-inch, 5-volt Standard Panel

Video Electronics Standards Association
860 Hillview Court, Suite 150
Milpitas, CA 95035
Phone: 408-957-9270
Fax: 408-957-9277

VESA STANDARD PANEL
19-inch, 5-volt

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Purpose

This specification will define the requirements for the standardization of mechanical dimensions and selected electrical interface requirements of 19-inch panels intended for use as LCD monitors. This panel is designed to operate from a 5-volt source. This should enable LCD manufacturers and panel consumers to better control supply and demand cycles. The intent is that panels built to this specification will be able to be used in most applications without requiring alterations in either the product tooling or the display module.

Summary

The described LCD panels are designed to make selection and implementation of LCD standardization easier, faster and more affordable.

Preface

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Fax: 408-957-9277, direct this note to Technical Support at VESA

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Mail: Technical Support
Video Electronics Standards Association
860 Hillview Court, Suite 150
Milpitas, CA 95035

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Name	**Company**	
CM Wung	AU Optronics	
CH Huang	AU Optronics	
Anny Yuan	Chi Mei Optoelectronics	
Chi Tai Hong	Chrontel	
Jae Lee	Dell	
Joe Goodart	Dell	Task Group Chair
Jeff Frankel	Genesis Microchip	Task Group Secretary
Bob Myers	Hewlett-Packard	
David Braun	Hewlett-Packard	
Karl Kwiat	Hirose Electric	
Susan Luerich	IBM	
S. Narisawa	International Display Technology	
Sue Wood	JAE Electronics	
Hunter Yu	LG.Philips LCD	
Young Sang Baek	LG.Philips LCD	
Albert Lee	National Semiconductor	
Ian Miller	Samsung	
Moo-kyung Son	Samsung	
James Chun	Samsung	
Kazo Takashi	Sharp	
Atsushi Iwata	Toshiba-Matsushita Display Technology	
Alain d'Hautecourt	ViewSonic	
Don Chambers	CONN-tech CONN-sulting	Editor

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1. OVERVIEW

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for industry compatible panels sized 19.0-inch.

1.2 Standard Objectives

This document establishes common panels for the 19.0-inch display sizes so that a Standard Panel can be mounted in any case designed to accept the maximum size defined. The dimensioning allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms.

2. Reference Documents

The following document forms a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the latest versions of this reference standard:
TIA/EIA-644 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
VESA Enhanced Display Data Channel Standard (E-DDC), Ver 1, Sept 2, 1999

3. System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: a LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 5:4 image format and square pixels (e.g. 1280 x 1024). Figure 1 shows the pixel formatting for the active display surface.

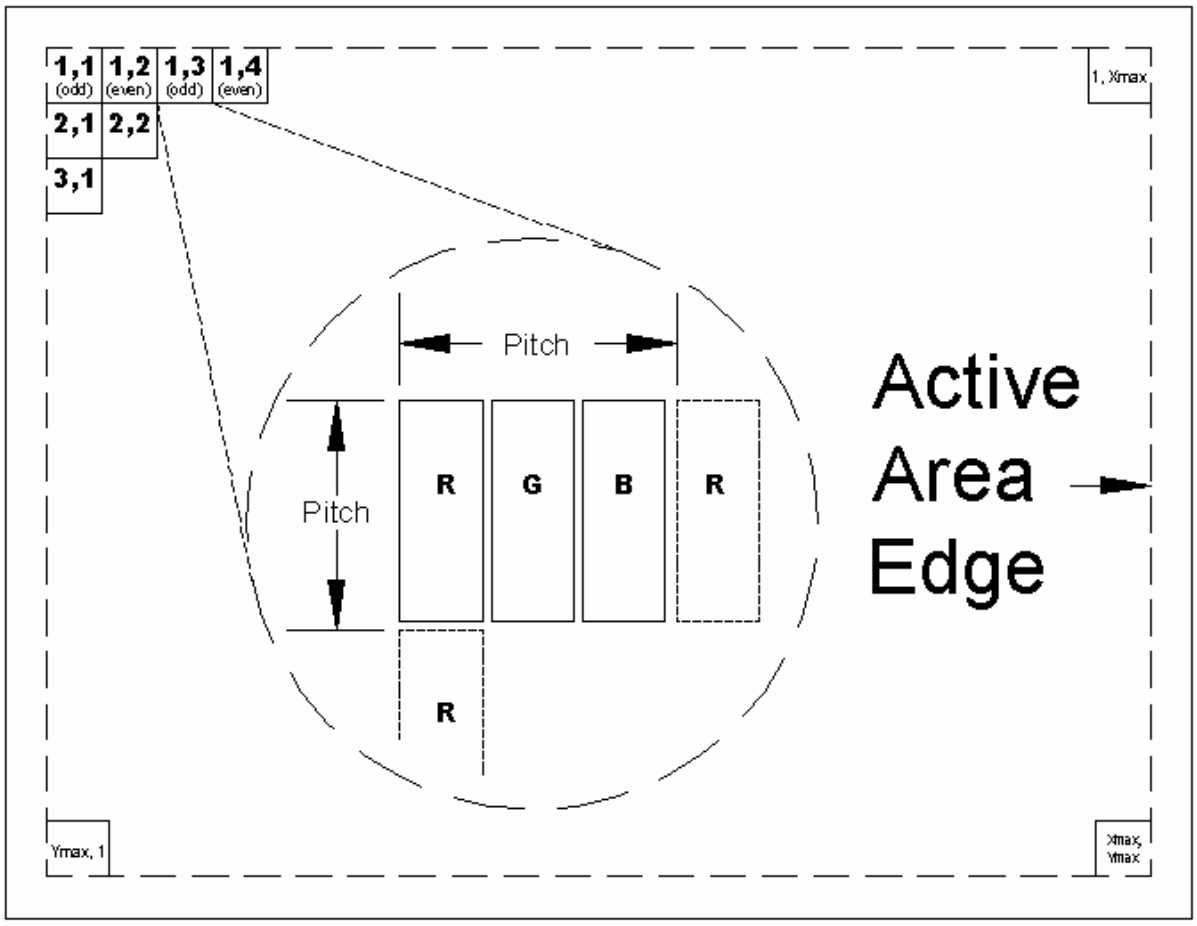


Figure 1--- Active Area Pixel Layout

3.1 LVDS Interfaced

3.1.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area shall be designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector keying relative to pin-one designation shall be as shown on Figure 5.

3.1.2 LVDS Interface Signal Definition

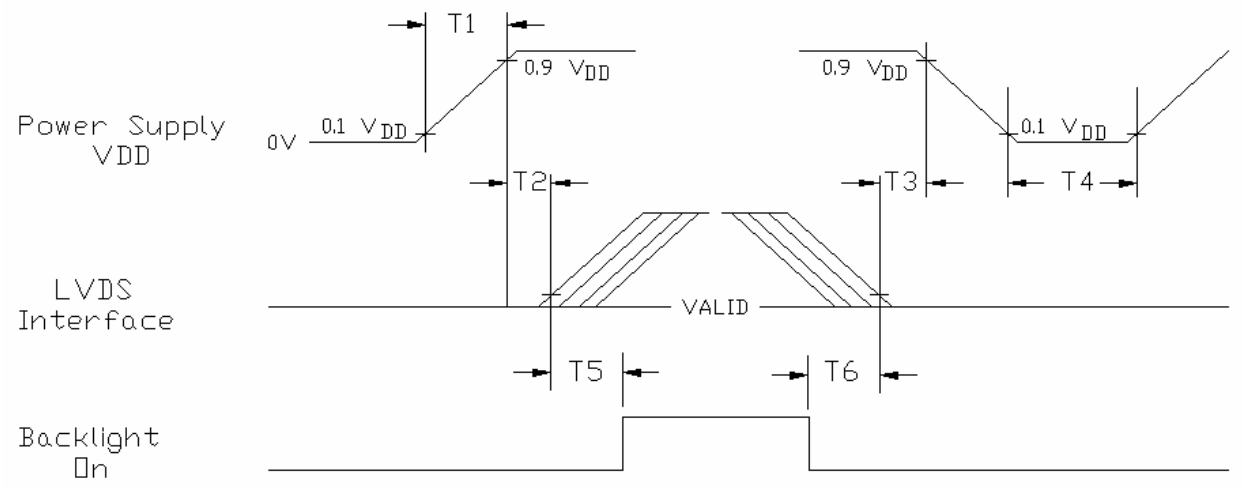
The LVDS signal interface cable shall be terminated into a JAE FI-XB30SSL-HF15, FCI 10041195, or mechanical interface equivalent connector. The interface connector pin assignments are listed in Table 1.

Pin No.	Symbol	Function
Frame	Vss	Ground
1	RXinO0-	- LVDS differential data input, Chan 0-Odd
2	RXinO0+	+ LVDS differential data input, Chan 0-Odd
3	RXinO1-	- LVDS differential data input, Chan 1-Odd
4	RXinO1+	+ LVDS differential data input, Chan 1-Odd
5	RXinO2-	- LVDS differential data input, Chan 2-Odd
6	RXinO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RXOC-	- LVDS Differential Clock input (Odd)
9	RXOC+	+ LVDS Differential Clock input (Odd)
10	RXinO3-	- LVDS differential data input, Chan 3-Odd
11	RXinO3+	+ LVDS differential data input, Chan 3-Odd
12	RXinE0-	- LVDS differential data input, Chan 0-Even
13	RXinE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RXinE1-	- LVDS differential data input, Chan 1-Even
16	RXinE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RXinE2-	- LVDS differential data input, Chan 2-Even
19	RXinE2+	+ LVDS differential data input, Chan 2-Even
20	RXEC-	- LVDS Differential Clock input (Even)
21	RXEC+	+ LVDS Differential Clock input (Even)
22	RXinE3-	- LVDS differential data input, Chan 3-Even
23	RXinE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	Vss	Ground
26	NC	No Connection
27	Vss	Ground
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply
Frame	Vss	Ground

Table 1 --- LVDS Interface Cable Pin Assignments

3.1.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data / control signal sequencing of Figures 2 and 3.



0.5 ms $\leq T_1 \leq$ 10 ms $0 \leq t_2 \leq$ 50 ms $0 \leq$ t3 $\leq$ 50 ms 500 ms $\leq T_4$ 200 ms $\leq$ T5 200 ms $\leq$ T6

Figure 2 --- Logic Power and LVDS Signals Sequencing Diagram

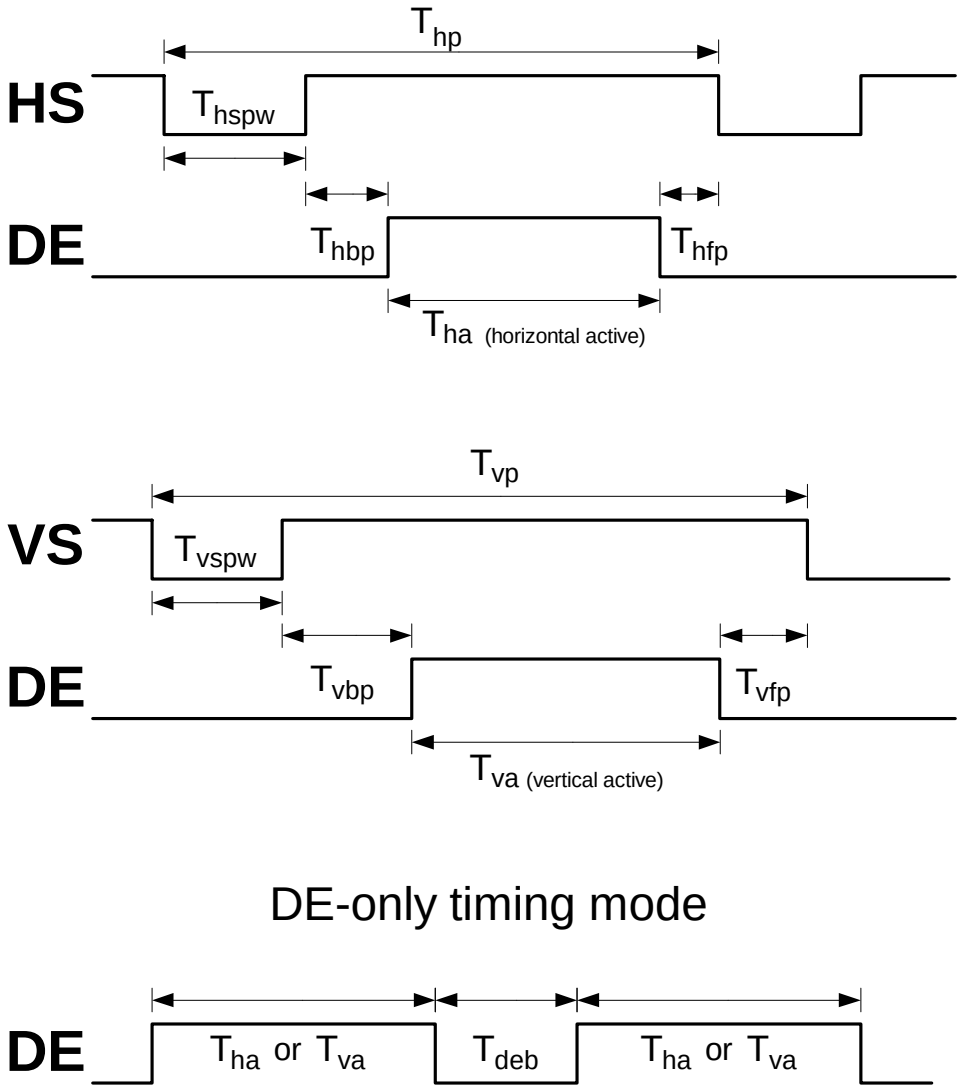
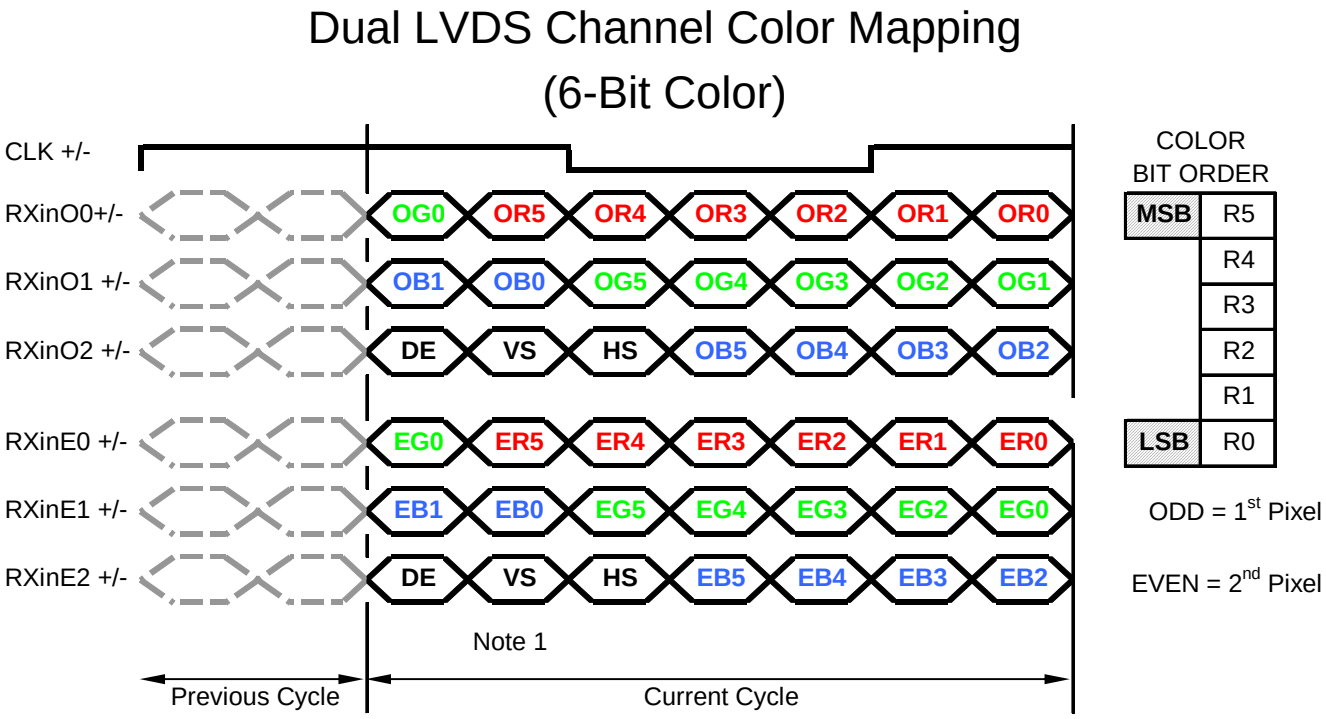


Figure 3 --- Data Enable Timing Parameters

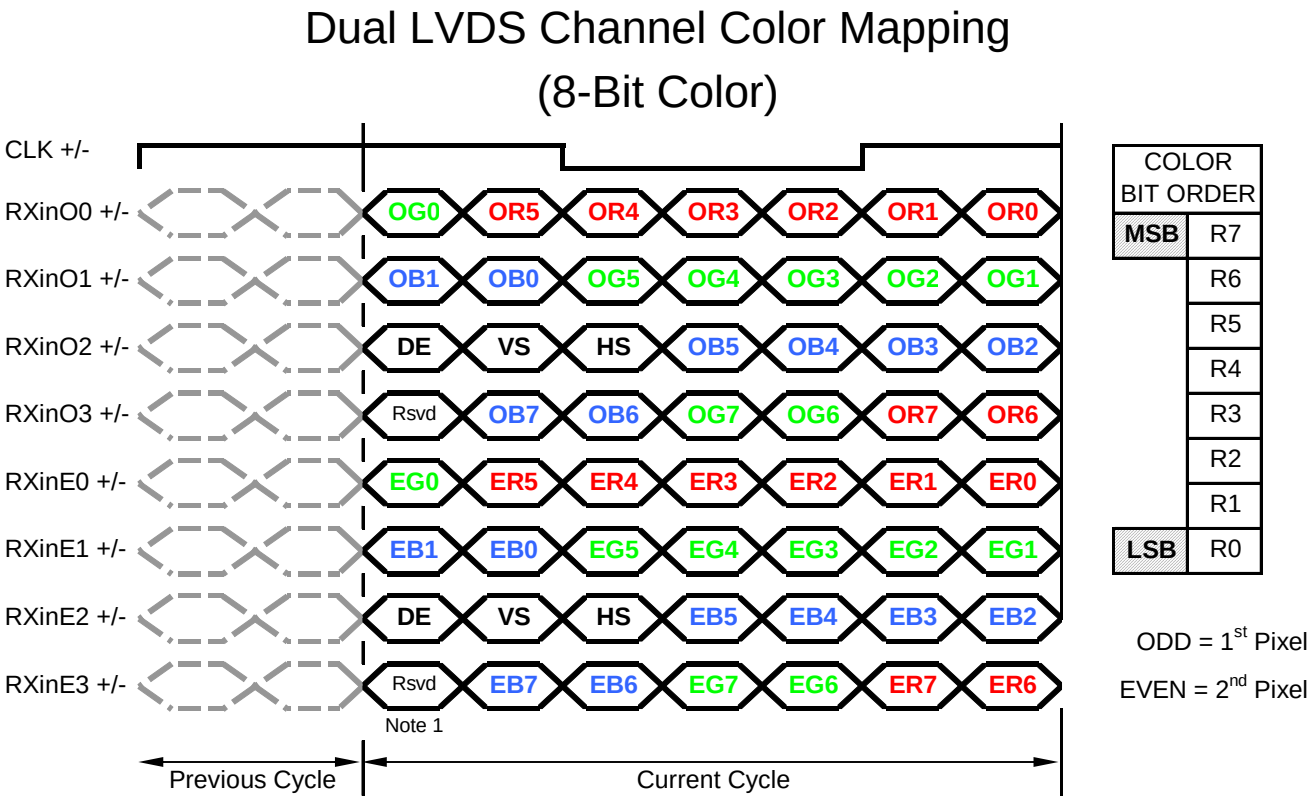
3.1.4 LVDS Data and Control Signal Interface

The modules LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 4 shows the data mapping diagram of each LVDS channel when 6-bit color is used, Figure 5 shows the data mapping diagram of each LVDS channel when 8-bit color is used. The LVDS differential signals line-to-line termination impedance, Z_T, shall be 100 ± 10 ohms.



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Figure 4 --- Dual LVDS Channel 6-Bit Color Mapping Diagram



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Figure 5 --- Dual LVDS Channel 8-Bit Color Mapping Diagram

3.2 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into JST BHSR-02VS-1, Sin Sheng P2408P2, Sunridge FPD-PB-35-2P or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 2.

Pin No.	Signal	Level	Function
1	V_{CCFL}	AC	Power Supply for CCFL
2	Gnd Rtn	Ground	Power return for CCFL

Table 2 --- Backlight Electrical Interface

4. Mechanical Interface Requirements

Figure 6 shows the critical exterior dimensions and connector location. ⊕ indicates center point of active area.

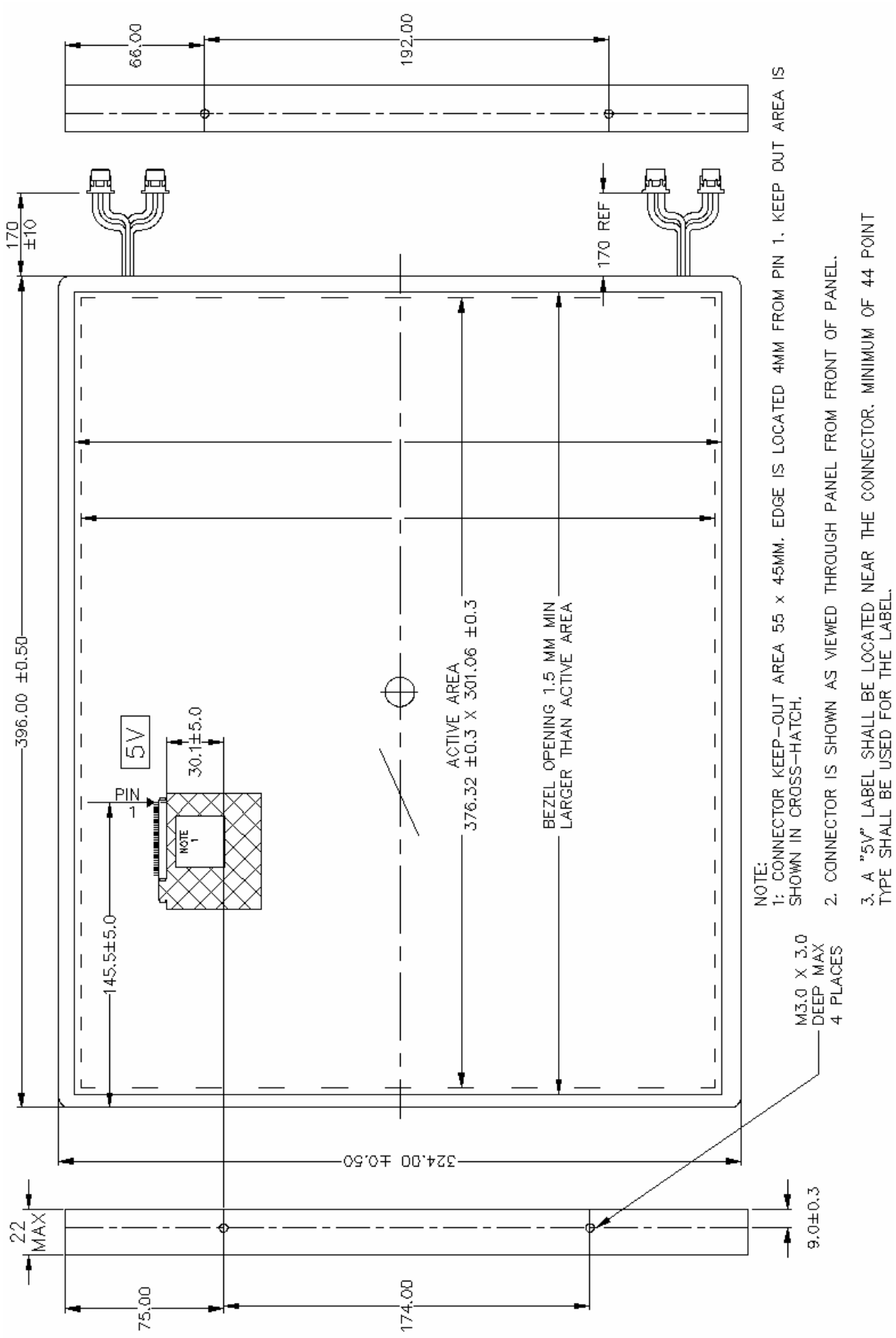


Figure 6 --- Mechanical Dimensions

Note: All dimensions in mm.

5. Glossary of Terms

Abbreviation		Explanation
CCFL	-	Cold Cathode Fluorescent Lamp
DE	-	Display Enable
HS	-	Horizontal Sync
LVDS	-	Low Voltage Differential Signaling
T_{DEB}	-	Time - Display Enable Blanking
T_{HA}	-	Time - Horizontal Active
T_{HBP}	-	Time - Horizontal Back Porch
T_{HFP}	-	Time - Horizontal Front Porch
T_{HP}	-	Total - Horizontal Period
T_{HSPW}	-	Time - Horizontal Sync Pulse Width
T_{VA}	-	Time - Vertical Active
T_{VBP}	-	Time - Vertical Back Porch
T_{VFP}	-	Time - Vertical Front Porch
Tvspw	-	Time - Vertical Sync Pulse Width
V_{CCFL}	-	Voltage for CCFL
VS	-	Vertical Sync