



VESA®

19-inch, 12-volt Standard Panel

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VESA STANDARD PANEL

19-inch, 12-volt

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Purpose

This specification will define the requirements for the standardization of mechanical dimensions and selected electrical interface requirements of 19-inch panels intended for use as LCD monitors, designed to operate from a 12-volt source. This should enable LCD manufacturers and panel consumers to better control supply and demand cycles. The intent is that panels built to this specification will be able to be used in most applications without requiring alterations in either the product tooling or the display module.

Summary

The described LCD Panels are designed to make selection and implementation of LCD standardization easier, faster and more affordable.

Preface

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product, which incorporates an Industry Standard Panel, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

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Table of Contents

<i>Intellectual Property</i>	2
REVISION HISTORY	3
1. OVERVIEW	5
1.1 SUMMARY	5
1.2 STANDARD OBJECTIVES	5
2. REFERENCE DOCUMENTS	5
3. SYSTEM ELECTRICAL INTERFACE REQUIREMENTS	5
3.1 LVDS INTERFACED	6
3.1.1 LVDS Signal Interface Connector Requirements	6
3.1.2 LVDS Interface Signal Definition	7
3.1.3 LVDS Power Sequencing Requirements	8
3.1.4 LVDS Data and Control Signal Interface	9
3.2 BACKLIGHT ELECTRICAL INTERFACE	11
4. MECHANICAL INTERFACE REQUIREMENTS	11
5. GLOSSARY OF TERMS	13

List of Figures

Figure 1--- Active Area Pixel Layout	6
Figure 2 --- Logic Power and LVDS Signals Sequencing Diagram	8
Figure 3 --- Data Enable Timing Parameters	9
Figure 4 --- Dual LVDS Channel 6-Bit Color Mapping Diagram	10
Figure 5 --- Dual LVDS Channel 8-Bit Color Mapping Diagram	11
Figure 6 --- Mechanical Dimensions	12

List of Tables

Table 1 --- LVDS Interface Cable Pin Assignments	7
Table 2 --- Backlight Electrical Interface	1

1. OVERVIEW

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for industry compatible panels sized 19-inch.

1.2 Standard Objectives

This document establishes common panels for the 19-inch display sizes so that a Standard Panel can be mounted in any case designed to accept the maximum size defined. The dimensioning allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms.

2. Reference Documents

The following document forms a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the latest versions of this reference standard:

TIA/EIA-644 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
VESA Enhanced Display Data Channel Standard (E-DDC), Ver 1, Sept 2, 1999

3. System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: a LVDS interface which encodes the digital R-G-B data and timing/control signals and a power interface for the panel backlight. This specification is only for panels with a 5:4 image format and square pixels (e.g. 1280 x 1024). Figure 1 shows the pixel formatting for the active display surface.

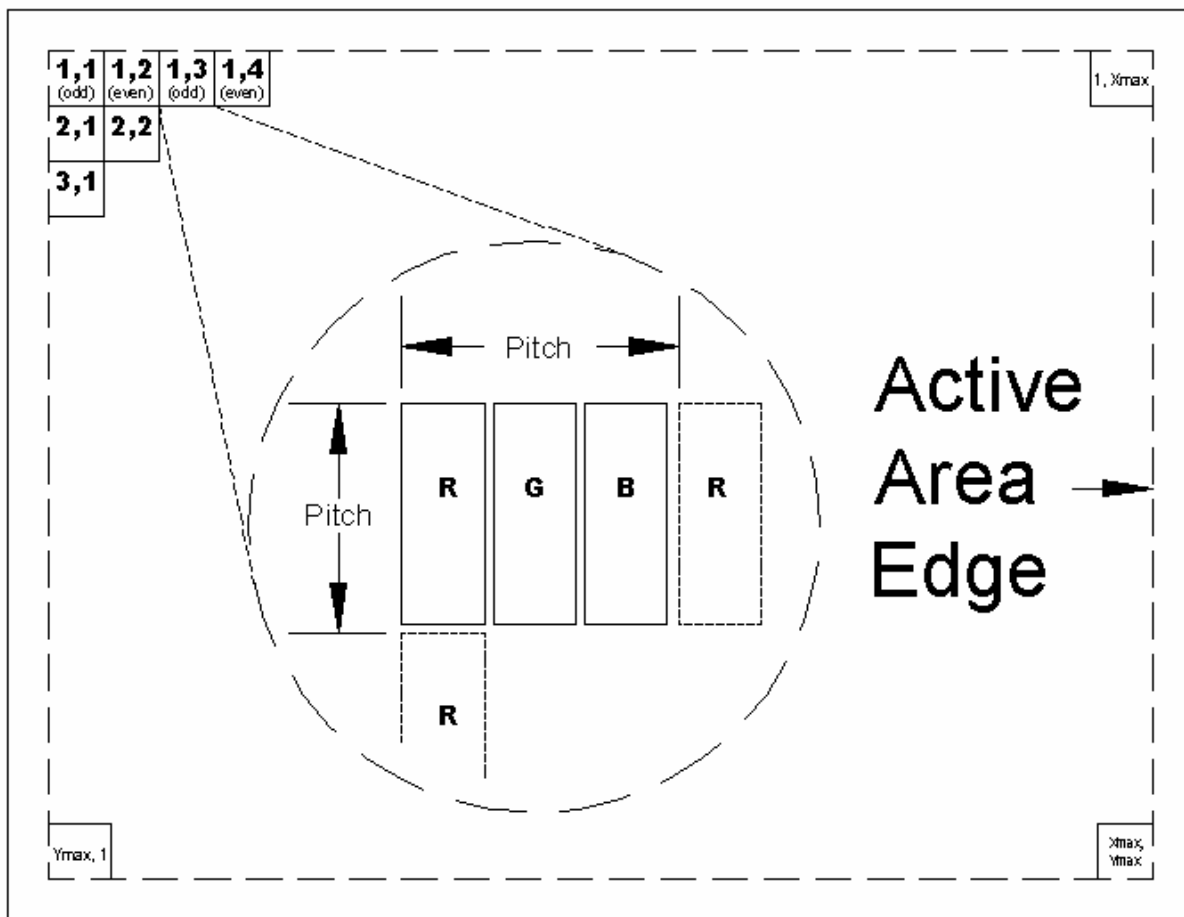


Figure 1--- Active Area Pixel Layout

3.1 LVDS Interfaced

3.1.1 LVDS Signal Interface Connector Requirements

The LVDS signal interface connector shall be as listed below. The connector keep-out area shall be designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector keying relative to pin-one designation shall be as shown on Figure 5.

3.1.2 LVDS Interface Signal Definition

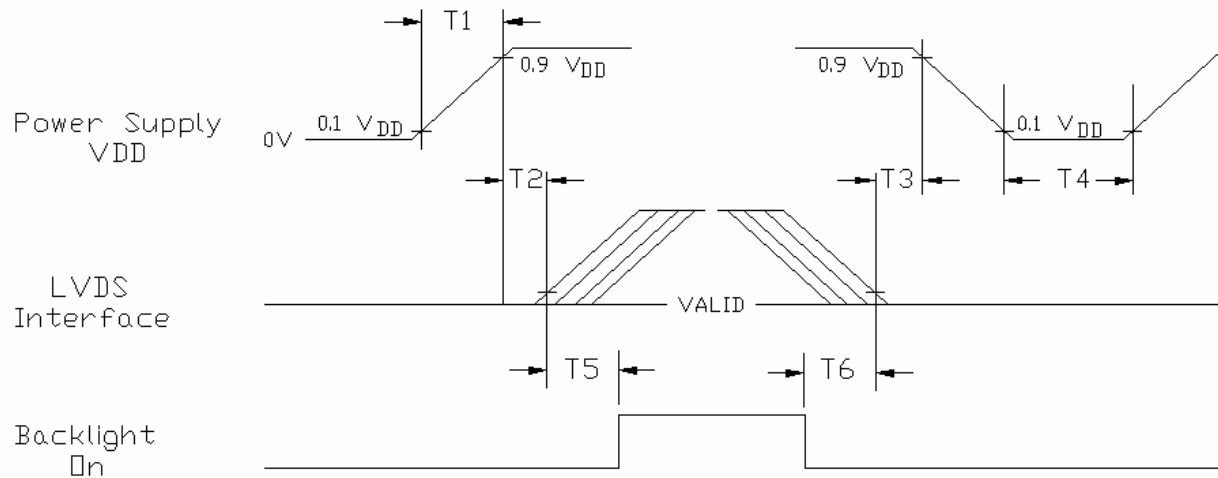
The LVDS signal interface cable shall be terminated into a JAE FI-XB30SSL-HF15, FCI 10041195, or mechanical interface equivalent connector. The interface connector pin assignments are listed in Table 1.

Pin No.	Symbol	Function
Frame	Vss	Ground
1	RXinO0-	- LVDS differential data input, Chan 0-Odd
2	RXinO0+	+ LVDS differential data input, Chan 0-Odd
3	RXinO1-	- LVDS differential data input, Chan 1-Odd
4	RXinO1+	+ LVDS differential data input, Chan 1-Odd
5	RXinO2-	- LVDS differential data input, Chan 2-Odd
6	RXinO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RXOC-	- LVDS Differential Clock input (Odd)
9	RXOC+	+ LVDS Differential Clock input (Odd)
10	RXinO3-	- LVDS differential data input, Chan 3-Odd
11	RXinO3+	+ LVDS differential data input, Chan 3-Odd
12	RXinE0-	- LVDS differential data input, Chan 0-Even
13	RXinE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RXinE1-	- LVDS differential data input, Chan 1-Even
16	RXinE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RXinE2-	- LVDS differential data input, Chan 2-Even
19	RXinE2+	+ LVDS differential data input, Chan 2-Even
20	RXEC-	- LVDS Differential Clock input (Even)
21	RXEC+	+ LVDS Differential Clock input (Even)
22	RXinE3-	- LVDS differential data input, Chan 3-Even
23	RXinE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	Vss	Ground
26	NC	No Connection
27	Vss	Ground
28	Vcc	+12.0V power supply
29	Vcc	+12.0V power supply
30	Vcc	+12.0V power supply
Frame	Vss	Ground

Table 1 --- LVDS Interface Cable Pin Assignments

3.1.3 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data / control signal sequencing of Figures 2 and 3.



$$0.5 \text{ ms} \leq T_1 \leq 10 \text{ ms} \quad 0 \leq t_2 \leq 50 \text{ ms} \quad 0 \leq t_3 \leq 50 \text{ ms} \quad 500 \text{ ms} \leq T_4 \quad 200 \text{ ms} \leq T_5 \quad 200 \text{ ms} \leq T_6$$

Figure 2 --- Logic Power and LVDS Signals Sequencing Diagram

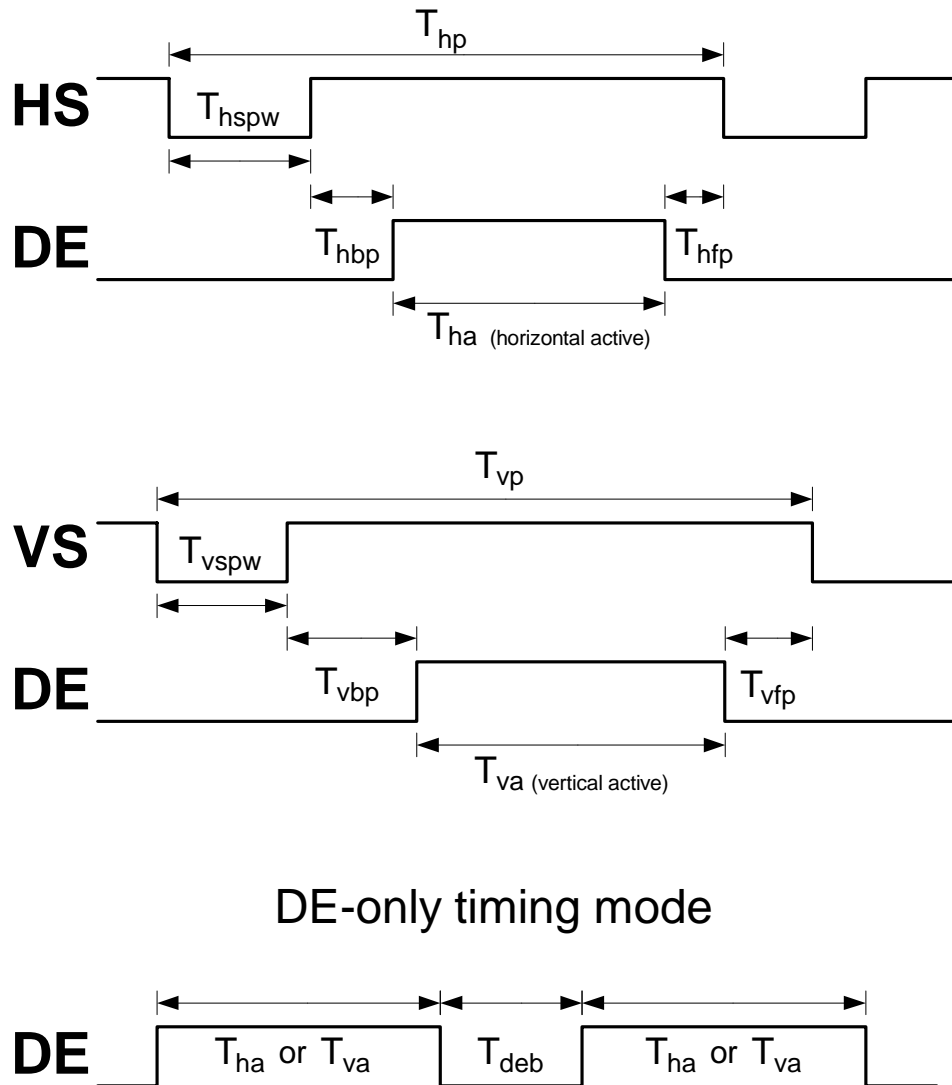
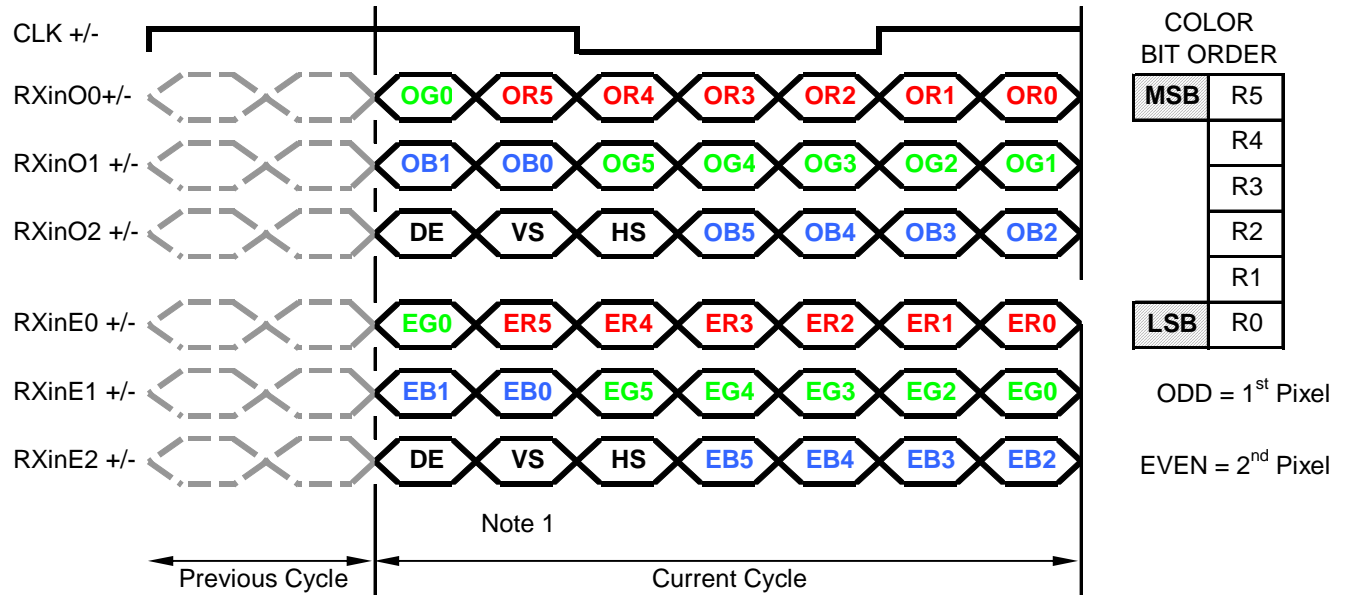


Figure 3 --- Data Enable Timing Parameters

3.1.4 LVDS Data and Control Signal Interface

The modules LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 4 shows the data mapping diagram of each LVDS channel when 6-bit color is used, Figure 5 shows the data mapping diagram of each LVDS channel when 8-bit color is used. The LVDS differential signals line-to-line termination impedance, Z_T , shall be 100 ± 10 ohms.

Dual LVDS Channel Color Mapping (6-Bit Color)



Note1: Normally, DE, VS, HS on EVEN channel are not used.

Figure 4 --- Dual LVDS Channel 6-Bit Color Mapping Diagram

COLOR BIT ORDER	
MSB	R5
	R4
	R3
	R2
	R1
LSB	R0

ODD = 1st Pixel

EVEN = 2nd Pixel

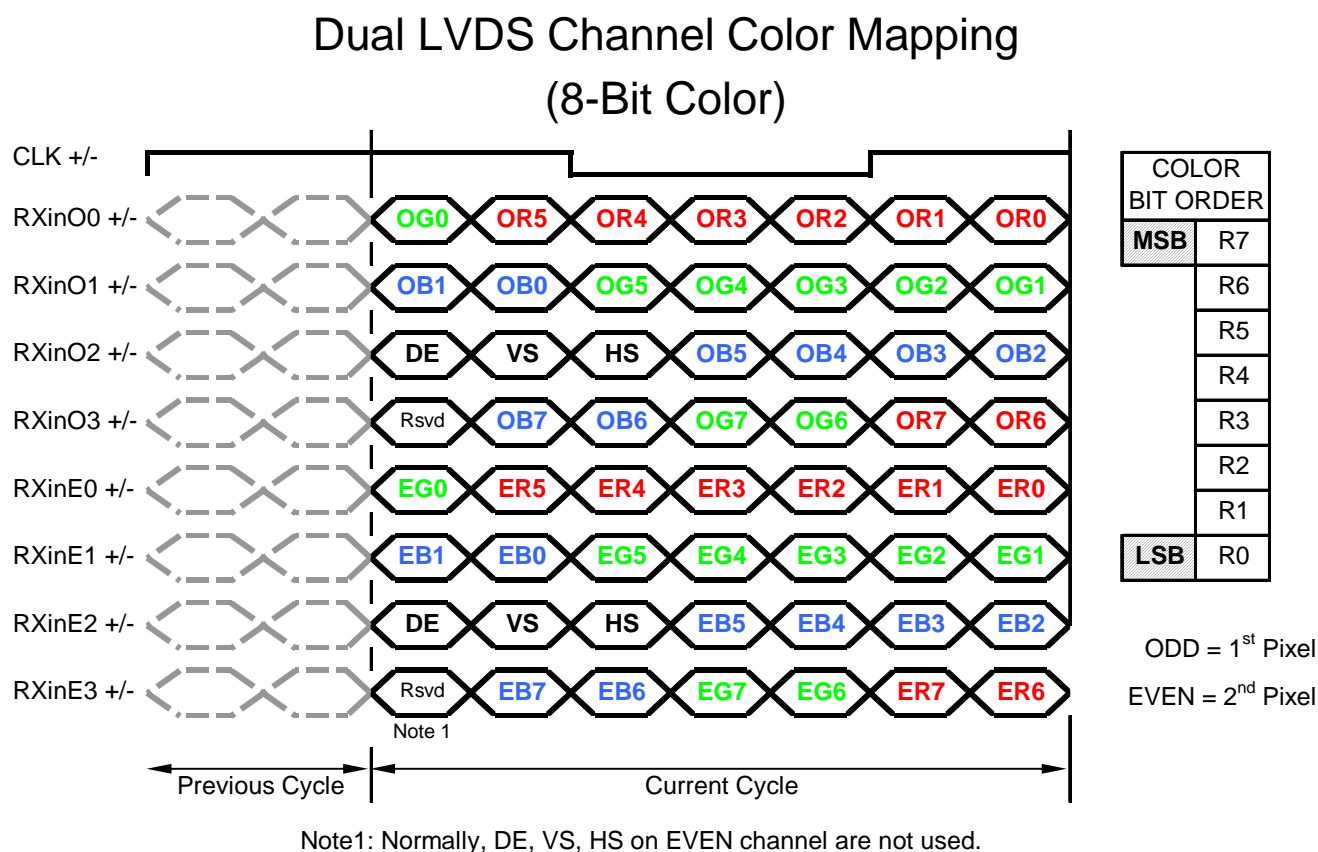


Figure 5 --- Dual LVDS Channel 8-Bit Color Mapping Diagram

3.2 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into JST BHSR-02VS-1, Sin Sheng P2408P2, Sunridge FPD-PB-35-2P or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 2.

Pin No.	Signal	Level	Function
1	V _{CCFL}	AC	Power Supply for CCFL
2	Gnd Rtn	Ground	Power return for CCFL

Table 2 --- Backlight Electrical Interface

4. Mechanical Interface Requirements

Figure 6 shows the critical exterior dimensions and connector location. indicates center point of active area.

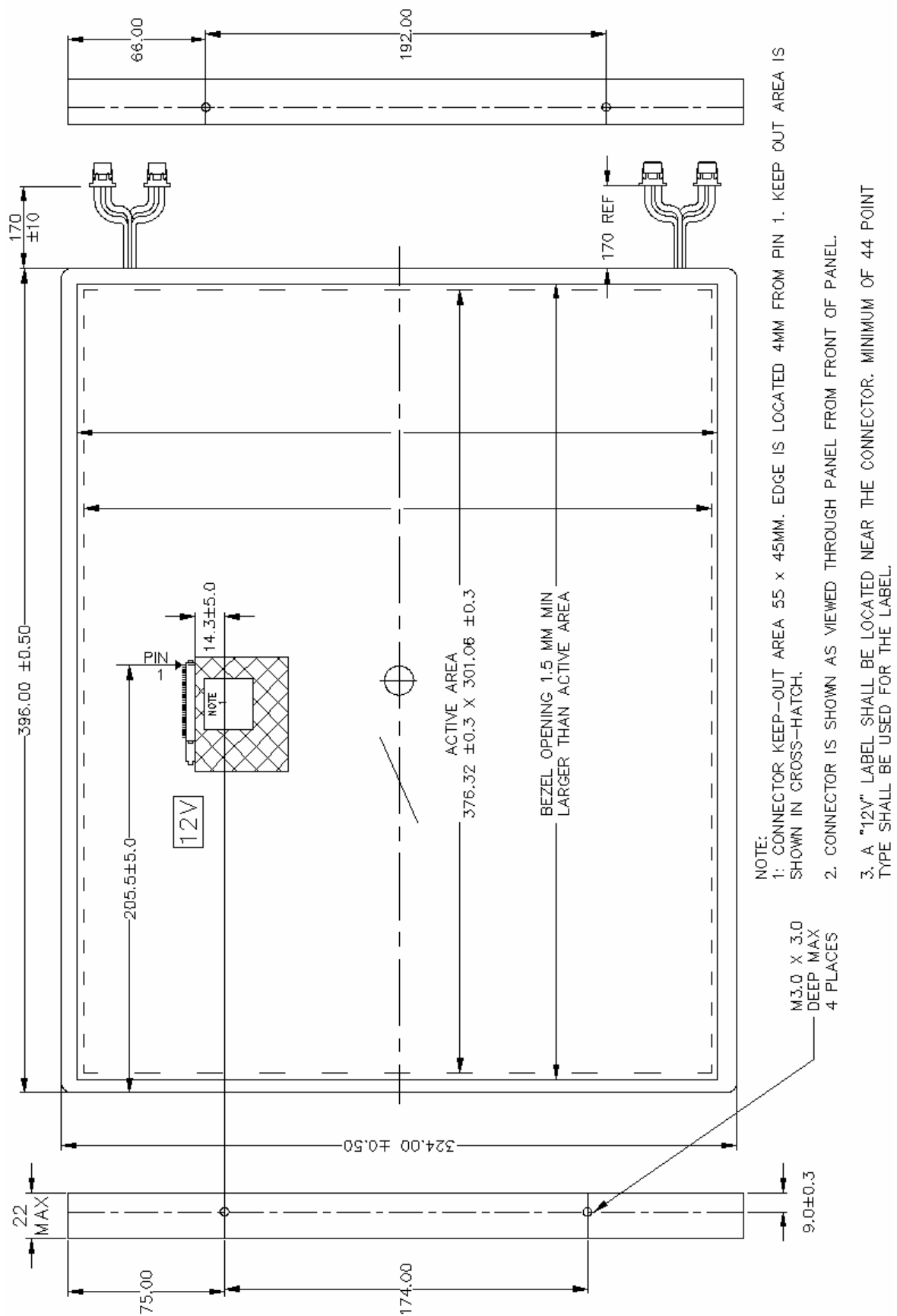


Figure 6 --- Mechanical Dimensions

Note: All dimensions in mm.

VESA Standard Panel, 19-inch, 12-volt

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Version 1

Page 12 of 14

5. Glossary of Terms

Abbreviation	Explanation
CCFL	- Cold Cathode Fluorescent Lamp
DE	- Display Enable
HS	- Horizontal Sync
LVDS	- Low Voltage Differential Signaling
T _{DEB}	- Time - Display Enable Blanking
T _{HA}	- Time - Horizontal Active
T _{HBP}	- Time - Horizontal Back Porch
T _{HFP}	- Time - Horizontal Front Porch
T _{HP}	- Total - Horizontal Period Time - Horizontal Sync Pulse
T _{HSPW}	- Width
T _{VA}	- Time - Vertical Active
T _{VBP}	- Time - Vertical Back Porch
T _{VFP}	- Time - Vertical Front Porch
T _{vspw}	- Time - Vertical Sync Pulse Width
V _{CCFL}	- Voltage for CCFL
VS	- Vertical Sync

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