



17-inch Wide Panel Standard

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VESA 17-inch Wide Panel Standard

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Purpose

This specification defines the requirements to standardize the mechanical dimensions and selected electrical interface elements of 17-inch wide format panels intended for use as LCD monitors.

This standard will help LCD manufacturers and panel consumers to better control panel supply and demand cycles.

The intent of this standard is that panels built to this specification are interchangeable without requiring alterations to tooling or drive electronics.

Summary

This proposal describes the mechanical dimensions, electrical interfaces and data formatting for 17-inch wide monitor panels.

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Preface

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Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Table 0-1: Reference Documents

Source	Name	Version / Date
TIA/EIA-644	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	March 1, 1996

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

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Revision History

Dec. 12, 2007 Initial Release of the Standard

1 Overview

1.1 Summary

This document defines the electrical interface requirements and mechanical dimensions for industry compatible 17-inch wide LCD panels.

1.2 Standard Objectives

This document establishes a common specification for 17-inch wide monitor LCD panels with the intent of creating standardization among these panels such that panels meeting this specification are interchangeable with respect to mechanical fit, electrical requirements, signal definitions and data formats.

2 System Electrical Interface Requirements

The panel's electrical interface to the system consists of two physical electrical interfaces: an LVDS interface which encodes the digital R-G-B data and timing/control signals; and a power interface for the panel backlight. This specification is only for panels with a 16:10 image format supporting a pixel format of 1,440 pixels horizontally by 900 pixels vertically.

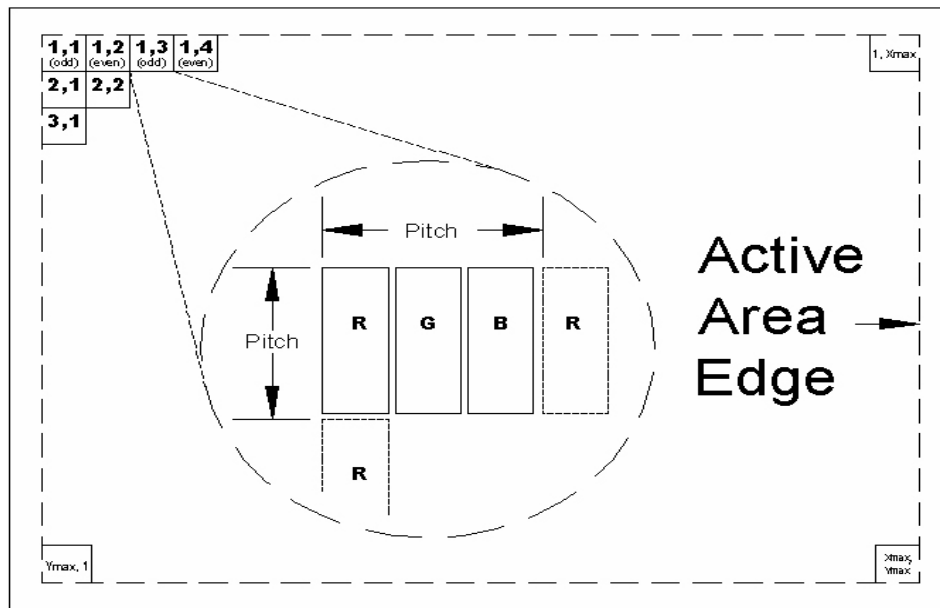


Figure 2-1: Active Area Pixel Layout

2.1 DisplayPort Interface

The DisplayPort Interface connector is described in a separate VESA standard

2.2 LVDS Interface

LVDS Signal Interface Connector Requirements.

The LVDS signal interface connector shall be as listed below. The connector keep-out area is designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. Connector orientation relative to pin-one designation shall be as shown on Figure 2.8: 17-inch Wide Standard Panel Mechanical Dimensions.

2.2.1 LVDS Interface Signal Definition

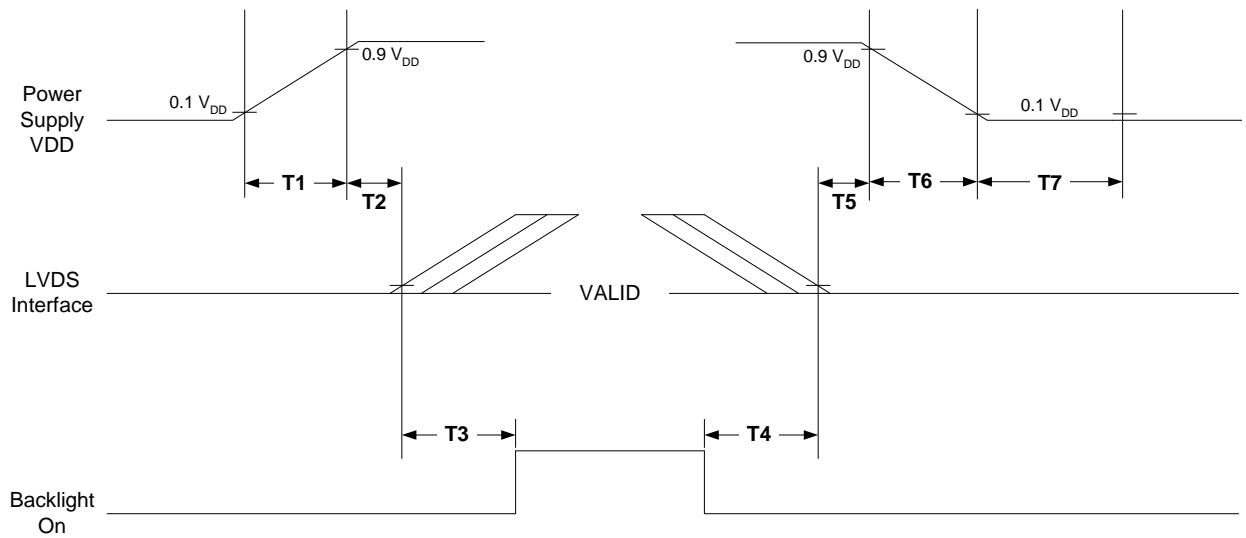
The LVDS signal interface cable shall be terminated to a JAE FI-XB30SSRL-HF16 or equivalent connector. This connector is a locking type. The interface connector pin assignments are listed below.

Table 2-1: LVDS Connector Pin Assignments

Pin No.	Symbol	Function
	Frame	Ground
1	RxO0-	- LVDS differential data input, Chan 0-Odd
2	RxO0+	+ LVDS differential data input, Chan 0-Odd
3	RxO1-	- LVDS differential data input, Chan 1-Odd
4	RxO1+	+ LVDS differential data input, Chan 1-Odd
5	RxO2-	- LVDS differential data input, Chan 2-Odd
6	RxO2+	+ LVDS differential data input, Chan 2-Odd
7	Vss	Ground
8	RxOC-	- LVDS Differential Clock input (Odd)
9	RxOC+	+ LVDS Differential Clock input (Odd)
10	RxO3-	- LVDS differential data input, Chan 3-Odd
11	RxO3+	+ LVDS differential data input, Chan 3-Odd
12	RxE0-	- LVDS differential data input, Chan 0-Even
13	RxE0+	+ LVDS differential data input, Chan 0-Even
14	Vss	Ground
15	RxE1-	- LVDS differential data input, Chan 1-Even
16	RxE1+	+ LVDS differential data input, Chan 1-Even
17	Vss	Ground
18	RxE2-	- LVDS differential data input, Chan 2-Even
19	RxE2+	+ LVDS differential data input, Chan 2-Even
20	RxEC-	- LVDS Differential Clock input (Even)
21	RxEC+	+ LVDS Differential Clock input (Even)
22	RxE3-	- LVDS differential data input, Chan 3-Even
23	RxE3+	+ LVDS differential data input, Chan 3-Even
24	Vss	Ground
25	NC	No Connection
26	NC	No Connection
27	NC	No Connection
28	Vcc	+ 5 Volts
29	Vcc	+ 5 Volts
30	Vcc	+ 5 Volts

2.2.2 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data/control signal sequencing of Figures 2-2, 2-3 and 2-4.



	Minimum time (ms)	Maximum time (ms)
T1	0.5	10
T2	0.0	50
T3	1000	-
T4	200	-
T5	0.0	50
T6	0.01	1000
T7	1000	-

Figure 2-2: Logic Power and LVDS Signals Sequencing Diagram

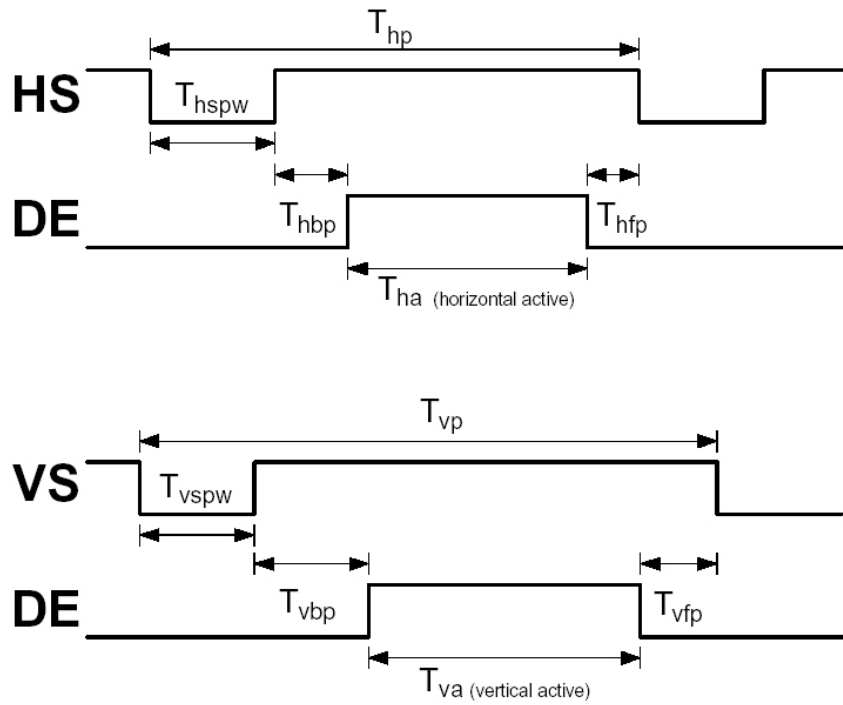


Figure 2-3: Data Enable Timing

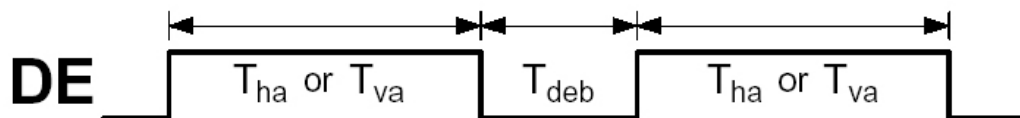


Figure 2-4: DE Only Timing Mode

2.2.3 LVDS Data and Control Signal Interface

The module's LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 2-5 shows the data mapping diagram of each LVDS channel when 8-bit color is used, Figure 2-6 shows the data mapping diagram of each LVDS channel when 6-bit color is used. The LVDS differential signals line-to-line termination impedance, ZT, shall be 100 ± 10 ohms.

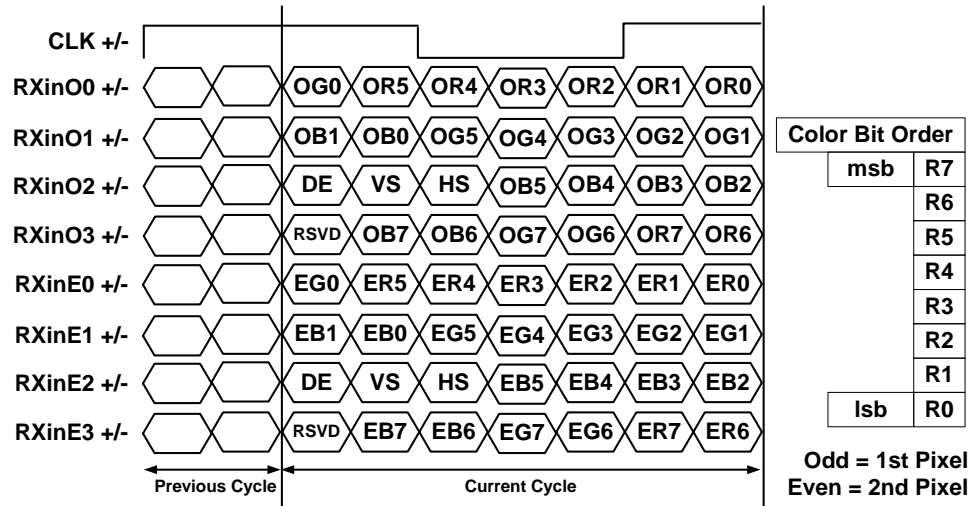


Figure 2-5: Dual LVDS Channel Color Mapping (8-bit)

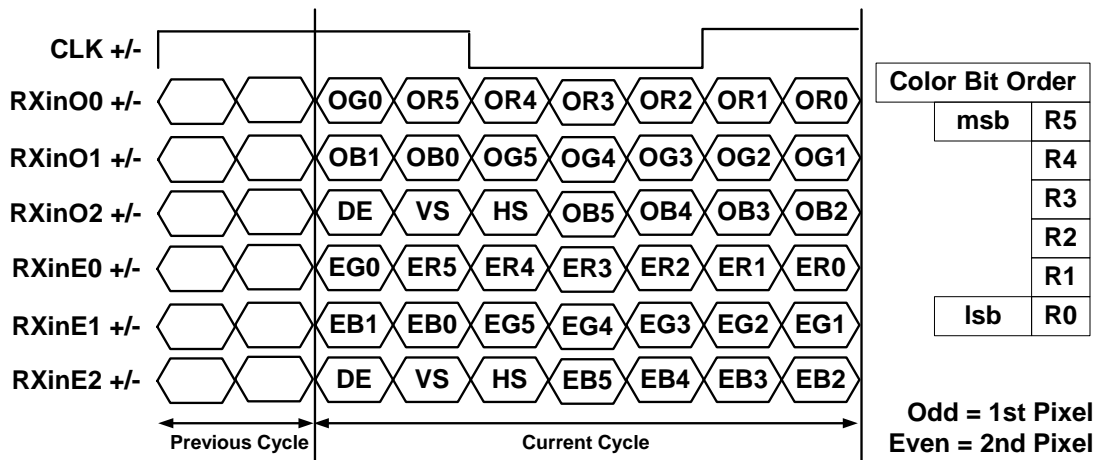


Figure 2-6: Dual LVDS Channel Color Mapping (6-bit)

2.3 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into JST BDBR-03 (4.0) V-1S locking (JST), BHR-03VS-1 non-locking (JST) or equivalent connectors. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in the figure below.

Table 2-2: Lamp Connector Configuration

PIN	Symbol	Description
1	HV	High Voltage
2	LV	Low Voltage
1	HV	High Voltage
2	LV	Low Voltage

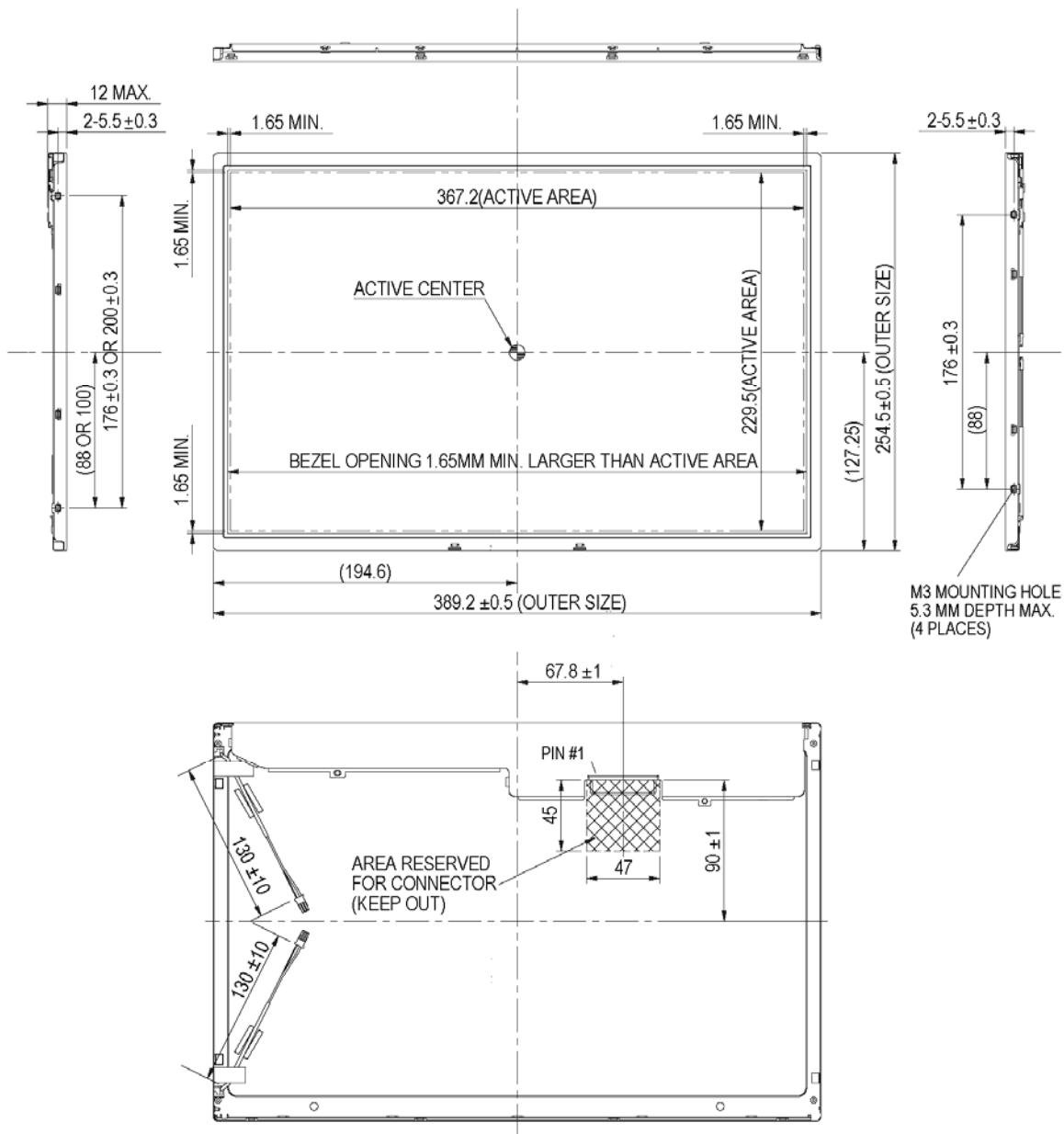


Figure 2-7: 17-inch Wide Standard Monitor Panel Mechanical Dimension

Drawing Notes:

1. All dimensions in mm.
2. Drawing not to scale.
3. Interface connector specification: FI-XB30SSRL-HF16 (JAE) or equivalent.
4. Lamp connector specification: Locking type - BDBR-03 (4.0) V-1S (JST) or equivalent. Non-locking type: BHR-03VS-1(JST) or equivalent
5. Torque per mounting hole: 2.5~3.5kgf-cm.
6. Panel weight specification: 1,350±100g.

Glossary of Terms

Abbreviation	Meaning
CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
lsb	Least Significant Bit
LVDS	Low Voltage Differential Signaling: TIA/EIA-644
msb	Most Significant Bit
NC	No Connection
T _{deb}	Time - Display Enable Blanking
T _{ha}	Time - Horizontal Active
T _{hbp}	Time - Horizontal Back Porch
T _{hfp}	Time - Horizontal Front Porch
T _{hp}	Time - Total Horizontal Period
T _{hspw}	Time - Horizontal Sync Pulse Width
T _{va}	Time - Vertical Active
T _{vbp}	Time - Vertical Back Porch
T _{vfp}	Time - Vertical Front Porch
T _{vp}	Time - Total Vertical Period
T _{vspw}	Time - Vertical Sync Pulse Width
VBR	Backlight Brightness
VIN	Backlight Power
VON/OFF	Backlight On / Off
VS	Vertical Sync