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VESA Notebook Panel Standard

Version 1
October 22, 2007

Purpose

This specification defines the requirements for standardization of mechanical dimensions and selected electrical interface requirements of LCD panels intended for use in the notebook computers. This will enable LCD manufacturers and panel consumers to better control supply and demand cycles.

Panels built to this specification will be able to be used in most applications without requiring alterations in either the product tooling or the display module.

Summary

This Document will replace all current (as of this publication date) notebook panel standards by consolidating them into this document.

In addition to the older panel standards we have added a 20.1 wide panel and defined the LVDS interface in more detail.

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Revision History

October 22, 2007 Initial release of Notebook Panel Standard, Version 1

1. Overview

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for industry compatible panels for notebook and similar applications.

1.2 Standard Objectives

This document establishes common standard panels that can be mounted in any notebook case designed to accept the maximum defined size. The dimensioning allows panel suppliers some product differentiation while meeting the goal of transparent usage across different platforms.

1.3 Reference Documents

Table 1-1: Reference Documents

Document	Version / Revision	Date
VESA Policy 200B Intellectual Property Rights	Version B	Feb 2005
VESA Glossary of Terms (www.vesa.org)	Current	Current
ANSI/TIA/EIA-644-A Electrical Characteristics Of Low Voltage Differential Signaling (LVDS) Interface Circuits	Revision A	Feb 2001
ANSI/EIA-364-D Electrical Connector/Socket Test Procedures Including Environmental Classifications	Revision D	July 2001
JSA JIS C 5402 Methods For Test Of Connectors For Use In Electronic Equipment	Revision 92	Mar 2004
SPWG	Version 2.0	Sep 2005
VESA Flat Panel Display Measurements (FPDM2)	Version 2.0	Jun 2001
VESA Enhanced Display Data Channel Standard (E-DDC)	Version 1	Sep 1999
VESA E-EDID Standard	Rel. A/ Rev. 2	Sep 2006
VESA Coordinated Video Timings Spreadsheet	Revision 1.1	Apr 2003
VESA Coordinated Video Timings (CVT)	Version 1.1	Sep 2003
VESA Coordinated Video Timing Generator	Revision 1.1	Apr 2003

2. System Electrical Interface Requirements

The panel's electrical interface to the system consists of LVDS interface which encodes the digital R-G-B data and timing control signals, and a power interface for the panel backlight.

2.1 Panel Resolution and Aspect Ratio

The notebook panel resolution and aspect ratios covered by this specification are shown in the Table 2-1.

Table 2-1: Panel Size, Resolution and Aspect Ratio

Panel Size	Resolution	Pixels	# of pixels	Aspect Ratio
12.1"	XGA	1024x768	0.7M	4:3
	SXGA+	1400x1050	1.4M	4:3
13.3"	XGA	1024x768	0.7M	4:3
	SXGA+	1400x1050	1.4M	4:3
14.1"	XGA	1024x768	0.7M	4:3
	SXGA+	1400x1050	1.4M	4:3
15.0"	XGA	1024x768	0.7M	4:3
	SXGA+	1400x1050	1.4M	4:3
	UXGA	1600x1200	1.9M	4:3
12.1"W	WXGA	1280x800	1M	16:10
	WXGA+	1440x900	1.2M	16:10
	WSXGA+	1680x1050	1.7M	16:10
13.3"W	WXGA	1280x800	1M	16:10
	WXGA+	1440x900	1.2M	16:10
	WSXGA+	1680x1050	1.7M	16:10
14.1"W	WXGA	1280x800	1M	16:10
	WXGA+	1440x900	1.2M	16:10
	WSXGA+	1680x1050	1.7M	16:10
15.4"W	WXGA	1280x800	1M	16:10
	WXGA+	1440x900	1.2M	16:10
	WSXGA+	1680x1050	1.7M	16:10
	WUXGA	1920x1200	2.3M	16:10
17.0"W	WXGA	1280x800	1M	16:10
	WXGA+	1440x900	1.2M	16:10
	WSXGA+	1680x1050	1.7M	16:10
	WUXGA	1920x1200	2.3M	16:10
19.0'W	WSXGA+	1680x1050	1.7M	16:10
	WUXGA	1920x1200	2.3M	16:10
20.1"W	WSXGA+	1680x1050	1.7M	16:10
	WUXGA	1920x1200	2.3M	16:10

2.2 Active Area Pixel Layout

Figure 2-1 shows the standard pixel format for the Notebook LCD panel's active display area.

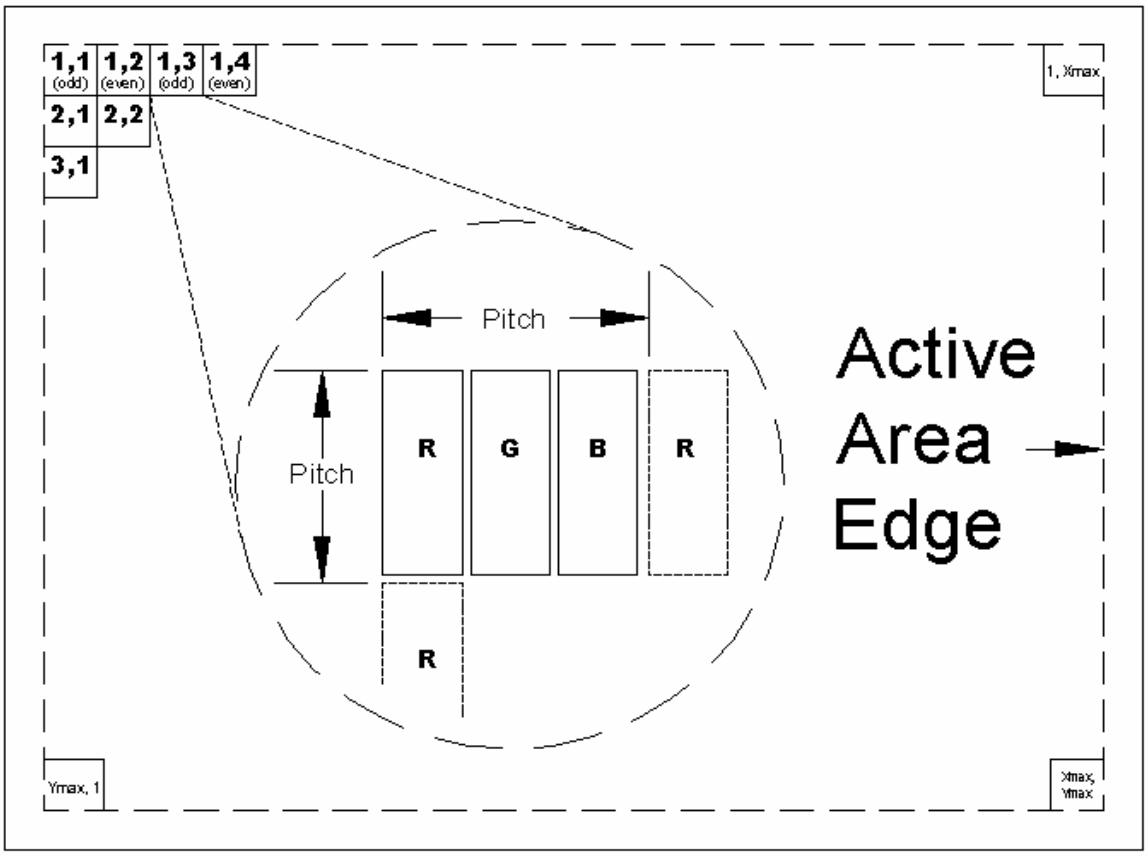


Figure 2-1: Active Area Pixel Format

3. LVDS Interface Signal Definition

3.1 Electrical Characteristics

The LVDS interface circuit is shown in Figure 3-1. The circuit consists of three parts: the generator (G), the balanced interconnecting media, and the load. The load is composed of termination impedance and receiver(s) (R). The receiver may incorporate the termination impedance internal to the integrated circuit package. The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the balanced interconnecting media is described in terms of its electrical characteristics.

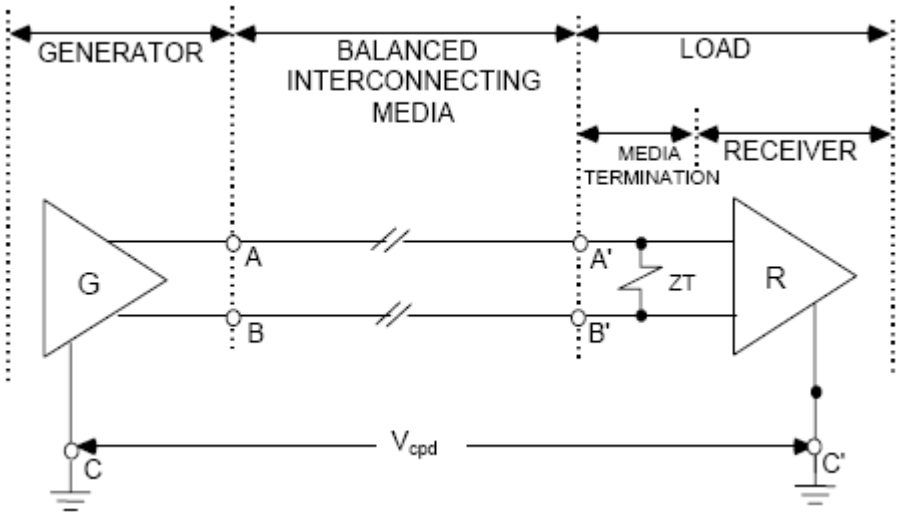


Figure 3-1: LVDS Interface Circuit

Legend:
G = Generator R = Receiver
A = Generator interface point A' = Receiver interface point
B = Generator interface point B' = Receiver interface point
C = Generator circuit common C' = Receiver circuit common
ZT = Termination impedance
Vcpd = Common potential difference

3.2 LVDS Generator Characteristics

The generator electrical characteristics are specified in accordance with the measurements in Table 3-1. A generator circuit meeting these requirements results in a balanced source that will produce a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV.

Table 3-1: LVDS Transmitter Electrical Characteristics

Name	Definition	Condition	Min	Typ	Max	Unit
V_{OD}	Normal Differential Output Voltage	R_L=100Ω	250	-	450	mV
	Reduced Differential Output Voltage		100	-	300	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States		-	-	35	mV
V_{OS}	Offset Voltage		1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States		-	-	35	mV
I_{OS}	Output Short Circuit Current		-	-	24	mA
I_{OZ}	Output TRY-STATE Current		-	-	10	µA
V_{ID}	Differential input voltage		0.1	-	0.6	V

The signaling sense of the voltages appearing across the termination resistor is defined in Figure 3-2 as follows:

a) The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 or OFF state.
b) The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 or ON state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

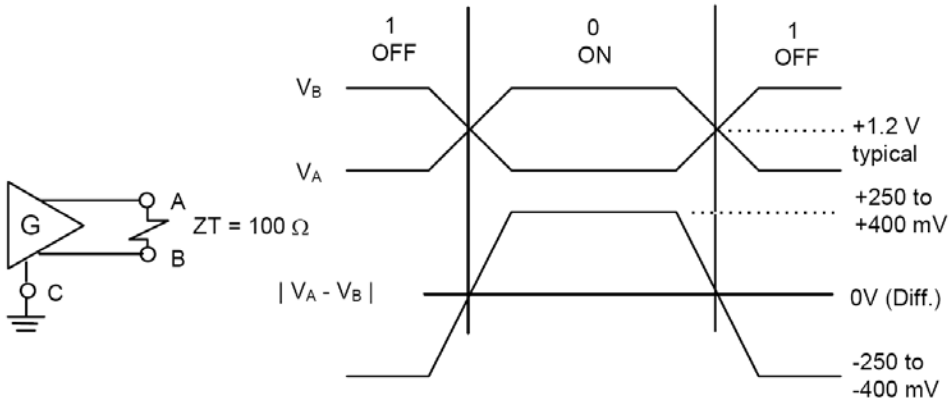


Figure 3-2: LVDS Signal Sense

3.3 Full Load Test Measurement

With a test load of three resistors, 100 Ω ±1% between the A and B generator output terminals, and 3.75 kΩ ±1% between each generator output terminal and a common mode supply (V_{CM}), as shown in Figure 3-5, the steady-state magnitude of the differential output voltage (VT), shall be greater than or equal to 247 mV and less than or equal to 454 mV with the common-mode voltage varied from Ground to +2.4 V. For the opposite binary state, the polarity of VT shall be reversed (VT *). The steady-state magnitude of the difference between VT and VT * shall be 50 mV or less.

$$247\ mV < |\ V_T\ | < 454\ mV$$
$$247\ mV < |\ V_T^*\ | < 454\ mV$$
$$|\ V_T\ | - |\ V_T^*\ | < 50\ mV$$

The 100 Ω resistor represents a typical termination load, and the 3.75 kΩ resistors represent the combined impedance of 32 receiver loads connected to the bus. The V_{CM} power supply represents the allowable range of biasing that the receivers may present to the bus.

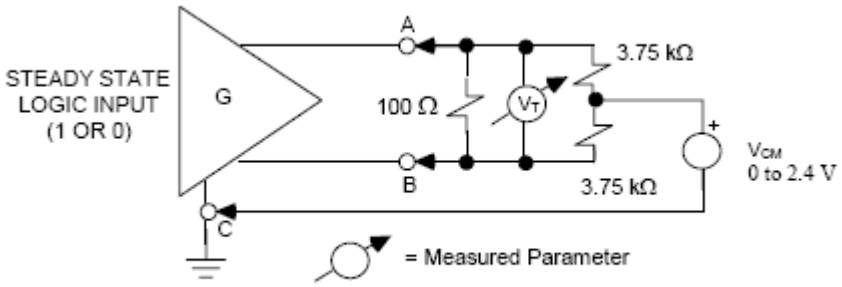


Figure 3-3: Full Load Test Measurement

3.4 Offset Voltage and Balance Measurement

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the steady-state magnitude of the generator offset voltage (V_{OS}), measured between the center point of the test load and the generator circuit common shall be greater than or equal to 1.125 V and less than or equal to 1.375 V for either binary state. The steady state magnitude of the difference of V_{OS} for one binary state and V_{OS} * for the opposite binary state shall be 50 mV or less.

$$\mathbf{1.125\ V \le V_{OS} \le 1.375\ V}$$
$$\mathbf{1.125\ V \le V_{OS}^* \le 1.375\ V}$$
$$\mathbf{|\ V_{OS}| - |V_{OS}^*| \le 50\ mV}$$

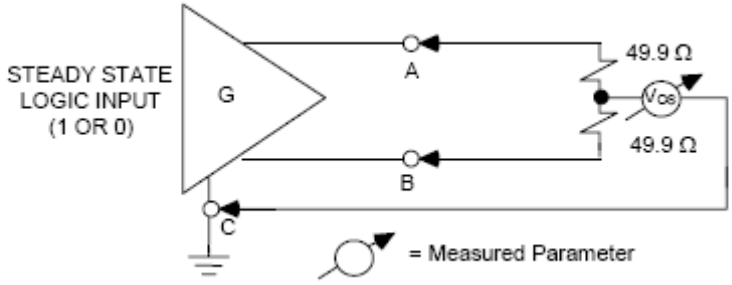


Figure 3-4: Test Termination Measurement

3.5 Short-circuit Measurement

With the generator output terminals short-circuited to the generator circuit common, the magnitudes of the currents (I_{SA} and I_{SB}) following through each output terminal shall not exceed 24.0 mA drop for either binary state.

$$| I_{SA} | \leq 24.0 \text{ mA}$$
$$| I_{SB} | \leq 24.0 \text{ mA}$$

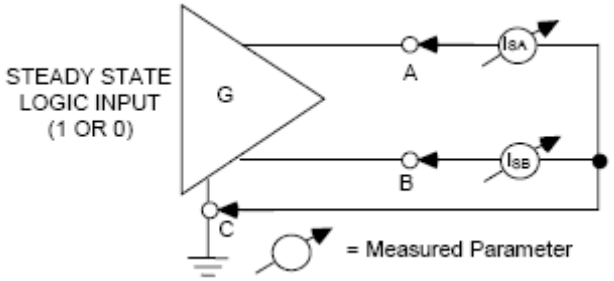


Figure 3-5: Short Circuit Measurement to Circuit Common

With the generator output terminals short-circuited to each other, the magnitude of the current (I_{SAB}) following through the output terminals shall not exceed 12.0 mA for either binary state.

$$| I_{SAB} | \leq 12.0 \text{ mA}$$

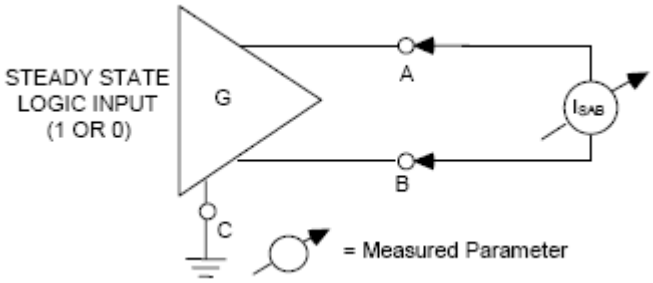


Figure 3-6: Short-circuit Measurement

3.6 Dynamic Output Signal Balance

During transitions of the generator output between alternating binary states (one-zero one-zero, etc.), the resulting imbalance of the offset voltage (V_{OS}) measured between the matched 49.9 Ω ±1% test load resistors (RL) to circuit common (C) and with a maximum lumped capacitance test load of 5 pF (CL) connected as shown in Figure 3-7 should not vary more than 150 mVpp (peak-to-peak). Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.

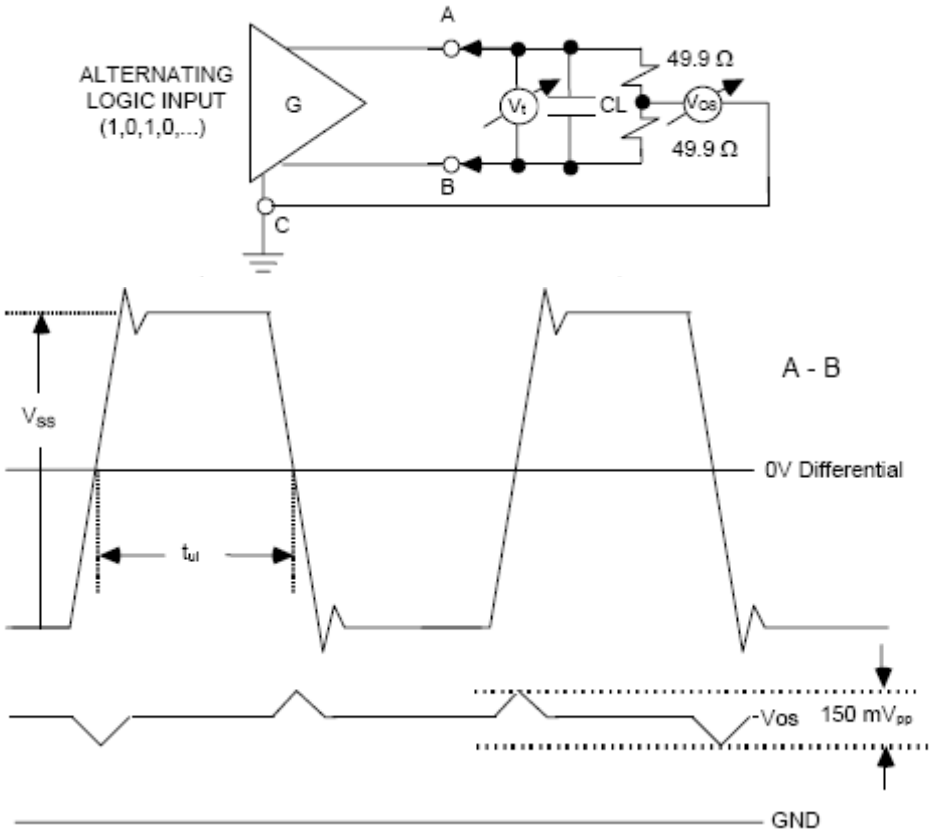


Figure 3-7: Dynamic Output Signal Balance Waveform

3.7 LVDS Receiver Characteristics

The load is defined as an impedance between A' and B' and is composed of a termination impedance and a receiver as shown in Figure 3-1.

Table 3-2: LVDS Received Electrical Characteristics

Name	Definition	Condition	Min	Typ	Max	Unit
V_{TH}	Differential Input High Threshold	V_{CM}=1.2V	-	-	+100	mV
V_{TL}	Differential Input Low Threshold		-100	-	-	mV
I_{IN}	Input Current				±10	µA
V_{ID}	Differential Input Voltage		100		600	mV
V_{CM} [*1]	Common-mode input voltage	Vdd = 3.3V (typical)	$\|V_{ID}\|/2$		2.4 - $\|V_{ID}\|/2$	V
		Vdd = 2.5V (typical)	$\|V_{ID}\|/2$		V_{DD} - 0.4 - $\|V_{ID}\|/2$	

Note:[*1)] LVDS V_{DD} is 3.3V or 2.5V in the industry standard macro design, depending on the process technology used and cell characteristics required. When V_{DD} is 2.5V, the LVDS macro can not normally meet with the original V_{CM} requirement of $|V_{ID}|/2$ to 2.4 - $|V_{ID}|/2$, due to its circuit architecture. As shown in Table 3-2, a separate V_{CM} specification has been defined for 2.5V V_{DD}. In EIA/TIA-644 standard, LVDS generator

V_{CM} range and receiver V_{CM} range differ for situations where LVDS generator and receiver ground levels may differ. In LCD applications, however, we generally assume that the ground is common to the generator and the receiver. This V_{CM} specification for 2.5V V_{DD} will still ensure the proper function as long as the LVDS generator meets with V_{OS} specification of 1.125 to 1.375V. For brevity, the following sections assume 3.3V V_{DD} when V_{CM} is mentioned. However, for the actual V_{CM} requirement, refer to Table 3-2.

3.8 LVDS Receiver Current-voltage Measurement

With the voltage Via (or Vib) ranging from 0 V to +2.4 V while Vib (or Via) is held at +1.2 V ± 50 mV, the resultant input current Iia (or Iib) shall be no greater than 20 μA in magnitude. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

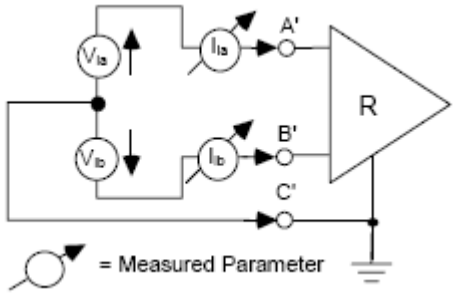


Figure 3-8: Receiver Input Current -voltage Measurement

3.9 LVDS Receiver Input Balance Measurements

The balance of the input currents (IA' and IB') shall be 6 uA or less for all test voltages between o and 2.4 V.

$$| I_{A'} - I_{B'} | <= 6\ uA$$

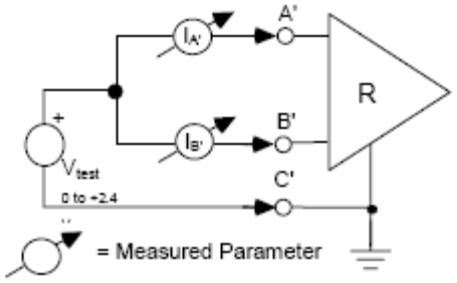


Figure 3-9: Receiver Input Balance Measurement

3.10 Terminating Receiver Input Current – Voltage Measurements and Input Impedance Measurement

With the applied voltage (Vin) and forced current (Iin) listed in Table 3.3 applied to the corresponding inputs, the resultant differential input voltage magnitude (Vid) shall be between the values listed in the table. The test circuit is shown in Figure 3-10 and applies only to receivers that provide internal termination impedance. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

Table 3-3: Receiver Input Current-voltage Measurement for Terminating Receiver

Applied Voltage V_{In} (V)	Forced Loop Current I_{In} (mA)	Switch Position S1 - S2	Resulting Input Voltage V_r (V)	Resulting Differential Input Voltage Range - V_{Id} (mV)
2.4	- 2.5	A' - B'	2.070 to 2.175	+225 to +330
2.4	- 4.5	A' - B'	1.806 to 1.995	+405 to +596
2.4	- 2.5	B' - A'	2.070 to 2.175	-225 to -330
2.4	- 4.5	B' - A'	1.806 to 1.995	-405 to -596
0	- 2.5	A' - B'	0.225 to 0.330	-225 to -330
0	- 4.5	A' - B'	0.405 to 0.594	-405 to -596
0	- 2.5	B' - A'	0.225 to 0.330	+225 to +330
0	- 4.5	B' - A'	0.405 to 0.594	+405 to +596

Note: Current into a terminal is positive, and current out of a terminal is negative

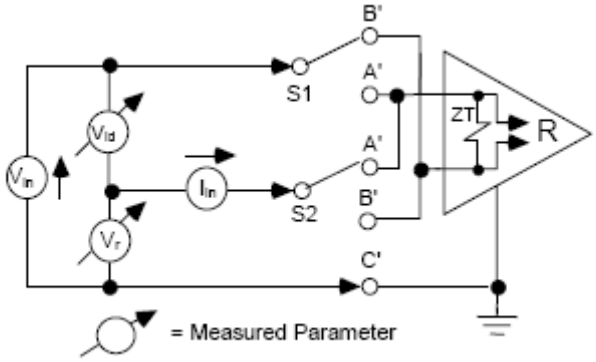


Figure 3-10: LVDS Signal Sense

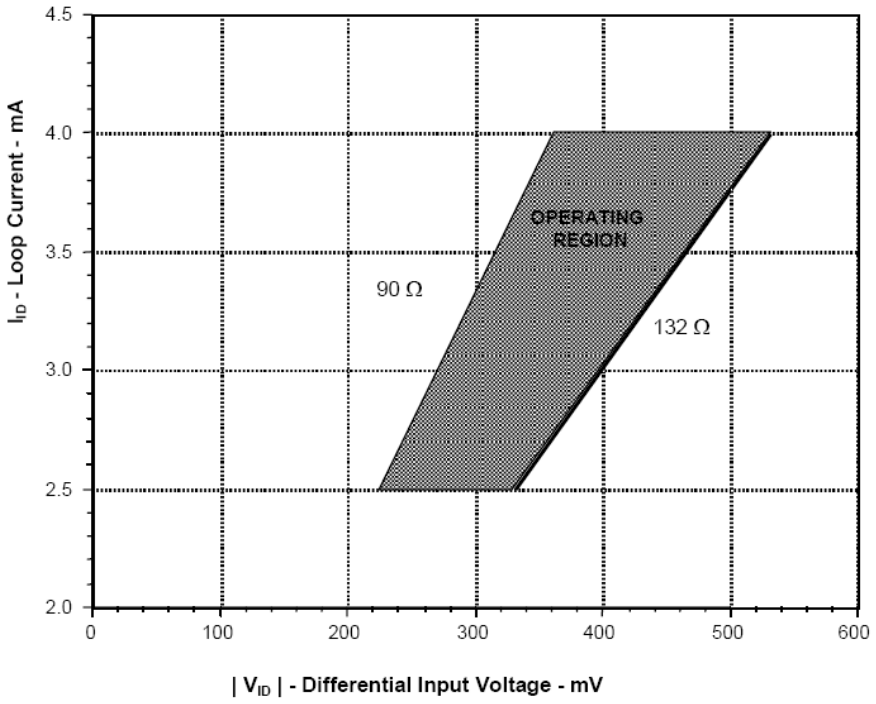


Figure 3-11: Terminating Receiver Input Current vs. Input Voltage Range

Note: The internal termination impedance may be a simple resistor incorporated into the package, integrated on the die, or composed of active devices on the die. The exact structure of the termination impedance is beyond the scope of this Standard.

The input impedance of the terminating receiver is dominated by the low impedance differential termination impedance (ZT). The resulting input impedance calculated from the measurements describe in table 3-3 shall be greater than or equal to 90 Ω, and less than or equal to 132 Ω.

90 Ω ZT 132 Ω

3.11 Receiver Input Sensitivity Measurement

Over an entire common mode voltage range of +0.050 V to +2.350 V (referenced to receiver circuit common), the receiver shall not require a differential input voltage of more than ±100 mV (threshold) to correctly assume the intended binary state.

Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 100 mV and 600 mV in magnitude. The maximum voltage applied to either the A' or B' terminals shall not greater than +2.4 V, or be less than 0 V with respect to receiver circuit common. The maximum differential input voltage applied to the receiver is 2.4 V with no damage occurring to the receiver inputs.

Thresholds ≤ ±100 mV (differential)
100 mV ≤ Valid Differential Input Voltage Range ≤ 600 mV
0 V ≤ Valid Input Voltage (to circuit common) ≤ +2.4 V

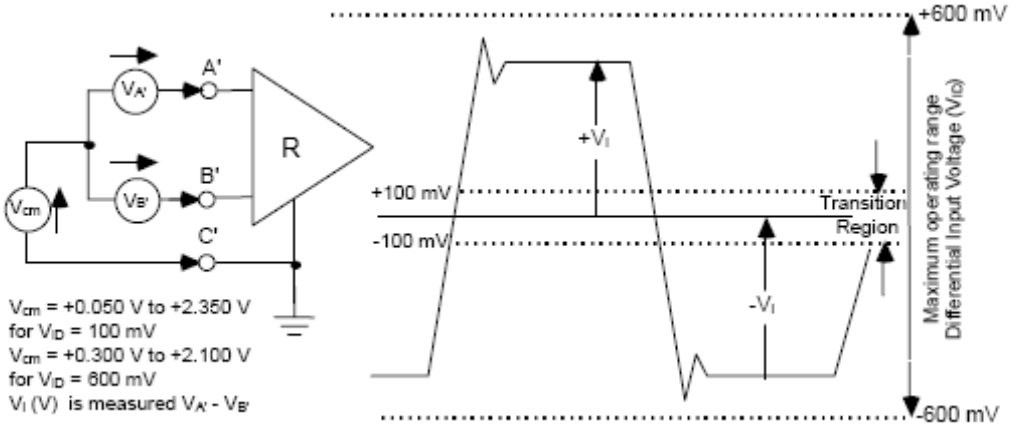


Figure 3-12: Receiver Input Sensitivity Measurements

The minimum and maximum operating voltages of the receiver (input voltage, differential input voltage, and common mode input voltage), and the test circuit is shown in Figure 3-13.

Table 3-4: Receiver Minimum and Maximum Operating Voltages

Applied Voltages (Input Voltage - referenced to circuit common - C')		Resulting Differential Input Voltage	Resulting Common Mode Input Voltage	Reason of Test
V_{ia}	V_{ib}	V_{ID}	V_{CM}	
+1.250 V	+1.150 V	+100 mV	+1.200 V	To guarantee operation with minimum V_{ID} applied versus V_{CM} range
+1.150 V	+1.250 V	-100 mV	+1.200 V	
+2.400 V	+2.300 V	+100 mV	+2.350 V	
+2.300 V	+2.400 V	-100 mV	+2.350 V	
+0.100 V	0 V	+100 mV	+0.050 V	
0 V	+0.100 V	-100 mV	+0.050 V	
+1.500 V	+0.900 V	+600 mV	+1.200 V	To guarantee operation with maximum V_{ID} applied versus V_{CM} range
+0.900 V	+1.500 V	-600 mV	+1.200 V	
+2.400 V	+1.800 V	+600 mV	+2.100 V	
+1.800 V	+2.400 V	-600 mV	+2.100 V	
+0.600 V	0 V	+600 mV	+0.300 V	
0 V	+0.600 V	-600 mV	+0.300 V	

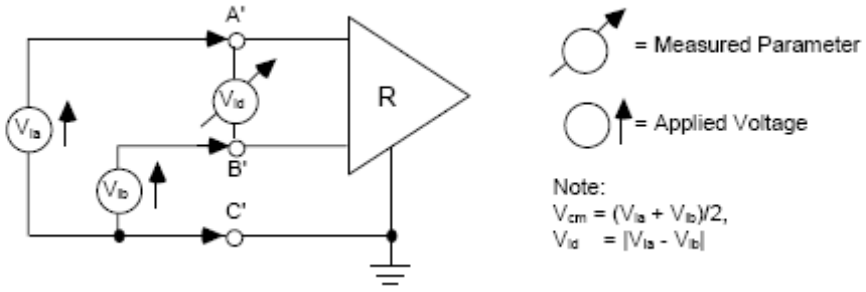


Figure 3-13: Receiver Input Sensitivity Measurements

3.12 Termination

All applications shall use termination impedance. The recommended value is between 90 Ω and 132 Ω. The actual value should be selected to match the media characteristic impedance (±10%) at the application frequency. If the termination impedance is not integrated into the receiver circuit, it shall be located at the load end of the balanced interconnecting media, as close to the receiver input as possible to minimize the resulting stub length between the termination impedance and the receiver input.

The value of this external impedance (ZT) is in the range of 90 Ω to 132 Ω. Ideally, the resistor value is equal to the characteristic impedance of the media or greater in value to minimize negative signal reflections. The media termination is shown in Figures 3-13 and 3-14.

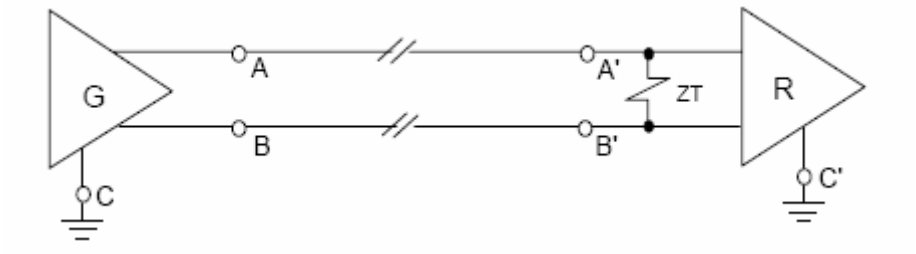


Figure 3-14: LVDS Point-to-Point Application with External Termination

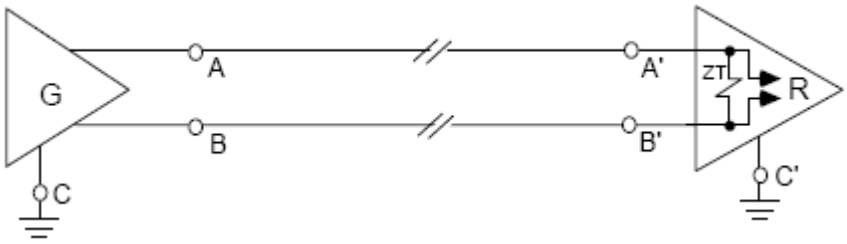


Figure 3-15: LVDS Point-to-Point Application with Internal Termination

Note: Matching of impedance of the PCB traces, connectors and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path should be minimized since they degrade the signal path and may cause reflections of the signal.

3.13 Failsafe Operation

Other standards and specifications using the electrical characteristics of the LVDS interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following:

1) Generator in power-off condition
2) Receiver not connected with the generator
3) Open-circuited interconnecting cable
4) Short-circuited interconnecting cable
5) Input signal to the load remaining within the transition region (±100 mV) for an abnormal period of time (application dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified:

1) Which interchange circuits require fault detection
2) What faults must be detected
3) What action must be taken when a fault is detected; the binary state that the receiver assumes
4) What is done does not violate this standard

The method of detection of fault conditions is application dependent and is therefore not further specified as it is beyond the scope of this Standard.

3.14 Circuit Protection

The LVDS interface generator and receiver devices, under either the power-on or power-off condition, complying with this Standard shall not be damaged under the following conditions:

a. Generator open circuit.
b. Short-circuit across the balanced interconnecting media.
c. Short-circuit to common.

4. LVDS Signal Interface Connector Requirements

4.1 LVDS 6 Bit Interface Signal Definition (20 pin version)

The LVDS signal interface cable shall be terminated into a Hirose DF19KR-20P-1H, DF19L-20P-1H or equivalent connector. The interface connector pin assignments are listed in Table 4-1.

Table 4-1: LVDS 6 Bit Single Channel Interface Pin Assignments

Pin No.	Symbol	Function
1	GND	Ground
2	AVDD	Power Supply, 3.3V (typical)
3	AVDD	Power Supply, 3.3V (typical)
4	DVDD	DDC 3.3V power
5	NC	Do Not Connect
6	SCL	DDC Clock
7	SDA	DDC Data
8	RinX0-	- LVDS differential data input (R0-R5, G0)
9	RnX0+	+ LVDS differential data input (R0-R5, G0)
10	GND	Ground
11	RinX1-	- LVDS differential data input (G1-G5, B0-B1)
12	RnX1+	+ LVDS differential data input (G1-G5, B0-B1)
13	GND	Ground
14	RinX2-	- LVDS differential data input (B2-B5,HS,VS, DE)
15	RnX2+	+ LVDS differential data input (B2-B5,HS,VS, DE)
16	GND	Ground
17	CLK-	- LVDS differential clock input
18	CLK+	+ LVDS differential clock input
19	GND	Ground
20	GND	Ground

4.2 LVDS 6 Bit Interface Signal Definition (30 pin version)

The LVDS signal interface cable shall be terminated into a JAE FI-XPB30SL-HF10, FI-XPB30SRL-HF11 or equivalent connector. The interface connector pin assignments are listed in Table 4-2.

Table 4-2: LVDS 6 Bit Single/Dual Channel Interface Pin Assignments

Pin No.	Symbol	Function
1	GND	Ground
2	AVDD	Power Supply, 3.3V (typical)
3	AVDD	Power Supply, 3.3V (typical)
4	DVDD	DDC 3.3V power
5	NC	No Connect
6	SCL	DDC Clock
7	SDA	DDC Data
8	RXinO0-	- LVDS differential data input (R0-R5, G0)
9	RXinO0+	+ LVDS differential data input (R0-R5, G0)
10	GND	Ground
11	RXinO1-	- LVDS differential data input (G1-G5, B0-B1)
12	RXinO1+	+ LVDS differential data input (G1-G5, B0-B1)
13	GND	Ground
14	RXinO2-	- LVDS differential data input (B2-B5,HS,VS, DE)
15	RXinO2+	+ LVDS differential data input (B2-B5,HS,VS, DE)
16	GND	Ground
17	CLKO-	- LVDS differential clock input
18	CLKO+	+ LVDS differential clock input
19	GND	Ground
20*	RXinE0-	- LVDS differential data input (even pixels R0-R5, G0)
21*	RXinE0+	+ LVDS differential data input (even pixels R0-R5, G0)
22*	GND	Ground
23*	RXinE1-	- LVDS differential data input (even pixels G1-G5, B0-B1)
24*	RXinE1+	+ LVDS differential data input (even pixels G1-G5, B0-B1)
25*	GND	Ground
26*	RXinE2-	- LVDS differential data input (even pixels B2-B5,HS,VS, DE)
27*	RXinE2+	+ LVDS differential data input (even pixels B2-B5,HS,VS, DE)
28*	GND	Ground
29*	CLKE-	- LVDS differential clock input (even pixels)
30*	CLKE+	+ LVDS differential clock input (even pixels)

Note: For single channel connection, do not connect pins 20* thru 30*

4.3 LVDS 8 Bit Interface Signal Definition (30 pin version)

The LVDS signal interface cable shall be terminated into a JAE FI-XPB30SL-HF10, FI-XPB30SRL-HF11 or equivalent connector. The interface connector pin assignments are listed in Table 4-3.

Table 4-3: 8 Bit 30 pin LVDS Input Pin Assignments

Pin No.	Symbol	Function
1	GND	Ground
2	GND	Ground
3	AVDD	Power Supply, 3.3V (typical)
4	AVDD	Power Supply, 3.3V (typical)
5	DVDD	DDC 3.3V power
6	SCL	DDC Clock
7	SDA	DDC Data
8	RXinO0-	- LVDS differential data input (R0-R5, G0)
9	RXinO0+	+ LVDS differential data input (R0-R5, G0)
10	RXinO1-	- LVDS differential data input (G1-G5, B0-B1)
11	RXinO1+	+ LVDS differential data input (G1-G5, B0-B1)
12	RXinO2-	- LVDS differential data input (B2-B5,HS,VS,DE)
13	RXinO2+	+ LVDS differential data input (B2-B5,HS,VS,DE)
14	CLKO-	- LVDS differential clock input
15	CLKO+	+ LVDS differential clock input
16	GND	Ground
17	RXinO3-	- LVDS differential data input (R6-R7,B6-B7,G6-G7)
18	RXinO3+	+ LVDS differential data input (R6-R7,B6-B7,G6-G7)
19*	RXinE0-	- LVDS differential data input (even pixels R0-R5, G0)
20*	RXinE0+	+ LVDS differential data input (even pixels R0-R5, G0)
21*	RXinE0-	- LVDS differential data input (even pixels G1-G5, B0-B1)
22*	RXinE0+	+ LVDS differential data input (even pixels G1-G5, B0-B1)
23*	RXinE2-	- LVDS differential data input (even pixels B2-B5,HS,VS, DE)
24*	RXinE2+	+ LVDS differential data input (even pixels B2-B5,HS,VS, DE)
25*	CLKE-	- LVDS differential clock input (even pixels)
26*	CLKE+	+ LVDS differential clock input (even pixels)
27*	GND	Ground
28*	RXinE3-	- LVDS differential data input (R6-R7,B6-B7,G6-G7)
29*	RXinE3+	+ LVDS differential data input (R6-R7,B6-B7,G6-G7)
30*	NC	No Connect

Note: For single channel connection, do not connect pins 19* thru 30*

4.4 LVDS 8 Bit Interface Signal Definition (40 pin version)

The LVDS signal interface cable shall be terminated into a JAE FI-NXB40SL-HF10, FI-NXB40SRL-HF11 or equivalent connectors. The interface connector pin assignments are listed in Table 4-4.

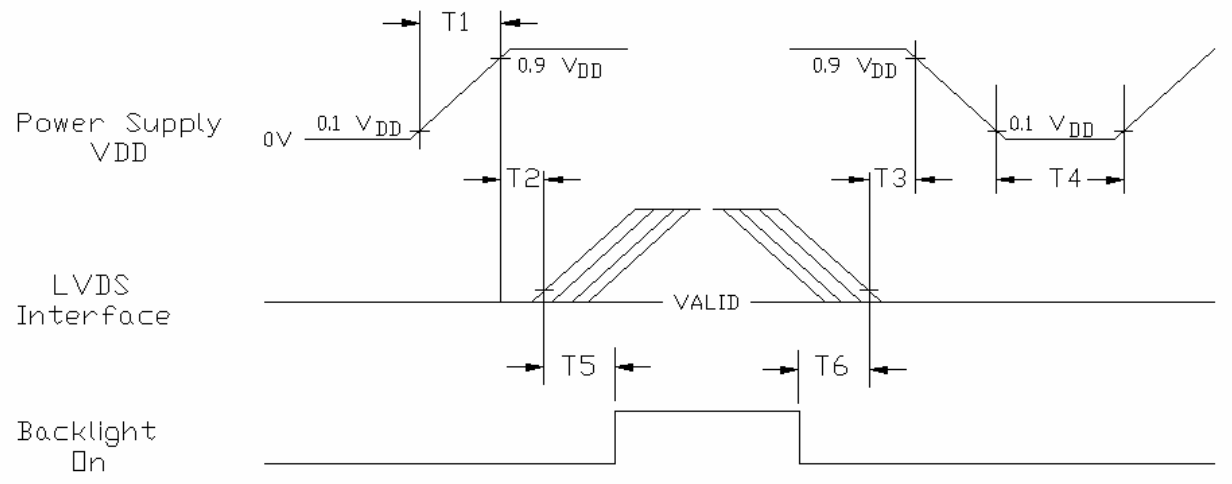
Table 4-4: 8 Bit 40 pin LVDS Interface Pin Assignments

Pin #	Symbol	Function
1	GND	Ground
2	GND	Ground
3	AVDD	3.3V Analog Power Supply(5.0V Optional)
4	AVDD	3.3V Analog Power Supply(5.0V Optional)
5	AVDD	3.3V Analog Power Supply(5.0V Optional)
6	DVDD	3.3V Digital Power Supply
7	DVDD	3.3V Digital Power Supply
8	SCL	Two wire serial interface clock
9	SDA	Two wire serial interface data
10	RXinO0-	- LVDS differential data input, Chan 0-Odd
11	RXinO0+	+ LVDS differential data input, Chan 0-Odd
12	GND	Ground
13	RXinO1-	- LVDS differential data input, Chan 1-Odd
14	RXinO1+	+ LVDS differential data input, Chan 1-Odd
15	GND	Ground
16	RXinO2-	- LVDS differential data input, Chan 2-Odd
17	RXinO2+	+ LVDS differential data input, Chan 2-Odd
18	GND	Ground
19	CLKO-	- LVDS Differential Clock input (Odd)
20	CLKO+	+ LVDS Differential Clock input (Odd)
21	GND	Ground
22	RXinO3-	- LVDS differential data input, Chan 3-Odd
23	RXinO3+	+ LVDS differential data input, Chan 3-Odd
24	GND	Ground
25*	RXinE0-	- LVDS differential data input, Chan 0-Even
26*	RXinE0+	+ LVDS differential data input, Chan 0-Even
27*	GND	Ground
28*	RXinE1-	- LVDS differential data input, Chan 1-Even
29*	RXinE1+	+ LVDS differential data input, Chan 1-Even
30*	GND	Ground
31*	RXinE2-	- LVDS differential data input, Chan 2-Even
32*	RXinE2+	+ LVDS differential data input, Chan 2-Even
33*	GND	Ground
34*	CLKE-	- LVDS Differential Clock input (Even)
35*	CLKE+	+ LVDS Differential Clock input (Even)
36*	GND	Ground
37*	RXinE3-	- LVDS differential data input, Chan 3-Even
38*	RXinE3+	+ LVDS differential data input, Chan 3-Even
39*	GND	Ground
40*	NC	No Connection

Note: For single channel connection, do not connect pins 25* thru 40*

4.5 LVDS Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the logic power and data/control signal sequencing of Figure 4-1.



0.5 ms ≤ T1 ≤ 10 ms : 0 ≤ T2 ≤ 50 ms : 0 ≤ T3 ≤ 50 ms : 500 ms ≤ T4 : 200 ms ≤ T5 : 200 ms ≤ T6

Figure 4-1: Logic Power and LVDS Signals Sequencing Diagram

4.6 LVDS Data and Control Signal Interface

The modules LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 4-2 shows the data mapping diagram of each LVDS channel. The LVDS differential signals line-to-line termination impedance, Z_T, shall be 100 ± 10 ohms.

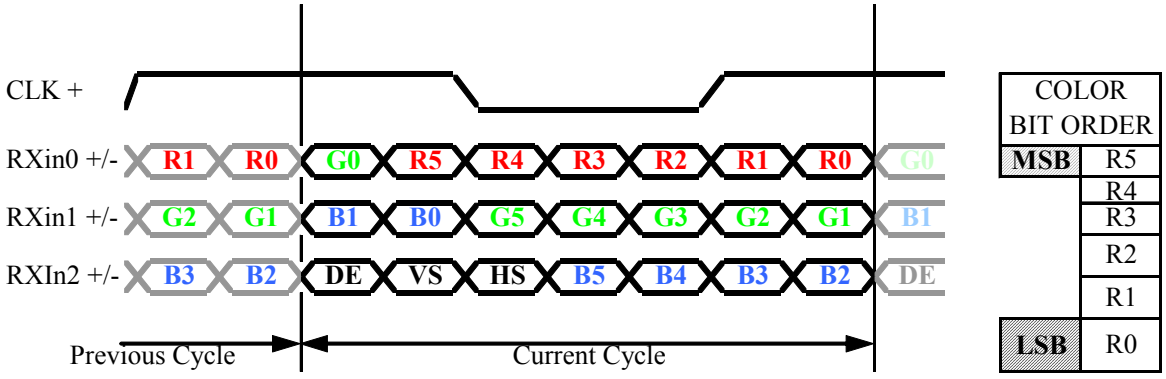
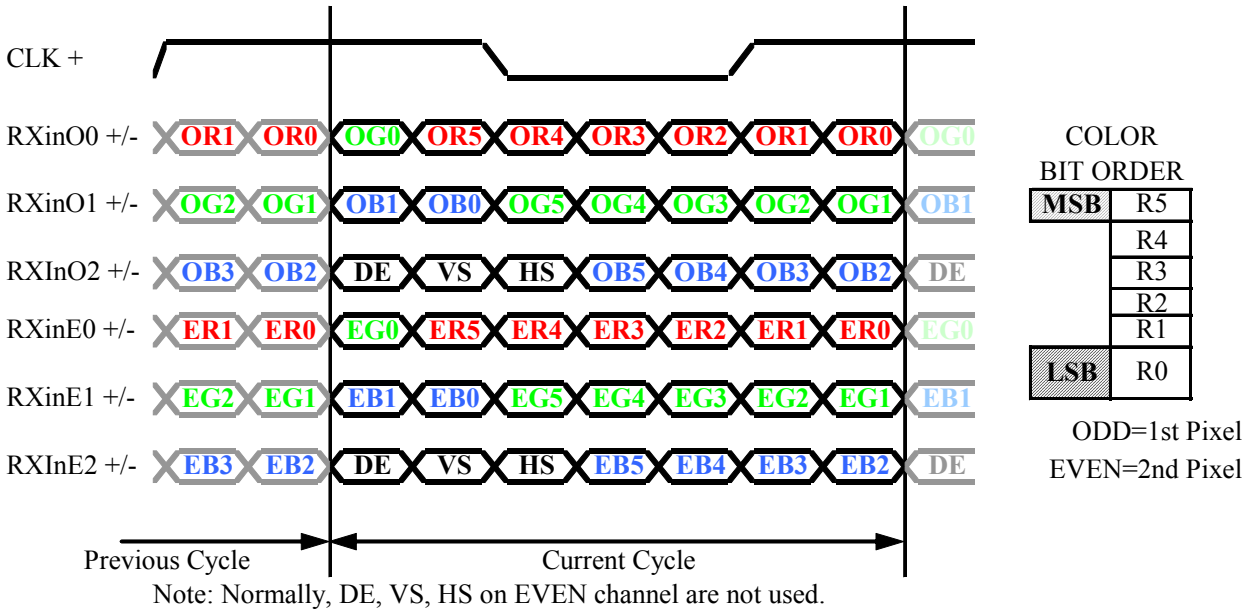


Figure 4-2: LVDS 6 Bit Single Channel Data Mapping Diagram



Note: Normally, DE, VS, HS on EVEN channel are not used.

Figure 4-3: LVDS 6 Bit Dual Channel Data Mapping Diagram

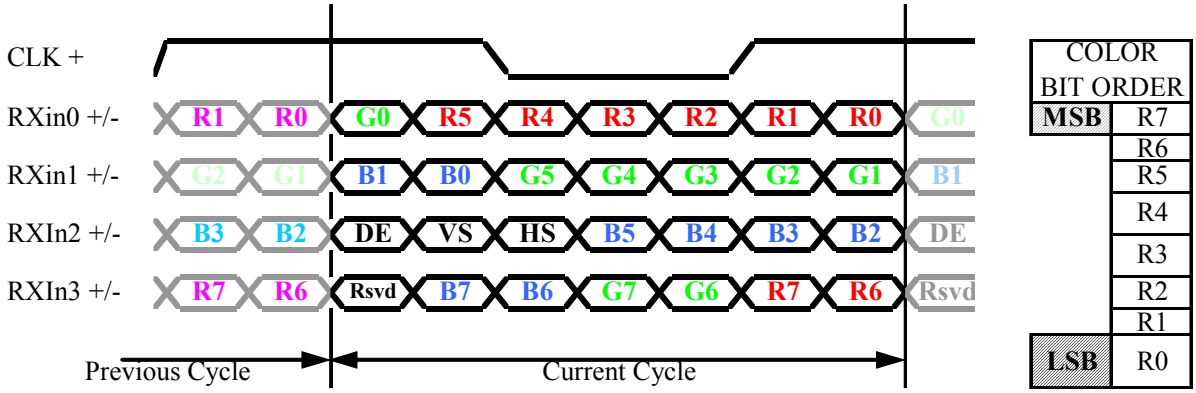


Figure 4-4: LVDS 8 Bit Single Channel Data Mapping Diagram

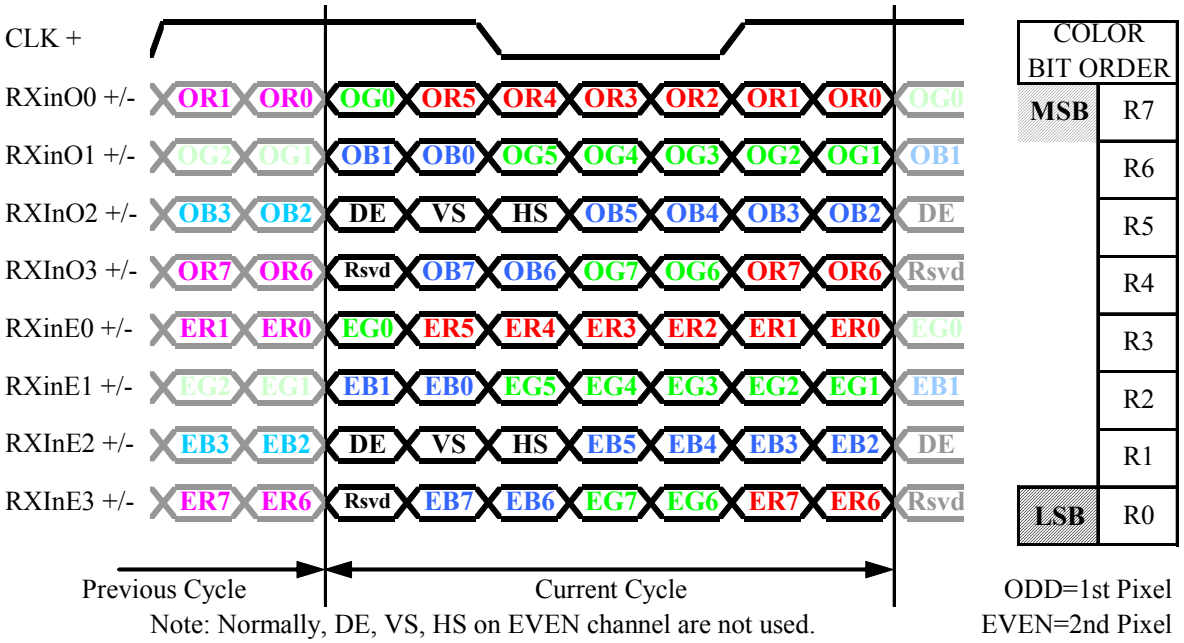


Figure 4-5: LVDS 8 Bit Dual Channel Data Mapping Diagram

5. Display Brightness Interface Definition

5.1 CCFL Lamp Interface Definition

The panel-side backlight interface cable shall be terminated into a JST BHSR-02VS-1, Sin Sheng P2408P2, Sunridge FPD-PB-35-2P, or equivalent connector. The lamp wires exiting the panel shall be sufficiently protected so that normal movement during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 5-1.

Table 5-1: CCFL Backlight Cable Two Pin Assignment

Pin No.	Signal	Level	Function
1	VCCFL	AC	Power Supply for CCFL
2	GND Return	Ground	Power return for CCFL

6. Mechanical Outline Requirements

6.1 12.1-inch Standard (4:3) Single CCFL Mechanical Outline

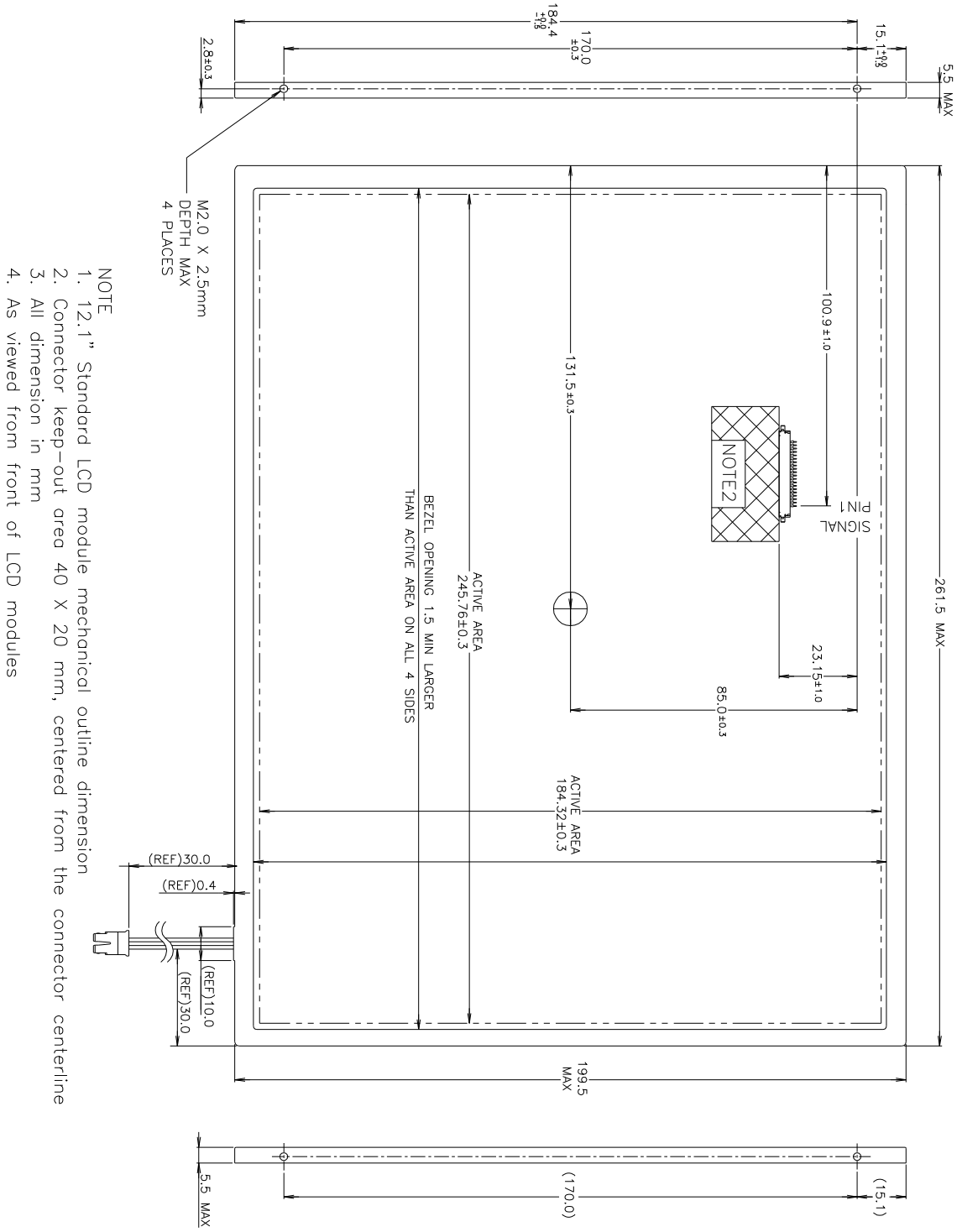


Figure 6-1: 12.1-inch Standard Single CCFL Mechanical Outline Dimension (Front View)

6.2 12.1-inch Wide (16:10) Single CCFL Mechanical Outline

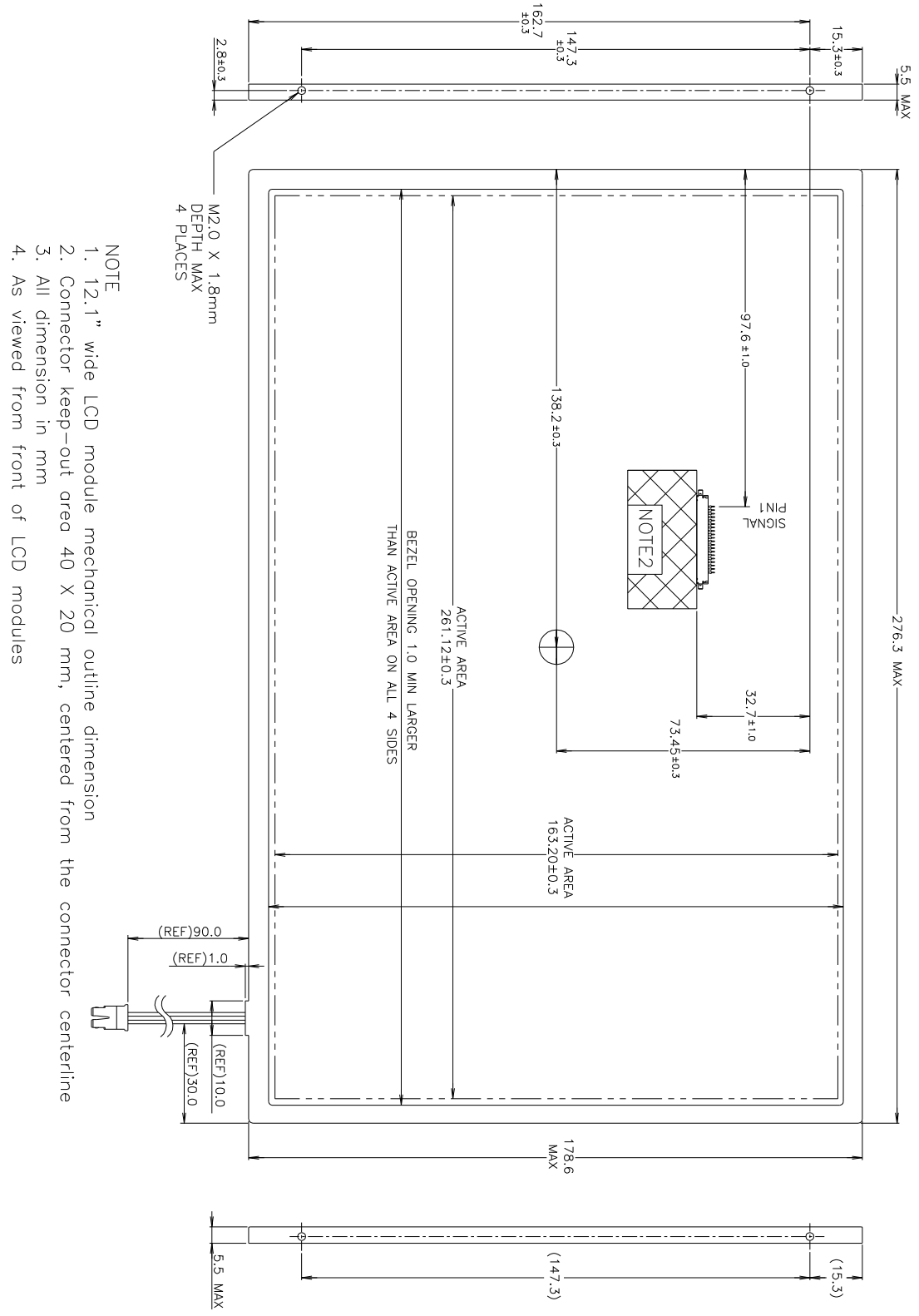


Figure 6-2: 12.1-inch Wide Single CCFL Mechanical Outline Dimension (Front View)

6.3 13.3-inch Standard (4:3) Single CCFL Mechanical Outline

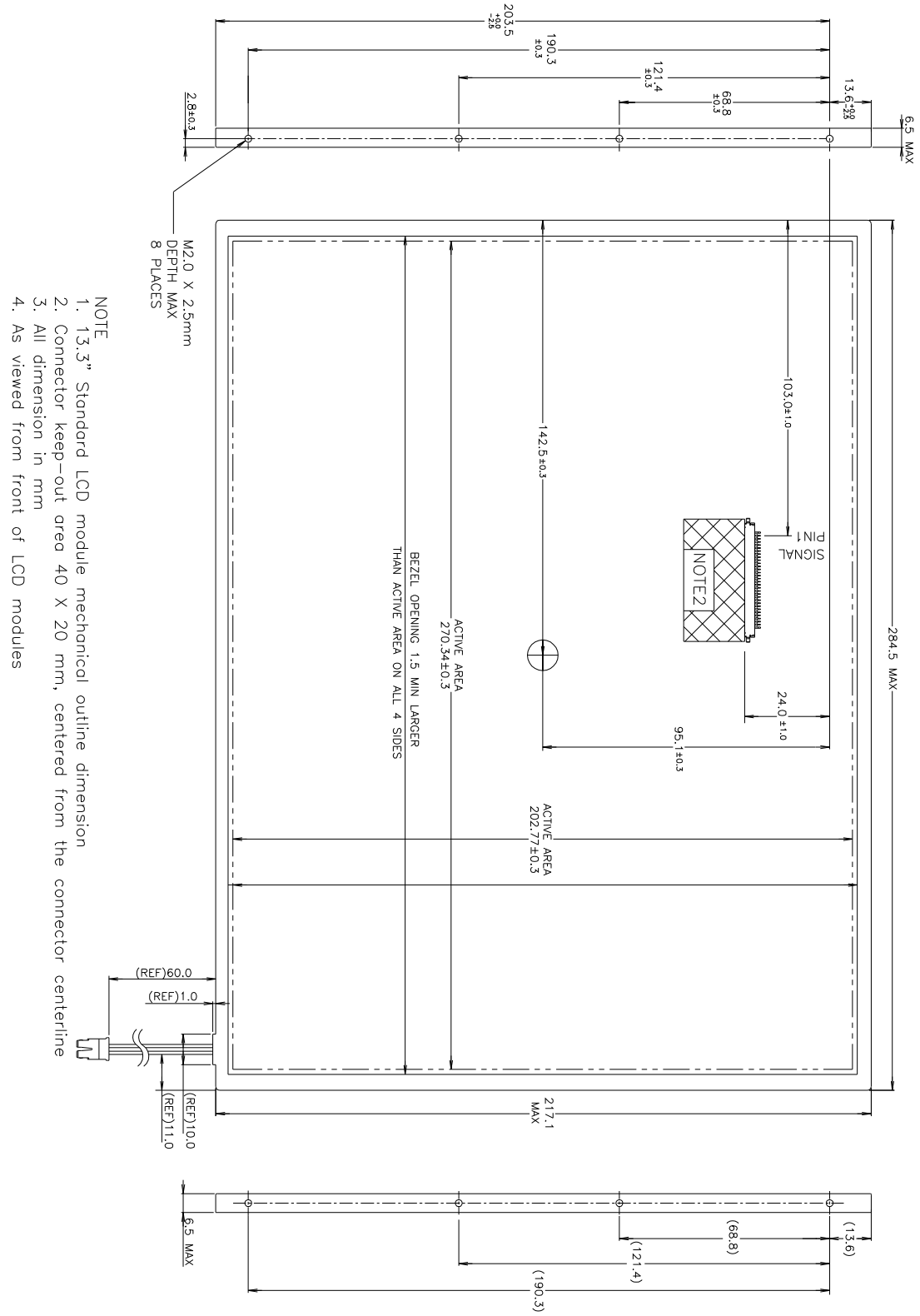


Figure 6-3: 13.3-inch Standard Single CCFL Mechanical Outline Dimension (Front View)

6.4 13.3-inch Wide (16:10) Single CCFL Mechanical Outline

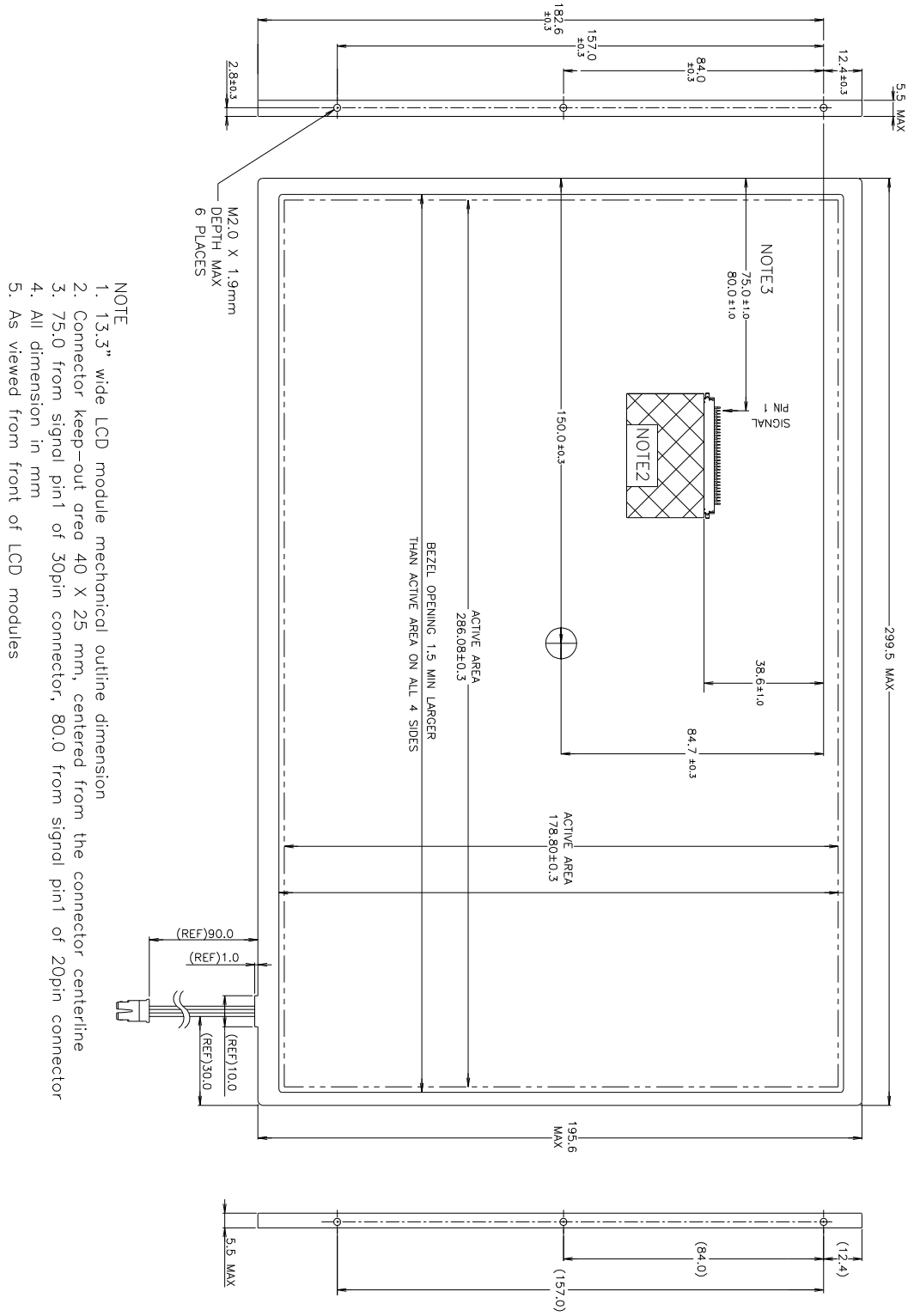


Figure 6-4: 13.3-inch Wide Single CCFL Mechanical Outline Dimension (Front View)

6.5 14.1-inch Standard (4:3) Single CCFL Mechanical Outline

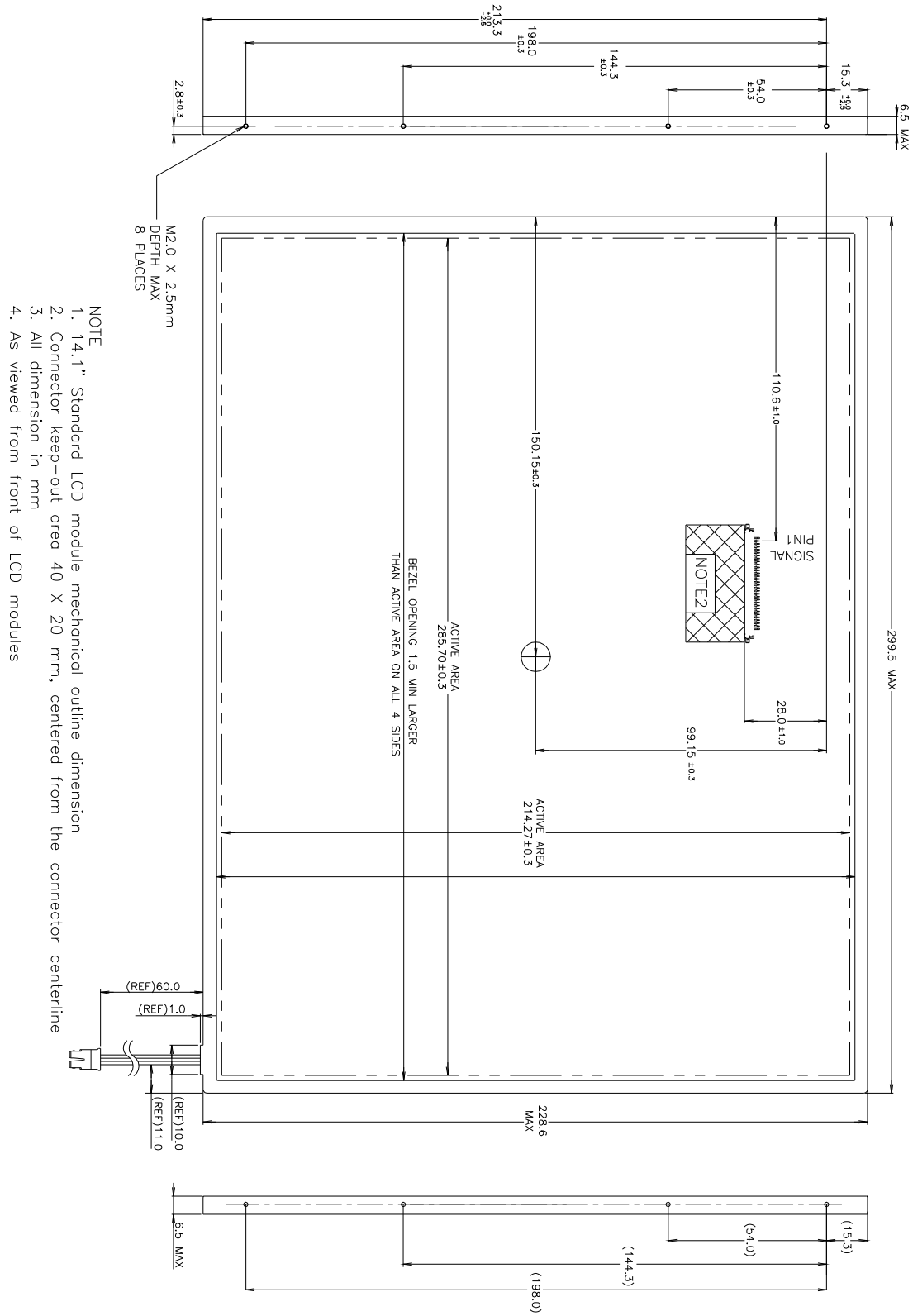


Figure 6-5: 14.1-inch Standard Single CCFL Mechanical Outline Dimension (Front View)

6.6 14.1-inch Wide (16:10) Single CCFL Mechanical Outline

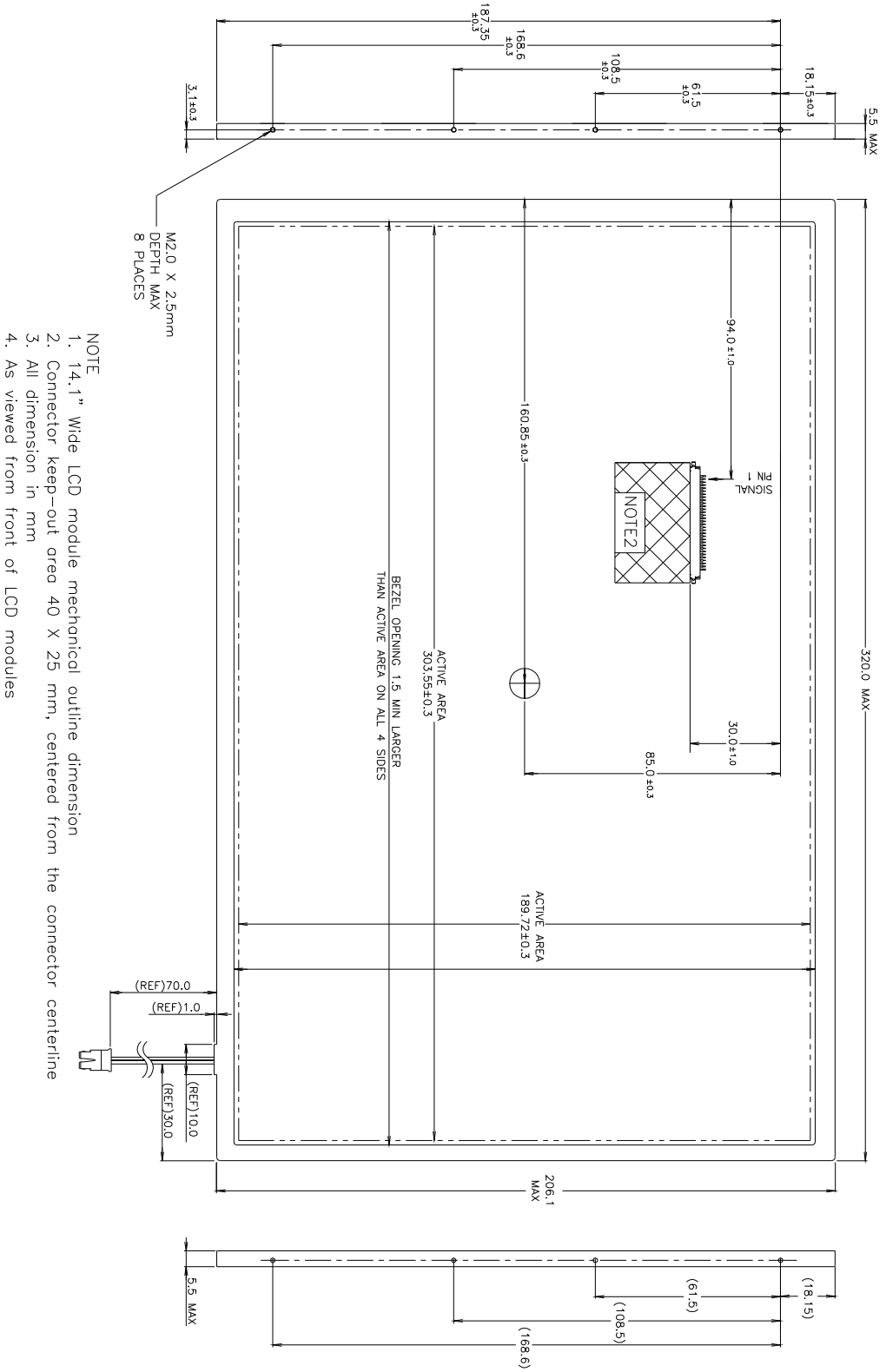


Figure 6-6: 14.1-inch Wide Single CCFL Mechanical Outline Dimension (Front View)

6.7 15-inch Standard (4:3) Single CCFL Mechanical Outline

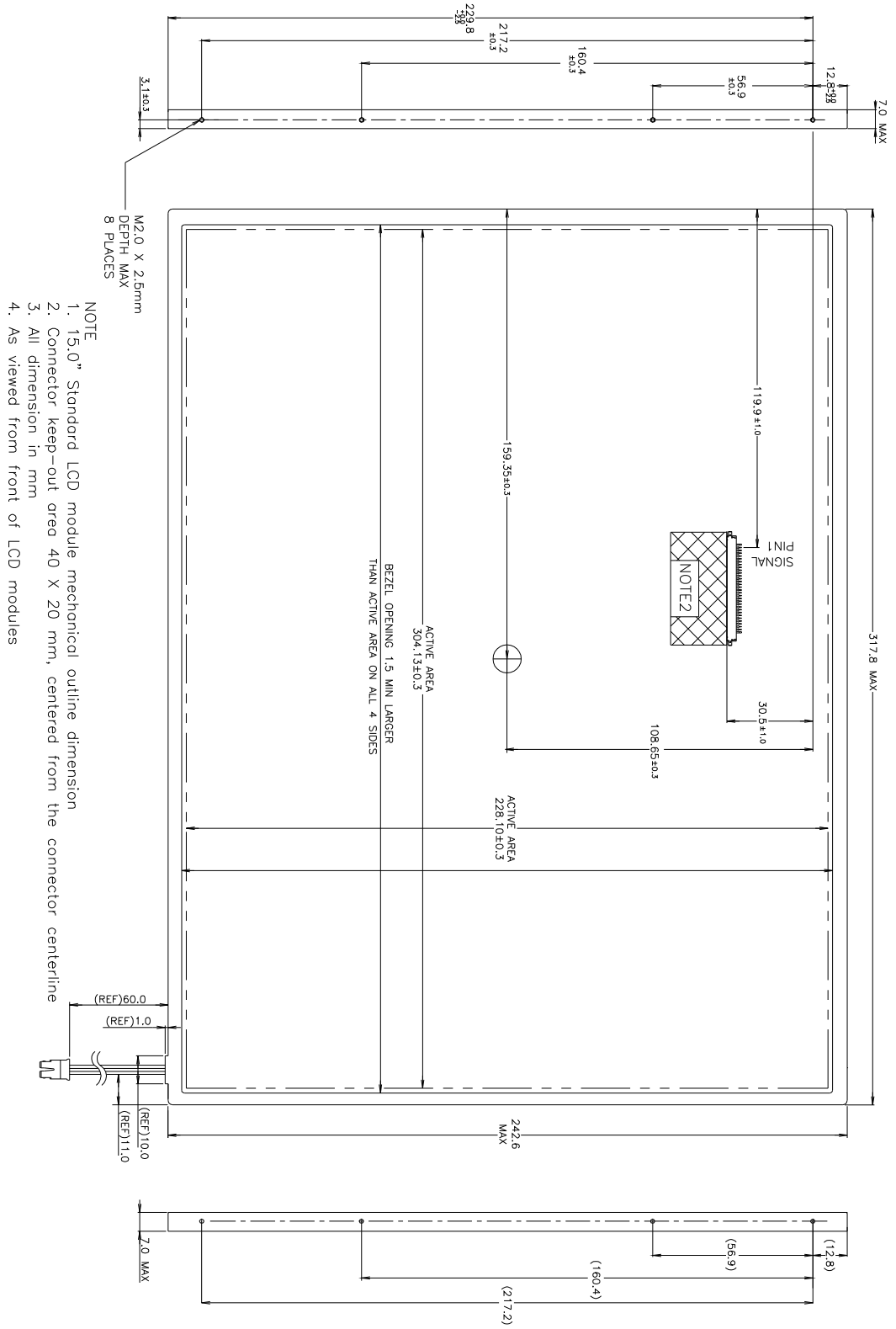


Figure 6-7: 15-inch Standard Single CCFL Mechanical Outline Dimension (Front View)

6.8 15.4-inch Wide (16:10) Single CCFL Mechanical Outline

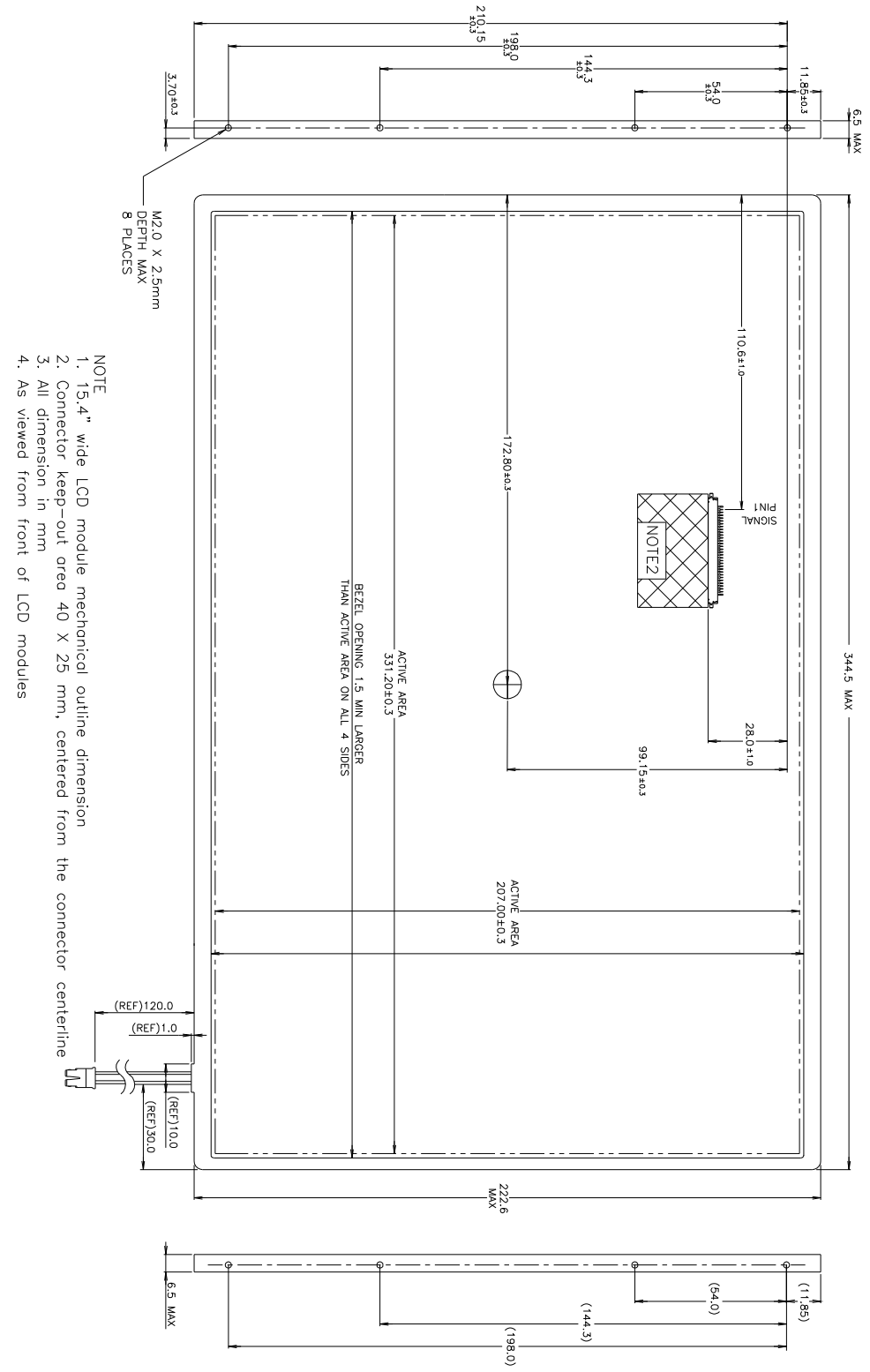


Figure 6-8: 15.4-inch Wide Single CCFL Mechanical Outline Dimension (Front View)

6.9 15.4-inch Wide (16:10) Dual CCFL, Y-stack Mechanical Outline

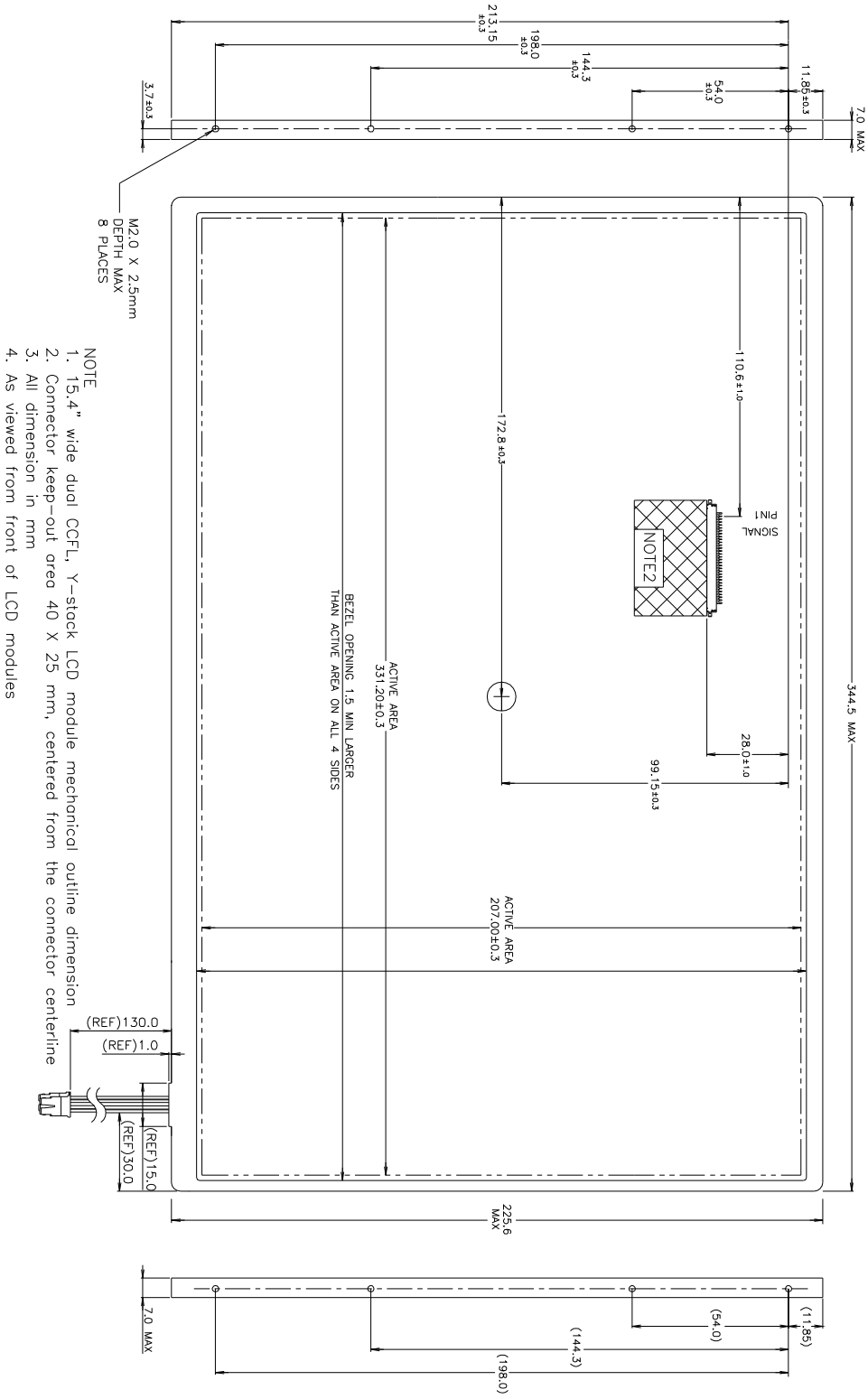


Figure 6-9: 15.4-inch Wide Dual CCFL, Y-stack Mechanical Outline Dimension (Front View)

6.10 17.1-inch Wide (16:10) Single CCFL Mechanical Outline

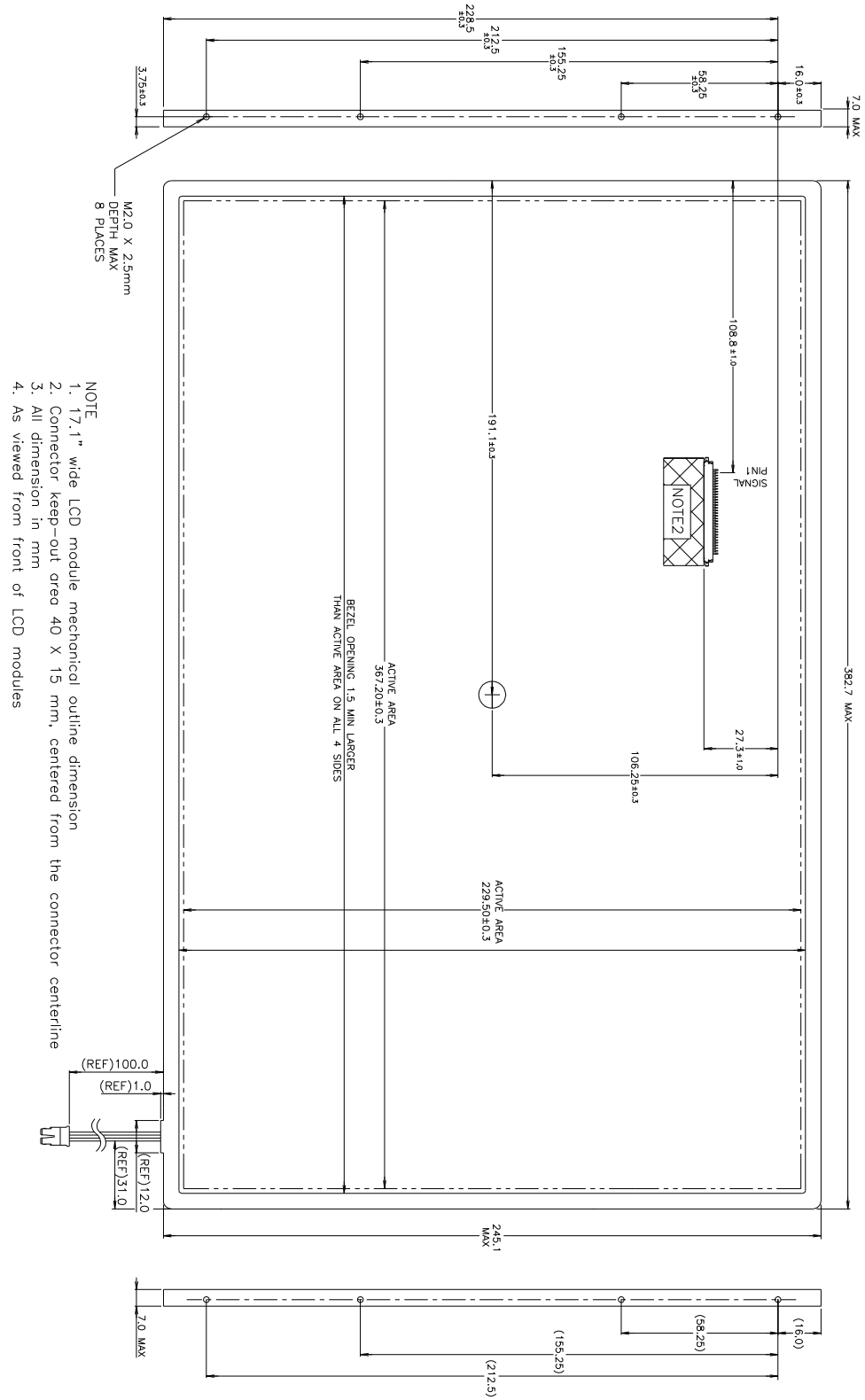


Figure 6-10: 17.1-inch Wide Single CCFL Mechanical Outline Dimension (Front View)

6.11 17.1-inch Wide (16:10) Dual CCFL, Y-stack Mechanical Outline

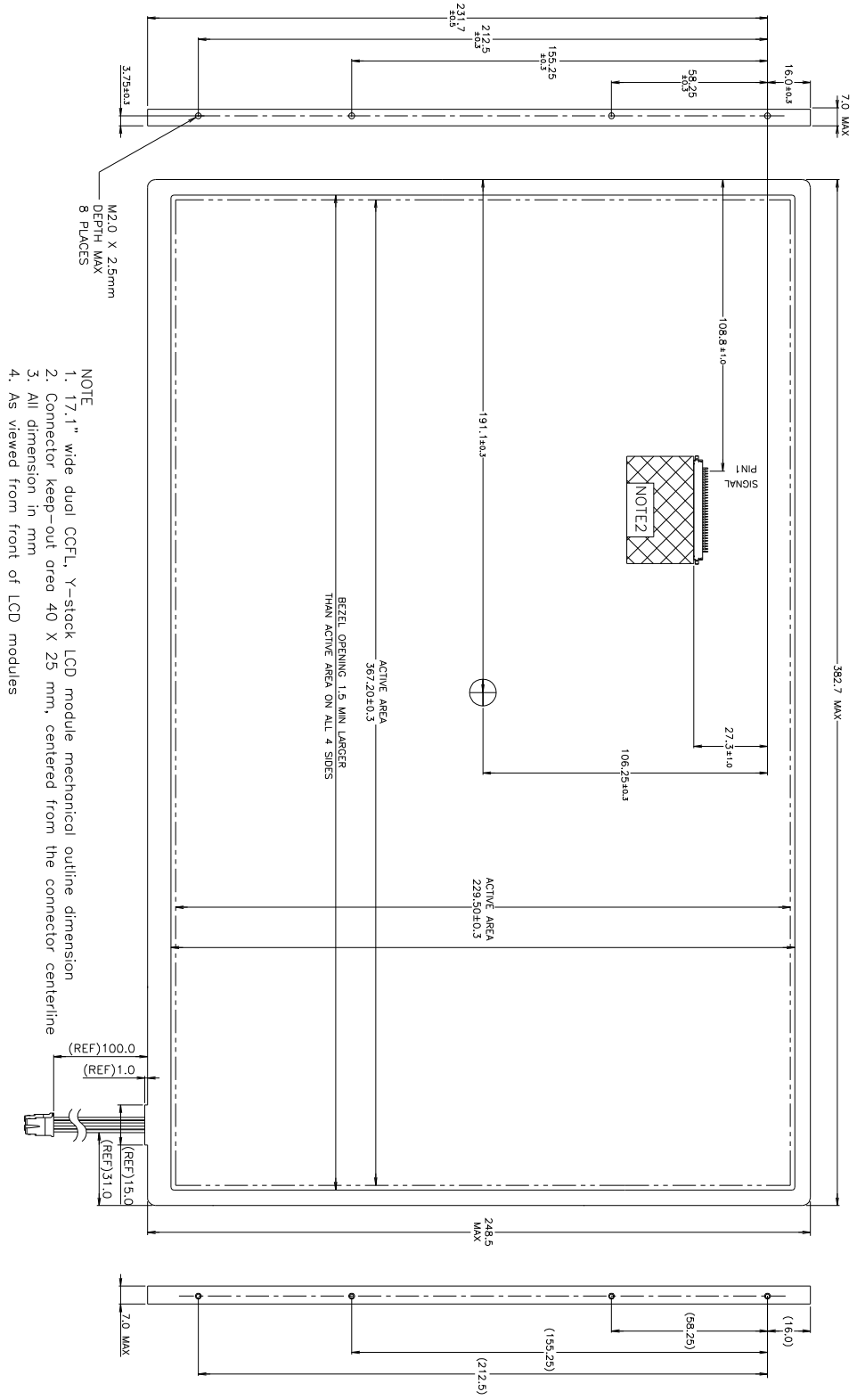


Figure 6-11: 17.1-inch Wide Dual CCFL, Y-stack Mechanical Outline Dimension (Front View)

6.12 17.1-inch Wide (16:10) Dual CCFL, Z-stack Mechanical Outline

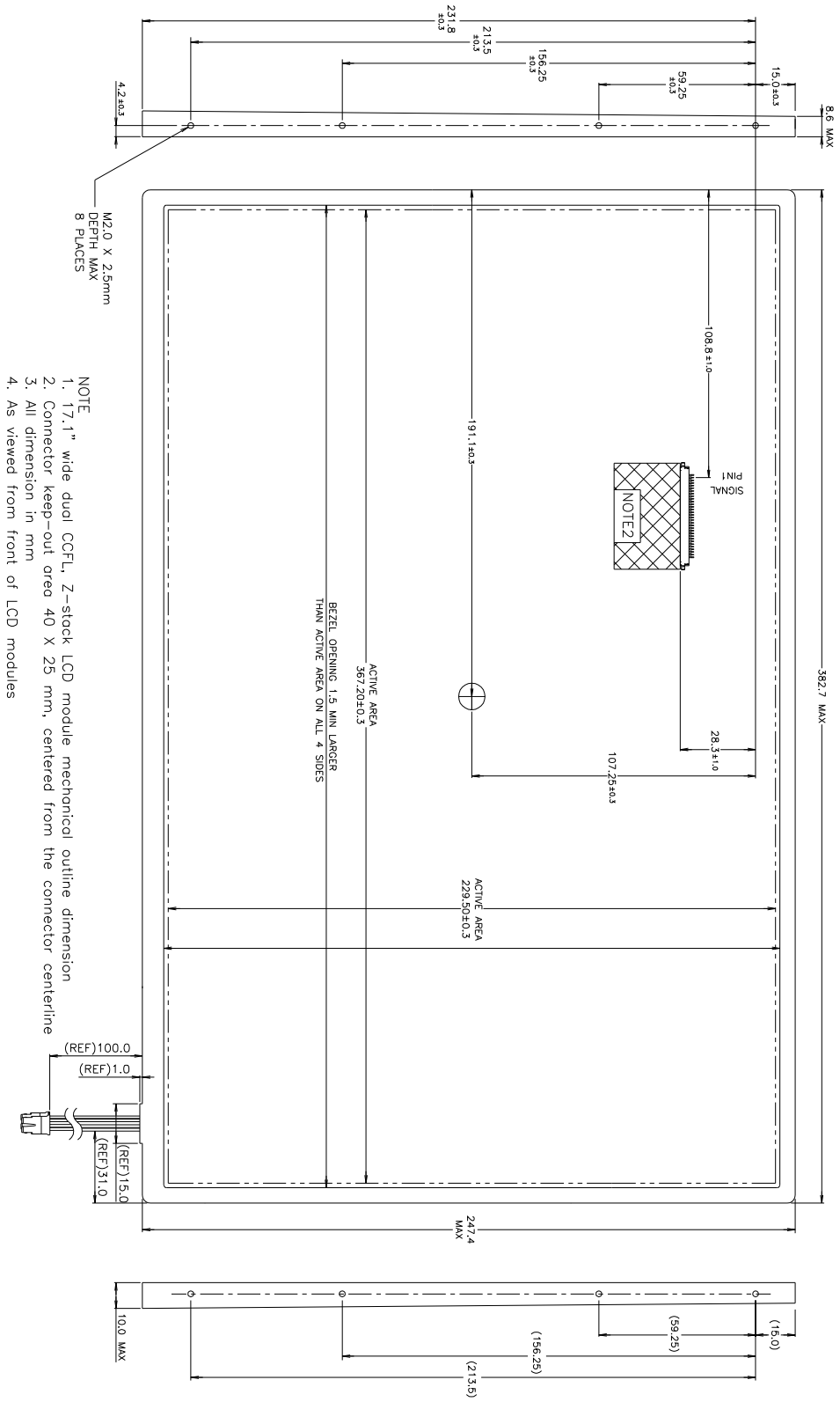


Figure 6-12: 17.1-inch Wide Dual CCFL, Z-stack Mechanical Outline Dimension (Front View)

6.13 20.1-inch Wide (16:10) Dual CCFL, Y-stack Mechanical Outline

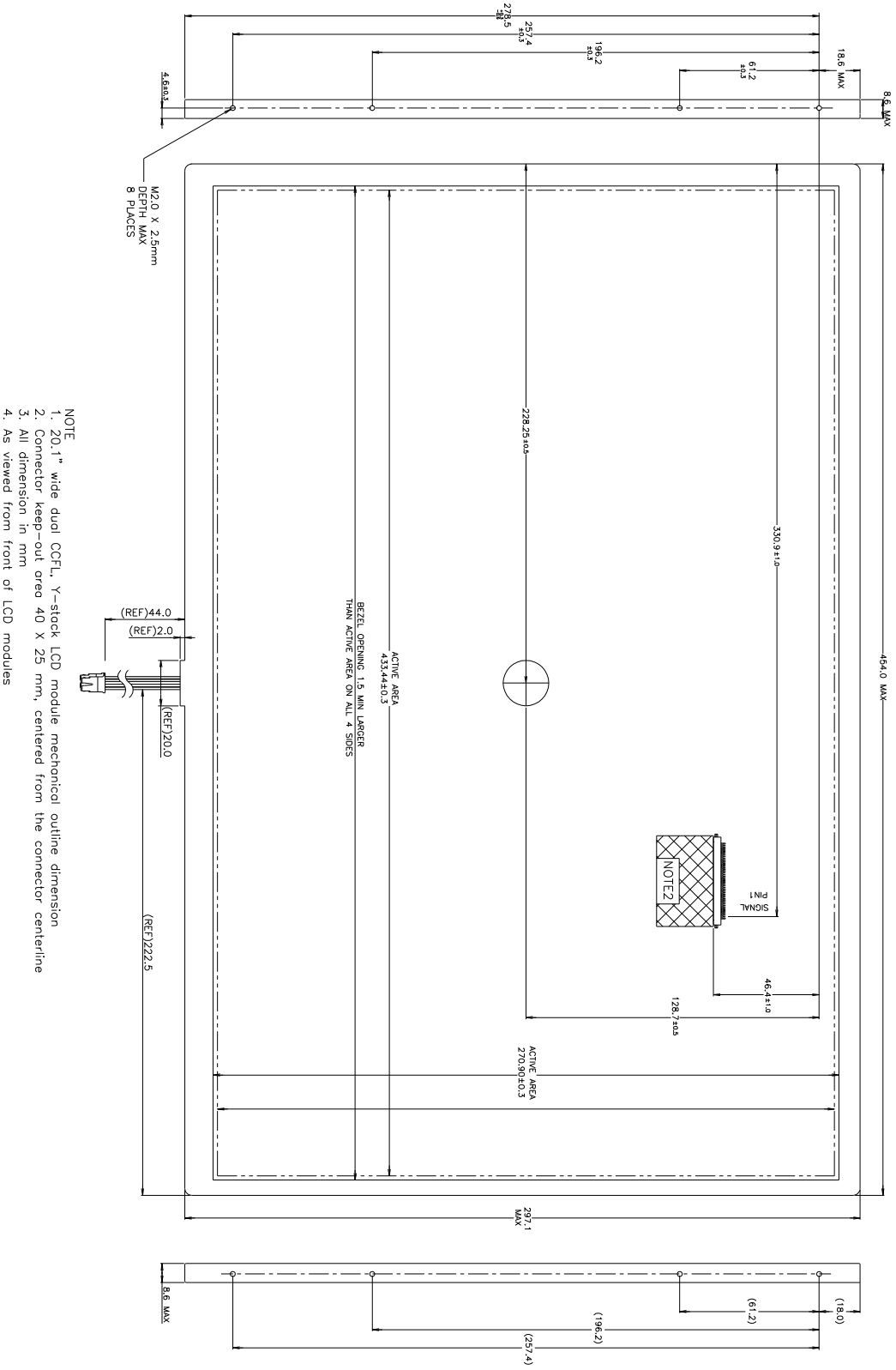


Figure 6-13: 20.1-inc Wide Dual CCFL, Y-stack Mechanical Outline Dimension (Front View)

6.14 20.1-inch Wide (16:10) Dual CCFL, Z-stack Mechanical Outline

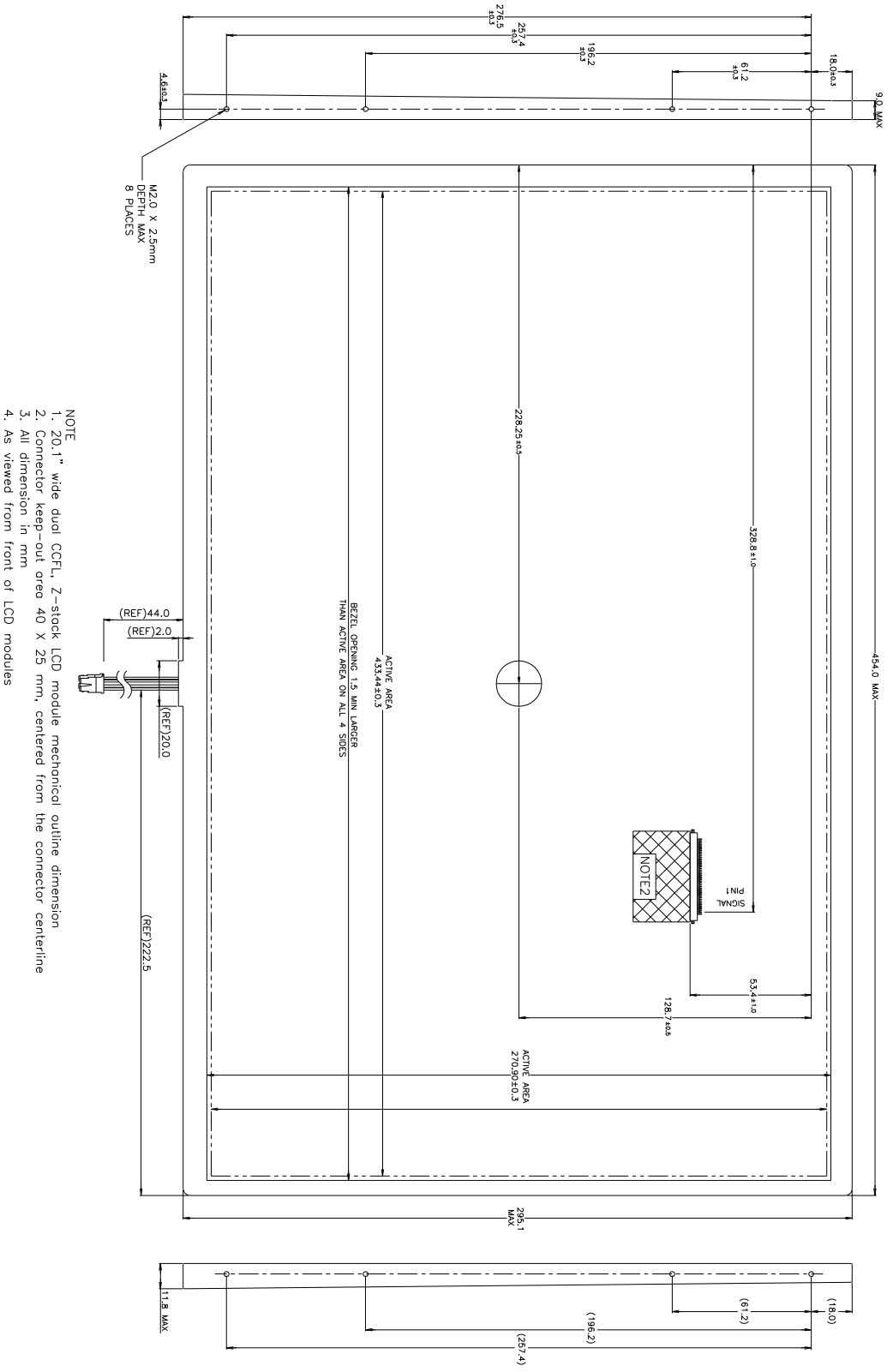
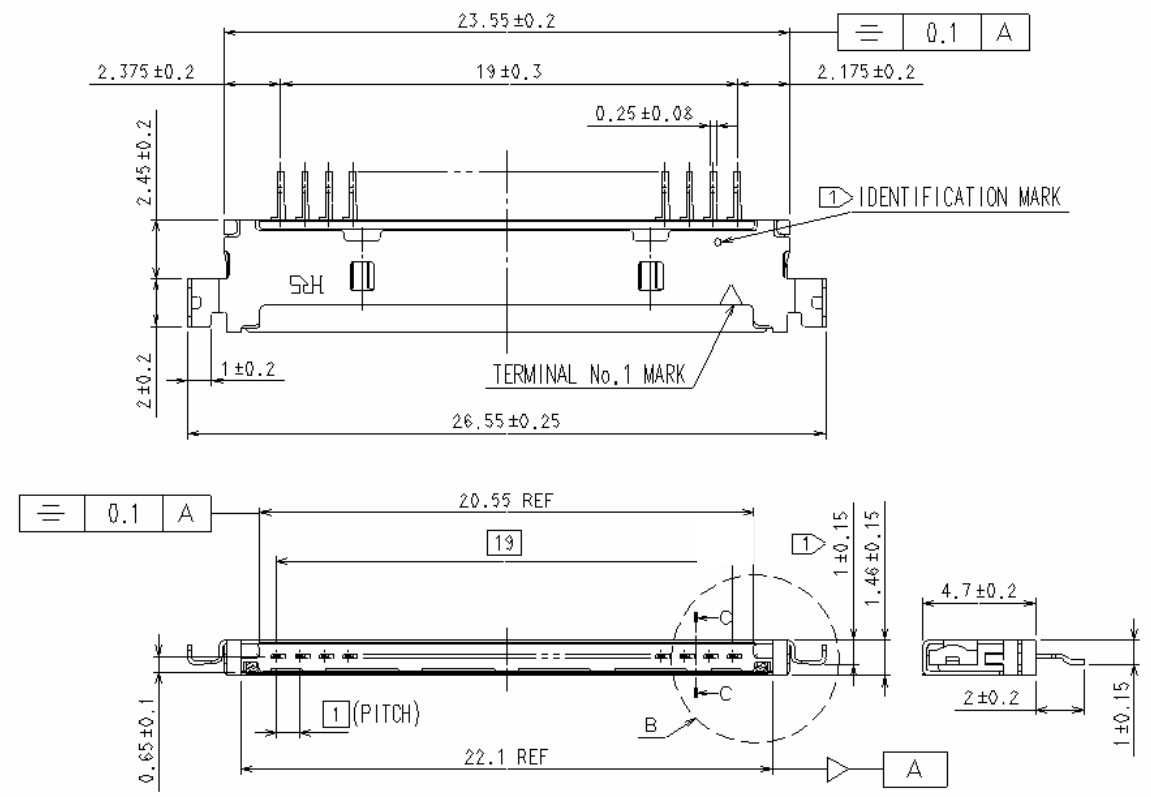


Figure 6-14: 20.1-inch Wide Dual CCFL, Z-stack Mechanical Outline Dimension (Front View)

7. Standard Connector Requirements

7.1 20 pin Connector

7.1.1 20 pin Panel-side Receptacle Connector



1 Identification mark for the 1 mm above the mounting surface height.

Figure 7-1: 20 pin DF19KR Compatible Panel-side Receptacle Connector

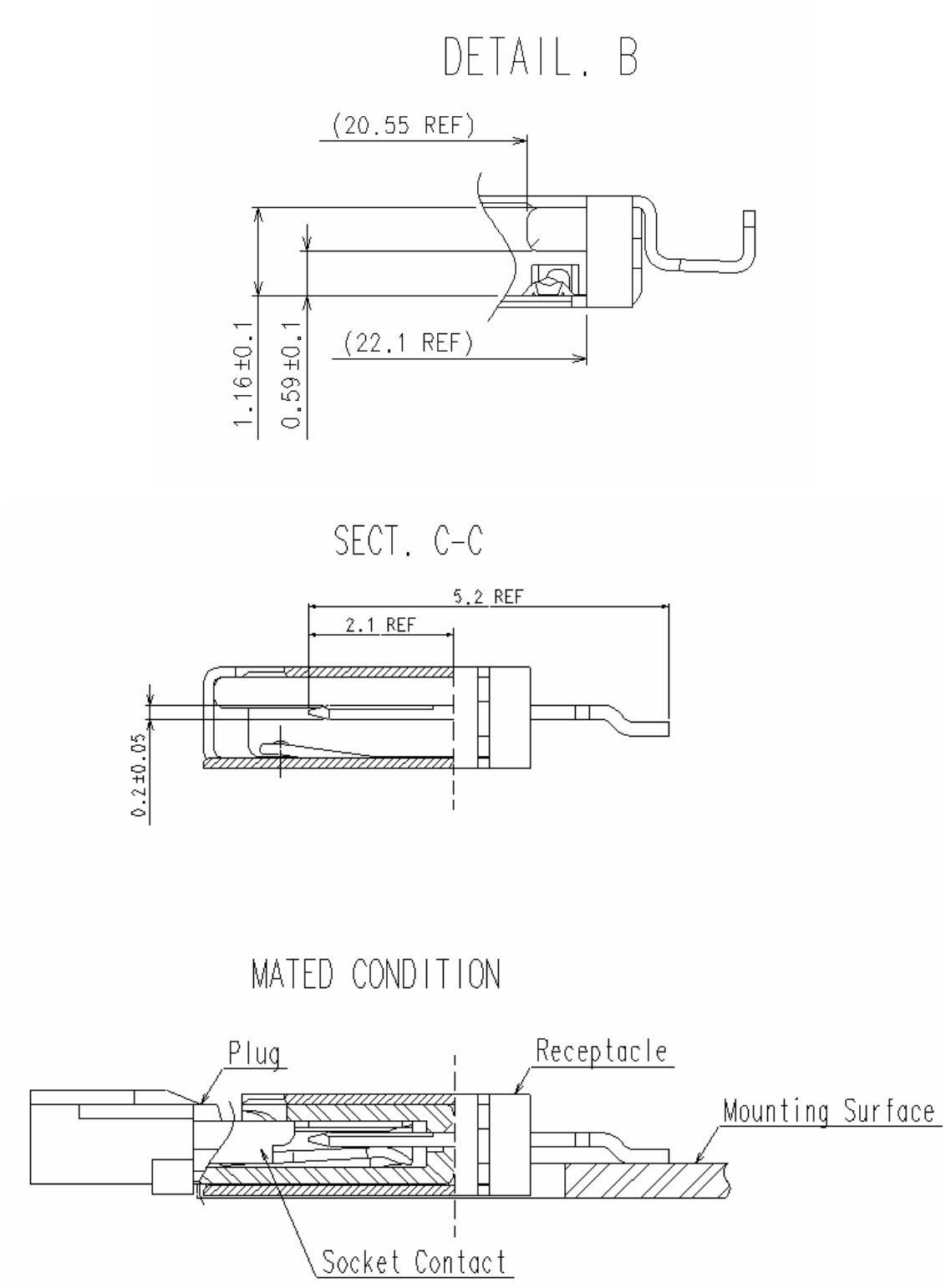


Figure 7-2: 20 pin DF19KR Compatible Panel-side Receptacle Connectors Detail

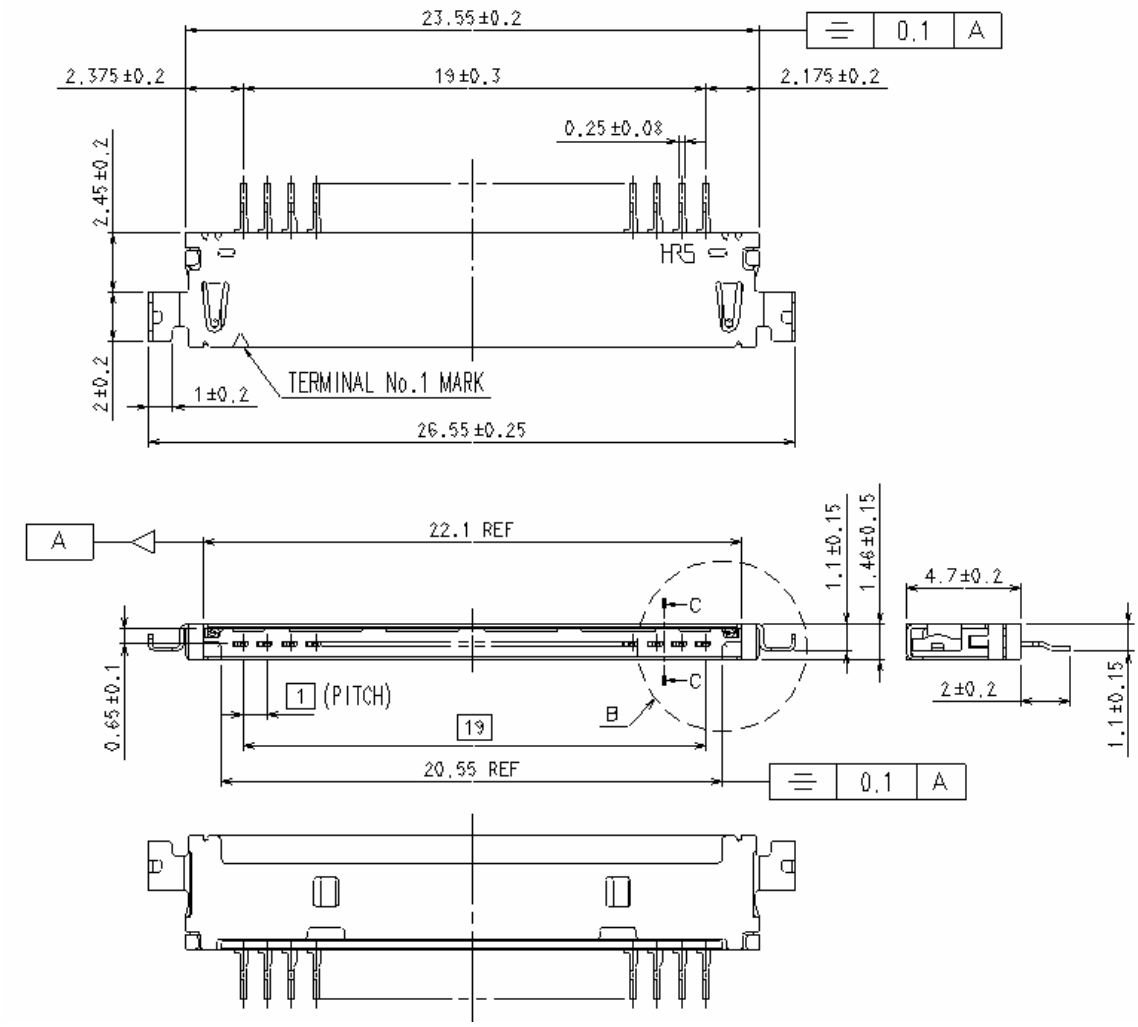


Figure 7-3: 20 pin DF19L Compatible Panel-side Receptacle Connectors

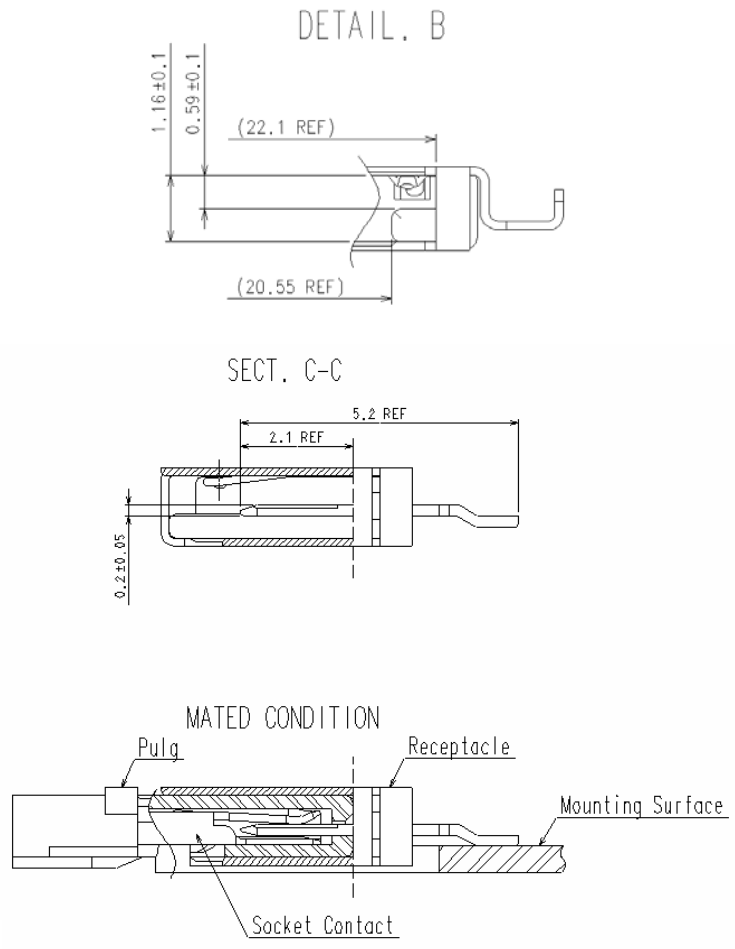


Figure 7-4: 20 pin DF19KR Compatible Panel-side Receptacle Connectors Detail

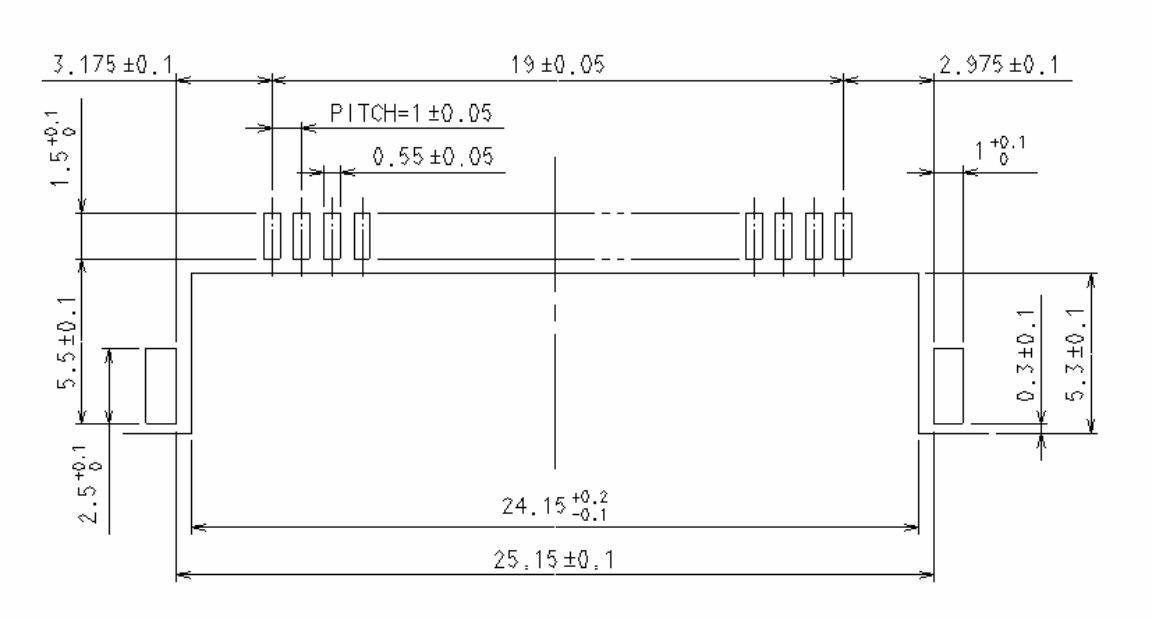


Figure 7-5: 20 pin Panel-side Receptacle Connector PCB Mounting Pattern

7.1.2 20 pin Cable Plug Connector

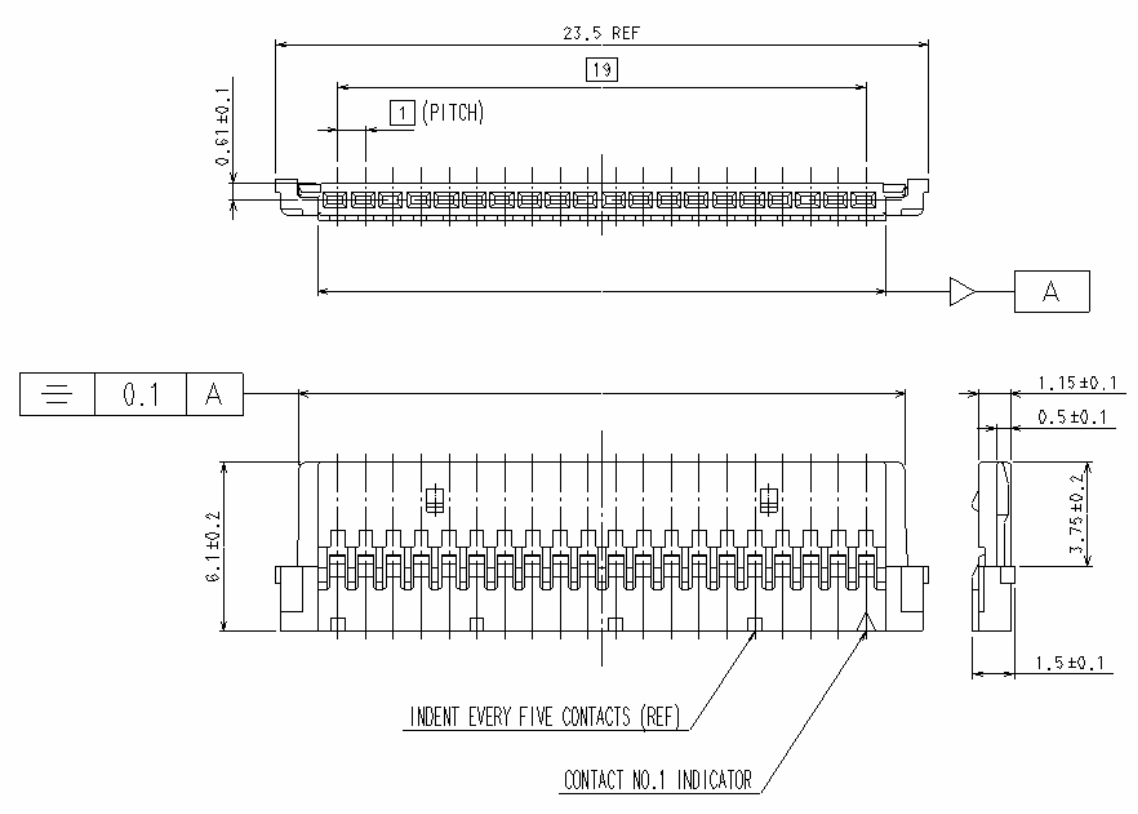


Figure 7-6: 20 pin Cable-side Plug Connector

7.2 30 pin Standard Connector

7.2.1 30 pin Panel-side Receptacle Connector

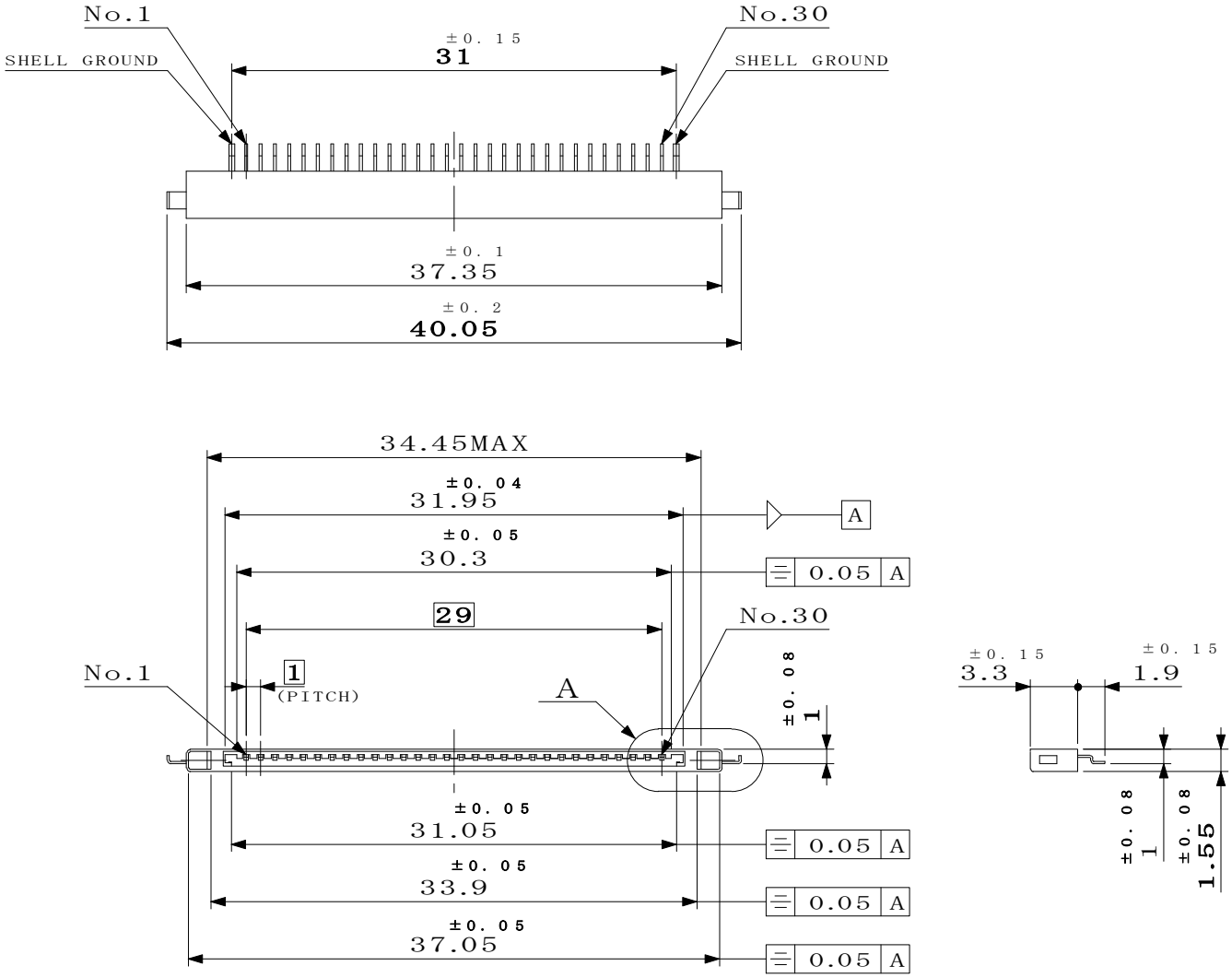


Figure 7-7: 30 pin Panel-side Receptacle Connector

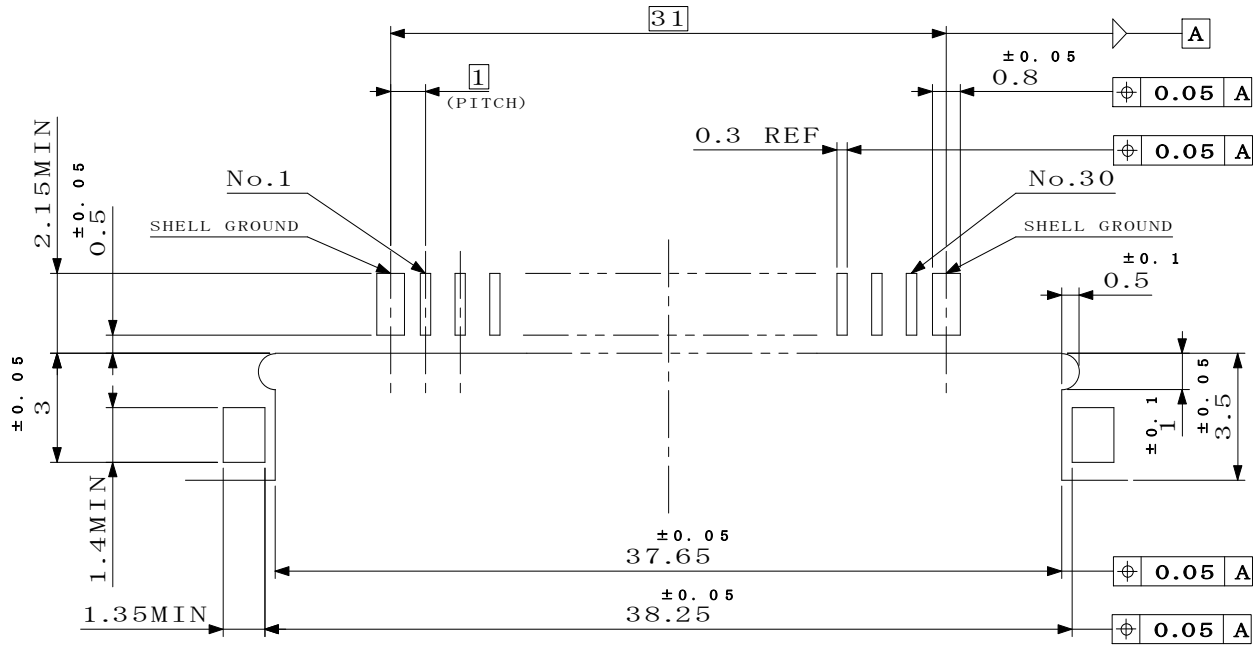


Figure 7-8: 30 pin Panel-side Receptacle Connector PCB Mounting Pattern

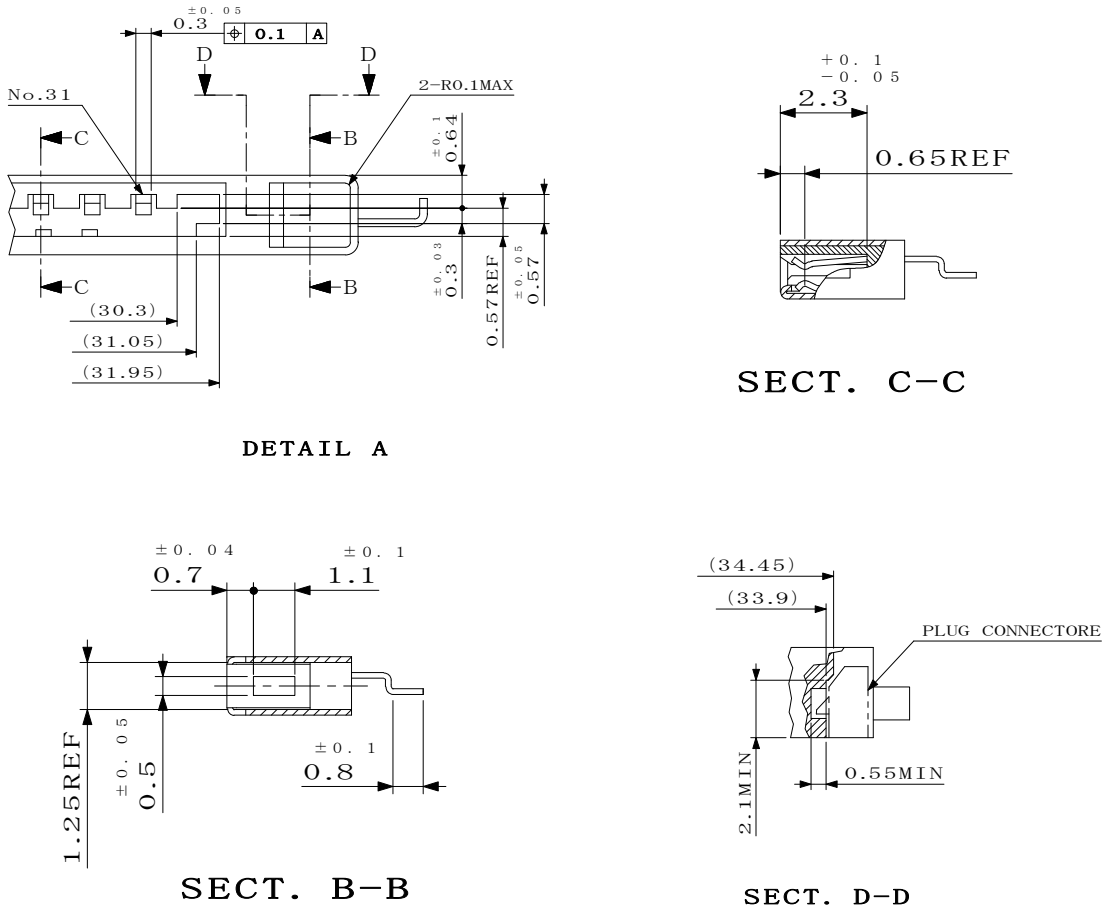
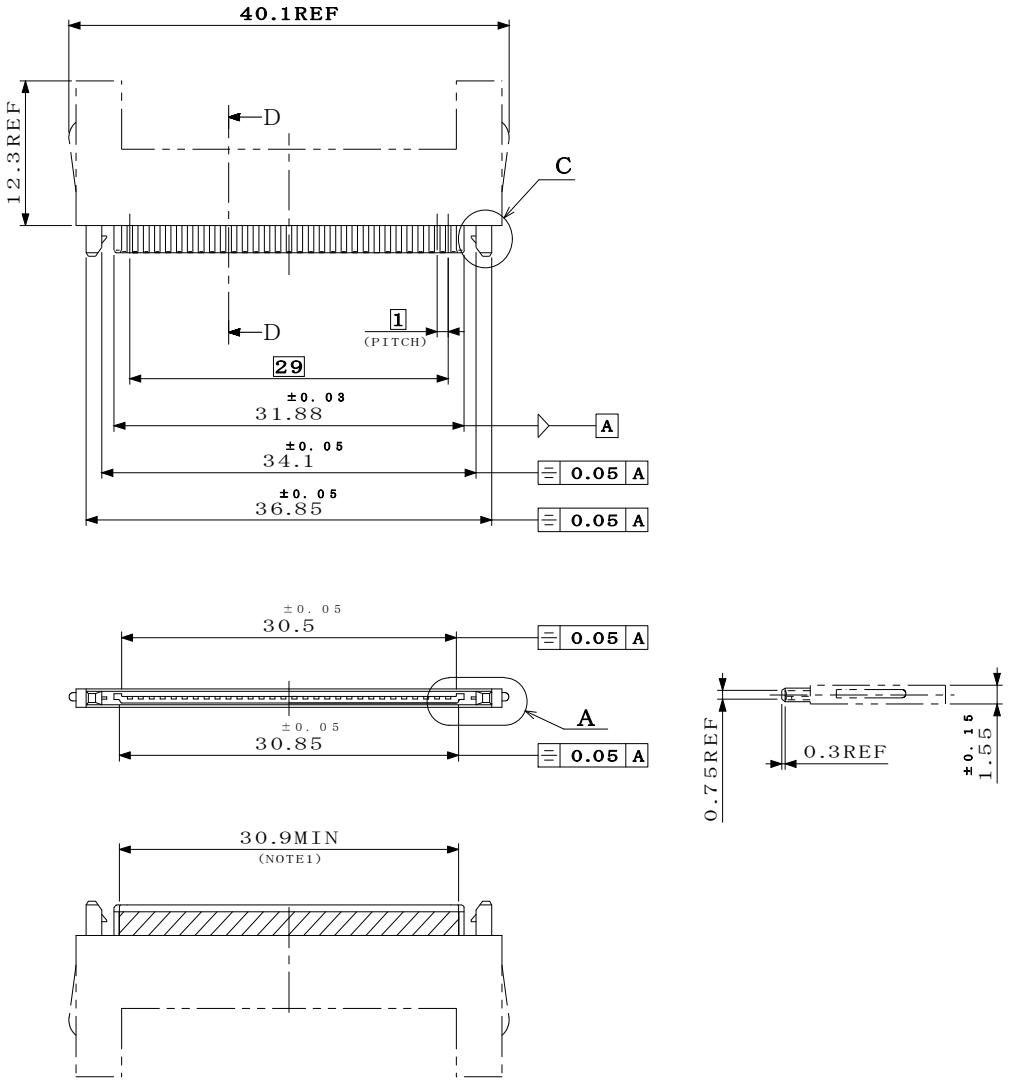


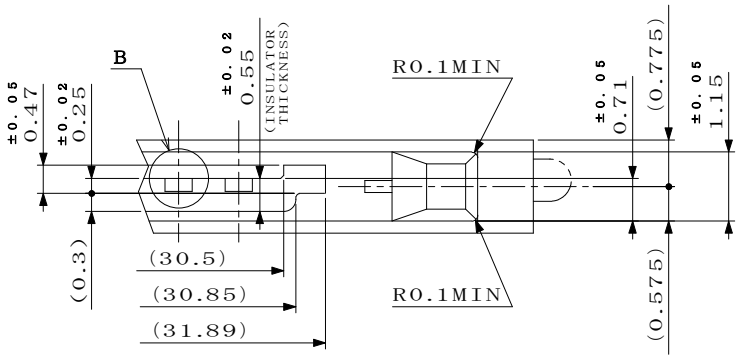
Figure 7-9: 30 pin Panel-side Receptacle Connectors Detail

7.2.2 30 pin Cable Plug Connector

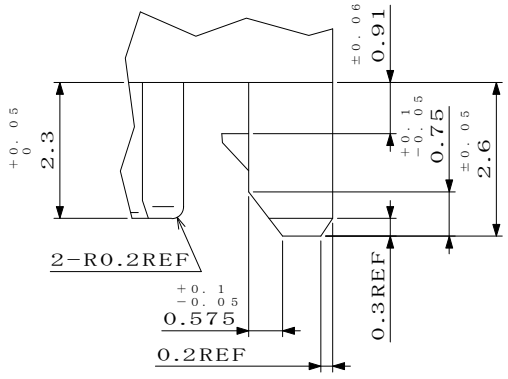


Note 1: This area is ground area

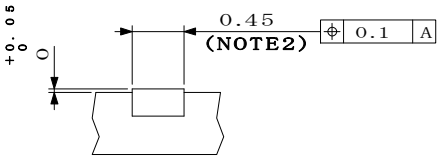
Figure 7-10: 30 pin Cable-side Plug Connector



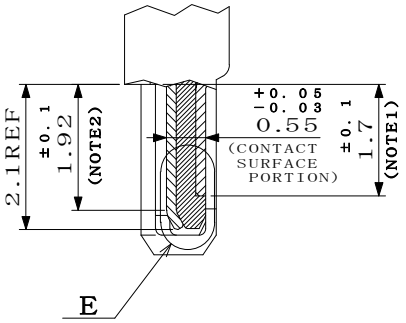
DETAIL A



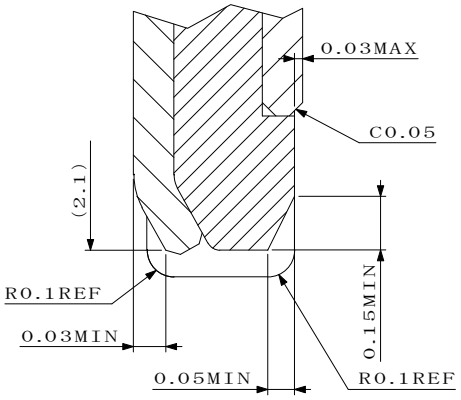
DETAIL C



DETAIL B



SECT. D-D



DETAIL E

Note 1: This area is ground area

Note 2: This area is signal contact area

Figure 7-11: 30 pin Cable-side Plug Connector Detail

MATED CONDITION(REF.)

Figure 7-12: 30 pin Mating Condition

7.3 40 pin Standard Connector

7.3.1 40 pin Panel-side Receptacle Connector

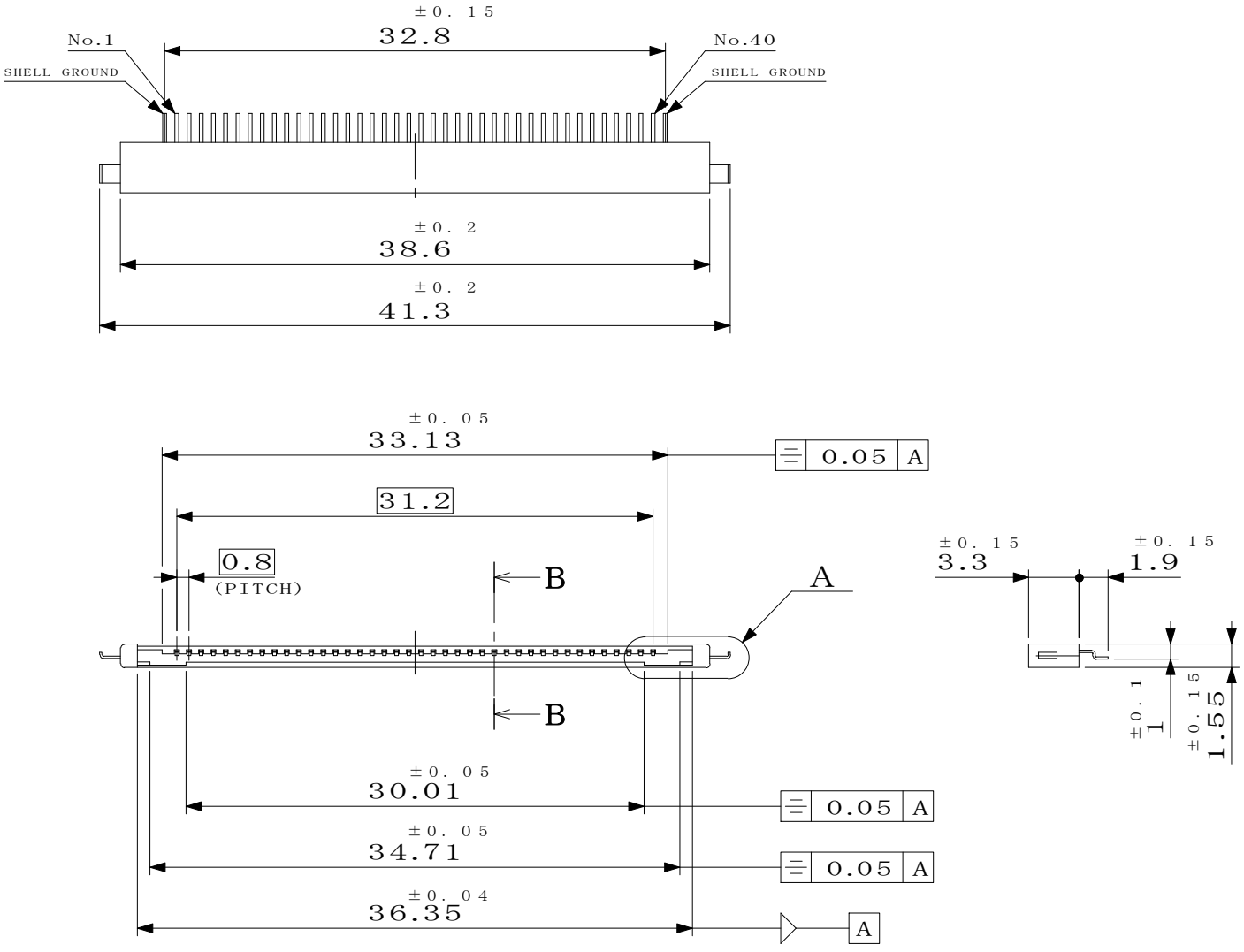


Figure 7-13: 40 pin Panel-side Receptacle Connector

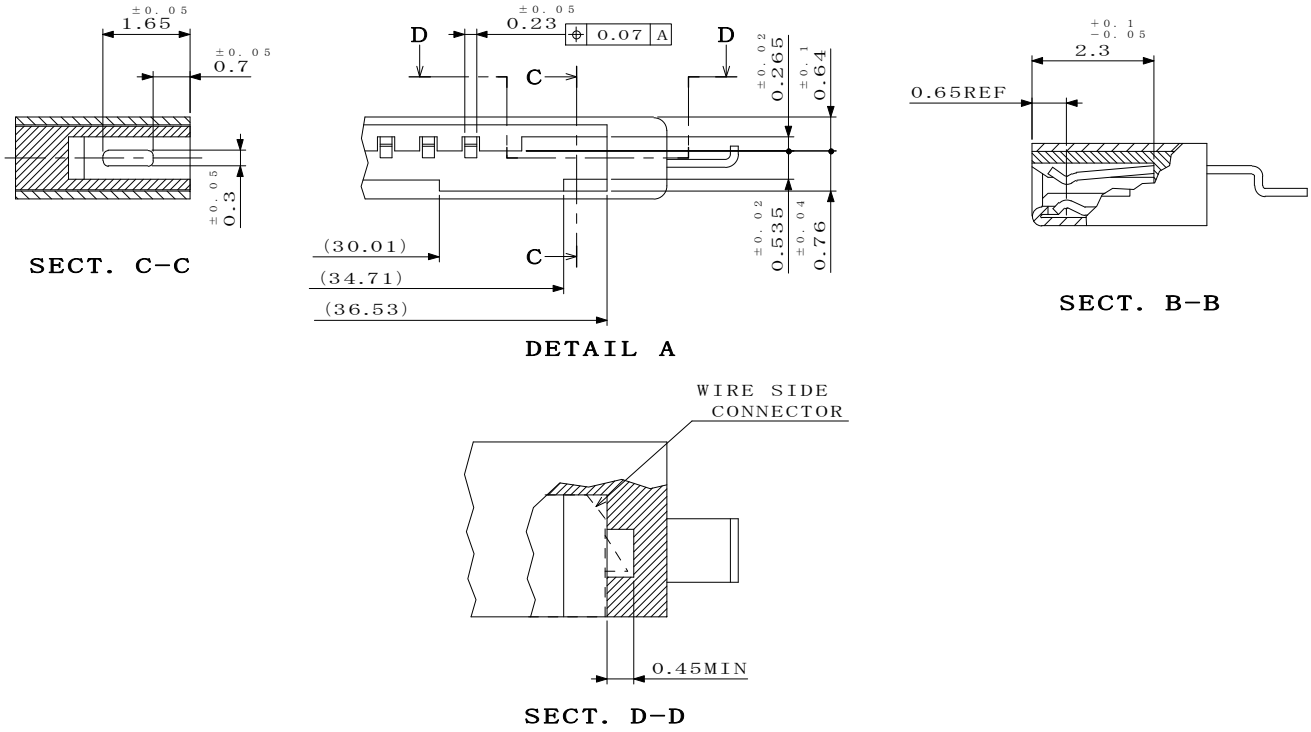


Figure 7-14: 40 pin Receptacle Connector Detail

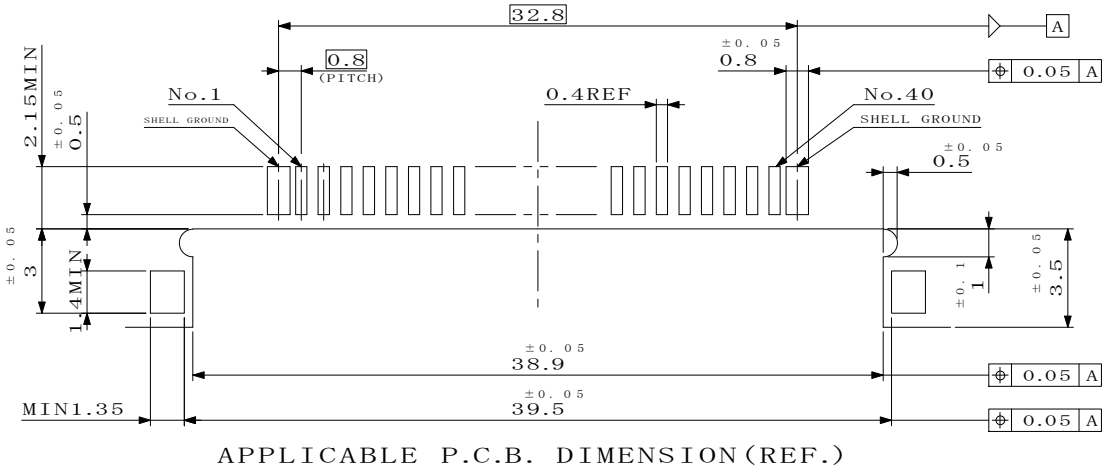
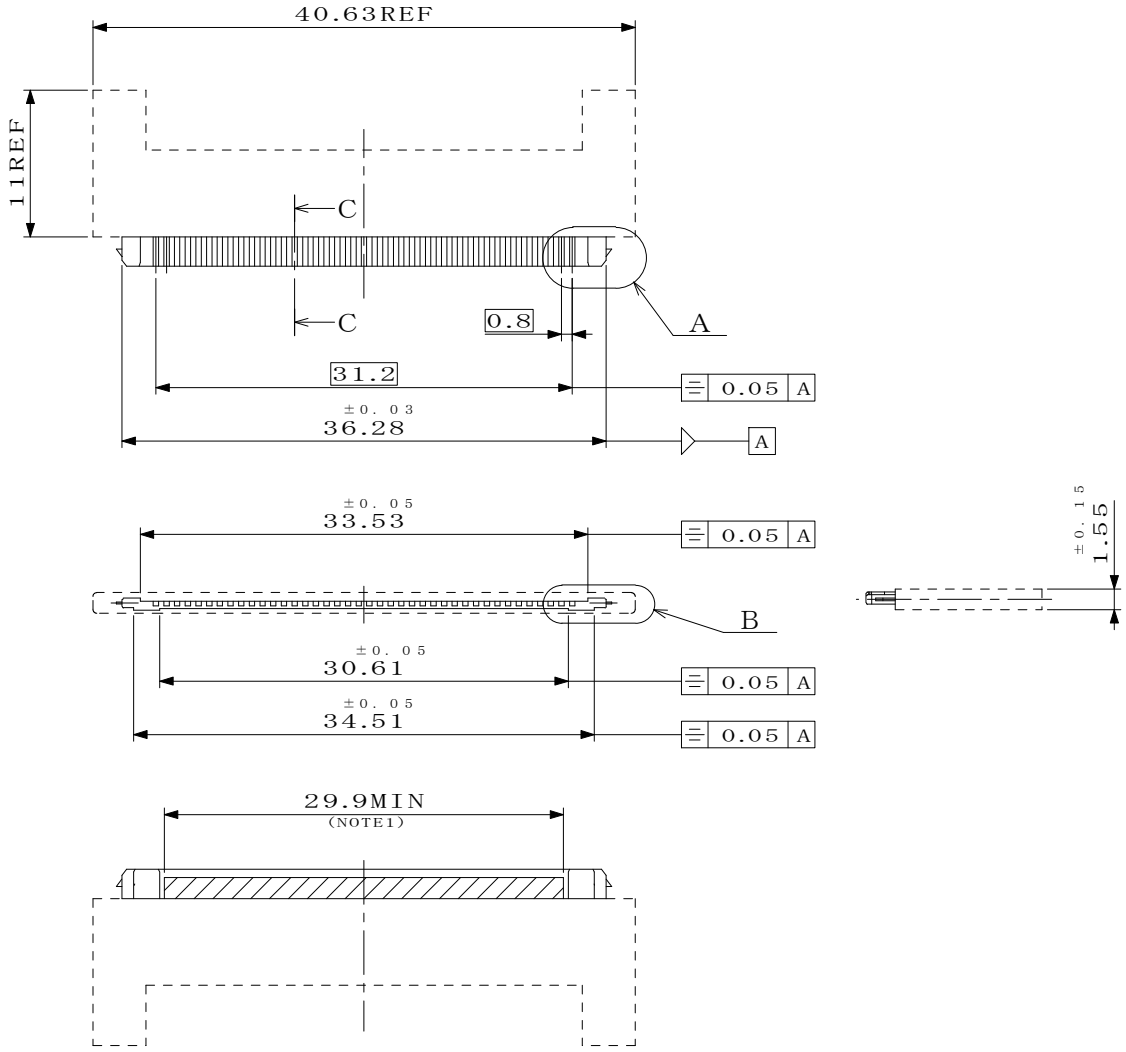


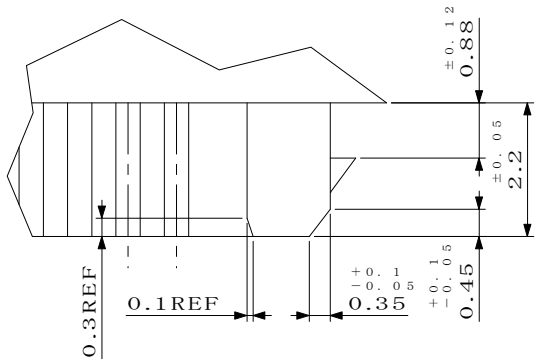
Figure 7-15: 40 pin Panel-side Receptacle Connector PCB Mounting Pattern

7.3.2 40 pin Cable Plug Connector

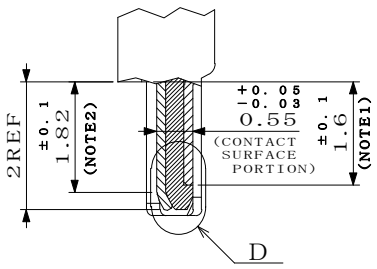


Note 1: This area is ground area

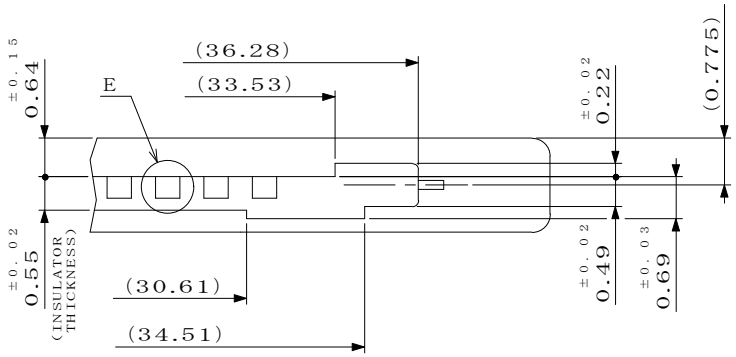
Figure 7-16: 40 pin Cable-side Plug Connector



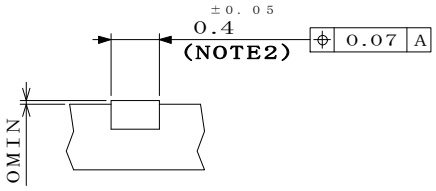
DETAIL A



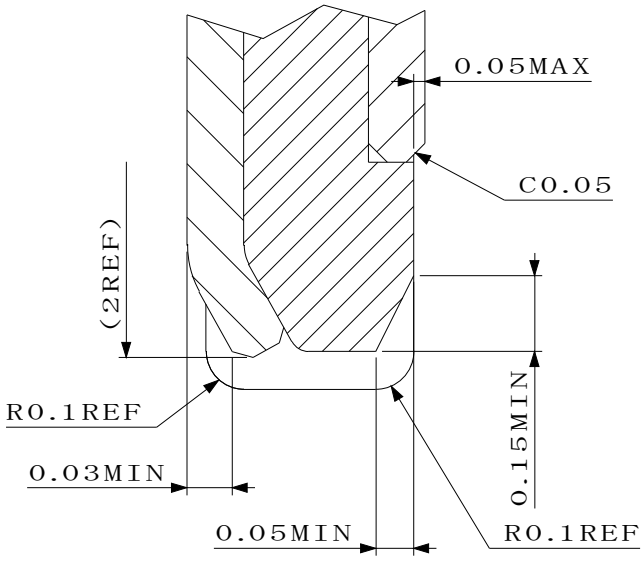
SECT. C–C



DETAIL B



DETAIL E



DETAIL D

Note 1: This area is ground area

Note 2: This area is signal contact area

Figure 7-17: 40 pin Cable-side Plug Connector Detail

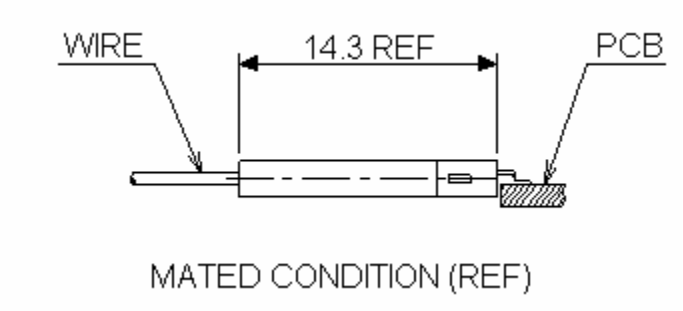


Figure 7-18: 40 pin Mating Condition

7.4 Connector Electrical, Mechanical and Environmental (EME) Requirements

The following tables describe EME requirements of the panel connector.

Table 7-7-1: 20 pin Connector EME Requirements

Item	Test Condition	Requirement
Vibration	Frequencies of 10 to 55Hz. Single amplitude 0.75 mm, 5 minutes x 10 times, on 3 axis. Per JIS-C-5402-5.5.6.1	1. No electrical discontinuity of 1μsec. 2. No physical damage, cracks or parts dislocation.
Shock	Acceleration 490m/s^2, pulse duration 11ms, 3 times in 3 axis. Waveform: Half sine. Per JIS-C-5402-5.5.6.2	1. No electrical discontinuity of 1μsec. 2. No physical damage, cracks or parts dislocation.
Durability (mating/unmating, with corresponding part)	30 cycles at 600 cycles/hour per JIS-C-5402-6.3	1. Contact resistance: 30mΩ max. 2. No physical damage, cracks or parts dislocation.
Connector insertion force	Measure the total force required to mate with corresponding part.	60N max.
Connector withdrawal force	Measure the total force required to un-mate with corresponding part.	4N min.
Dielectric withstanding voltage (voltage proof)	300V AC for 1 min. per JIS-C-5402-5.1C	No flashover or breakdown.
Insulation resistance	100V DC Between adjacent circuits, unmated connectors, for 1 minute per JIS-C-5402-5.2C	500MΩ min.
Low level contact resistance	Mated connectors, contacts assembled in housing. Dry circuit 20mV max. open circuit at 10mA, per JIS-C-5402-5.4	30mΩ max.
Temperature raise	Measure temperature raise caused by the flow of the current.	AWG# 28 = 1.0A, AWG# 30 = 0.9A, AWG# 32 = 0.8A, AWG# 36 = 0.5A Per contact, 30°C max temp raise over ambient.
Humidity and temperature (steady state)	40°C ±2°C, 90 to 95% RH, 96 hrs per JIS-C-5402-7.3	1. Contact resistance; 30 mΩ max. 2. Insulation resistance: 500 MΩ min. 3. No physical damage, cracks or parts dislocation.
Thermal shock	Temp (C): -55 -> +5 to +35->+85 >+5 to +35 Time (min.): 30->2 to 3 -> 30 -> 2 to 3 5 cycles per JIS-C-5402-7.2	1. Contact resistance; 30 mΩ max. 2. Insulation resistance: 500 MΩ min. 3. No physical damage, cracks or parts dislocation.
Temperature life (heat age)	85°C for 96 hours per JIS-C-5402-7.8	1. Contact resistance; 30 mΩ max. 2. No physical damage, cracks or parts dislocation.

Table 7-2: 30 & 40 pin Connector EME Requirements

Item	Test Condition	Requirement
Vibration (Random)	Frequency: 10Hz to 2000Hz Acceleration Vel. 30.38m/s^2 (3.1G) RMS. Application direction: In each of 3 mutually perpendicular axes. Duration: 15 minutes per sample per EIA-364-28, Test condition VII, test condition D.	100mA applied with no electrical discontinuity greater than 1µ sec.
Physical Shock	Sample shall be mounted on the test jig as mounted on the PCB. Acceleration velocity 490m/s^2 or 50G. Waveform: half sine Duration: 11 msec. Number of drops: 3 drops each to normal and reversed directions of X, Y and Z axes. Total 18 drops. Per EIA-364-27, Method A.	No electrical discontinuity greater than 1 µsec shall occur.
Durability (mating and unmating).	Number of cycles: 50 Cycling Rate: 100 ± 50 cycles per hour per EIA-364-09	R = 40mΩ Max. (Initial) R = 80mΩ Max. (Final)
Connector Insertion Force	Operation speed: 12.5mm/min. Measure the force required to mate connector including the latching mechanism per EIA-364-13	35N Max per connector (30pin) 47N Max per connector (40pin)
Connector Withdrawal Force	Operation speed: 12.5mm/min. Measure the force required to unmate connector excluding the latching mechanism; per EIA-364-13	5N Min-25N Max per connector (30 pin) 7N Min-33N Max per connector (40 pin)
Dielectric withstanding voltage	0.25 kVAC for 1 minute Test between adjacent circuits of unmated connectors; per EIA-364-20	No creeping discharge or flashover shall occur. Current leakage: 0.5 mA Max.
Insulation Resistance	Impressed voltage 100 VDC between adjacent circuits of unmated connectors for 2 minutes; per EIA-364-21.	100 MΩ Min (initial) 50 MΩ Min. (final)
Low Level Contact Resistance	Subject mated contacts assembled in housing measured by dry circuit 20mV maximum open circuit at 10 mA per EIA-364-23	R = 40mΩ Max. (Initial) R = 80mΩ Max. (Final)
Temperature Rise	Measure temperature rise by energizing current per EIA-364-70, Method 1.	Maximum rated current per contact: 0.50 A at 30° C max ΔT over ambient.
Humidity and Temperature Cycling	Cycle mated connector, 25ºC to 65ºC and 50% to 80% R.H. 10 cycles and 10 cycles of cold shock at -10ºC per EIA-364-31, Method 4	Mated Condition: Contact Resistance: R = 80mΩ Max. (final) Unmated condition: Insulation resistance (final) 50MΩ Min. ΔR = 50MΩ Max.
Thermal Shock	Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes; repeat for 10 cycles, per EIA-364-32	R = 40mΩ Max. (Initial) R = 80mΩ Max. (Final)
Temperature Life (heat age)	Subject mated connector to 105ºC for 168 hours per EIA-364-17	R = 40mΩ Max. (Initial) R = 80mΩ Max. (Final)