NAVI ™ Standard

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VESA New Analog Video Interface

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Purpose

This proposal defines new features and functionality for both the existing (VGA) analog interface, as well as defining how these may be implemented on later, higher-performance interface systems. It also defines a new compact connector for providing this high-performance analog interface and a standard digital video interface for PDAs, notebooks, and similar portable appliances. This new interface definition is intended to be usable for PC, information appliance, and consumer electronics applications.

Summary

In recent years, various attempts have been made to define digital interfaces as a replacement for the existing analog RGB display connections provided by the "VGA" and similar connector systems. These efforts have faced significant problems due to the very large installed base of the traditional VGA interface. This specification defines a means for adding many of the features of existing digital interface standards - such as improved performance on fixed-format displays, data communications, and content protection – to existing analog and mixed analog/digital interface standards, such as the "VGA" (15-pin high-density D-subminiature connector). One completely new connector, the VESA NAVI-D (for "NAVI-Desktop"), is also defined by this standard.

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Intellectual Property

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As of this writing, several companies are known to hold patents or other intellectual property relating to the interface operation and specifications contained within this proposal. These include, but are not necessarily limited to, the following. The holder of the intellectual property in question should in each case be contacted for information regarding the licensing of such property as it may be necessary to implement various portions of the interface system described in this standard.

Hewlett-Packard Co.	Methods and protocols relating to the advanced analog interface features, including the sampling clock reference transmission, active video detection and gain control, data transmission, and analog interface content protection features as described in this proposal, and the "Mode D" transmission system.
Molex, Inc.	The "MicroCross"™ and contact technology/designs used in the "NAVI-D" connector described in this proposal.
Silicon Image, Inc.	Unspecified intellectual property.

Other Documents Referenced

Several other standards and specifications are referenced by this standard, and their requirements may be considered a part of this specification as indicated herein. These include the following, listed along with the controlling group or authority in each case:

VESA Enhanced Display Data Channel (E-DDC) Standard, Version 1.1, March 24, 2004
VESA Enhanced Extended Display Identification Data Standard (E-EDID), Rel. A, Rev. 1, Feb. 9, 2000
VESA Monitor Command Control Set (MCCS), Version 2, October 17, 2003
VESA Video Signal Standard (VSIS), Version 1, Rev. 2, December 12, 2002
VESA Digital Packet Video Link (DPVL) proposal, Version 1, April 18, 2004

Universal Serial Bus 2.0 Specification (USB Implementer's Forum, Inc.)

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product which incorporates any variant of the NAVI system, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

- Fax: 408-957 9277, *direct this note to Technical Support at VESA*
- e-mail: support@vesa.org
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1. Overview

VESA's New Analog Video Interface standard was developed in response to a desire on the part of many VESA members to provide the advantages of current "digital" interfaces, while not requiring an interface which is completely incompatible with the installed base of analog ("VGA" and other) video systems. The NAVI standard achieves this by adding features and functionality to the existing analog video signal set, in such a way that compatibility with VGA and similar interfaces is maintained. The result is an interface which provides excellent support for both CRT and non-CRT (fixed-format) display devices, and a clear growth path from the existing VGA standard connector through new types providing improved performance and form factors. In addition, the NAVI interface also provides a true "digital" mode, enabling digital video transmissions (and ultimately, the support of advanced digital-only functionality such as packetized video, compression and encryption, etc.) on this same basic VGA-compatible physical and electrical interface.

To understand how this is possible, it is first necessary to realize that many of the advantages of the "digital" interface systems have very little, if anything, to do with the fact that the data is being conveyed in "digital" form. The primary advantages of these systems with fixed-format displays comes from the addition of signals which could also be of use in an analog video system – the transmission of a data sampling clock ("pixel clock"), and additional signals (generically referred to as a "display enable") which clearly identify the start and stop of active video. The traditional analog interface systems, with their roots in CRT-based display systems, have to date not provided such signals, and so have been difficult to use with fixed-format displays such as the LCD. The NAVI system corrects this, and adds support for these features to the existing VGA interface as well as defining how these may be added to newer interface definitions.

The NAVI standard also defines several additional features which greatly enhance the usefulness of the traditional analog interface in modern systems. First, two levels of serial data transmission, using the existing connections of the VGA interface, are defined by this specification, including a medium-speed bi-directional communications protocol. These provide support for digital audio transmission from the host system to the display, as well as enabling a content-protection system to be optionally supported in NAVI-compliant devices. There is also support for automatic compensation for cable losses and skew, again significantly improving the performance of the basic analog interface. In addition, an optional "true digital" mode (NAVI Mode D) is defined, which takes advantage of the basic NAVI enhancements and an AM digital encoding scheme to transmit digital information in the 2-5 Gbit/second range, a capacity equal to that of existing digital interface standards and more than adequate to support advanced video standards such as the VESA Digital Packet Video Link (DPVL) specification. This is achieved while keeping the physical and electrical interfaces fully VGA-compatible and capable of supporting unmodified "legacy" VGA devices.

Within the NAVI system, three standard connectors are defined at this time. First, the use of the NAVI features on the standard "VGA" (15-pin HD) connector is defined; this provides the functionality described above for systems which also wish to retain complete compatibility with the existing analog video interface. This is referred to as the "NAVI-V" (for "VGA") implementation. Also, a new connector has been defined, providing the NAVI functionality with additional features and improved performance in new physical form factors. The "NAVI-D" (for Desktop) is intended to be the standard connector for desktop systems and monitors, and similar larger equipment. It provides greatly improved analog signal performance (and support for faster operation in the digital NAVI Mode D) as compared with the VGA connector, as well as support for added features such as power.

With the added functionality, and especially the support for digital audio and video transmission and content protection on both the analog and digital display interfaces, it is expected that the NAVI definition may also be very attractive for use in consumer electronics applications, such as televisions, VCRs, set-top converter boxes, and similar appliances. To make the system better suited to such use, this standard also defines the use of optional color encoding methods (such as composite video, Y/C video, and YUV) on the various NAVI implementations.

Digital Transmission Modes

While NAVI is fundamentally an enhancement of the existing VGA "analog video" standard, it also includes several means of carrying "digital" information over this physical/electrical interface. Two of these are intended as general-purpose channels for the transmission of supplemental information (such as ID information, command and control codes, audio, etc.) between the host and display; in addition, a protocol for conveying a digitally-encoded form of video over the existing "analog" video channels. These provide a means of supporting a number of features requiring "digital" communications between the host system and the display device. They are distinguished primarily by their data capacity and the fact that the "base" digital protocol (the "Type 1" data channel, defined in section 2.6 of this document) permits bi-directional communications (and thus permits data to be sent from the display to the host system). The basic characteristics of each of these systems are summarized in the table below. Please note that support for any or all of these modes is optional under the NAVI standard. As the data capacity of these varies with the video timing currently in use, examples of the capacity at several clock rates (i.e., what would typically be considered the "pixel" rate for a given timing) are given below.

	Serial data, Type 1	**Serial data, Type 2**	**Mode D Video**
Ref. section of standard	2.6	2.7	3
Physical channel	HSYNC line	HSYNC line	RGB video lines
Encoding method	Serial data at 1/8 pixel clock rate*	Serial data at 1/8 pixel clock rate*; data modulates falling edge of clock reference signal.	Video encoded at 3 or 4 bits/symbol, multi-level encoding, symbols transmitted at 2X the desired pixel rate.
Directionality	Bi-directional	Host-to-display only	Host-to-display only
Intended use(s)	General-purpose low-speed data; ID, command & control functions, etc.	General-purpose medium-speed data; supplemental data such as digital audio, etc.	Digital video (replaces analog video as an alt. mode of communicating with the display itself).
Data capacity[1]			
At 25 MHz "pixel" rate	~15.8 kbps[2]	~2.75 Mbit/sec.[3]	450-600 Mbit/sec.[4]
At 100 MHz "pixel" rate	~ 63 kbps[2]	~10-11 Mbit/sec.[3]	1.8 - 2.4 Gbit/sec.[4]
At 200 MHz "pixel" rate	~126 kbps[2]	~20-22 Mbit/sec.[3]	3.6 - 4.8 Gbit/sec.[4]
Error detection	CRC	CRC	Checksum (1 per frame)

1. Standard-definition TV uses a slightly different clocking scheme; see sections 2.3.2 and 2.6.
2. Type 1 capacities listed are the total of both outbound (host to display) and inbound (display to host) transmissions. Typically, the outbound channel is allocated 1/3 of this total.
3. Type 2 capacity depends on the percentage of the total H. time used by the HSYNC pulse.
4. Mode D capacities are totals assuming 3 video lines (i.e., a standard RGB connection) used.

2. Analog Interface – Electrical Specifications

This section defines the requirements for the electrical characteristics of the analog video interface used in all implementations of the NAVI system. Please note that this also includes the definitions for the two forms of serial data communications that are associated with this interface, as these involve one of the basic video interface physical connections (the reference clock/HSYNC connection described in 2.3).

Signals and operation specified in this section include the following (with section numbers and starting pages for each):

Analog video signals; amplitude and system impedance requirements ..... Sec. 2.1, pg. 8
Synchronization signals; impedance, termination, VSWR ..... Sec. 2.2, pg. 9
Sampling clock reference signal; combination with HSYNC and gen'l requirements ..... Sec. 2.3, pg. 9
Amplitude references; amplitude reference pulse (ARP) ..... Sec. 2.4, pg. 12
Active video location (AVL) pulses ..... Sec. 2.5, pg. 14
Serial data transmission via reference clock/HSYNC line, Type 1 ..... Sec. 2.6, pg. 16
Basic operation ..... Sec. 2.6.1-2.6.3, pg. 18
Format and CRCs ..... Sec. 2.6.4, pg. 18
Secondary header codes ..... Sec. 2.6.5-2.6.8, pg.21
Timing requirements for Type 1 operation ..... Sec. 2.6.9, pg. 30
Serial data transmission via reference clock/HSYNC line, Type 2 ..... Sec. 2.7, pg. 31

2.1 Video Signals

All implementations of the NAVI system shall provide, at a minimum, analog RGB video and sync signals per the specifications of this section. Note that these are intended to be compatible with the VESA Video Signal Standard (VSIS) specification, with differences as explicitly noted here. The use of non-RGB forms of video is covered by the specifications and requirements of Section 7 of this standard. The video source is further required to comply with all requirements of the VESA Video Signal Standard (VSIS) not explicitly mentioned here.

2.1.1 Signal Amplitude and Video System Impedance

All video signals shall have a nominal amplitude of 0.700 V peak-to-peak, as measured from the nominal blanking (black/reference) level to the maximum normal white level, and with a system impedance of a nominal value of 75 ohms, resistive. Except as noted under section 2.5, below, the DC offset of any video signal shall not exceed 1.0 VDC as measured between the nominal blanking (black/reference) level and the video return pin as defined by the specification for the physical connector in question.

All other requirements regarding the video signal characteristics, including rise/fall times, noise, linearity, overshoot, ringing/settling time, etc., shall be as defined by the VESA Video Signal (VSIS) Standard unless otherwise noted here.

2.2 Synchronization Signals

All implementations of the NAVI shall provide horizontal and vertical synchronization signals for the analog interface ("HSYNC" and "VSYNC," respectively) as separate TTL-level signals, per the requirements of the VSIS standard, with the following exceptions:

2.2.1 Horizontal Sync Signal Impedance/Termination.

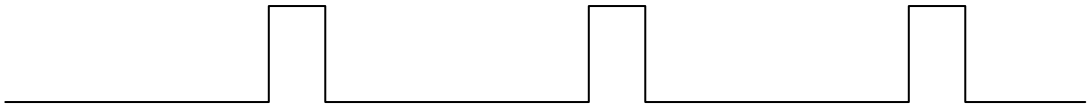
All NAVI-compliant devices and cable assemblies shall supply the horizontal sync signal via 75 ohm characteristic impedance path, and with a termination impedance at both source and receiver of 75 ohms, resistive, such that a VSWR of 1.2:1 or less is maintained on this line over the frequency range of 0 to 100 MHz, minimum.

2.3 Sampling Clock Reference Signal

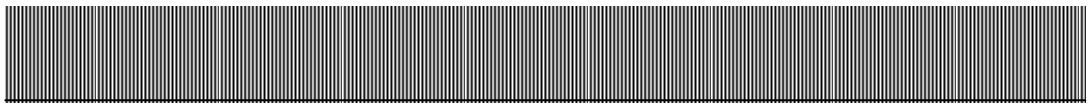
All NAVI-compliant video sources shall be capable of providing a combined HSYNC/sampling clock reference signal, via the horizontal sync line, per the specifications of this section. This function must be enabled immediately (within one frame time at the current timing) upon the assertion of the NAVI_ENABLE signal (provided by the display, as defined for the physical connector in question), and similarly must be disabled immediately upon the negation of NAVI_ENABLE by the display. Note that use of the sampling clock reference is optional for the display, and not all displays will make use of this feature. When NAVI_ENABLE is not asserted, the horizontal sync signal must be provided as is normal under the requirements of the VESA VSIS standard and the video timing standard in use. When present, the sampling clock reference signal shall be used by NAVI-compliant displays to generate a sampling clock with which to sample the incoming video signal, as described elsewhere in this standard; if the reference signal is not provided by the host (as in the case of a NAVI-compliant display connected to a non-NAVI host), the display must also be capable of deriving such a sampling clock from the standard horizontal sync signal or otherwise establish suitable sampling (such that a usable image is obtained for all timings within the capabilities specified for the display) without user intervention.

2.3.1 Sampling Clock Reference and HSYNC combination

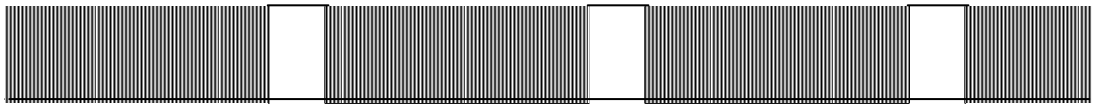
Whenever NAVI_ENABLE is asserted by the display, the host will provide a combined HSYNC and sampling clock reference via the horizontal sync signal connection, by combining a 1/8 pixel clock rate signal with the HSYNC as shown in Fig. 2-1. The circuitry combining these signals must be designed such that a spurious transition does not occur at the leading and trailing edges of the HYSNC pulse, i.e., all edges in the combined signal must be aligned with the sampling clock reference, plus or minus the skew introduced by the combining process. Note that an HSYNC pulse of either polarity may be used.



a. Original HSYNC signal (provided when NAVI_ENABLE not asserted)



b. Clock reference (1/8 pixel clock rate)



c. HSYNC/Sampling Clock Reference signal (provided on HSYNC line when NAVI_ENABLE is asserted by the display)

Fig. 2-1 – HSYNC and clock reference combination

2.3.2 Sampling Clock Reference Signal Frequency, Active Edge, and Duty Cycle

The frequency of the sampling clock reference signal shall be 1/8 that of the pixel rate (pixel clock frequency) defined for the video timing currently in use. The only exception to this is for systems employing a NAVI interface to carry standard-definition television video, i.e., 525-line or 625-line interlaced timings at 50 or 60 Hz field rates. In those cases, the sampling clock reference signal is transmitted at the full pixel clock rate. The active edge of this clock reference signal shall be the rising (positive-going) transition. The sampling clock reference signal shall be provided with a duty cycle of 50% nominal (max. 55% high, min. 45% high, ignoring the HSYNC periods), except when used for Type 2 serial data communications as defined in section 2.7.

2.3.3 Sampling Clock Reference Signal Amplitude

The amplitude of the combined HSYNC/sampling clock reference signal should nominally be 1.0 Vp-p, as measured at the output of the video signal source into a standard 75 ohm resistive load. Note that this requirement applies only during the NAVI mode of operation, i.e., when the combined reference clock and HSYNC signal is being transmitted to a NAVI-compliant host; during those times when only a conventional HSYNC signal is being transmitted, the signal should conform to the standard TTL levels and other requirements as described in the VSIS specification.

2.3.4 Sampling Clock Reference Signal Rise/Fall Time; Other Parameters

The rise/fall times of the combined HSYNC/sampling clock reference signal, as measured at the source connector into a standard 75 ohm resistive load, shall not exceed 80% of the minimum pixel clock period supported by the host hardware. All other parameters regarding this signal shall also conform to the requirements of the VESA Video Signal Standard, section 2.2, with the exception of the substitution of the 50 ohm resistive load for the termination specified in that standard.

2.3.5 NAVI_ENABLE Signal Requirements

The NAVI_ENABLE signal shall be provided by NAVI-compliant displays when the sampling reference clock is desired to be supplied by the host, via the appropriate physical connection as defined for the connector in question (in later sections of this standard). To assert NAVI_ENABLE, the display will set this line to the HIGH state (≥ 2.4 VDC with respect to the defined sync return connection at the display input connector), and must be capable of supplying up to 2 mA while maintaining this condition. When the NAVI_ENABLE signal is not asserted by the display, the display may permit this line to "float", or it may be grounded. It is acceptable under this standard that the display assert NAVI_ENABLE simply by tying the appropriate +5VDC pin from the NAVI connected to the NAVI_ENABLE pin, through a resistance of not greater than 2.2 kohm, or less than 1 kohm.

2.3.6 HSYNC Drive Disabling

In order to avoid possible drive conflicts on the HSYNC line, it is mandatory that all NAVI-compliant video sources stop driving the HSYNC line, with either the HSYNC pulse itself or with the sampling clock reference signal as described in this section, during the period of the VSYNC pulse. For more information, see section 2.6 describing Serial Data Transmission, Type 1.

2.4 Amplitude References; Amplitude Reference Pulse

All NAVI-compliant video sources shall be capable of providing, whenever NAVI_ENABLE is asserted, a full-white-level pulse on all video outputs during each horizontal blanking period, including those which occur during the vertical blanking period, as specified in this section. This pulse may be used by the display to determine the error due to cable losses or other factors in the delivered video signal amplitude, and thus to provide an automatic correction for such losses. These pulses will be provided during each horizontal blanking period whenever the signal NAVI_ENABLE is asserted by the display. Each pulse is positioned within the blanking period such that the display may use the recovered HSYNC pulse as a blanking signal, thus ensuring that the amplitude reference pulse or ARP will not be visible in the displayed image.

2.4.1 Amplitude Reference Pulse Amplitude, Duration, and Position

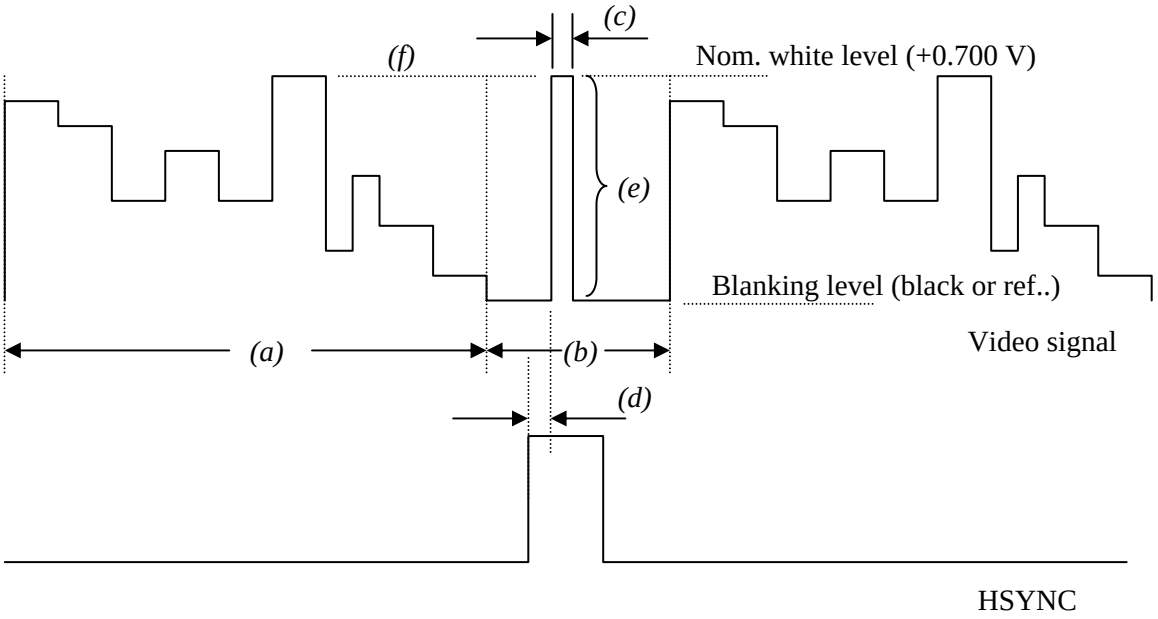
Referring to Fig. 2-2 (following page), the characteristics of the NAVI amplitude reference pulse, or ARP, shall be as follows. The amplitude of this pulse, as measured under the same conditions as specified for the active video itself, shall be nominally equal to the standard full-scale white amplitude (+0.700 V, with respect to the reference blanking (black or 0) level), and must not differ from the actual amplitude produced by the hardware in question, when set to the full white level during the active video period, by a peak error of greater than ± 0.5%. The duration of the ARP shall be 32 pixel periods (based on the video timing currently in use), and the ARP shall begin 32 pixel periods following the leading edge of the HSYNC pulse (as measured at the video source).

2.4.2 ARP Signal Characteristics

Beyond the requirements specified for the amplitude reference pulse above, all other video signal requirements of the VESA Video Signal Standard (i.e., rise and fall times, overshoot, etc.) also apply to this pulse. When enabled, these pulses are to be supplied by the video source on all video outputs.

2.4.3 Detection of ARP by Display

The display is to consider any pulse occurring on its video inputs during the period specified above, and having an amplitude as received of at least +0.400 V with respect to the reference blanking level, as a valid ARP and may use such pulses for video gain control. The nature and operation of the gain control function is up to the individual manufacturer, and may be made so as to be disabled by the user. Should no pulse be detected of the required amplitude, the display should assume failure or absence of the ARP function in the host, and disable any automatic video gain control or other features based on this pulse.



Item	Description	Specification
a	Active video period	As defined by video timing in use.
b	Blanking period	As defined by video timing in use.
c	ARP duration	32 pixel periods at current video timing
d	ARP delay from HSYNC	32 pixel periods at current video timing
e	ARP amplitude	Nom. +0.700 V with respect to blanking level*
f	(note)	ARP amplitude to be within ± 2% of full white as it would be produced during the active video period.

Fig. 2-2 – Amplitude Reference Pulse (ARP) specifications

* - Note: The Amplitude Reference Pulse shall be generated using the same drivers, reference, etc., as the normal video white level, so as to ensure that its amplitude will always track that of the nominal white level as seen during the active video time. It is, for example, not acceptable to insert a pulse from a separate driver into the video signal in order to produce the ARP.

2.5 Active Video Location Pulses

In addition to the amplitude reference pulse described in the previous section, all NAVI-compliant video sources shall also provide pulses which are to be used by the display in determining the start and stop of the active video period of each line and frame. These pulses are again to be provided on all video outputs whenever the NAVI_ENABLE signal is asserted by the display (see section 2.4.4), and must occur as specified below at the start and stop of each horizontal blanking period, including those which occur during the vertical blanking period. These are referred to as Active Video Location, or AVL, pulses.

2.5.1 AVL Pulse Amplitude, Duration, and Positions

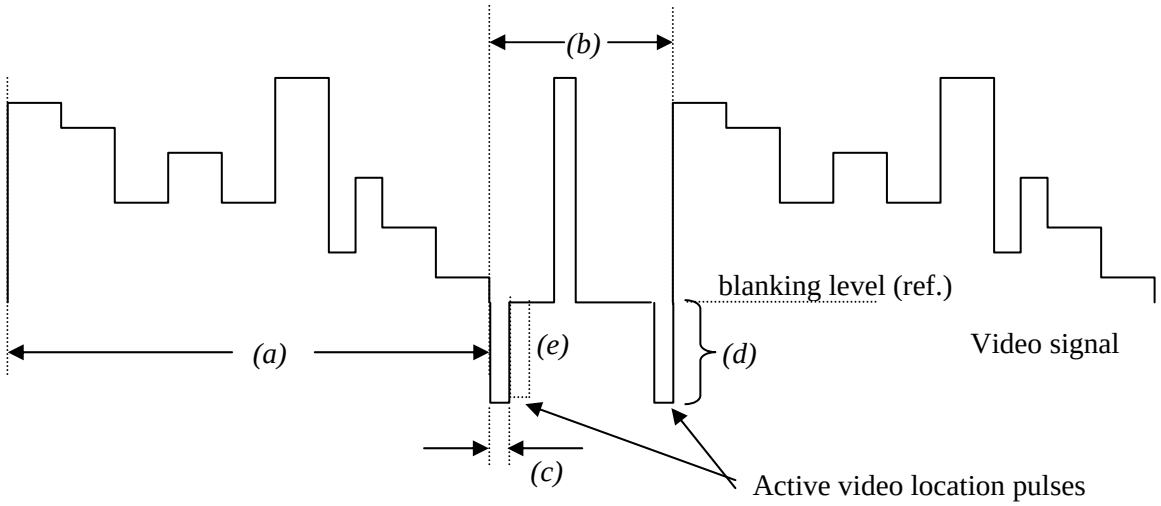
Referring to fig. 2-3 and the accompanying table, the AVL pulses are provided by the video source on all video outputs whenever the NAVI_ENABLE signal is asserted by the display, per the following requirements. The AVL pulses are negative-going (with respect to the blanking level) pulses of 8 pixel periods (at the current video timing) duration, positioned immediately at the start and end of each horizontal blanking period; i.e., the pulse defining the end of active video is located such that its leading edge occurs at the start of the blanking period, and the pulse defining the start of active video is positioned such that its leading edge occurs 8 pixel periods before the start of active video. These pulses must be aligned with the video data such that the leading edge of the pulse occurs within +/- 10% of the nominal pixel leading edge time (max. error). Note that as these pulses are intended as the phase reference from which alignment of the pixel sampling clock will be determined by the display, it is important that the circuits which generate these pulses in the video output be carefully designed so as to align them as closely as possible with the nominal pixel periods as seen within the active video line. In order to be able to identify the start and end of a given frame, the pulses which occur immediately after the last line of the active frame, and immediately after the last line of the vertical blanking period, are exceptions to this duration requirement. These (and only these) pulses are to be 32 pixel periods in duration (see (c) and (e) below, as well as section 2.5.3). The amplitude of all AVL pulses is nominally –0.300V with respect to the blanking level, and must be within the limits specified in the table.

2.5.2 Other Requirements for AVL Pulses

Beyond the requirements specified for the Active Video Location pulses above, all other video signal requirements of the VESA Video Signal Standard (i.e., rise and fall times, overshoot, etc.) also apply to these pulses. When enabled, these pulses are to be supplied by the video source on all video outputs.

2.5.3 AVL Pulses in Interlaced Operation

In addition to identifying the start and stop of the active frame, as described in 2.5.1 above, it is often desirable in the case of interlaced video signals to be able to distinguish the odd and even fields. In the case of 2:1 interlaced timings being supported on a NAVI-compliant system, it shall be the standard that the AVL pulses immediately after the last line of the active frame, and immediately after the last line of the vertical blanking period (which are normally 32 pixels in duration per section 2.5.1) shall be 32 pixels in duration immediately following the field designated as the first field, and 16 pixels in duration when immediately following the field designated as the second field, under the definitions of the timing standard in question.



Item	Description	Specification
a	Active video period	As defined by video timing in use.
b	Blanking period	As defined by video timing in use
c	AVL pulse duration	8 pixel periods at current video timing (applies to both AVL pulses) (see note e)
d	AVL amplitude	Nom. – 0.300V with respect to blanking level (min. –0.250 V, max. –0.350 V), under VSIS standard measurement conditions.
e	AVL pulse duration note	For the pulses that occur immediately after the last line of active video in each frame, and immediately after the last line of the vertical blanking period in each frame, the duration shall be 32 pixel periods (16 in the case of the second field of an interlaced timing, see section 2.5.3). Note that both of these occur at the *start* of their respective H. blanking periods. The pulses at the end of the H. blanking period for these lines are unchanged.

Fig. 2-3 – Active Video Location pulses (shown with amplitude reference pulse (ARP) per sec. 2.4)

2.6 Serial Data Transmission, Type 1

The NAVI system permits two forms of serial data communications between the host video source and the display device. Support for these is optional, although it should be noted that at least Type 1 support will be required in order to support certain other functions on the NAVI analog interface, including the "Mode D" digital transmission method. Both types depend on the combined clock reference/HSYNC signal as the data carrier, and the maximum data rate of both types is dependent on the reference clock rate. They are distinguished by the Type 1 protocol providing a low-speed (min. ~5 kbps) bi-directional channel, while the Type 2 method provides a higher-capacity (> 2 Mbps, min.) channel for data transmission from host to display only. It is important to note that the two types are completely independent.

Type 1 Data Transmission Protocol – Functional Description

In the Type 1 protocol, the clock signal on the HSYNC line is replaced by a serial data stream at the same rate, during the period defined by the vertical sync pulse (VSYNC). This period is further divided into windows for host-to-display ("outbound") communications, and for display-to-host ("inbound") communications. The basic exchange is as follows: immediately upon the assertion of VSYNC, the host will no longer transmit reference clock information on the HSYNC line, but instead will be sending serial data at the same rate. This will continue until the next assertion of HSYNC within the host timing controller, at which time the outbound data transmission will cease. During the HSYNC period, the host will stop driving the HSYNC line, and will switch to a mode of receiving data FROM the display on this path. The display will, at the same time (based on its own horizontal timing, which is assumed to continue to run independently of input from the host during this time) switch from being a data receiver to driving the HSYNC line. The display will then transmit data, again at the reference clock rate, to the host until the negation of VSYNC. Both devices will return to the normal mode of operation immediately upon the end of the VSYNC pulse.

Note that while support for this data transmission method is optional, NAVI-compliant displays must be designed so that any Type 1 signals on the HSYNC line during the VSYNC time are *not* passed to either the display's horizontal timing circuits or the sampling clock generation, to avoid the data stream causing errors. In addition, displays which are designed to support Type 1 communications back to the host must not drive the HSYNC line unless and until it has been established (through receipt of a Type 1 transmission from the host) that the host also supports this protocol.

Please note that this section defines only the basic protocol of this communications path; the data formats to be used here will be defined elsewhere.

Type 1 Data Transmission – Capacity Analysis

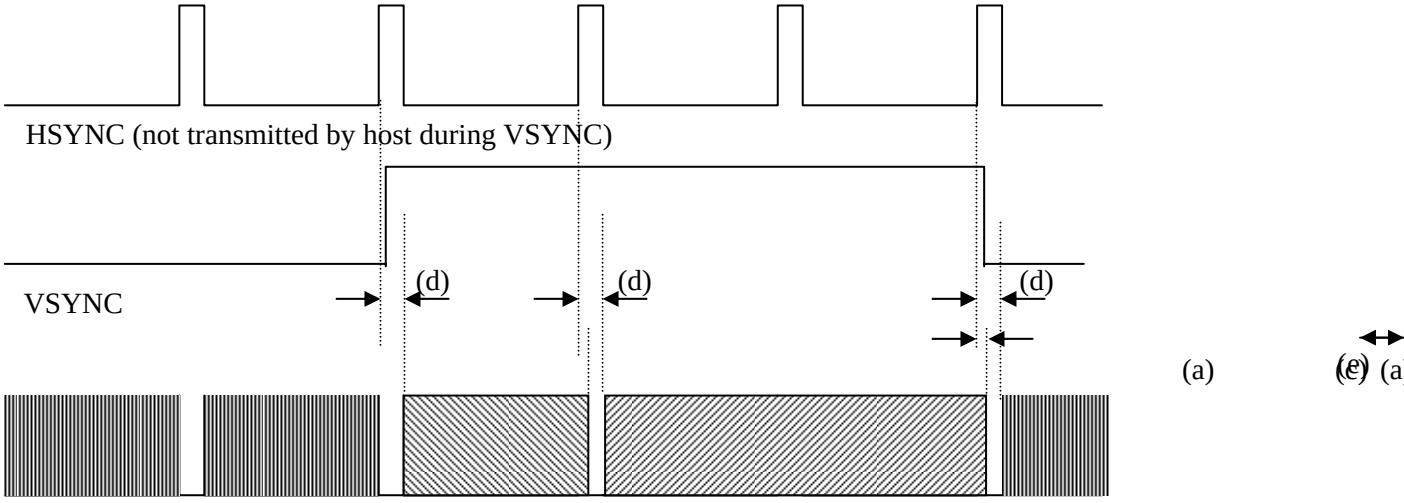
As noted above, the capacity of the Type 1 data communications method depends on the video timing in use, as it is based on the pixel clock and line timing. The data rate is the same as the fractional pixel clock transmitted as the sampling clock reference, i.e., 1/8 the rate of the pixel clock for the video timing currently in use (see exceptions for certain timings, section 2.3.2). If we assume that the slowest clock to be used under this system is that of the standard 60 Hz "VGA" (640 x 480) timing (~25 MHz), and this also represents the shortest line time (in pixels), then we have in this case a raw data rate of 25 MHz/8 = 3.125 Mbps and a total capacity as follows:

"Outbound" (host to display) capacity; one line time – horizontal sync time (in pixels/8) =

800 pixels/line – 96 pixels (HSYNC) = 704 pixels/line = 88 bits/line (at 1/8 pixel rate)

Total capacity = 88 bits/frame x 60 frames/sec. = 5.28 kbps

"Inbound" capacity (display to host) - One line/frame available for "inbound" transmission; inbound capacity same as above. (Note that for most VESA-standard timings, the VSYNC pulse is 3 horizontal line times in duration; therefore, it will more commonly be the case that the inbound path provides twice the capacity of the outbound, as shown in the diagram below.)



Ref.	Description	Specifications
a	Sample clock reference signal	See section 2.3; 1/8 pixel rate except as defined in 2.3.2.
b	"Outbound" data transmission window	Serial data at 1/8 times the current pixel clock rate, host-to-display (see 2.3.2, 2.6.1)
c	"Inbound" data transmission window	Serial data at 1/8 times the current pixel clock rate, display-to-host (see 2.3.2, 2.6.1)
d	Transmission start time	See 2.6.2, below
e	Transmission stop time	See 2.6.3, below

Fig. 2-4 – Type 1 Serial Data Communications

2.6.1 Type 1 Serial Data Transmission; Rates and Duration of Transmissions

All data transmissions using the Type 1 protocol shall occur at a bit rate equal to 1/8 the pixel clock frequency for the video timing currently in use by the system. "Outbound" (host-to-display) transmissions shall occur only during the first horizontal line time following the assertion of VSYNC, while "inbound" (display-to-host) transmissions shall occur only during the second and subsequent horizontal line times of the vertical sync period, until the negation of VSYNC, allowing for the transmission start time limitations of 2.6.2 below. These are referred to as the "outbound window" and "inbound window," respectively.

The transmission of data which occurs within a given window is referred to as a "block." Completing transmission of the data may require multiple windows to complete, and therefore may require more than one block.

2.6.2 Transmission Start Time Restriction

The start of any of (a) the serial data transmission from host to display, (b) the serial data transmission from display to host, and (c) the resumption of the sampling clock reference following these data transmission windows, must not occur earlier than 8 clock periods (i.e., 8 periods of the sampling reference clock as defined in 2.3.2) following the assertion of the host HSYNC pulse defining the beginning of the relevant period. The display must produce its own equivalent of the HSYNC signal, during the vertical sync period, with sufficient accuracy to meet this requirement.

2.6.3 Transmission Stop Time Restriction

Each of the serial data transmissions must cease, and that transmission source end its active drive of the HSYNC line, no later than 4 clock periods (i.e., 4 periods of the sampling reference clock as defined in 2.3.2) after the assertion of the HSYNC pulse defining the start of the next window or resumption of reference clock signal transmission. The display must identify, with sufficient accuracy, the video timing currently in use so that it can properly format its data transmissions to meet this requirement.

2.6.4 Restrictions - Type 1 Support in Displays

NAVI-compliant displays must be designed so that any Type 1 signals on the HSYNC line during the VSYNC time are *not* passed to either the display's horizontal timing circuits or the sampling clock generation, to avoid the data stream causing errors. In addition, displays which are designed to support Type 1 communications back to the host must not drive the HSYNC line unless and until it has been established (through receipt of a Type 1 transmission from the host) that the host also supports this protocol.

2.6.5 Transmission Header and Format; CRCs (Cyclic Redundancy Checks)

2.6.5.1 Basic Header

Both inbound and outbound transmissions must begin with an 8-bit header, consisting of the following pattern: 10101100. This is to both identify the start of the transmission and to permit the receiving device to properly synchronize the incoming data stream to its local sampling clock reference signal. If no transmission is to be made during the current window, the line must remain idle (at the default undriven state) during the entire time.

2.6.5.2 Byte Count, Secondary Header and Block CRC

In addition, the 8-bit header must be immediately followed by one byte giving the total number of valid data bytes in this transmission (not including the header or secondary header), and then one (and only one) additional 8 bit secondary header which describes the contents of the transmission, per the following tables. This will leave a minimum of 64 bits (outbound) or 152 bits (inbound) for the data packet (and CRC bytes) to be transmitted during this VSYNC period (given the minimum expected 640 x 480 format using the standard timings for this format). The specific format or required action on the part of the receiving device for each type of data transmission is described in the following sections. The final two bytes transmitted in each block shall, unless otherwise noted for a specific header/format, be a CRC of all data, including the secondary header (but not the basic 8-bit header described above) transmitted in that block. In any case where such a CRC is required to be transmitted, but the receiving device detects a CRC error, the receiving device shall issue the appropriate error response code (see below). Note that the CRC is provided at the end of each block, not at the end of each complete transmission (complete transmissions may span multiple windows). Only one secondary header, and therefore only one type of transmission or content, may be sent within a given transmission window, whether inbound or outbound.

The polynomial used for the CRC calculation is known as the CRC-16, $X^{16} + X^{15} + X^2 + X^0$. A sample implementation of the CRC generator and checker is shown in fig. 2-5. The CRC register is initialized to 0x0001 just prior to entering the first bit, and then the bytes of the transmission are shifted into the register LSB first. Note that the register bit numbers in this figure correspond to the order of the polynomial and not the bit numbers. It is more efficient to shift the CRC register in a single direction, and this results in having CRC bit 15 appear in bit position 0 of the CRC field, and CRC register bit 14 in CRC field bit 1, and so on.

The following is an example of this CRC calculation. The block contents are: 0x0007, 0x46, 0x000400, 0x00 (or represented as a sequence of bytes this is 0x07, 0x00, 0x46, 0x00, 0x04, 0x00, 0x00) and the resulting CRC is 0x0ea1 (or represented as a sequence of bytes is 0xa1, 0x0e).

When configured as a CRC checker, the CRC that is received is compared bit by bit with the value in the CRC register. If there are any errors the CRC counter will be incremented once for every block that contains a CRC error. Note that the example diagram shown in fig. 2-5 can output more than one CRC error signal within a CHECK_CRC_NOW window. Therefore, the CRC error counter must only count the first CRC error instance within each interval where CHECK_CRC_NOW is active.

If configured as a CRC generator, the CRC is clocked out of the CRC register at the end of the block.

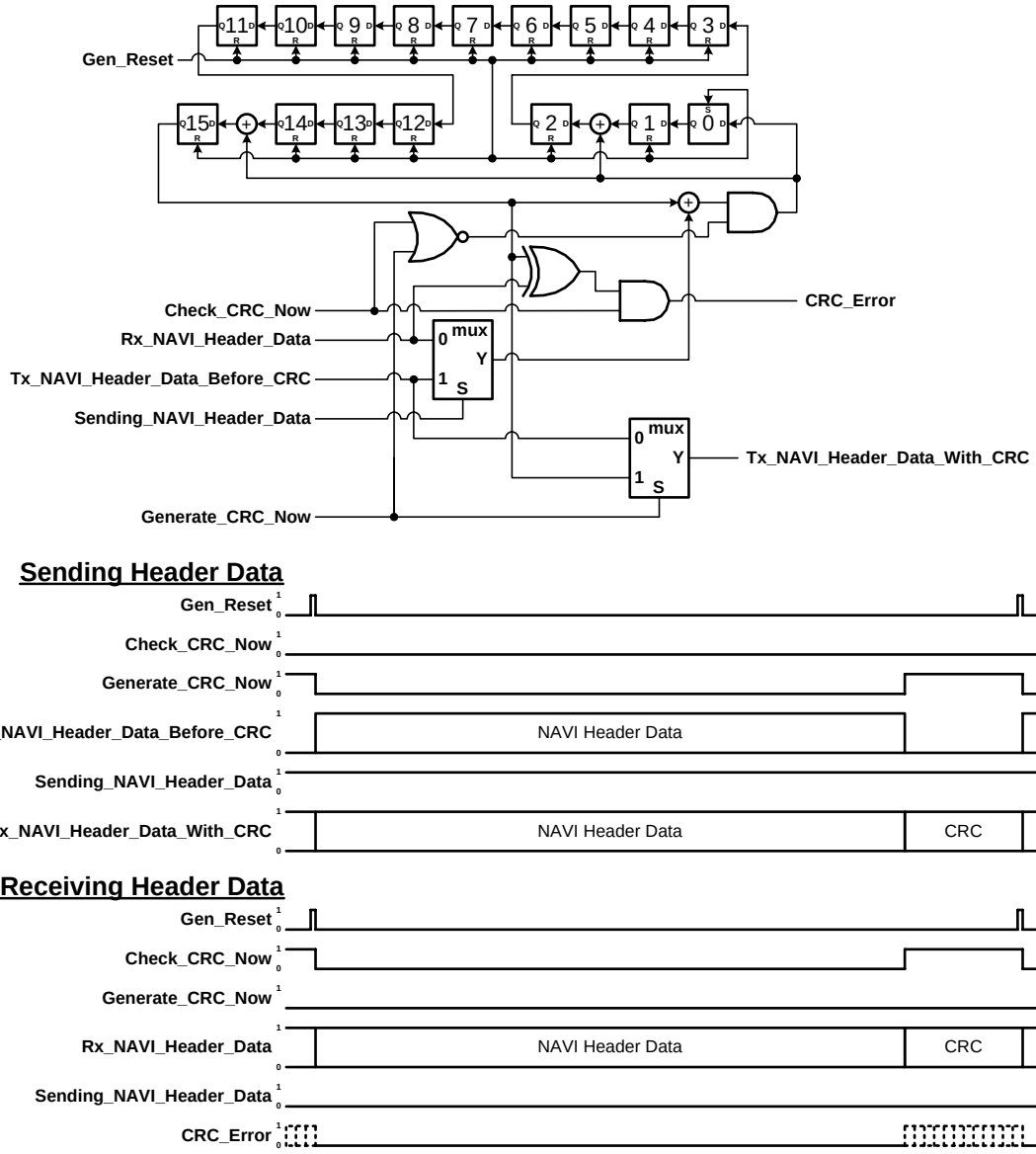


Figure 2-5 – Details of CRC generation

2.6.5.3 Transmission Data Format

Unless otherwise specified for a particular header or content type in this section, all data transmitted using the Type 1 mode is transmitted in order from least significant bit to most significant bit, and least significant byte to most significant byte.

2.6.6 Standard Secondary Header Codes

The following secondary header codes, in the series 00-0Fh, cover most of the normal transmissions over the type 1 data channel. Details of the transmission and/or the required actions on the part of the receiving device are given in sections 2.6.5.1 through 2.6.5.16.

Code	Description		Code	Description
00h	Channel Reset		08h	Continuation of current transmission
01h	VESA MCCS command or reply		09h	Resend of last block
02h	Manufacturer's prop. command/data		0Ah	End of current transmission
03h	Text string		0Bh	Current transmission aborted.
04h	Monochrome image		0Ch	Error – data type not supported
05h	Reserved		0Dh	Error – abort and reset
06h	Reserved		0Eh	Error – resend previous block
07h	Clear message		0Fh	Acknowledge

2.6.6.1 – 00h – Channel Reset

All transmissions currently in progress are aborted; the contents of any transmission received to this point should be ignored by the receiving device, and no action taken based on that command or data.

2.6.6.2 – 01h – VESA MCCS Command/Reply

The contents of this transmission constitute either a command from the VESA Monitor Control Command Set standard, or a required response to such a command issued on the previous frame. The length and format of the data transmitted is per the VESA MCCS standard.

2.6.6.3 – 02h – Manufacturer's proprietary command or data

The format for this transmission is as determined by the manufacturers of the product(s). Note that this mode may not be used until and unless both the receiving and transmitting device have determined that the proprietary system in question is supported by both. Receipt of an "unexpected" transmission using the 02h header should result in a Data Type Not Supported (0Ch) error.

2.6.6.4 – 03h – Text string

This header should be immediately followed by one byte giving the length of the string in characters (1-255), then the text string itself sent as one byte per character using ISO-8859-1 ("ISO Latin 1") standard encoding. Note that text string transmissions may span more than one block, in which case the "Continuation" and "End" headers (08h and 0Ah, respectively) shall be used in the subsequent blocks until completion of the transmission. Received text messages must be displayed by the receiving device, using whatever means are provided (e.g., OSD, separate text display device, etc.) until such time as the Clear Message (07h) command is received. If text display is not supported by the receiving device, a Data Type Not Supported (0Ch) error should be transmitted in response, and the remainder of the text transmission ignored until/unless aborted.

The receiving device should respond to this transmission with an Acknowledge (08h) on the next available transmission window, if no error condition has occurred.

2.6.6.5 – 04h – Monochrome image

The 04h header identifies the transmission of a simple monochrome bitmap graphics image, which is upon completion of the transmission to be displayed by the receiving device (using whatever display method has been established for that device – e.g., OSD, a separate display, etc.) until such time as the Clear Message (07h) command is received. The format of this transmission is as follows:

> First byte – header (04h)
> Second byte – horizontal size of image, pixels (1-255)
> Third byte – vertical size of image, pixels (1-255)
> Subsequent bits – image data, where a value of "1" corresponds to an "on" pixel and "0" corresponds to an "off" pixel, in sequence from left to right and top to bottom through the desired image space as defined by the previous two bytes.
>
> Images may require more than one transmission window, and so subsequent transmissions must begin with either the Continuation (08h) or End (0Ah) headers. Unused bits in the last transmission window should be set to zero.

The receiving device should respond to this transmission with an Acknowledge (0Fh) on the next available transmission window if no error condition has occurred.

2.6.6.6 – 05h, 06h – Reserved

The 05h and 06h secondary header codes are currently reserved for possible future use in identifying additional data transmission types. They should not at this time be used; receipt of a transmission using these secondary header codes should result in an Error – Data Type Not Supported (0Ch) response from the receiving device.

2.6.6.7 – 07h – Clear Message

Upon receipt of a transmission using the 07h secondary header, the receiving device should immediately clear the last message (text or image) from its display and issue an Acknowledge (0Fh) response on the next available transmission window. If received with no current message displayed, or unexpectedly (as in the middle of a message transmission), the receiving device should issue an Error – Abort and Reset (0Dh) response.

The receiving device should respond to this transmission with an Acknowledge (0Fh) on the next available transmission window if no error condition has occurred.

2.6.6.8 – 08h – Continuation of Current Transmission

The 08h code is used only by the sending device (in the context of the current transmission) to identify a block sent in the current window which is a continuation of a transmission (e.g., a data stream) begun in an earlier window, but which will not be completed in the current window (i.e., at least one more block beyond the current one will be required in order to complete the transmission). Such a transmission should only follow the initiation of a data transmission spanning multiple blocks (e.g., the previous block would have used the 03h or 04h secondary header codes), and should only be followed by either another block using a Continuation header code, or by a block identified as the final block via an End of Current Transmission (0Ah) block. If any other condition occurs, the receiving device shall issue either an Error – Resend Previous Block (0Eh) response (in the case of a CRC error for this block), or, if some other error occurs, an Error – Abort and Reset (0Dh) response. Note that continuations must follow the initiation of the transmission, on immediately successive frames, until the entire transmission is completed (i.e., no other Type 1 communications may be initiated until completion of the current transmission). Failure to

follow this requirement shall result in the receiving device issuing a 0Dh (Abort and Reset) code, and the entire transmission will be abandoned.

The receiving device should respond to this transmission with an Acknowledge (0Fh) on the next available transmission window if no error condition has occurred.

2.6.6.9 – 09h – Resend of Last Block

The 09h code is used only by the sending device (in the context of the current block within a multi-block transmission) to identify a transmission which is a resend of the last block sent by the transmitting device. This might occur, for example, in the response to an Error – Resend Previous Block (0Eh) having been issued by the receiving device upon CRC failure on the original transmission of the block. The receiving device will respond as it would have to the original transmission, or in the event of continued problems in receiving this block, issue an Error – Abort and Reset (0Dh) response. Note that a resend may, however, be initiated by the sending device without a previous error condition having been reported by the receiver. In that case, the receiver should ignore the previous block and instead use the new information.

2.6.6.10 – 0Ah – End of Current Transmission

The 0Ah code is used only by the transmitting device (in the context of the current transmission) to identify a block which is the end of a transmission initiated in an earlier window; therefore, it must follow either a block which was identified as the start of a multiple-block transmission, or a block identified as a Continuation (08h secondary header). If this code is received in any other situation, the receiving device should issue an Error – Abort and Reset (0Dh) response. If the transmission is completed without error, the receiving device should issue an Acknowledge (0Fh) on its next available transmission window.

2.6.6.11 – 0Bh – Current Transmission Aborted

The 0Bh code is used by the receiving device (in the context of the current transmission) to acknowledge receipt of a Channel Reset (00h), or the occurrence of any other condition which has resulted in the current transmission being aborted or rendered unusable. It is not itself acknowledged by the transmitting device.

2.6.6.12 – 0Ch – Error; Data Type Not Supported

The 0Ch code is issued only by the receiving device (in the context of the current transmission) to indicate that an error has occurred; specifically, that the receiving device does not support use of the data type identified in the current transmission. The transmitting device must abort the current transmission and issue a Clear Channel (00h) to acknowledge this.

2.6.6.13 – 0Dh – Error; Abort and Reset

The 0Dh code is issued only by the receiving device (in the context of the current transmission) to indicate that an error has occurred; specifically, that the receiving device has encountered a fault which makes it impossible to complete the current transmission or to use the data transmitted. This code shall also be issued if more than three attempts to send a given block have been made without success. The transmitting device must abort the current transmission and issue a Clear Channel (00h) to acknowledge this.

2.6.6.14 – 0Eh – Error; Resend Previous Block

The 0Eh code is issued only by the receiving device (in the context of the current transmission) to indicate that an error has occurred which renders the most recent block transmitted unusable (e.g., a checksum

error on that block). The transmitting device may respond either by retransmitting the previous block (using the Resend of Last Block secondary header, 09H), or by aborting the transmission (by issuing a Clear Channel, 00h).

2.6.6.15 – 0Fh – Acknowledge

The 0Fh code is issued only by the receiving device (in the context of the current transmission) to acknowledge the receipt of a block or command without error.

2.6.7 Type 2 Channel Control Secondary Header Codes

Since the Type 2 data channel (see section 2.7) is unidirectional (host-to-display) only, the Type 1 channel must be used to control the transmission of information over it. For this purpose, the following set of secondary header codes in the range 30-3Fh have been defined. Note that, unless otherwise noted for a specific code, these secondary headers act as self-contained commands and responses, and so no data follows them in the current transmission window (i.e., for the remainder of the available transmission window, the channel will be in the idle state).

Code	Description		Code	Description
30h	Request to initiate Type 2 trans.		38h	Reserved - do not use
31h	Type 2 data identifier		39h	Resend of last frame
32h	Type 2 abort		3Ah	Acknowledge of Resend
33h	Reserved - do not use		3Bh	Error – Type 2 not supported
34h	Reserved - do not use		3Ch	Error – data type not supported
35h	Reserved - do not use		3Dh	Error – abort and reset
36h	Reserved - do not use		3Eh	Error – resend previous frame
37h	End of Type 2 transmission		3Fh	Acknowledge

2.6.7.1 – 30h – Request to Initiate Type 2

The 30h code is issued only by the host system, and signals that the host wishes to initiate Type 2 data communications. The display or other receiving device should respond with an Acknowledge (3Fh) or the appropriate error code; if (and only if) an Acknowledge (3Fh) is received, the host may initiate Type 2 transmission immediately (i.e., at the start of the next frame following receipt of the Acknowledge response).

2.6.7.2 – 31h – Type 2 Data Identifier

The 31h secondary header is used to identify the type of data being carried on the Type 2 channel, beginning with the next frame following receipt of the Acknowledge response (3Fh) to this header. On the frame immediately following receipt of the Acknowledge, the host may initiate transmission of the data type specified, and transmission of that data type will proceed until either the host changes to transmission of a different type (preceded by the issuance of a new Type 2 Data Identifier and receipt of the response to that identifier) or ends Type 2 transmission (see 2.6.6.4, below), or the display reports an error condition.

Data identifier codes will be carried in the byte immediately following the 31h secondary header. The data ID codes currently defined for Type 2 transmission include the following

ID code block	Data type		ID code block	Data type
00h - 0Fh	Text		80h - 8Fh	Reserved; do not use

10h - 1Fh	Text		90h - 9Fh	Reserved; do not use
20h - 2Fh	Audio data		A0h - AFh	Reserved; do not use
30h - 3Fh	Audio data		B0h - BFh	Reserved; do not use
40h - 4Fh	Still image data		C0h - CFh	Reserved; do not use
50h - 5Fh	Still image data		D0h - DFh	Reserved; do not use
60h - 6Fh	Supplemental video		E0h - EFh	Reserved; do not use
70h - 7Fh	Supplemental video		F0h - FFh	Proprietary encodings

Within each set of data type ID codes, the data type is further identified per the following table. Codes not explicitly defined here, except for the proprietary encoding block (E0h - FFh) are not to be used:

ID	Text (00h - 0Fh)	Audio (20h - 2Fh)[1]	Image (40h - 4Fh)	Video (60h - 6Fh)
0	ASCII text string	.WAV file	.GIF file	.WMV file
1		.MP3 file	.JPG/.JPEG file	.MPG file
2		.WMA file	.TIFF file	.AVI file
3		.AIF/.AIFF file	.BMP file	.MOV file
4		.RA file	.PNG file	.RM/.RAM file
5		.QT file		.QT file
6		.AU file		
7		Proprietary format		
8		32 kHz, 16 bits/sample		
9		44.1 kHz, 16 bits/smp		
A		48 kHz, 16 bits/smp		
B		96 kHz, 16 bits/smp.		
C		44.1 kHz, 24 bits/smp		
D		48 kHz, 24 bits/smp.		
E		96 kHz, 24 bits/smp		
F		8 kHz, 8 bits mono		

Notes:

1 - Audio codes 29-2Eh describe stereo formats per the appropriate industry standard.

2 - The additional sixteen codes in each block (e.g., 30-3Fh for audio) are at this time reserved and not to be used.

2.6.7.3 – 32h – Type 2 abort

The 32h code is issued only by the host system, and shall be used when the host recognizes a fault condition which prevents Type 2 communication from proceeding. When issued, Type 2 communications will cease immediately (as of the frame following the transmission window in which this code is issued), and the receiving device (display) should cease usage of the Type 2 data. The receiver may issue an Acknowledge (3Fh) to signify receipt of the abort code, but the host will abort transmission with or without receipt of the Acknowledge code.

2.6.7.4 – 33h through 36h, 38h – Reserved Type 2 Header Codes

As of this writing, codes 33h through 36h, and 38h, are reserved for future use in Type 2 data communication control, and shall not be issued by either host or display. Receipt of a code in this code is an error condition, and should result in the device recognizing the error issuing the appropriate error or abort code.

2.6.7.5 – 37h – End Type 2 Transmission

The 37h code is issued only by the host, and indicates the normal termination of the Type 2 data stream occurring in the frame immediately following. The receiving device should issue an Acknowledge (3Fh) or the appropriate error code (such as a Request to Resend, 3Eh) upon receipt of this code, and should expect that the following frame will constitute the end of the current transmission. Re-starting Type 2 communication following transmission of this code and the receipt of the corresponding Acknowledge requires transmission of a new Request to Initiate (30h).

2.6.7.6 – 39h – Resend of Last Frame

The 39h code is issued only by the host, and is used to indicate that the frame immediately following will be a retransmission of the previous frame, triggered either by a request for a resend sent by the receiver, or due to an error being detected by the host. The receiver should respond with an Acknowledge of Resend (3Ah) during the inbound window immediately following the transmission of the frame (i.e., during the VSYNC period *following* the period in which the Resend code is issued). If this does not occur, and another Request to Resend is not received instead, the host should abort Type 2 transmission.

2.6.7.7 – 3Ah – Acknowledge of Resend

The 3Ah code is issued only by the display or other receiving device, and is used to acknowledge receipt of a retransmitted frame (see 2.6.6.6 above). Upon receipt of this acknowledgement, the host may resume normal Type 2 transmission, continuing with the next frame of new data.

2.6.7.8 – 3Bh – Error; Type 2 Not Supported

The 3Bh code is issued only by the display or other receiving device, and is sent if the host system attempts to initiate Type 2 communications with a receiver which does not support this mode. Upon receipt of this error code, the host must immediately cease the attempt to initiate Type 2 communications, without transmission of any further Type 2 data or secondary header codes.

2.6.7.9 – 3Ch – Error; Data Type Not Supported

The 3Ch code is issued only by the display or other receiving device, and is sent if the host system attempts to initiate a Type 2 transmission of a data type not supported by the received. Upon receipt of this error code, the host must immediately cease transmission of this data type. Resumption of Type 2 transmission with a different data type requires transmission of a new Request to Initiate (30h).

2.6.7.10 – 3Dh – Error; Abort & Reset

The 3Dh code is issued only by the display or other receiving device, and is sent if the receiver detects any error condition which prevents continuation of the current transmission. Upon receipt of this code, the host shall immediately cease Type 2 transmission, and should not expect further acknowledgement of such transmissions from the receiver. Resumption of Type 2 transmission will require transmission of a new Request of Initiate (30h).

2.6.7.11 – 3Eh – Error; Request to Resend Previous Frame

The 3Eh code is issued only by the display or other receiving device, and is sent if the receiver detects, through a checksum error or any other means, an error which renders the most recently-transmitted frame of Type 2 data unusable. The receiver will ignore that frame of data, and any subsequent frames until the host re-transmits the erroneous frame using a Resend of Last Frame (39h) secondary header code.

2.6.7.12 – 3Fh – Acknowledge

The 3Fh code is issued only by the display or other receiving device, and is used to acknowledge the receipt of certain Type 2 secondary header codes as required above. Note that the receiver does *not* send an Acknowledge code upon correctly receiving each individual frame of data in the Type 2 transmission; the host is to assume that Type 2 communications is proceeding normally until and unless an error code is received. This leaves the Type 1 channel free during the majority of Type 2 communications so that it may be used for other purposes.

2.6.8 Content Protection Control Secondary Header Codes

At this time, the NAVI standard does not include specifications for content protection in either the analog or digital transmission modes. However, it is anticipated that such specifications will be added in a later release of the standard. For this reason, secondary header codes in the range C0h to CFh are reserved for the control of the content protection system, and may not be used for any other purpose.

2.6.9 Mode D Control Secondary Header Codes

Code	Description		Code	Description
70h	Initiating Mode D(3) transmission		78h	Mode D acknowledge
71h	Resend of Last Frame		79h	Error – Mode D Not Supported
72h	Initiating Mode D(4) transmission		7Ah	Error – Mode D(4) Not Supported
73h	Ending Mode D transmission		7Bh	Error – checksum error last frame
74h	Initiating DPVL transmission		7Ch	Error – DPVL not supported
75h	Ending DPVL transmission		7Dh	Error – CP not supported
76h	Initiating CP transmission		7Eh	End Mode D CP operation ack.
77h	Ending CP transmission		7Fh	Mode D End acknowledge

2.6.9.1 – 70h – Initiating Mode D(3) Transmission

The 70h secondary header code is sent only by the transmitting device, and is used to indicate a frame in which Mode D(3) (digital transmission at three bits per symbol) operation begins. All subsequent frames are also to be assumed to be sent via Mode D(3) unless some other explicit indication is given. Note that this code may be used immediately following a Mode D(4) frame without any preceding indication that Mode D(4) is ending, in the case of the transmitting device continuing digital transmission but changing the number of bits per symbol.

The receiving device should respond to this code with a Mode D Acknowledge (78h) on the next available transmission window if no error condition has occurred.

2.6.9.2 – 71h – Resend of Last Frame

The 71h code is sent only by the transmitting device, and is used to indicate the retransmission of the frame of data which was originally sent immediately prior to the frame in which a Mode D Checksum Error (7Bh) code was received from the display. See section 2.6.8.12.

2.6.9.3 – 72h – Initiating Mode D(4) Transmission

The 72h secondary header code is sent only by the transmitting device, and is used to indicate a frame in which Mode D(4) (digital transmission at four bits per symbol) operation begins. All subsequent frames are also to be assumed to be sent via Mode D(4) unless some other explicit indication is given. Note that this code may be used immediately following a Mode D(3) frame without any preceding indication that Mode D(3) is ending, in the case of the transmitting device continuing digital transmission but changing the number of bits per symbol.

The receiving device should respond to this code with a Mode D Acknowledge (78h) on the next available transmission window if no error condition has occurred.

2.6.9.4 – 73h – Ending Mode D Transmission

The 73h code is sent only by the transmitting device, and is used to indicate that Mode D operation will be terminated effective with the frame immediately following. If no other mode is initiated on subsequent frames, the next frame and all subsequent frames should be assumed to use the conventional analog mode.

The receiving device should respond to this code with a Mode D End Acknowledge (7Fh) to indicate that it has switched back to conventional analog operation.

2.6.9.5 – 74h – Initiating DPVL Transmission

The 74h secondary header code is sent only by the transmitting device, and is used to indicate a frame in which transmission using the VESA Digital Packet Video Link (DPVL) protocol begins. All subsequent frames are assumed to be DPVL unless some other explicit indication is given. Note that this code may be used immediately following a standard Mode D(3) or Mode D(4) frame without any preceding indication that Mode D(3) or D(4) is ending. Transmission of the DPVL content will proceed using the Mode D mode (three or four bits per symbol) previously established; i.e., Mode D(3) or Mode D(4) operation must be initiated, using the appropriate code, prior to initiating DPVL operation, so that the receiving device will be set to receive the correct encoding.

The receiving device should respond to this code with a Mode D Acknowledge (78h) on the next available transmission window if no error condition has occurred.

2.6.9.6 – 75h – Ending DPVL Transmission

The 75h code is sent only by the transmitting device, and is used to indicate that DPVL operation will be terminated effective with the frame immediately following. If no other mode is initiated on subsequent frames, the next frame and all subsequent frames should be assumed to use the standard digital mode that was in use prior to the initiation of DPVL operation.

The receiving device should respond to this code with an Mode D End Acknowledge (7Fh) to indicate that it has switched back to its previous mode of operation.

2.6.9.7 – 76h – Initiating Content Protected Transmission

The 76h secondary header code is sent only by the transmitting device, and is used to indicate a frame in which a content-protected transmission begins. All subsequent frames are also to be assumed to be sent using the appropriate content protection system unless some other explicit indication is given. Note that this code may be used only after Mode D(3) or Mode D(4) operation has been established, and, if required, DPVL operation, using the appropriate codes.

The receiving device should respond to this code with a Mode D Acknowledge (78h) on the next available transmission window if no error condition has occurred.

2.6.9.8 – 77h – Ending Content Protected Transmission

The 77h code is sent only by the transmitting device, and is used to indicate that the transmission of content-protected material will be terminated effective with the frame immediately following. If no other mode is initiated on subsequent frames, the next frame and all subsequent frames should be assumed to use the standard digital mode that was in use prior to the initiation of content-protected operation.

The receiving device should respond to this code with an Mode D End Acknowledge (7Fh) to indicate that it has switched back to its previous mode of operation.

2.6.9.9 – 78h – Mode D Acknowledge

The 78h code is sent only by the receiving device (e.g., display), and is used to indicate the receipt of any Mode D control code from the host that did not result in an error condition. The host should, upon receipt of this acknowledgement, assume that the Mode D transmission may proceed normally.

2.6.9.10 – 79h – Error – Mode D Not Supported

The 79h code is sent only by the receiving device (e.g., display), and is used to indicate an error condition in which the transmitting device has attempted to initiate a Mode D transmission, but Mode D is not supported by the receiving device. The host shall, upon receipt of this error code, immediately cease Mode D transmission and proceed with the standard analog mode only.

2.6.9.11 – 7Ah – Error – Mode D(4) Not Supported

The 7Ah code is sent only by the receiving device (e.g., display), and is used to indicate an error condition in which the transmitting device has attempted to initiate a Mode D(4) transmission, but Mode D(4) is not supported by the receiving device. The host shall, upon receipt of this error code, immediately cease Mode D(4) transmission but may attempt to initiate Mode D(3) operation if this was not previously established. If Mode D(3) was previously in use, the host device should return to that mode of operation.

2.6.9.12 – 7Bh – Error – Checksum Error Last Frame

The 7Bh code is sent only by the receiving device (e.g., display), and is used to indicate an error condition in which a checksum error has been detected in the video data sent on the previous frame via Mode D. The host shall, upon receipt of this error code, either re-send the frame in question (identified using the 72h code), proceed with the transmission (in which no explicit response will be sent to the display, which then must simply continue to accept new data), or switch to a different mode of operation. It is expected that the transmitting device will track the error rate reported by the display or other receiving device, and use this information to trigger changing to a more robust mode of transmission (i.e., switching from Mode D(4) to Mode D(3), or switching to the standard analog transmission method) when appropriate. See Section 3 (Digital Video Transmission – NAVI Mode D) for further information.

2.6.9.13 – 7Ch – Error- DPVL Not Supported

The 7Ch code is sent only by the receiving device (e.g., display), and is used to indicate an error condition in which the transmitting device has attempted to initiate a DPVL transmission, but DPVL operation is not supported by the receiving device. The host shall, upon receipt of this error code, immediately cease DPVL transmission and resume operation using the standard Mode D(3) or Mode D(4) previously established.

2.6.9.14 – 7Dh – Error – Content Protection Not Supported

The 7Dh code is sent only by the receiving device (e.g., display), and is used to indicate an error condition in which the transmitting device has attempted to use content-protected Mode D transmission, but Mode D content protection is not supported by the receiving device. The host shall, upon receipt of this error code, immediately cease transmission of the content-protected material; transmission of non-CP material may continue using the transmission mode (Mode D(3) or Mode D(4), with or without DPVL operation) previously established.

2.6.9.15 – 7Eh – End Mode D Content Protection Acknowledge

The 7Eh code is sent only by the receiving device (e.g., display), and is used to indicate acknowledgement of the end of content-protected transmissions; the receiving device may from this point on be assumed to be operating using the transmission method and encoding established prior to the start of Mode D content-protected transmission.

2.6.9.16 – 7Fh – End Mode D Acknowledge

The 7Fh code is sent only by the receiving device (e.g., display), and is used to indicate acknowledgement of the end of the Mode D method and encoding which had been indicated by the host; the receiving device may from this point on be assumed to be operating using the transmission method and encoding established prior to the start of this mode of operation. If the host had indicated the cessation of digital operation altogether, via a 73h code, the receiving device may now be assumed to be operating in the conventional NAVI analog mode.

2.6.10 Display-to-Host Serial Data Timing

In order to qualify as compatible for Type 1 data transmission under this standard, the display must be capable of internally producing a 1/8 pixel-clock-rate signal, for the purposes of clocking its serial data transmissions, of sufficient stability such that the frequency does not drift by more than ±5%, relative to the host-provided reference clock signal, should that reference be unavailable for up to 10 horizontal periods. This is to ensure that the display's serial data, transmitted during the VSYNC period when the host-generated clock is not provided, will remain recoverable by the host.

2.7 Serial Data Transmission, Type 2

A second form of data transmission is permitted under the NAVI system; this is an "outbound" (host-to-display) only channel of significantly higher capacity than the Type 1 transmissions described in the previous section. The Type 2 transmission again relies on the combined HSYNC/sample clock reference signal as a carrier, and so will only be available to those displays which enable this via the /CLK_ENABLE signal. It is again important to note that support for these systems is optional; however, Type 1 support is required if Type 2 is to be supported, as the Type 1 channel is used to control the Type 2 transmissions.

The Type 2 serial data transmission transmits one bit per sample clock reference period, via modulation of the inactive or "falling" edge of this clock. All clock periods outside of the VSYNC period (which is reserved for the Type 1 communications) are available for the Type 2 transmission, which may thus be treated by the display as essentially a continuous serial bit stream. The capacity of the Type 2 channel is at least 2 Mbps for all timings expected to be used with the NAVI system (assuming the standard 640 x 480, 60 Hz timing as the minimum case), making it suitable for digital audio and other relatively high-bandwidth applications.

The final line of each frame (i.e., the line immediately preceding the VSYNC period) is reserved for transmission of a checksum; see 2.7.2 below.

Capacity Analysis

As noted above, assuming one bit transmitted per sample clock reference period, the capacity of the Type 2 transmission is easily derived from the video timing itself; it is the number of pixel clocks per second, minus the overhead of the VSYNC period (reserved for the Type 1 transmissions) and the HSYNC pulses (during which nothing is transmitted on the HSYNC/sample clock reference line). The 640 x 480, 60 Hz standard timing is again assumed to be the minimum-rate case:

525 lines/frame – 3 lines (VSYNC) – 1 line (checksum) = 521 lines/frame available for Type 2 data.

at 704 pixels/line (800 pixels – 96 pixel HSYNC time), we have 88 bits/line transmitted,
or

521 x 88 = 45,848 bits/frame

And at 60 frames/second, we have

45,848 x 60 = 2.75 Mbits/second

2.7.1 Type 2 Serial Data Transmission

The host may, at any time, transmit data via the HSYNC/sample clock reference signal via the modulation of the inactive or falling edge of the sample clock reference, as shown in fig. 2-6. However, it should be noted that the host must not rely on this data being received and interpreted by the display unless acknowledgement of Type 2 support is received via the proper exchange of Type 1 control codes; see section 2.6.6. Type 1 communications and the transmission of the proper Type 2 initiation codes, data descriptors, etc., must be completed prior to the initiation of Type 2 transmissions.

Note that, as was the case for Type 1 transmissions, all information transmitted using the Type 2 channel is to be transmitted least-significant-bit first, unless otherwise specified for the particular type of information to be carried.

The smallest block of Type 2 data is that transmitted during a given horizontal line time of the current video timing; this is, therefore, referred to as a "line" of data. Most Type 2 control is, however, performed on the basis of complete "frames" of data, i.e., all data transmitted between the end of a given VSYNC period and the start of the next.

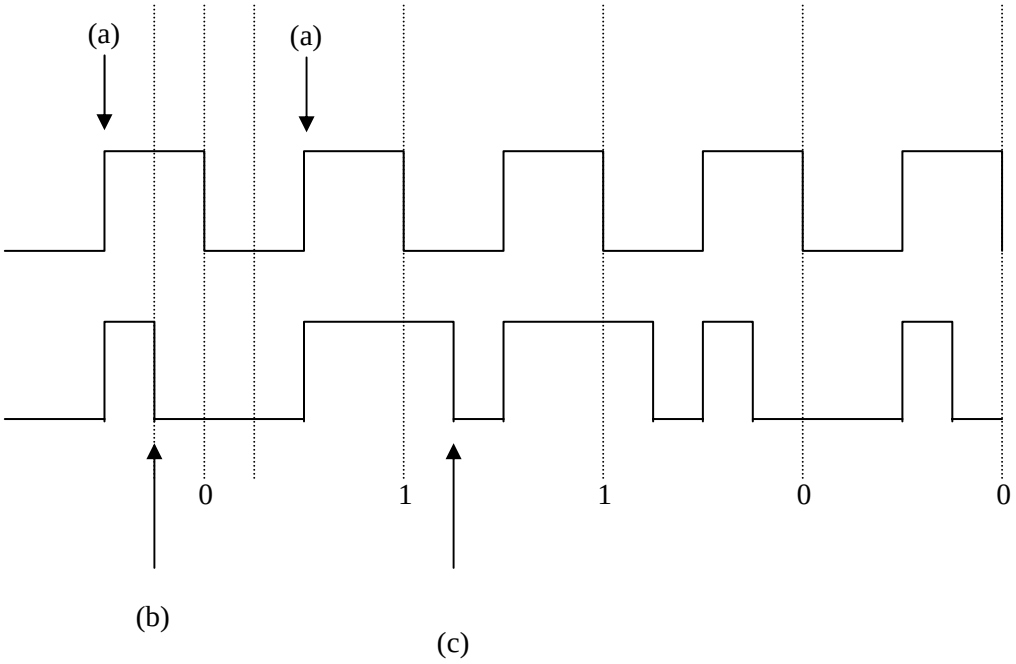


Fig. 2-6 – Type 2 Serial Data Transmission

The top signal is the unmodified sample clock reference signal; the falling edge of this signal (or equivalently, the rising edge of an inverted version of this same signal) defines the points at which the display should sample this signal to recover the serial data stream.

The lower signal is this same clock, showing the Type 2 data transmission via modulation of the falling edge. A "0" is transmitted by advancing the falling edge such that it occurs ¼ of the period (a-a) earlier than normal; similarly, a "1" is transmitted by delaying this edge by ¼ of the period.

Item	Requirement

(a)	Reference clock signal rising edge. (a) to (a) represents one nominal period for this clock.
(b)	Falling edge advanced for "0" transmission. When transmitting a "0", this edge must occur not earlier than 20% of the period after the preceding rising edge, and not later than 30% of the period after the preceding rising edge.
(c)	Falling edge delayed for "1" transmission. When transmitting a "1", this edge must occur not earlier than 30% of the period before the next rising edge, and not later than 20% of the period before the next rising edge.

Note that all other requirements for this signal (see section 2.3) remain in effect during the Type 2 data transmission.

2.7.2 Type 2 CRC (Cyclic Redundancy Check)

The final line of each frame (i.e., the line of data immediately preceding the start of the next VSYNC period) must consist of a sixteen-bit CRC, obtained via the method described below as applied over all information transmitted during over the previous lines of this frame. The CRC data occupies the first sixteen bits of that line, transmitted least significant bit first. The remainder of the data on that line shall be zeroes.

The polynomial used for the CRC calculation is known as the CRC-16, $X^{16} + X^{15} + X^2 + X^0$. A sample implementation of the CRC generator and checker is shown in the previous section, as fig. 2-6 The CRC register is initialized to 0x0001 just prior to the first bit of a packet, then the bytes of the packet are shifted into the register LSB first. Note that the register bit numbers in this Figure correspond to the order of the polynomial and not the actual bit numbers. It is more efficient to shift the CRC register in a single direction, and this results in having CRC bit 15 appear in bit position 0 of the CRC field, and CRC register bit 14 in CRC field bit 1, and so on.

The following is an example of a CRC calculation. The packet contents are: 0x0007, 0x46, 0x000400, 0x00 (or represented as a sequence of bytes this is 0x07, 0x00, 0x46, 0x00, 0x04, 0x00, 0x00) and the resulting CRC is 0x0ea1 (or represented as a sequence of bytes is 0xa1, 0x0e).

When configured as a CRC checker the CRC that is received is compared bit by bit with the value in the CRC register. If there are any errors the CRC counter will be incremented once for every packet that contains a CRC error. Note that the example diagram shown in fig. 2-5 can output more than one CRC error signal within a CHECK_CRC_NOW window. Therefore, the CRC error counter must only count the first CRC error instance within each interval where CHECK_CRC_NOW is active.

If configured as a CRC generator, the CRC is clocked out of the CRC register at the end of the packet.

3. Digital Video Transmission (NAVI Mode D)

In addition to the VGA-compatible video transmission modes described in the previous section of this document, the NAVI system also supports a true digital transmission mode referred to as Mode D. This mode uses the same basic electrical and physical interface as the analog modes, but permits transmission of video information in digital form at up to approx. 5 Gbit/sec, depending on the limitations of the particular implementation in question. (Note: support for high rate Mode D operation may require cabling and connectors certified for such use; please see section 7 of this specification for details.)

Support of Mode D operation is mandatory in all NAVI-compliant host systems, but not all hosts may support this mode up to the maximum data capacity described here; see section 3.1.4. Support of Mode D operation in NAVI-connected displays is optional. Note that Mode D is supported on all physical implementations of NAVI described by this specification, including NAVI as used on the standard "VGA" connector ("NAVI-V").

3.1 Basic NAVI Mode D Operation

NAVI Mode D uses either eight-level or sixteen-level amplitude encoding to transmit three or four bits per symbol, with one symbol transmitted per cycle of what in the analog mode would be considered the "pixel clock" (i.e., a clock operating at eight times the rate of the NAVI clock reference signal carried by the HSYNC physical channel, see section 2.3). In the case of this encoding being used to carry "straight" RGB information (i.e., no packetization or compression; the digital transmission is the equivalent of that which would be carried by the analog RGB signals), each pair of symbols is considered to be the digital value for one pixel in the color assigned to that physical channel. The first symbol of each pair carries the odd-numbered bits (i.e., bits 5,3, and 1 when transmitting six bits per color per pixel in the three bit per symbol mode, and bits 7,5,3, and 1 when transmitting in the four bits/symbol or eight bits per color per pixel mode), while the second symbol carries the even bits. This separation of the bits of six- or eight-bit data into even and odd-bit symbols is done in order to preserve the greater noise immunity of the most significant bits of each pixel's information; were the bits simply divided between the two symbols (i.e., bits 7-4 in the first symbol and bits 3-0 in the second, in an eight-bit-per-pixel mode), note that bit 4 would wind up being more likely to be corrupted by noise than bits 3-1. See figure 3-1 for a pictorial representation of the basic NAVI Mode D transmission.

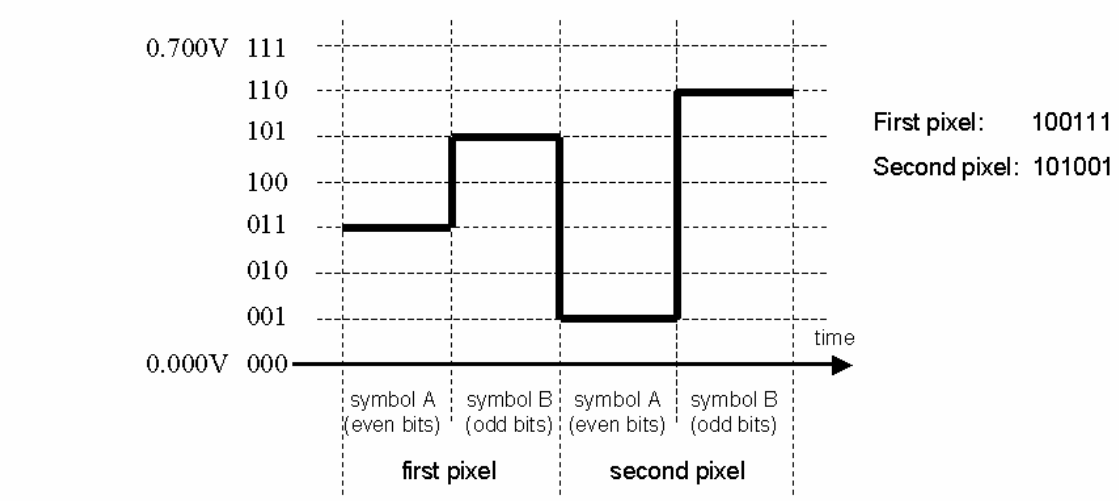


Fig. 3-1 – Basic Mode D operation (in this example, at three bits per symbol, or six bits/color/pixel

3.1.1 Mode D Encoding

NAVI mode D operates with eight- or sixteen-level amplitude encoding of three or four bits per symbol (i.e., per clock), respectively; these levels are evenly spaced across the standard 0.000 to 0.700 analog video signal amplitude range. These are also identified as “Mode D(3)” and “Mode D(4)”, respectively. The default mode of operation is three bits per symbol (AKA “six bits per color”) mode. The first symbol transmitted during each active video time shall provide the odd-numbered bits of the six-bit or eight-bit value (bits 5, 3, and 1 or bits 7, 5, 3, and1), the second symbol shall provide the even-numbered bits (bits 4, 2, and 0 or bits 6, 4, 2, and 0). All NAVI-compatible sources must be capable of operating in either the three bit per symbol or four bit per symbol format. Displays may operate solely in the three-bit (Mode D(3)) format; a display which supports Mode D(4), however, must also be capable of operating in Mode D(3).

It is assumed that NAVI Mode D will use the same output drivers as used in the analog video modes. As these will typically be digital-to-analog converters of greater than three- or four-bit resolution, a mapping of the three- or four-bit inputs codes into the appropriate D/A input values will generally be required. For an eight-bit D/A converter, the appropriate inputs for each mode would be as follows:

Three-bit code to transmit	Nominal Mode D signal level	Eight-bit D/A input (binary)	Eight-bit D/A input (decimal)
000	0.000V	0000 0000	0
001	0.100V	0010 0100	37
010	0.200V	0100 1001	73
011	0.300V	0110 1101	109
100	0.400V	1000 0010	146
101	0.500V	1011 0110	182
110	0.600V	1101 1011	219
111	0.700V	1111 1111	255

Four-bit code to transmit	Nominal Mode D signal level	Eight-bit D/A input (binary)	Eight-bit D/A input (decimal)
0000	0.000V	0000 0000	0
0001	0.047V	0001 0001	17
0010	0.093V	0010 0010	34
0011	0.140V	0011 0011	51
0100	0.187V	0100 0100	68
0101	0.233V	0101 0101	85
0110	0.280V	0110 0110	102
0111	0.327V	0111 0111	119
1000	0.373V	1000 1000	136
1001	0.420V	1001 1001	153
1010	0.467V	1010 1010	170
1011	0.513V	1011 1011	187
1100	0.560V	1100 1100	204
1101	0.607V	1101 1101	221
1110	0.653V	1110 1110	238
1111	0.700V	1111 1111	255

3.1.2 Mode D Signal Requirements

As with the NAVI analog video modes, all NAVI sources when used in Mode D must remain fully compliant with the requirements of the VESA Video Signal Standard (VSIS), except as otherwise noted here.

3.1.3 Initiation and Cessation of Mode D Transmission

Mode D transmission shall not be initiated by the host system at any time unless (a) the display has been identified as Mode D capable, and (b) Mode D operation has been requested by the display or indicated (via EDID or similar means) as the preferred method of video transmission. Note that in the case of displays capable of Mode D, in addition to either the standard or enhanced analog modes supported under NAVI, switching between modes may occur via a "hot plug" event being triggered by the display, at which time the host shall re-read the EDID information in order to determine the desired mode of operation.

Mode D operation shall always default to the three bits per symbol format ("Mode D(3)"), unless the display has explicitly identified itself as capable of using the four bits/symbol format ("Mode D(4)"). If transmission cannot be maintained with an acceptable error rate using the four bits/symbol format, as determined through monitoring of the frame checksum errors reported by the display, the host must switch to the Mode D(3) format. This must occur if checksum errors occur at a rate of greater than one per every 1000 transmitted frames (or once per every 5 seconds, whichever is the lower error rate), on average, although it is permissible to set up systems such that more restrictive (lower error rate) limits are used.

Initiation of Mode D operation will be identified and acknowledged via the appropriate command/response sequence using the Type 1 data communications channel; see section 2.6.8 for details. Note that it is not required that Mode D transmissions be identified on each frame; once Mode D operation is initiated, it is assumed that transmission will continue in this mode until such time as cessation of Mode D is explicitly indicated.

3.1.4 Mode D Transmission Rate Requirements/Limits and Data Capacity

As noted earlier in this section, the data capacity of Mode D operation depends on both the specific format of the transmission (three bits or four bits per symbol) and the maximum symbol or "pixel" clock rate that can be reliably supported on a given physical interface (e.g., the "NAVI-V" (or "VGA") implementation, the "NAVI-D", etc.).

On the NAVI-V implementation (see section 5), the maximum standard rate supported under Mode D is a 200 MHz symbol clock (100 MHz pixel rate). On the NAVI-D implementation, the maximum standard rate supported is a 400 MHz symbol clock (200 MHz pixel rate). In either case, higher rates may be attempted, but must not be used if the error rate limits given in section 3.1.3 cannot be met.

At the above rates, NAVI Mode D provides maximum total data capacities as follows (per channel; i.e., 3X this rate is available, total, in an RGB or other three-channel system):

Mode	Capacity at 200 MHz symbol rate	Capacity at 400 MHz symbol rate
Mode D(3) (six bits/pixel)	600 Mbit/sec.	1200 Mbit/sec.

Mode D(4) (eight bits/pixel)	800 Mbit/sec.	1600 Mbit/sec.

3.1.5 Mode D Checksum

During Mode D operation, the host will transmit a 16-bit checksum of all data transmitted in each frame on the line (i.e., R, G, or B) in question at the end of the last line of the frame. This will be transmitted at the first sixteen symbol times following the completion of the active video portion of that line, using simple binary encoding (i.e., a "1" will be sent as the full white level, and "0" sent as black), LSB first. The display may use this information to monitor the error rate of the Mode D transmission, and to request frame re-transmission and/or a change from Mode D(4) to Mode D(3) as noted above. Note that the display should ensure that the checksum information transmitted by the host is not visible in the displayed image.

3.1.6 Digital Packet Video Link Operation with NAVI Mode D

As NAVI Mode D provides a high-speed, general-purpose digital communications channel, support of other digital protocols is possible. Specifically, it is expected that the support of packetized video as described in the VESA DPVL standard proposal will the possible using NAVI Mode D. This will permit the support of very high resolution display systems, including tiled displays, via this interface.

The details of DPVL operation under NAVI are not yet defined as of this release of the NAVI standard. However, please note that control codes for the support of DPVL operation have been defined in section 2.6.9.

4. Supplemental Interfaces and Functions

The NAVI system, in its various implementations, requires support for various additional interfaces and functions not directly associated with the video interface itself. These are described in this section. While not all of these functions are supported on all NAVI implementations, they are all mandatory on those which do support them, unless explicitly otherwise noted in a particular physical implementation description.

4.1 Display Data Channel

All implementations of NAVI require support for the VESA Enhanced Display Data Channel (E-DDC) standard as the only recognized means of display identification (via the E-EDID information transmitted over this channel). The operation and performance specifications for this channel shall be as described in the latest revision of the relevant VESA standards. Support for features beyond the basic display ID capability over E-DDC (such as display control, etc.) are optional unless otherwise mandated by the E-DDC standard itself or other relevant VESA documents.

4.2 Power

The NAVI-D implementation provides for a power connection, which may be used either to power the display from the video source, or to power/charge the source (host product) from the display or similar external device. The following specifications define the operation of this feature in all NAVI implementations.

4.2.1 Mandatory/Option Support Requirements

While support for the power function is required on all NAVI-D implementations, the specifics of this support vary depending on the connector type and the nature of the product. Some products may provide only a power output; others may support only the ability to accept power from the other device, while some may provide bi-directional power support (with “who drives who” determined based upon which device has the most robust power source at the time). The following table defines what degree of power feature support is mandatory and which are optional. (NOTE: The +5 VDC output on an NAVI-V (“VGA” connector)-equipped host device is NOT to be considered as a power output under this section, as this output is already defined by and expected to be used for the Display Data Channel (DDC) support on that connector.) In all cases, the type of power-feature support defined as “mandatory” shall be the default mode for the NAVI power function on that device. (For example, it shall be the default condition that a PDA or similar portable device equipped with an NAVI-P output will be configured to ACCEPT power via the NAVI-P connector.)

Connector Type	Type of Device	Power Output Support (the device can PROVIDE power to another via the NAVI)	Power Input Support (the device can ACCEPT power from another via the NAVI)	Default NAVI power state (source or load)
NAVI-D	Desktop PC or similar (a)	Mandatory	Not supported	Source
	Portable PC, PDA, notebook, or similar (b)	Optional	Optional	Source (b)
	Low-power fixed display (c)	Optional	Optional	Load
	Portable display (d)	Not supported	Optional	Load
	High-power fixed display (e)	Mandatory	Not supported	Source
NAVI-P	Portable PC, PDA, notebook, or similar(b)	Optional	Optional	Load (b)
	Low-power fixed display (c)	Not supported	Optional	Load
	Portable display (d)	Not supported	Optional	Load
	High-power fixed display (e)	Mandatory	Not supported	Source

Notes:

(a) The “desktop PC” category includes all NAVI-compatible video sources contained within products which, in normal operation, rely on a built-in AC power supply, and are not normally used without such a power source.

(b) The “portable PC”, etc., category includes all NAVI-compatible video sources or products which are normally used apart from an AC power source, i.e., operating from a battery or other self-contained source of electrical energy. Note that this class of devices are expected to default to PROVIDING power to the display or other “downstream” NAVI device if the host device provides an NAVI-D output, and ACCEPTING power (for the purpose of operation and/or charging the internal power source) if any other connection is used. In either case, the product may also optionally support the other mode (i.e., receiving power if NAVI-D equipped or sourcing power if otherwise equipped); see section 4.3.3, below.

(c) The “low-power fixed display” category includes all forms of display devices or other video output products which are (a) normally operated as conventional direct-view displays and (b) require 20W or less for operation. Note that this category may either source or accept power; it is expected that there will be some AC-powered desktop monitors which will provide the ability to power or charge portable PCs and similar devices if connected; there may also be other desktop displays using the NAVI system in which the NAVI connection is the display’s primary source of power.

(d) "Portable displays" includes all forms of display devices, including separable handheld or other portable screens, head-mounted or "eyeglass" displays, etc., which are not normally used in a fixed location and which do not normally have their own AC power supply or other direct connection to an external power source. Such devices are NOT expected to source power at any time, but may be powered if desired from a suitably-equipped NAVI host.

(e) The "high-power fixed display" category includes all displays devices which (a) may reasonably be expected to contain an AC power supply or otherwise have access to external power, whether or not these might also be considered "portable" devices, and/or (b) require more than 20W for operation. All conference-room projectors, plasma or other displays in excess of 24" (61 cm) diagonal screen size, including television receivers and monitors, shall be considered as being in this category. Note that such products are required to be able to output power via any NAVI connector used.

4.2.2 Power Specifications; Over-Current & Short-Circuit Protection

The following minimum/maximum limits shall apply to the NAVI-D power outputs/inputs, under the conditions noted. In all cases, it is further required that output power be limited such that not more than 5A of current shall be provided for any period of time under any conditions. In addition, all NAVI power outputs must be designed such that continuous exposure to any load condition, up to and including a "short circuit" of the output power pin(s) directly to the power return path, for an indefinite period of time, must not result in any permanent damage to the product or require replacement of any parts (i.e., it is not acceptable that this requirement be met simply by fusing the output power line). However, it is acceptable the output protection be provided via a user-resettable protective device, such as a circuit breaker, as long as the resetting of such a device may be readily accomplished by the user, without the use of tools, other than use of a probe such as may be needed to access the reset control.

Voltage: The nominal voltage of the NAVI power connection shall be 20.0 VDC. Under no conditions shall any NAVI power output provide a voltage in excess of 24.0 VDC, and all such outputs shall maintain a voltage of not less than 18.5 VDC under the maximum load conditions specified below. Should the output voltage drop below 18.5 VDC, the output should be disabled until load and/or supply conditions are such that these voltage requirements can be met.

Device	Min. available current or max. load
NAVI-D source (power output)	1.0 A min.
NAVI-D load	1.0 A max.

4.2.3 Directionality Control in Bi-Directional Systems

As noted above, there is the possibility of a system in which either the host device or the display device could have the capability of acting as the power source for the other. All devices must default to one mode or the other (source or load) as described in 3.3.1, except for the "desktop display" class which has no mandatory power-feature support required. These requirements basically equate to saying that fixed-location, AC-powered devices default to being power sources under the NAVI system, while portable, battery-operated equipment defaults to being powered or charged by the NAVI connection.

In the case where two devices which default to being "loads" are connected together, as in the case of a notebook computer being connected to a low-power or portable display device, the host (computer) controls the directionality of the NAVI power connection. Neither device should enable power output until a read of the EDID data from the display has been completed. If, from that data, the host determines that the display is capable of providing the host with power, it may enable power output from the display via the appropriate MCCS command. (See the VESA MCCS standard for details.) If, on the other hand, the host determines that it is capable of supplying power to the display, and/or power output by the host is required for the display to function (i.e., a portable display with no independent power source of its own), the host may then enable its power output.

4.3 Hot Plug Detect

A "hot plug detect" function is supported in the NAVI-D implementation. This permits the host system to detect disconnection/re-connection of the display device during normal operation (i.e., following initial system boot-up and detection of the display), and so may be used to initiate a re-read of the display ID information and a reconfiguration of the host video output. The "hot plug detect" (HPD) feature functions basically as defined in the original VESA "M1" interface standard, although it has been expanded upon slightly here.

4.3.1 Basic HPD Functionality

All NAVI-compliant displays using the NAVI-D, or other connector which provides for HPD support, must provide support for this feature by supplying a voltage of between +2.7 VDC and +5.5 VDC on this pin at any time the display is either (a) powered up in its normal operating condition or (b) receiving +5 VDC from the host, via the DDC +5V line as defined for the connector in question. Note that on the "NAVI-V" (VGA) implementation, it is permissible that the /NAVI-ENABLE signal be used to implement the "hot plug detect" functionality.

Host load limit. No NAVI-compliant host shall place a load of more than 5 mA, under any conditions, on this line. (NOTE: Under the original M1 specification, use of the HPD line as a display-provided power source was permitted under certain circumstances; this is NOT supported in the NAVI system, as both NAVI connectors provide power separately as described in section 3.3 above.)

"Hot plug" event; change of display or display state: The host will use the presence of voltage within the specified range on this line as indicating that the display is connected; should the HPD signal, once detected, be absent for a period of at least 1.0 seconds, the host shall consider this as indicating that the display has been disconnected or otherwise has changed state such that re-initialization may be required. Upon re-assertion of the HPD signal, the host shall then initiate a re-read of the E-EDID data and re-initialize the display and/or video output system. Even if not physically disconnected, the display may

cause such re-initialization to occur if needed by holding the HPD signal low (≤ 0.4 VDC at the display connector) for a period of at least one second, and then returning it to the high state. This might occur, for instance, in the case of a change of display orientation (from “landscape” to “portrait” mode or back) or a change in the video interface to be used.

Use of HPD Signal to Control Host Power Output: Under the NAVI system, the display may optionally use the HPD signal to indicate to the host that the display requires power to be supplied by the host. This is indicated by the display sending an interrupted HPD signal, within the voltage limits established above, but with a pulse rate of 2-5 Hz and an “on” time of 25-50%. This condition shall be maintained for as long as the display requires power from the host. Should power no longer be required, but the display remains connected and available for use, the HPD signal shall revert to the steady condition as described above. Should the display be disconnected or otherwise change state, the same criteria for detection of a “hot plug event” by the host (absence of a high state on this line for at least 1.0 second) shall still apply.

5. Physical Implementation I – NAVI on the VGA connector (NAVI-V)

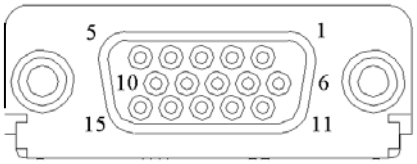
This section defines the NAVI system on the traditional 15-pin high-density D-subminiature video connector, commonly referred to as the "VGA" connector. This implementation is to be identified as the "NAVI-V" implementation. All of the analog interface features described in section 2 of this standard are supported in this implementation; however, no support for the digital video interface (section 3) or any supplemental interfaces (section 4), with the exception of the VESA DDC, is provided.

5.1 Physical Connector

The physical connector used for the NAVI-V implementation is the common "VGA" or "15HD" video connector, such as AMP p/n 787066-1, 787066-2, 787506-1; Molex p/n 89263-*7**, 89141-70**, 89046-70**; or equivalent. The connector's insert shall be colored "royal blue" (per the VESA EDDC standard), indicating E-DDC compatibility. Pin #9 is recessed 0.050" relative to the other pins. (For a detailed description of this connector, see Appendix A.)

5.2 NAVI-V Pinout

The pin assignments for this connector as used under the NAVI system shall be as described in the following table/diagram.



Pin	Signal	Pin	Signal
1	Red video	9	DDC +5 VDC
2	Green video	10	Sync return
3	Blue video	11	NAVI_ENABLE
4	(NC)	12	DDC Data (SDA)
5	DDC Return	13	Horizontal sync.
6	Red video return	14	Vertical sync.
7	Green video return	15	DDC Clock (SCL)
8	Blue video return		

6. Physical Implementation II – The NAVI-Desktop (NAVI-D) Connector

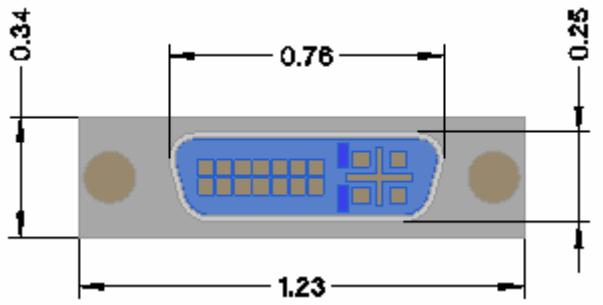
This section defines the implementation of the NAVI system on a new connector, unique to this standard. The NAVI-Desktop (or "NAVI-D") connector has been designed to provide support for this new interface system on a physically small connector, suitable for use on "desktop" PCs, notebooks, some "tablet" PCs, and similar large/medium-sized devices, while still providing all the features of the system and full analog video support. In short, NAVI-D is expected to provide the most direct replacement for the traditional "VGA" connector in most of that standard's current applications.

6.1 Physical Connector

See drawing.

6.2 Pin Assignments

Pin assignments for the NAVI-D connector are given in the following table.



	Signal		Pin	Signal
1	NAVI_ENABLE		8	V. sync return
2	Hot Plug Detect		9	Vertical sync
3	NAVI Power Return		10	NAVI Power
4	NAVI Power Return		11	NAVI Power
5	DDC Data (SDA)		12	DDC Clock (SCL)
6	DDC Return		13	DDC +5 VDC
7	RESERVED – Do not use*		14	RESERVED – Do not use*
C1	Red Video		C3	Horizontal sync/Clock reference
C2	Green Video		C4	Blue Video
C5 (crossed "ground planes" in MicroCross): Shared video return connection				

* - The pins identified here as RESERVED must be treated as "no connects" by any NAVI 1.0 compliant product, including all video signal sources (PCs, etc.), displays, and associated cabling. They must not be grounded or otherwise connected to any signal or conductor as of this version of the NAVI standard.

7. Use of the NAVI System with Alternate Color Encodings ("CE Usage")

As it is expected that the NAVI system, and especially the NAVI-D implementation (see section 6), will be attractive for "consumer electronics" (e.g., television systems) use, it is desirable to provide a standard method for supporting non-RGB video within this interface system. This section defines the assignments of the common non-RGB video signal forms to the physical and/or logical channels provided by the NAVI, and the conditions under which these alternate forms may be used. See also sections 2.3.2 and 2.5.3, which have to do with the operation of NAVI with standard-definition television timings and interlaced video, respectively.

7.1 Alternate Color Encoding Support and Defaults

NAVI-compatible video sources and displays may optionally support any or all of the alternate video types defined in section 7.2 below. However, all such products must also be capable of supporting standard RGB encoding, using the signal definitions established here and in the VESA VSIS signal standard, and shall use this type of video as the default input or output type. Only after a video source has determined, through reading the E-EDID or similar information, that the display currently in use is capable of any of the alternate video types on the interface selected, may the host switch to providing video of the alternate type.

7.2 Alternate Video Channel Assignments

Should the host determine that the display is capable of handling non-RGB video, such video signals may be provided as noted in 8.1 above, and shall be assigned to the physical and/or logical channels normally used for "Red", "Green", and "Blue" video as follows:

Standard assignment	Composite video	Y/C video	YUV, etc.[1]
Red	Unused	C	$V/Q/C_R/P_R$
Green	Y	Y	Y
Blue	Unused	unused	$U/I/C_B/P_B$

NOTES:

1 – "YUV" video is understood to mean all forms of encoding employing two separate "color difference" signals, including "YIQ", "YC_BC_R", and "YP_BP_R". These map equivalently to YUV in the above as follows: Y = Y throughout, $U = I = C_B = P_B$, and $V = Q = C_R = P_R$.

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