FPDI-1B™ Standard

Video Electronics Standards Association

860 Hillview Court, Suite 150 Phone: (408) 957-9270
Milpitas, CA 95035 FAX: (408) 957-9277

Flat Panel Display Interface Standard
FPDI-1B™

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Purpose
This document describes the electrical, logical, and connector interface between flat panel displays and display controllers in an integrated environment. It applies to the following flat panel displays:

- 640 x 480 (VGA) Addressability, Color Passive Matrix Liquid Crystal Displays, Dual Scan, with 16 Data Lines;
- 800 x 600 (SVGA) Addressability, Color Passive Matrix Liquid Crystal Displays, Dual Scan, with 16 Data Lines,
- 640 x 480 (VGA) Addressability, Active Matrix Liquid Crystal Displays with 18-bit Color;
- 800 x 600 (SVGA) Addressability, Active Matrix Liquid Crystal Displays with 18-bit Color.

Summary
Flat panel displays have advanced to the point of being comparable to CRTs with respect to resolution, color capabilities, and image quality. In most integrated environments, flat panel displays are more desirable than CRTs due to their compact and portable size and weight. However, due to the proliferation of different and incompatible flat panel display interfaces, it is difficult, costly, and time consuming to integrate flat panel displays into notebook computers, instrumentation, and other devices with integrated displays. VESA, as the prominent standards organization for graphics subsystems, has developed a flat panel display interface standard that will ease the system integration task.

Preface

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

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- E-mail support@vesa.org
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  VESA - Video Electronics Standards Association
  860 Hillview Court, Suite 150
  Milpitas, CA 95035

Acknowledgments

This document would not have been possible without the efforts of the members of the 1995-1996 VESA Flat Panel Display Interface Committee and the professional support of the VESA staff.

1. Overview

1.1 Summary

The Flat Panel Display Interface 1B "FPDI-1B" standard described within this document will allow the integration of flat panel displays to graphics controllers in an integrated environment, such as notebook computers, instruments, and hand-held devices. This standard addresses color passive matrix and active matrix displays. This standard is based on current liquid crystal display technology, however it also applies to other flat panel displays.

The FPDI document defines the electrical, logical, and connector interfaces between the graphics controller and flat panel displays. These are base level specifications for functional compliance while providing flexibility for product differentiation and technological innovation. This standard applies to the following flat panel displays:

- 640 x 480 (VGA) Addressability, Color Passive Matrix Liquid Crystal Displays, Dual Scan, with 16 Data Lines;
- 800 x 600 (SVGA) Addressability, Color Passive Matrix Liquid Crystal Displays, Dual Scan, with 16 Data Lines;
- 640 x 480 (VGA) Addressability, Active Matrix Liquid Crystal Displays with 18-bit Color;
- 800 x 600 (SVGA) Addressability, Active Matrix Liquid Crystal Displays with 18-bit Color.

1.2 Background

The lack of flat panel display interface standards has resulted in difficulties for system OEMs and for systems integrators in interfacing a variety of flat panels to a single motherboard design. Graphics controller manufacturers also have difficulty supporting many different interfaces in a single piece of hardware. The lack of standards leads to many difficulties in the development of graphics controllers, column drivers, and in-systems integration.

FPDI-1B™ was created to continue the standardization process which was started with FPDI-1™, by tightening the specifications and concentrating on new panel technology. The panel types supported have been changed to those described in the previous section. The recommended PCB layout has been modified to permit the optional use of grounded connectors. Pin assignments have been added. The LCD driving voltage Vee has been removed, since it is not used in new designs. Power specifications have been clarified. Panel ground, GND, has been renamed Vss. The document has been reorganized to separate the specifications for active matrix panels and passive matrix panels.

1.3 Standard Objectives

- Establish standard electrical, logical, and connector interfaces between the graphics controller and the flat panel display in integrated environments.
- Ensure scalability, ease of integration, low cost, interchangeability, and fast international market acceptance.
- Establish a base level of functional compliance while providing flexibility for product differentiation and technological innovation.
- Establish standards for active and passive matrix, color flat panel displays.

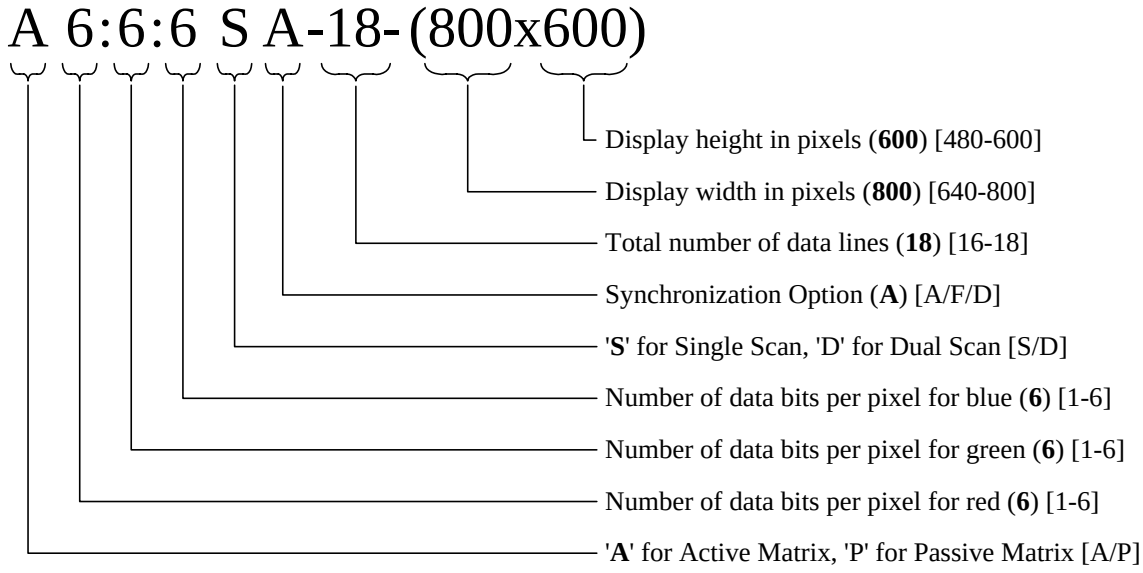
1.4 Reference Documents

ASME Y14.5M - 1994, “Dimensioning and Tolerancing”
UL 94V-0 “Test for Flammability of Plastics Materials for Parts in Devices and Appliances”

2. Signals and Timing

2.1 Panel Type Format

Figure 2.1.1: Panel Type Format Example



The above example conforms to the following format:

Ax:y:z B[C]-W-(H x V)

A Panel Technology
‘A’ = Active
‘P’ = Passive

x:y:z: Number of colors/shades

Monochrome	-	1:0:0
Color, 3-bit	-	1:1:1
Color, 9-bit	-	3:3:3
Color, 18-bit	-	6:6:6

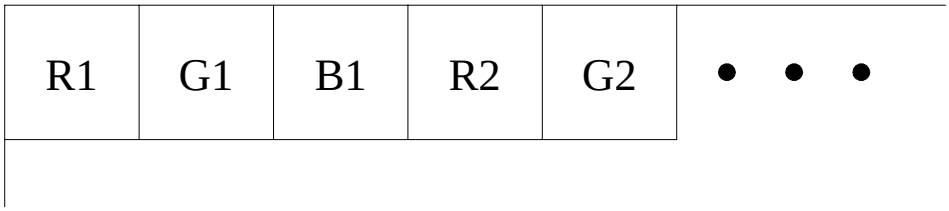
B Panel Construction
‘S’ = Single Scan VGA = ~1/480 Duty, SVGA = ~1/600 Duty
‘D’ = Dual Scan VGA = ~1/240 Duty, SVGA = ~1/300 Duty

C Synchronization Options (Active Matrix only)
‘F’ = FPFRAME/FPLINE sync.
‘D’ = DRDY only sync. (recommended for new designs)
‘A’ = both FPFRAME/FPLINE sync. and DRDY sync.

W Number of panel data bits (not pixels) latched per shift

(H x V) Horizontal x Vertical addressability

Figure 2.1.2: Pixel Data Map Representation



Timing: LCD panels are deemed to comply with FPDI-1B if all of their specifications have minimums equal to or lower and maximums equal to or higher than FPDI-1B values.

Active matrix tables and diagrams in this standard depict ‘A’ type synchronization, with FPLINE, FPFRAME, and DRDY. For the ‘F’ and ‘D’ synchronization options, the unnecessary sync signals can be omitted.

3.0 Power Specifications

3.1 Introduction

Flat panel displays require specific power sequencing. Improper power sequencing can cause permanent damage to the flat panel display.

Power sequencing and power requirements can be broken into several major sub-topics:

* Absolute maximum power ratings
* Panel Interface power requirements and power sequencing (3.3, 5, and 3.3-5 Volt panels)

Backlight power requirements:

Given that backlights (and power requirements) vary greatly across the spectrum of flat panel product/vendors, this section will focus only on the interface power requirements.

It should be noted that the three Operating Power Specification tables (5.0 Volt, 3.3-5.0 Volt, and 3.3 Volt) are mutually exclusive - a panel is required to conform to just one of these specifications.

3.2 Absolute Maximum Power Rating

Symbol	Function	Condition	Rating	Unit	Remark
Data	Input voltage of timing signals	Ta=25°C	-0.3~Vdd+0.3	V	Note 1
V_{dd}	Power supply (5V panels)		-0.3~+6.5	V	
V_{dd}	Power supply (3.3-5V panels)		-0.3~+6.5	V	
V_{dd}	Power supply (3.3V panels)		-0.3~+4.5	V	
V_{con}	Contrast adjustment voltage		N/A	V	Note 2

3.3 Operating Power Specification-5.0 Volt Panel Interface

Symbol	**Function**	**Min**	**Typ**	**Max**	**Unit**	**Remark**
V_{dd}	Supply voltage	+4.5	+5.0	+5.5	V	
V_{rp}	Voltage input ripple	-------	-------	100	mV p-p	
V_{il}	Input voltage low	-------	-------	0.2Vdd	V	Note 1
V_{ih}	Input voltage high	0.8Vdd	-------	-------	V	Note 1

3.4 Operating Power Specification-3.3-5.0 Volt Panel Interface

Symbol	**Function**	**Min**	**Typ**	**Max**	**Unit**	**Remark**
V_{dd}	Supply voltage	+3.0		+5.5	V	
V_{rp}	Voltage input ripple	-------	-------	100	mV p-p	
V_{il}	Input voltage low	-------	-------	0.2Vdd	V	Note 1
V_{ih}	Input voltage high	0.8Vdd	-------	-------	V	Note 1

3.5 Operating Power Specification-3.3 Volt Panel Interface

Symbol	Function	Min	Typ	Max	Unit	Remark
V_{dd}	Supply voltage	+3.0	+3.3	+3.6	V	
V_{rp}	Voltage input ripple	-------	-------	100	mV p-p	
V_{il}	Input voltage low	-------	-------	0.2Vdd	V	Note 1
V_{ih}	Input voltage high	0.8Vdd	-------	-------	V	Note 1

Notes:

1). Includes FPSHIFT, Data, FPLINE, FPFRAME, DRDY, MOD, and FPEN.

2). Passive matrix LCDs that include a DC/DC converter will have a contrast adjustment input. Again, the individual panel specification should be used.

4. Connector Interface

4.1 Introduction

This section of the standard defines the connector interface at the flat panel display which is integral to the PC system.

4.2 Connector Characteristics

4.2.1 Construction

Insulator: High temperature thermoplastic, UL 94V-0 rated material
Contacts: Copper alloy, plated as required

4.2.2 Mechanical

Durability: 30 cycles minimum

4.2.2.1 Insertion and Extraction Force

No. Contacts	Connector Insertion Force	Connector Extraction Force
31	60N Maximum	12N Minimum
41	80N Maximum	16N Minimum

4.2.3 Electrical

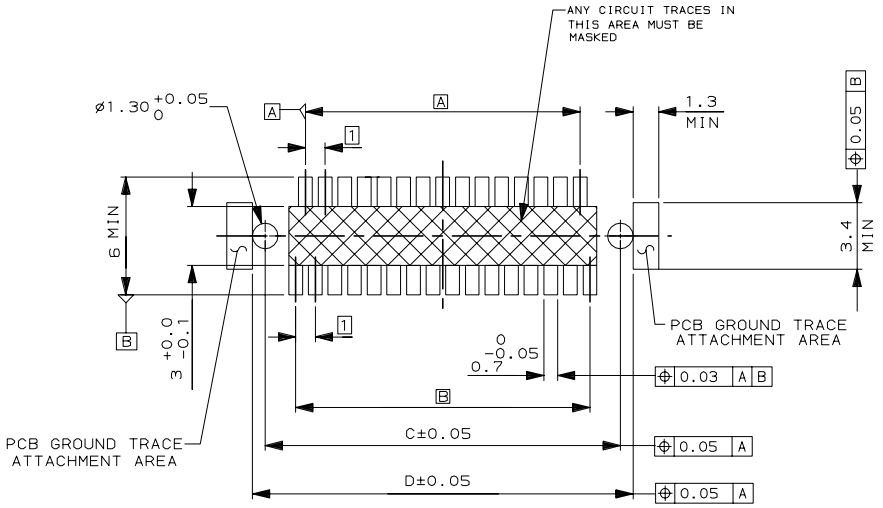
Operating Current: 0.5A maximum per contact
Operating Voltage: 150 vac rms, maximum
Dielectric Withstanding Voltage: 250 vac rms for minimum of 1 minute
Insulation Resistance: 500 MΩ minimum
Contact Resistance: 50mΩ, maximum @ 0.1A DC

4.2.4 Environmental

Operating Temperature: -40°C to 85°C
Resistance to Solder Heating: 240°C for 15 seconds

4.3 Recommended PCB Layout

Figure 4.3.1: Recommended PCB Layout



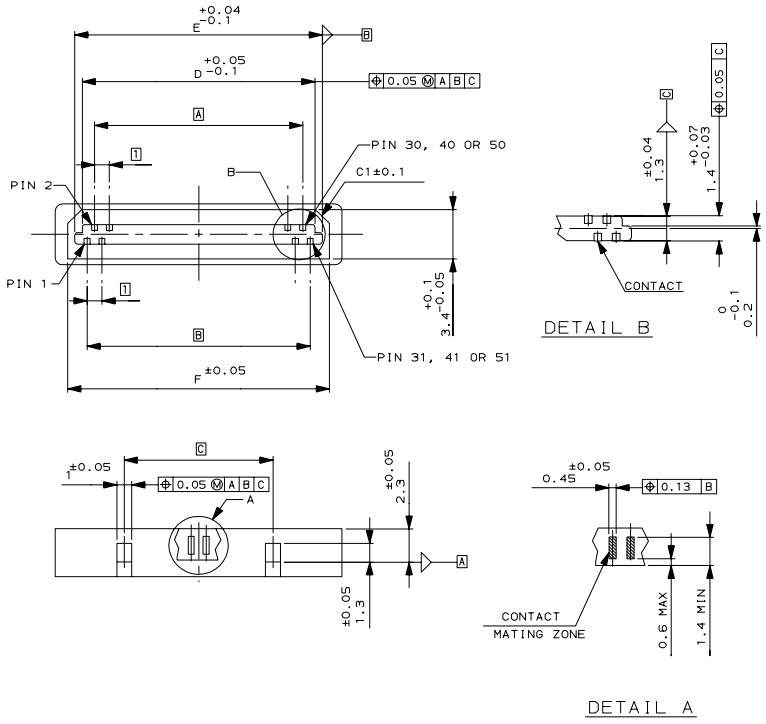
NO. OF CONTACTS	A	B	C	D
31	14.0	15.0	18.1	19.4
41	19.0	20.0	23.1	24.4

Notes:

- Plug dimensions are the controlling interface standard
- Dimensions are in millimeters
- Dimensioning as per ASME Y14.5M - 1994 “Dimensioning and Tolerancing”
- Not to Scale
- Mounting holes are optional

4.4 Plug Interface Dimensions

Figure 4.4.1: Plug Interface Dimensions



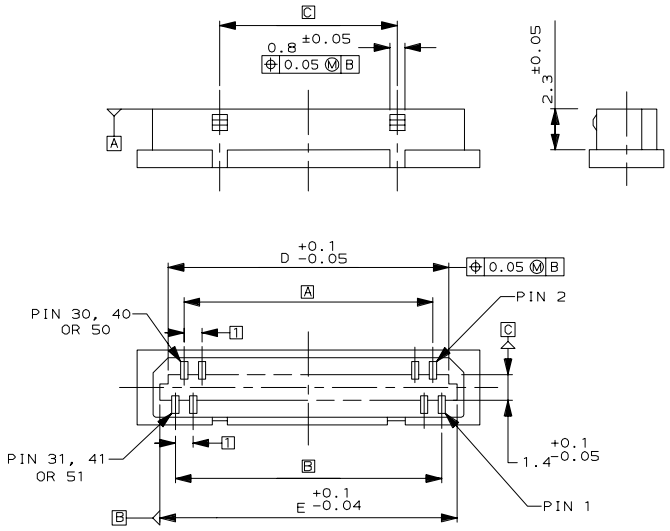
NO. OF CONTACTS	A	B	C	D	E	F
31	14.0	15.0	10.0	15.57	16.6	17.6
41	19.0	20.0	15.0	20.57	21.6	22.6

Notes:

- Plug dimensions are the controlling interface standard
- Dimensions are in millimeters
- Dimensioning as per ASME Y14.5M - 1994 “Dimensioning and Tolerancing”
- Not to scale
- The plug is mounted on the panel.

4.5 Receptacle Interface Dimensions

Figure 4.5.1: Receptacle Interface Dimensions



NO. OF CONTACTS	A	B	C	D	E
31	14.0	15.0	10.0	15.73	16.7
41	19.0	20.0	15.0	20.73	21.7

Notes:

- Plug dimensions are the controlling interface standard
- Dimensions are in millimeters
- Dimensioning as per ASME Y14.5M - 1994 “Dimensioning and Tolerancing”
- Not to scale
- Receptacle shall mate with plug interface

5. Passive Matrix Panels

5.1 Passive Matrix Signals and Timing

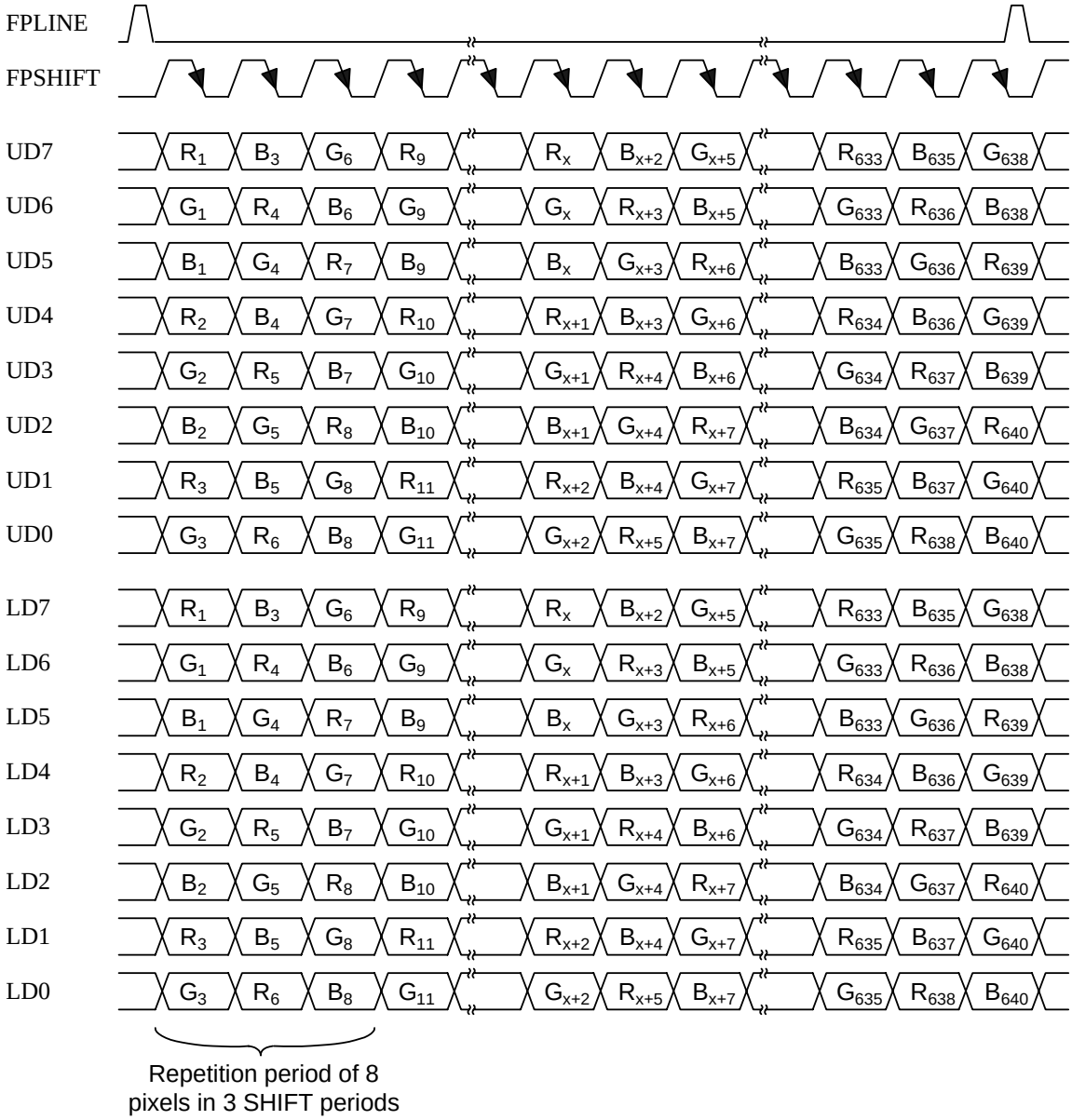
The following section identifies the standard signals and timing specifications for each of the specified flat panel types.

5.1.1.1 P1:1:1D-16-(640x480) Signals

Signal	Function	Comments
UD0	Pixel Data 0, Upper	See Figure Next Page
UD1	Pixel Data 1, Upper	See Figure Next Page
UD2	Pixel Data 2, Upper	See Figure Next Page
UD3	Pixel Data 3, Upper	See Figure Next Page
UD4	Pixel Data 4, Upper	See Figure Next Page
UD5	Pixel Data 5, Upper	See Figure Next Page
UD6	Pixel Data 6, Upper	See Figure Next Page
UD7	Pixel Data 7, Upper	See Figure Next Page
LD0	Pixel Data 0, Lower	See Figure Next Page
LD1	Pixel Data 1, Lower	See Figure Next Page
LD2	Pixel Data 2, Lower	See Figure Next Page
LD3	Pixel Data 3, Lower	See Figure Next Page
LD4	Pixel Data 4, Lower	See Figure Next Page
LD5	Pixel Data 5, Lower	See Figure Next Page
LD6	Pixel Data 6, Lower	See Figure Next Page
LD7	Pixel Data 7, Lower	See Figure Next Page
MOD	Modulation	Optional Signal for AC Bias Control, timing not specified
FPSHIFT	Pixel Clock	See Glossary
FPLINE	Line Pulse	See Glossary
FPFRAME	Frame Pulse	See Glossary
FPEN	Flat Panel Enable	High = Flat Panel ON; Low = Flat Panel OFF
VSS	Ground	Recommendation: a minimum of 4 grounds should be used. FPSHIFT should be bracketed with one VSS placed on each side. The data bits should also be bracketed with one VSS placed prior to the first data signal and one VSS placed after the last data signal. V_{dd} should be separated from DATA by at least one VSS.

Note: Upper = Lines 1-240
Lower = Lines 241-480

Figure 5.1.1.1: P1:1:1D-16-(640x480) Data Formatting



5.1.1.2 P1:1:1D-16-(640x480) Timing

Signal	Parameter	Symbol	Min	Typ	Max	Unit
FPSHIFT	Period	t_s	83			ns
	Frequency	$1/t_s$			12	MHz
	High Time	t_{sh}	30			ns
	Low Time	t_{sl}	30			ns
	Setup to FPLINE	t_{ls}	200			ns
DATA	Setup	t_{ds}	30			ns
	Hold	t_{dh}	30			ns
FPLINE	Period	t_{lp}	Note1			
	Pulse Width	t_{lw}	50			ns
	FPLINE to FPSHIFT hold	t_{lh}	250			ns
FPFRAME	Frequency	$1/t_{fp}$	59	73		Hz
	Period	t_{fp}	240			Line Periods
	Setup	t_{fl}	150			ns
	Hold	t_{fh}	80			ns
	FPLINE Polarity	Positive				
	FPFRAME Polarity	Positive				

Note1: 240 FPSHIFT clocks + 500 ns

Frame frequency for passive matrix panels impacts overall power consumption and optical performance via flickering and shadowing. The user should select this parameter based on system design requirements and front of screen performance.

Because of simultaneous display timing requirements, additional line clocks may be provided at the end of every other frame period (concurrent with CRT vertical retrace). These clocks may be required for AC modulation and image quality considerations.

Figure 5.1.1.2a: P1:1:1D-16-(640x480) Horizontal Data Timing

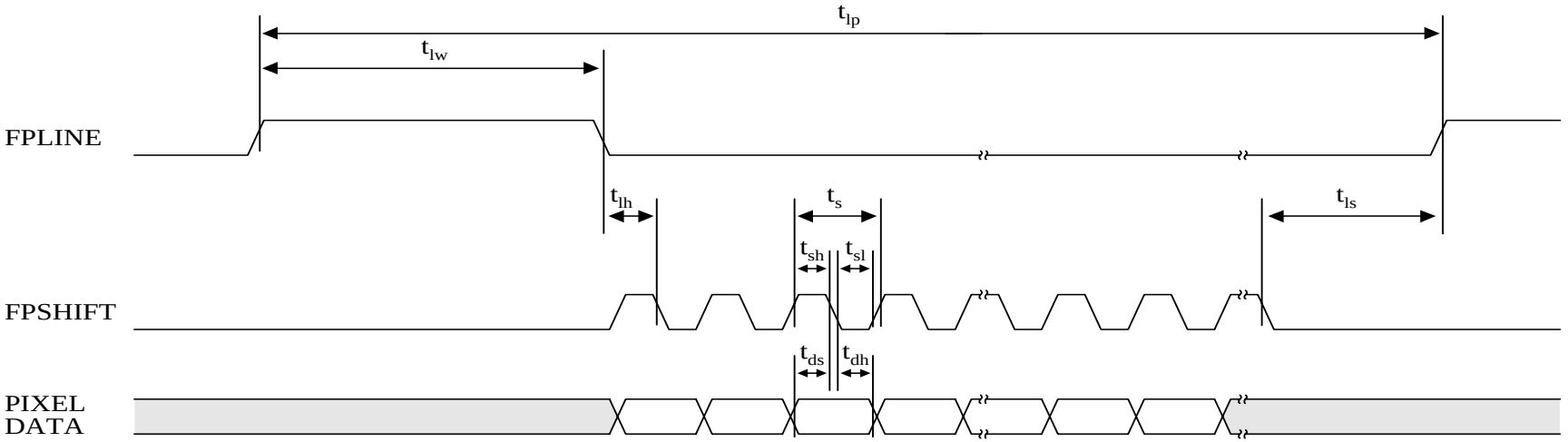
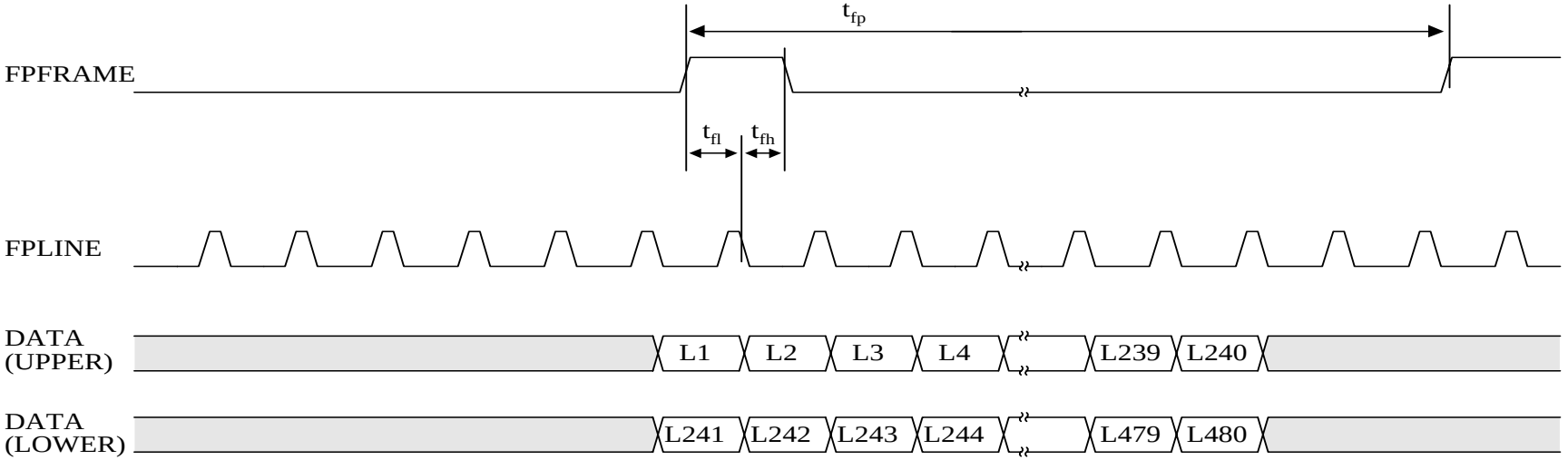


Figure 5.1.1.2b: P1:1:1D-16-(640x480) Vertical Data Timing

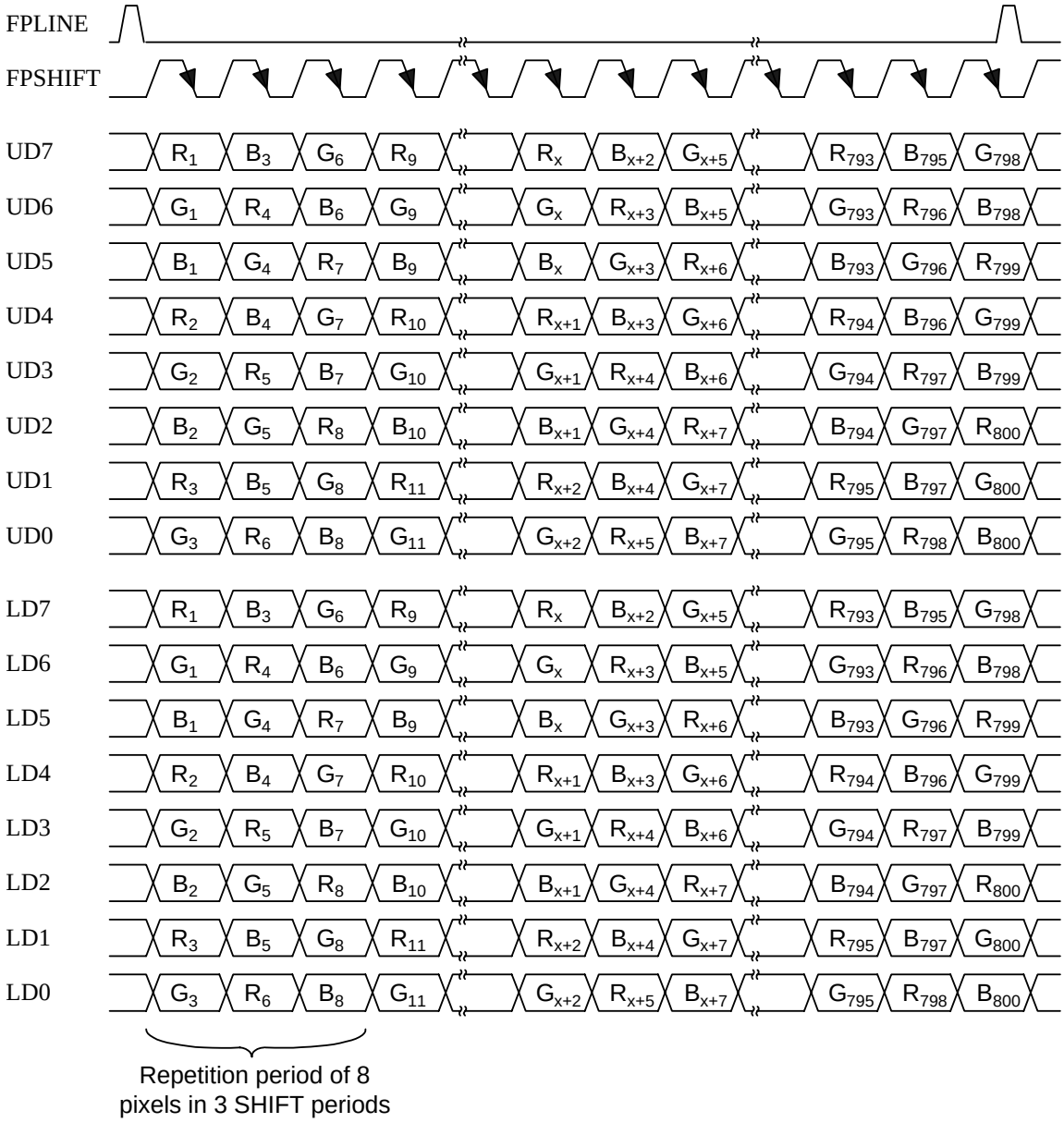


5.1.2.1 P1:1:1-D-16-(800x600) Signals

Signal	Function	Comments
UD0	Pixel Data 0, Upper	See Figure Next Page
UD1	Pixel Data 1, Upper	See Figure Next Page
UD2	Pixel Data 2, Upper	See Figure Next Page
UD3	Pixel Data 3, Upper	See Figure Next Page
UD4	Pixel Data 4, Upper	See Figure Next Page
UD5	Pixel Data 5, Upper	See Figure Next Page
UD6	Pixel Data 6, Upper	See Figure Next Page
UD7	Pixel Data 7, Upper	See Figure Next Page
LD0	Pixel Data 0, Lower	See Figure Next Page
LD1	Pixel Data 1, Lower	See Figure Next Page
LD2	Pixel Data 2, Lower	See Figure Next Page
LD3	Pixel Data 3, Lower	See Figure Next Page
LD4	Pixel Data 4, Lower	See Figure Next Page
LD5	Pixel Data 5, Lower	See Figure Next Page
LD6	Pixel Data 6, Lower	See Figure Next Page
LD7	Pixel Data 7, Lower	See Figure Next Page
MOD	Modulation	Optional Signal for AC Bias Control, timing not specified
FPSHIFT	Pixel Clock	See Glossary
FPLINE	Line Pulse	See Glossary
FPFRAME	Frame Pulse	See Glossary
FPEN	Flat Panel Enable	High = Flat Panel ON; Low = Flat Panel OFF
VSS	Ground	Recommendation: a minimum of 4 grounds should be used. FPSHIFT should be bracketed with one VSS placed on each side. The data bits should also be bracketed with one VSS placed prior to the first data signal and one VSS placed after the last data signal. V_{dd} should be separated from DATA by at least one VSS.

Note: Upper = Lines 1-300
Lower = Lines 301-600

Figure 5.1.2.1: P1:1:1D-16-(800x600) Data Formatting



5.1.2.2 P1:1:1D-16-(800x600) Timing

Signal	Parameter	Symbol	Min	Typ	Max	Unit
FPSHIFT	Period	t_s	62		152	ns
	Frequency	$1/t_s$	6.6		16.2	MHz
	High Time	t_{sh}	25			ns
	Low Time	t_{sl}	25			ns
	Setup to FPLINE	t_{ls}	100			ns
DATA	Setup	t_{ds}	25			ns
	Hold	t_{dh}	25			ns
FPLINE	Period	t_{lp}	Note1			
	Pulse Width	t_{lw}	70			ns
	FPLINE to FPSHIFT hold	t_{lh}	200			ns
FPFRAME	Frequency	$1/t_{fp}$	67			Hz
	Period	t_{fp}	300			Line Periods
	Setup	t_{fl}	100			ns
	Hold	t_{fh}	100			ns
	FPLINE Polarity	Positive				
	FPFRAME Polarity	Positive				

Note1: 300 FPSHIFT clocks + 370 ns

Frame frequency for passive matrix panels impacts overall power consumption and optical performance via flickering and shadowing. The user should select this parameter based on system design requirements and front of screen performance.

Because of simultaneous display timing requirements, additional line clocks may be provided at the end of every other frame period (concurrent with CRT vertical retrace). These clocks may be required for AC modulation and image quality considerations.

Figure 5.1.2.2a: P1:1:1D-16-(800x600) Horizontal Data Timing

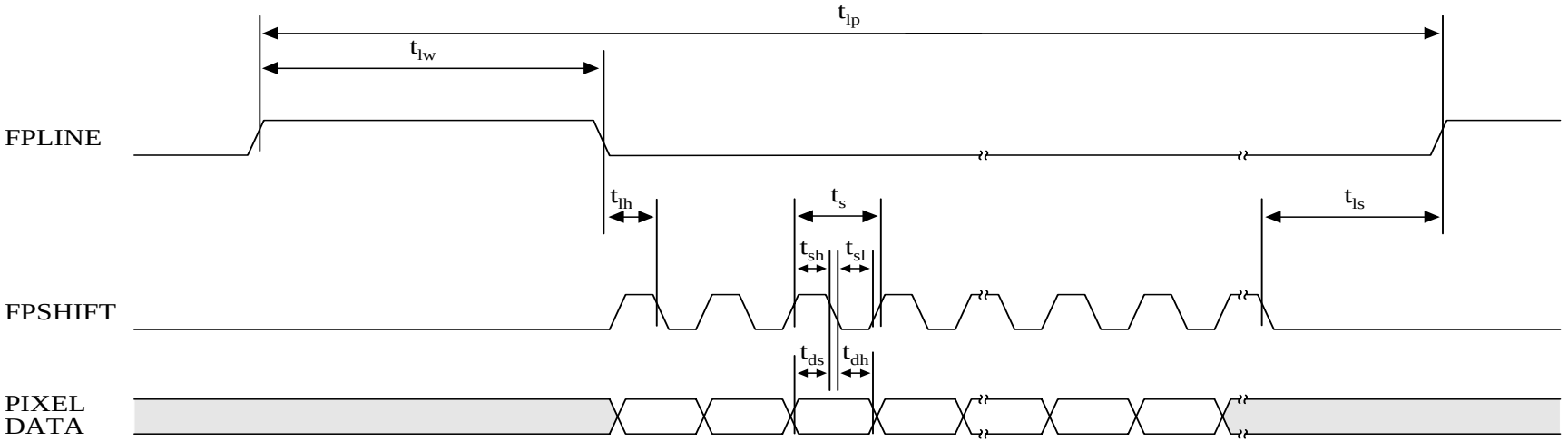
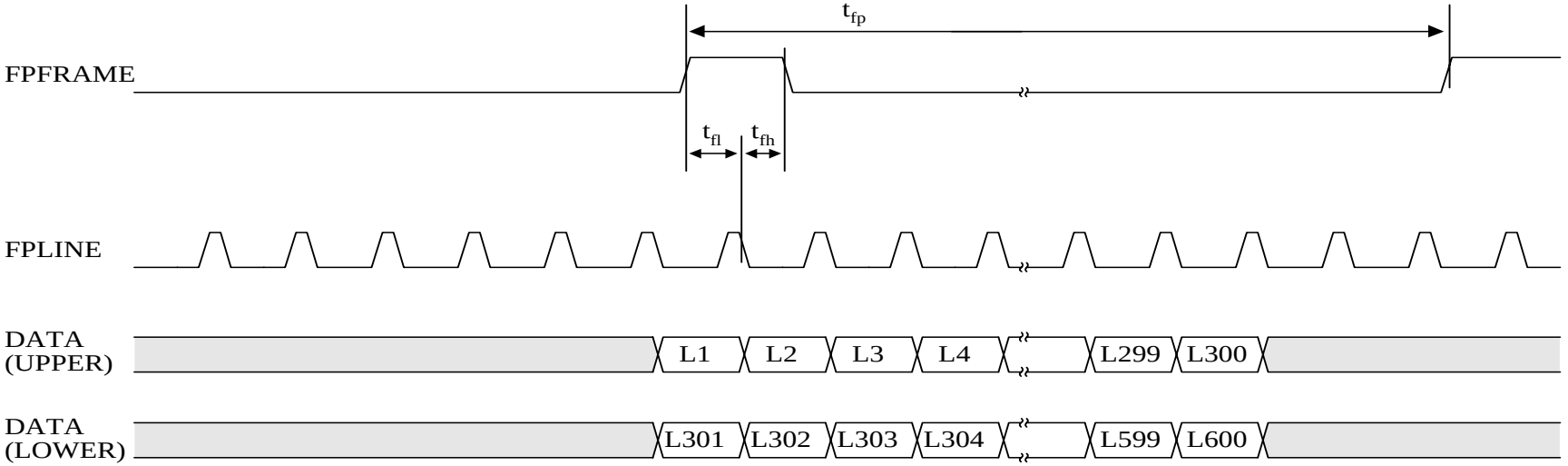
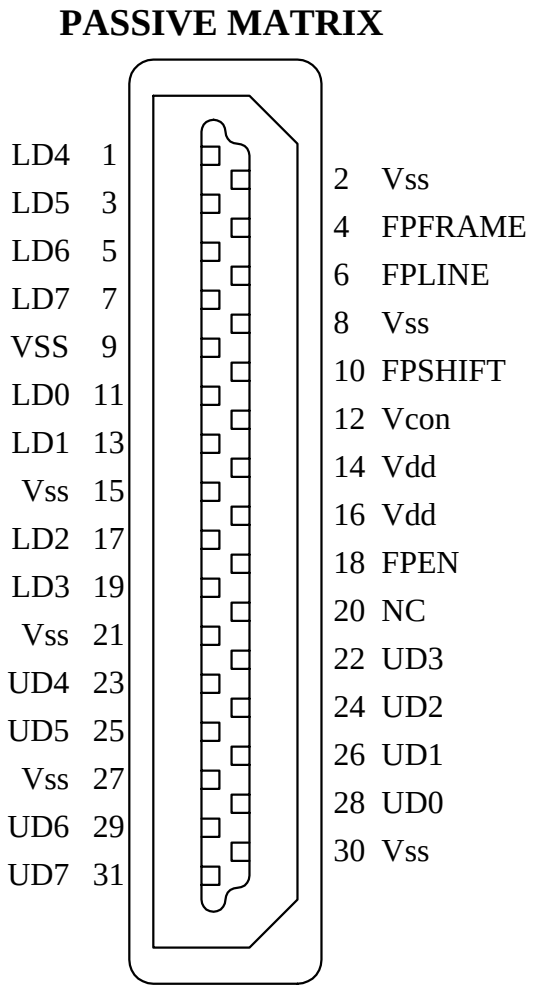


Figure 5.1.2.2b: P1:1:1D-16-(800x600) Vertical Data Timing



5.2 Passive Matrix Pin Assignment

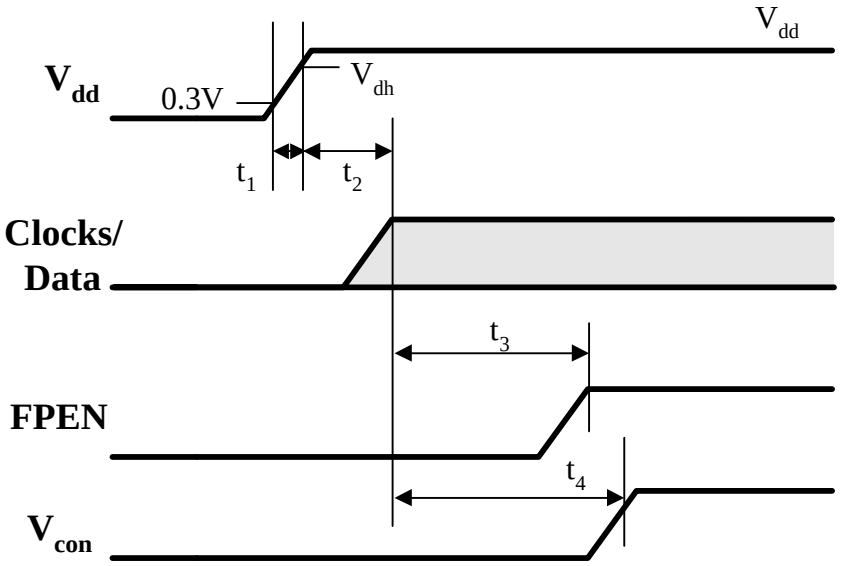
Figure 5.2.1: Recommended Passive Matrix Pin Assignment (Plug Interface)



Note: See Glossary for explanation of Vcon.

5.3 Passive Matrix Power Sequencing

Figure 5.3.1: Passive Matrix Power-up Sequencing



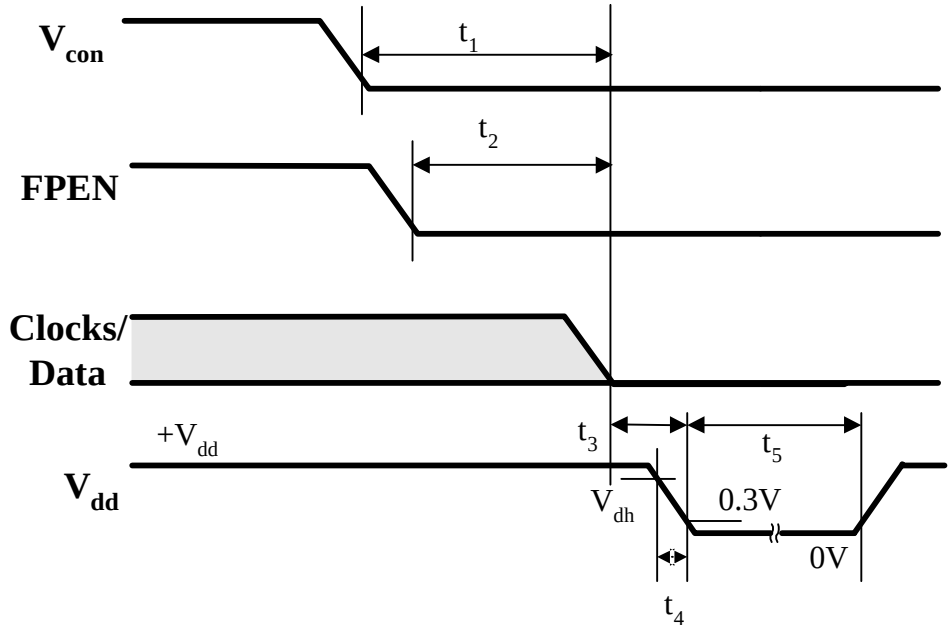
5.3.1 Passive Matrix Power-up Sequence Timing

Symbol	Function	Min	Max	Units
t_1	V_{dd} rise time	-------	10	ms
t_2	V_{dd} to clock	0	40	ms
t_3	clock to FPEN	30	100	ms
t_4	clock to V_{con}	20		ms

Note: All signals (FPEN, V_{con}) may not be present.

	Vdh (Volts)
5.0 Volt panel interface	4.5
3.3-5.0 Volt panel interface	3.0
3.3 Volt panel interface	3.0

Figure 5.3.2: Passive Matrix Power-down Sequencing



5.3.2 Passive Matrix Power-down Sequence Timing

Symbol	Function	Min	Max	Units
t_1	V_{con} to clock	0		ms
t_2	FPEN to clock	0		ms
t_3	clock to V_{dd}	0	40	ms
t_4	V_{dd} fall time	-------	10	ms
t_5	Power retry	500		ms

Note: All signals (FPEN, V_{con}) may not be present.

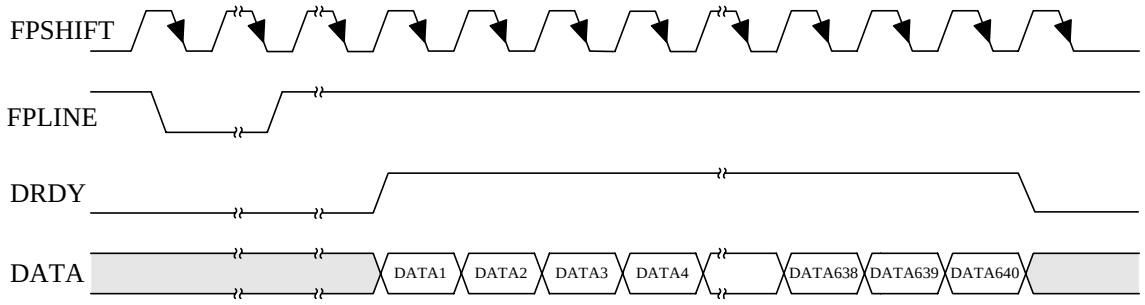
6. Active Matrix Panels

6.1 Active Matrix Signals and Timing

6.1.1.1 A6:6:6S-18-(640x480) Signals

Signal	Function	Comments
R0	Red Data (LSB)	
R1	Red Data	
R2	Red Data	
R3	Red Data	
R4	Red Data	
R5	Red Data	
G0	Green Data (LSB)	
G1	Green Data	
G2	Green Data	
G3	Green Data	
G4	Green Data	
G5	Green Data	
B0	Blue Data (LSB)	
B1	Blue Data	
B2	Blue Data	
B3	Blue Data	
B4	Blue Data	
B5	Blue Data	
FPSHIFT	Pixel Clock	See Glossary
FPLINE	Line Pulse	See Glossary
FPFRAME	Frame Pulse	See Glossary
DRDY	Data Ready	See Glossary
VSS	Ground	Recommendation: **if FPSHIFT is less than or equal to 28 MHz**, a minimum of 6 grounds should be used. The FPSHIFT signal should be bracketed with one ground on each side. There should be a minimum of one ground for every six DATA signals and V_{dd} should be separated from DATA by a ground signal. **If FPSHIFT is greater than 28 MHz**, a minimum of 9 grounds should be used. There should be a minimum of one ground for every three DATA signals and V_{dd} should be separated from DATA by a ground signal.

Figure 6.1.1.1: A6:6:6S-18-(640x480) Data Formatting



DATA = { R5, ... , R0 , G5 , ... , G0 , B5 , ... , B0 } for A6:6:6S-18

For panels using only DRDY type control timing (Ax:y:zSD-W-(HxV), the FPFRAME and FPLINE signals need not be present. Where equalities appear in the timing tables (e.g. $t_{lpd}=t_{lpl}$), the first parameter (e.g. t_{lpd}) applies to DRDY type control timing. Panels using FPFRAME and FPLINE type control timing require FPFRAME and FPLINE signals.

6.1.1.2 A6:6:6S-18-(640x480) Timing

Signal	Parameter	Symbol	Min	Typ	Max	Unit
FPSHIFT	Period	t_s	35.3	39.72		ns
	Frequency	$1/t_s$		25.18	28.32	MHz
	High Time	t_{sh}	10			ns
	Low Time	t_{sl}	10			ns
FPLINE	Setup to FPSHIFT	t_{ls}	10			ns
	Pulse Width	t_{lw}	10			Shift Clocks
FPFRAME	Pulse Width	t_{fw}	2	2	34	Line Periods
	FPFRAME to DATA	t_{fd}	34			Line Periods
	Setup to FPLINE	t_{fl}	20			ns
	Line Period	$t_{lpd} = t_{lpl}$	770	800	860	Shift Clocks
			31.5	31.77	35.74	μs
	Horizontal Display Time	t_{hd}	640	640	640	Shift Clocks
	Frame Frequency	$1/t_{fpd}$	56	59.95		Hz
	Frame Period	$t_{fpd} = t_{fpf}$	514	525		Line Periods
	Vertical Display Time	t_{vd}	480	480	480	Line Periods
DATA	Setup	t_{ds}	10			ns
	Hold	t_{dh}	10			ns
DRDY	Setup	t_{drs}	10			ns
	Hold	t_{drh}	10			ns
	Display Start	t_{drds}		144	164	Shift Clocks
	FPLINE Polarity	Negative				
	FPFRAME Polarity	Negative				

Figure 6.1.1.2a: A6:6:6S-18-(640x480) Horizontal Data Timing

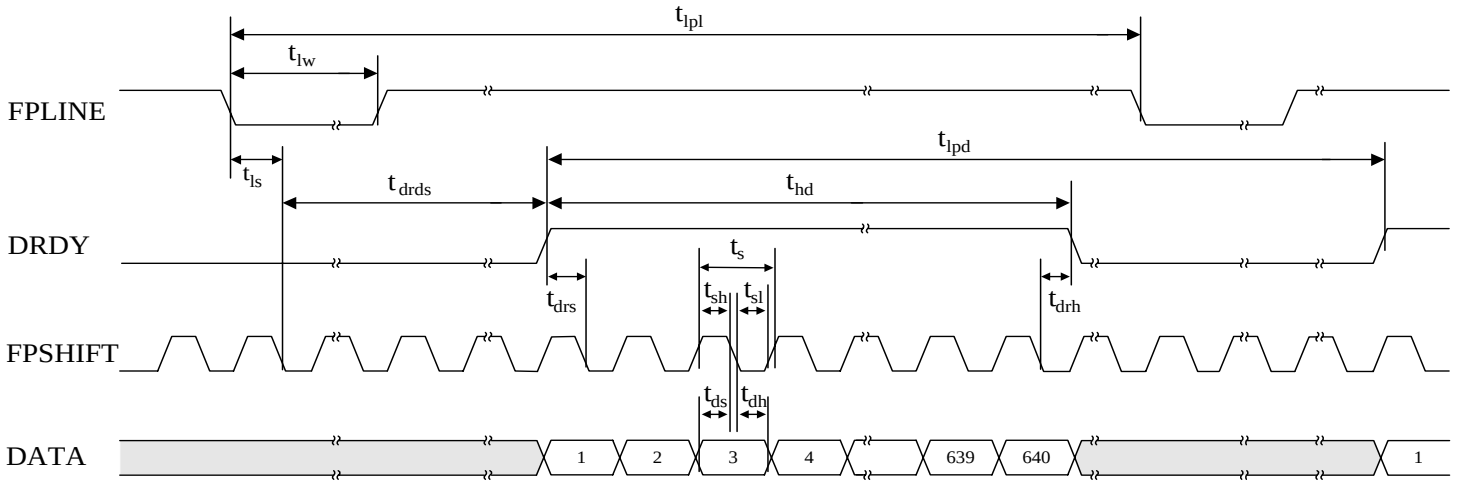
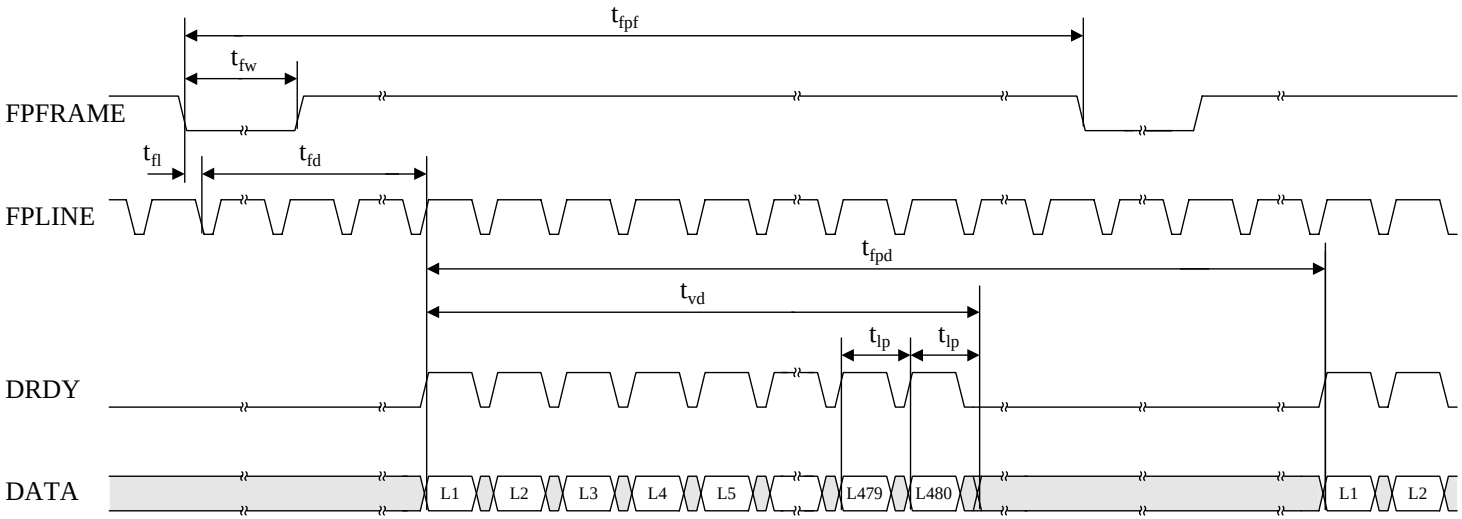


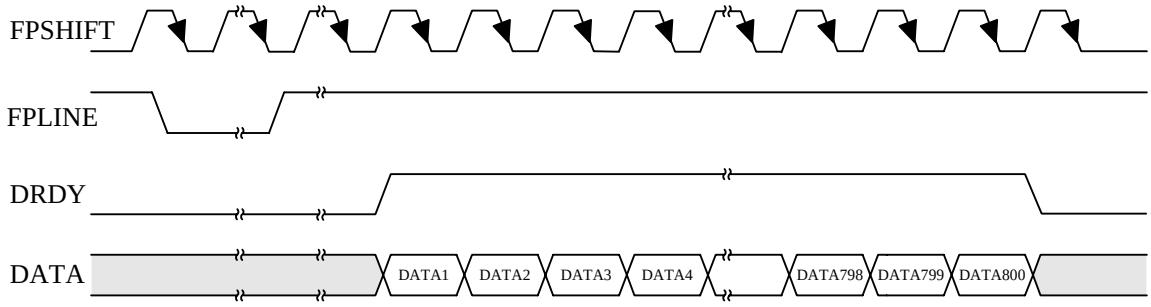
Figure 6.1.1.2b: A6:6:6S-18-(640x480) Vertical Data Timing



6.1.2.1 A6:6:6S-18-(800x600) Signals

Signal	Function	Comments
R0	Red Data (LSB)	
R1	Red Data	
R2	Red Data	
R3	Red Data	
R4	Red Data	
R5	Red Data	
G0	Green Data (LSB)	
G1	Green Data	
G2	Green Data	
G3	Green Data	
G4	Green Data	
G5	Green Data	
B0	Blue Data (LSB)	
B1	Blue Data	
B2	Blue Data	
B3	Blue Data	
B4	Blue Data	
B5	Blue Data	
FPSHIFT	Pixel Clock	See Glossary
FPLINE	Line Pulse	See Glossary
FPFRAME	Frame Pulse	See Glossary
DRDY	Data Ready	See Glossary
VSS	Ground	Recommendation: **if FPSHIFT is less than or equal to 28 MHz**, a minimum of 6 grounds should be used. The FPSHIFT signal should be bracketed with one ground on each side. There should be a minimum of one ground for every six DATA signals and V_{dd} should be separated from DATA by a ground signal. **If FPSHIFT is greater than 28 MHz**, a minimum of 9 grounds should be used. There should be a minimum of one ground for every three DATA signals and V_{dd} should be separated from DATA by a ground signal.

Figure 6.1.2.1: A6:6:6S-18-(800x600) Data Formatting



DATA = { R5, ... , R0 , G5 , ... , G0 , B5 , ... , B0 } for A6:6:6S-18

For panels using only DRDY type control timing (Ax:y:zSD-W-(HxV), the FPFRAME and FPLINE signals need not be present. Where equalities appear in the timing tables (e.g. $t_{lpd}=t_{lpl}$), the first parameter (e.g. t_{lpd}) applies to DRDY type control timing. Panels using FPFRAME and FPLINE type control timing require FPFRAME and FPLINE signals.

6.1.2.2 A6:6:6S-18-(800x600) Timing

Signal	Parameter	Symbol	Min	Typ	Max	Unit
FPSHIFT	Period	t_s	25	27.78		ns
	Frequency	$1/t_s$		36	40	MHz
	High Time	t_{sh}	10			ns
	Low Time	t_{sl}	10			ns
FPLINE	Setup to FPSHIFT	t_{ls}	10			ns
	Pulse Width	t_{lw}	4			Shift Clocks
FPFRAME	Pulse Width	t_{fw}	2	2	34	Line Periods
	FPFRAME to DATA	t_{fd}	34			Line Periods
	Setup to FPLINE	t_{fl}	20			ns
	Line Period	$t_{lpd} = t_{lpl}$	844	1024	1056	Shift Clocks
			26.4	28.44	29.33	μs
	Horizontal Display Time	t_{hd}	800	800	800	Shift Clocks
	Frame Frequency	$1/t_{fpd}$	56.25	56.8		Hz
	Frame Period	$t_{fpd} = t_{fpf}$	606	625		Line Periods
	Vertical Display Time	t_{vd}	600	600	600	Line Periods
DATA	Setup	t_{ds}	7			ns
	Hold	t_{dh}	10			ns
DRDY	Setup	t_{drs}	7			ns
	Hold	t_{drh}	10			ns
	Display Start	t_{drds}		200	255	Shift Clocks
	FPLINE Polarity	Negative				
	FPFRAME Polarity	Negative				

Figure 6.1.2.2a: A6:6:6S-18-(800x600) Horizontal Data Timing

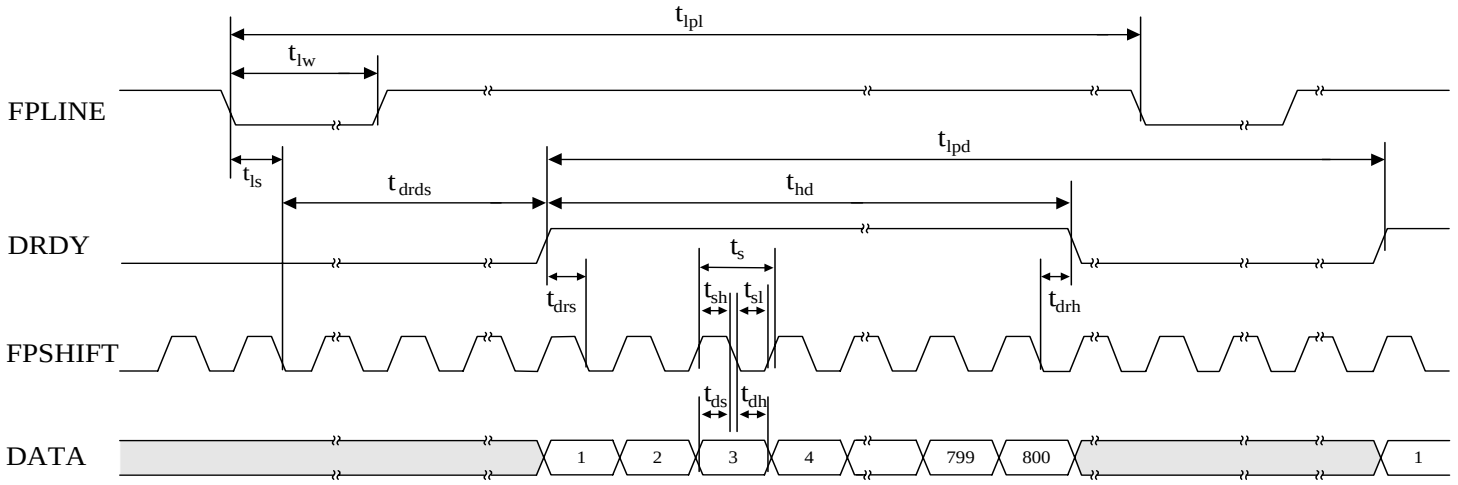
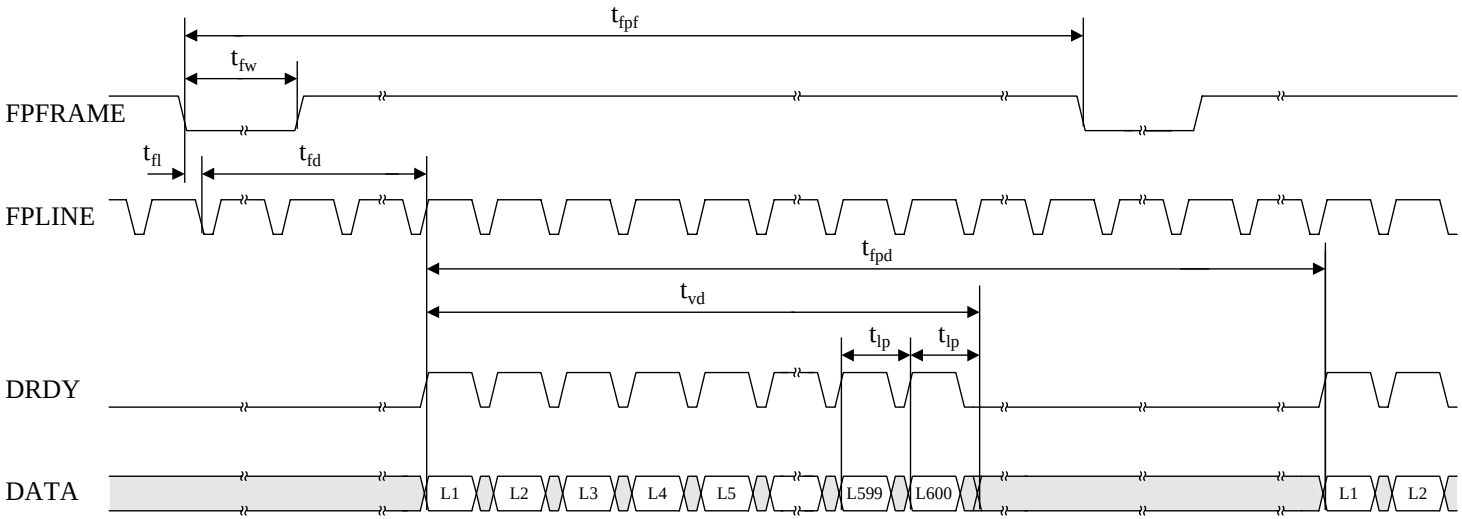
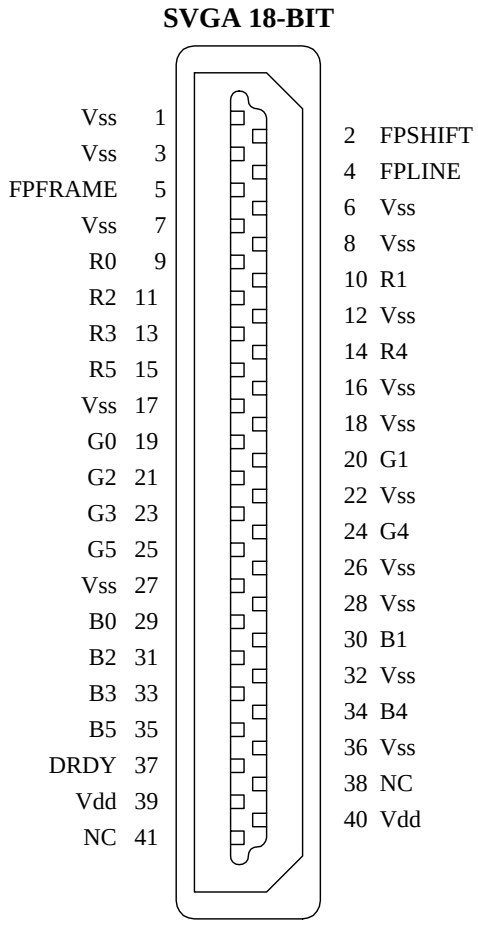


Figure 6.1.2.2b: A6:6:6S-18-(800x600) Vertical Data Timing



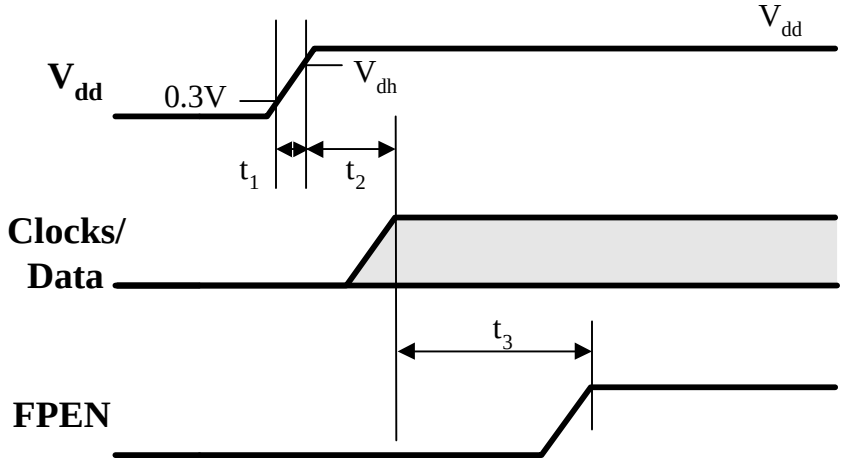
6.2 Active Matrix Pin Assignment

Figure 6.2.1: Recommended Active Matrix Pin Assignment (Plug Interface)



6.3 Active Matrix Power Sequencing

Figure 6.3.1: Active Matrix Power-up Sequencing



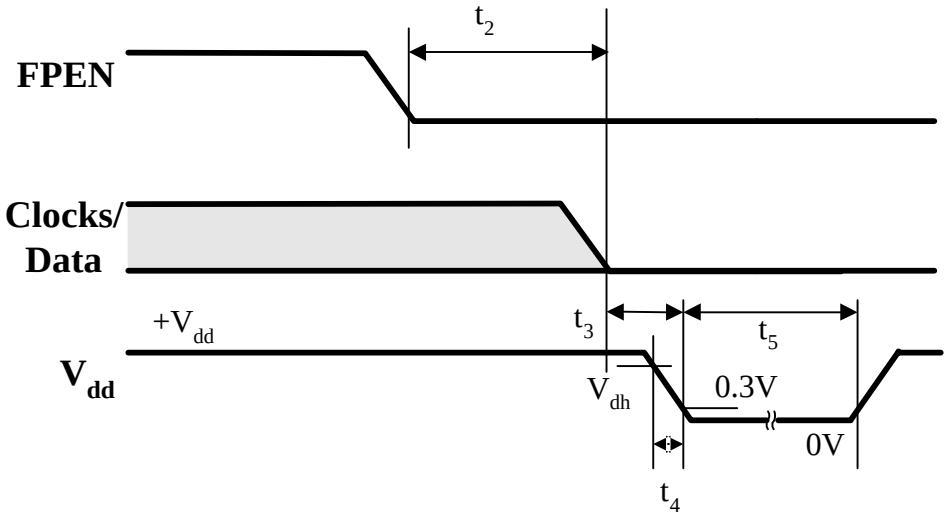
6.3.1 Active Matrix Power-up Sequence Timing

Symbol	Function	Min	Max	Units
t_1	V_{dd} rise time	-------	10	ms
t_2	V_{dd} to clock	0	40	ms
t_3	clock to FPEN	30	100	ms

Note: All signals (FPEN) may not be present.

	Vdh (Volts)
5.0 Volt panel interface	4.5
3.3-5.0 Volt panel interface	3.0
3.3 Volt panel interface	3.0

Figure 6.3.2: Active Matrix Power-down Sequencing



6.3.2 Active Matrix Power-down Sequence Timing

Symbol	Function	Min	Max	Units
t_1	FPEN to clock	0		ms
t_2	clock to V_{dd}	0	40	ms
t_3	V_{dd} fall time	-------	10	ms
t_4	Power retry	500		ms

Note: All signals (FPEN, V_{con}) may not be present.

7. Glossary

7.1 Timing Signals

DRDY

Alias: Data Ready, Display Enable, DE, DTMG, ENAB

Definition: This signal has similar timing to FPLINE, but is valid ONLY when valid data is presented on the panel data interface. It is inactive during horizontal and vertical blanking and can be used for Horizontal only, or for Horizontal AND Vertical positioning.

FPFRAME

Alias: Frame Pulse, FCLK, Frame Clock, LFS, FRM, YD, S, FP

Definition: This is the flat panel display equivalent of the CRT signal VSYNC. It is a signal that cycles once per frame and, when active, indicates that the line being latched is to be displayed on the first line of the panel.

FPLINE

Alias: Line Pulse, CLK, Line Clock, LLCLK, LP, LOAD, HSYNC, CP1, CL1

Definition: This is the flat panel display equivalent of the CRT signal HSYNC. It cycles once per line and, when going active, indicates the next data will be for a new line.

MOD

Alias: M, Modulation, A.C. Modulation, MCLK, ACDCLK

Definition: A signal with a 50% duty cycle that is supplied to the panel and MAY BE used internally to prevent D.C. polarization (charge build-up) and panel damage. This signal toggles every N lines, where N is generally programmable, is a prime number, and differs among panels and manufacturers.

FPSHIFT

Alias: Shift Clock, SCLK, Data Clock, VDCLK, CP, CP2, SCP, Load, Cl2, CK, NCK, XCK, XCKU, XCKL, SCLKU, SCLKL, DCLK.

Definition: Shift Clock for panel data: sometimes called serial shift clock because it shifts the panel data into serial shift registers. This is the clock that causes the panel to latch the data presented on the panel data interface. This clock generally cycles once for every time data changes on the panel interface.

7.2 Power and Control Signals

FPEN

Alias: Panel Enable, Display On, PE

Definition: This signal goes active concurrently OR after all panel voltages, clocks, and data are supplied. This signal goes invalid concurrently or before ANY panel voltages or signals are removed. It MAY BE used within the panel to enable the row and column driver chips output.

V_{dd}

Alias: Panel logic voltage, V_{cc}

Definition: This is the power supply voltage that drives the panel logic, for example +5V or +3.3V. Some panels include DC-DC converters to derive other needed voltages from Vdd.

V_{ss}

Alias: Ground, GND

Definition: This is the generic term for ground within this standard.

V_{con}

Alias: Contrast Adjustment Voltage

Definition: External contrast adjustment input generally for passive matrix LCDs (analog).

7.3 Data Signals

By0

Alias: Blue Data LSB

Definition: In an X bit interface, this data represents the LSB of the Blue data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on).

ByX

Alias: Blue Data MSB

Definition: In an X bit active matrix interface, this data represents the MSB of the Blue data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on). In a passive matrix interface, this data represents the Blue subpixel of pixel ‘X’ in the row (y is not used).

Dy0

Alias: Data Bit 0

Definition: In an X bit interface, this data bit would appear in location X (leftmost pixel being 0). The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on).

DyX

Alias: Data Bit X

Definition: In an X bit interface, this data bit would appear in location 0 (leftmost pixel being 0). The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on).

Gy0

Alias: Green Data LSB

Definition: In an X bit interface, this data represents the LSB of the Green data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on).

GyX

Alias: Green Data MSB

Definition: In an X bit active matrix interface, this data represents the MSB of the Green data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on). In a passive matrix interface, this data represents the Green subpixel of pixel ‘X’ in the row (y is not used).

LD(n-1)

Alias: Lower Data Bit n-1

Definition: In an n bit interface, this data represents the first subpixel on the lower panel (LD0 would be n subpixels from the left-hand side on the top row of the lower panel).

LDx

Alias: Lower Data Bit x

Definition: In an n bit interface, this data represents the (n-x)th subpixel on the lower panel (LD0 would be n subpixels from the left-hand side on the top row of the lower panel).

Ry0

Alias: Red Data LSB

Definition: In an X bit interface, this data represents the LSB of the Red data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on).

RyX

Alias: Red Data MSB

Definition: In an X bit active matrix interface, this data represents the MSB of the Red data. The 'y' is an optional field used if the interface contains more than one pixel per clock (0 for the first pixel, 1 for the second pixel, and so on). In a passive matrix interface, this data represents the Red subpixel of pixel ‘X’ in the row (y is not used).

UD(n-1)

Alias: Upper Data Bit n-1

Definition: In an n bit interface, this data represents the first subpixel on the upper panel (UD0 would be n subpixels from the left-hand side on the top row of the upper panel).

UDx

Alias: Upper Data Bit x

Definition: In an n bit interface, this data represents the (n-x)th subpixel on the upper panel (UD0 would be n subpixels from the left-hand side on the top row of the upper panel).

7.4 Terminology

Addressability

Alias: (Resolution)

Definition: Number of picture elements that can be addressed horizontally or vertically on a display. Often incorrectly called ‘resolution’.

Active Matrix

Alias: AMLCD, TFT

Definition: A display in which an active switching element is present at each pixel/subpixel of the display, to provide electrical isolation and quick charging/discharging of display elements.

Dual Scan

Alias:

Definition: A display which is logically divided into an upper half and a lower half, such that a line in the upper half and a line in the lower half are simultaneously written, over different data lines.

Passive Matrix

Alias: PMLCD, STN

Definition: A display which does not have active switching elements at each pixel/subpixel.

Single Scan

Alias:

Definition: A display to which data is written one line at a time, starting at the top row and proceeding to the bottom row.

SVGA

Alias: 800x600, 8x6, 8 by 6

Definition: 800 pixels wide by 600 pixels high screen addressability.

VGA

Alias: 640x480, 6x4, 6 by 4

Definition: 640 pixels wide by 480 pixels high screen addressability.