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Video Electronics Standards Association

Flat Panel Display Interface -2 Standard

Video Electronics Standards Association

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Flat Panel Display Interface -2

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Purpose

The purpose of this standard is to define an electrical, logical, and connector interface for flat panel displays. The usage is within closed environments, typically notebook computers or monitor enclosures.

Summary

Earlier standards, FPDI-1 and FPDI-1B, were compilations of existing flat panel display specifications in production at that time. FPDI-2 defines a common interface that is display technology independent and scalable through HDTV addressabilities. The goal is to reduce flat panel display manufacturers design costs, system integration costs, and time to market.

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FPDI-2 Workgroup Members

Effective industry standard requires input from many sources. The FPDI Committee members listed below were instrumental in providing valuable industry input into this proposal.

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Terms and Abbreviations

Term or Abbreviation	Description
ASIC	Application Specific Integrated Circuit
CRT	Cathode Ray Tube
CMOS	Complimentary Metal Oxide Semiconductor
DDC	VESA Display Data Channel
DDC2B	Simplest of the VESADDC2 modes defined in VESA DDC standard
DDC2B+	Adds bi-directional communications to VESA DDC2B
DDC2AB	An ACCESS.bus mode defined in VESA DDC standard
DPMS	VESA Display Power Management Signaling
DSTN	Dual Scan Super Twist Nematic LCD
EDID	VESA Extended Display Identification Data
EMI	Electromagnetic Interference
EVC	VESA Enhanced Video Connector
FEC	Flexible Etched Circuit
FPD	Flat Panel Display
FPDI	VESA Flat Panel Display Interface
HDTV	High Definition Television
IEEE 1394	High Performance Serial Bus Standard
IC	Integrated Circuit
I^2C	Trademark of Philips, Inter IC or I^2C - Bus
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling[1]
Logical Layer	Indicates a section of code
MCCS	VESA Monitor Control Command Set
P&D	VESA Plug and Display standard
PanelLink™	Trademark of Silicon Image
PCB	Printed Circuit Board
PLL	Phase Lock Loop
Physical Layer	Indicates a physical layer, electrical or mechanical
RGB2S	Red, Green & Blue Video, HSYNC and VSYNC
Rxn	TMDS Receiver Number ‘n’
TFT	Thin Film Transistor LCD
TMDS	Transition Minimized Differential Signaling[2]
TTL	Transistor, Transistor Logic
Txn	TMDS Transmitter number ‘n’
USB	Universal Serial Bus
VESA	Video Electronics Standards Association

[1] The term LVDS is used in this document as a generic term and does not imply any particular LVDS technology.

[2] The term TMDS, a trademark of Silicon Image, Inc., will generally be used in this document to denote PanelLink™ or compatible technologies.

1. Introduction

1.1 Overview

This standard describes the electrical, logical, and connector interface for a flat panel display. The FPD with its standardized interface will be used in mobile computers, desktop monitors, or in embedded industrial applications. The electrical signal layer is PanelLink™ Technology developed by Silicon Image, Inc. of Cupertino, California (www.SiImage.com), hereafter called Transition Minimized Differential Signaling (TMDS). The TMDS technology converts parallel data to high speed serial data. The serial data is transmitted over suitable transmission media to the defined interface connector of this standard. The TMDS receiver mounted on the FPD reconverts the serial data to parallel data usable by the FPD. This standard defines a connector interface and pin assignment but does not define a suitable transmission media construction. The pixel data format transmitted over the suitable transmission media is defined in this standard. Initialization control using VESA DDC2B for transmission of VESA EDID, Version 3.0, data block is optional. The LCD backlight connector interface, inverter, and luminance control is outside the scope of this document.

The envisioned usage for a compliant FPD is in closed systems, typically notebook computers or desktop monitors. The connector is rated as an internal connector. The electrical and logical interface can extend outside the closed environment. An optional monitor bulkhead connector interface is described in the VESA P&D standard.

The VESA P&D standard defines the video port for the host system using TMDS. The FPDI-2 standard is fully compatible with and is an extension of that standard as the receiver of the video data. The dual use FPDI-2 display provides for the following:

- Compatibility with video graphics controllers using integrated TMDS transmitters,
- Reduction of the number of software device drivers that need to be written,
- Reduction of the system integrator's display inventory,
- Independence of the display technology ,
- Enables FPD manufacturers to produce a common panel interface regardless of size and resolution requirements.

1.2 References

Several standards are referenced by this document and should be considered a part of the FPDI-2 specification.

Name of Standard	Version / Reference #	Date of Issue
ANSI/EIA-364—1994, Electrical Connector /Socket Test Procedures Including Environmental Classifications	C	Nov. '94
ACCESS.bus Specification	3.0	Sept. '95
ASME Y14.5M-1994		Jan. '95
IEC 801-1, Electromagnetic compatibility for industrial-process measurement and control equipment. Part 1 - General introduction	1984-11	
VESA Display Data Channel (DDC)	3.0	Dec. '97
VESA Display Power Management Signaling (DPMS)	1.0	Aug. '93
VESA Extended Display Identification Data (EDID)	3.0	Nov. '97
VESA Flat Panel Display Interface Timing		
VESA Monitor Control Command Set (MCCS)	0.9p	June '97
VESA Plug and Display (P&D)	1.0	June '97

2. Connector Interface Pin Assignment

2.1 Pin Assignments for the Mandatory 20-Contact Position Connector Interface

The 20 contact position connector is mandatory for this standard and represents a minimal configuration. Within this minimal configuration, the VESA DDC initialization channel is optional. If DDC is not used, the three contact positions 2, 3, and 4 shall not be used for any other electrical functions.

For notebook applications, VDD1 and VDD2 would typically be tied together. For monitor applications, VDD1 and VDD2 would be sequenced as described in the Section 6 Power Sequencing. The table below lists the pin assignments required for compliance with this connector interface specification.

Pin #	Description	Pin #	Description
1	VCONT (STN only)	11	TMDS Data 2 Return
2	+5 VDC [optional]	12	TMDS Data 1 +
3	DDC Clock (SLA) [optional]	13	TMDS Data 1 -
4	DDC Data (SDA) [optional]	14	TMDS Data 1 Return
5	VDD2 for Panel Drivers (3.3 Volt)	15	TMDS Data 0 +
6	VDD1 for TMDS and Panel Logic (3.3 Volt)	16	TMDS Data 0 -
7	Ground/Vcc Return/DDC Return	17	TMDS Data 0 Return
8	Ground/Vcc Return/DDC Return	18	TMDS Clock +
9	TMDS Data 2 +	19	TMDS Clock -
10	TMDS Data 2 -	20	TMDS Clock Return

Table 2-1: Pin Assignments for Mandatory 20-Contact Position Connector Interface

2.2 Pin Assignments For The Optional 8-Contact Position Connector Interface

In addition to the 20-contact position connector interface, some monitor applications may require the use of an 8-position connector. This connector is optional. Use of any or all contacts is also optional. The contact positions and functions are defined by this specification and are not optional. The intent of this connector interface is to provide for FPD customization and added functionality needed for general desktop monitor applications.

Pin #	Description	Pin #	Description
1	VSYNC_OUT (from TMDS Receiver)	5	CTL2 (TMDS Control Bit 2)
2	HSYNC_OUT (from TMDS Receiver)	6	CTL1 (TMDS Control Bit 1)
3	TIMINGVALID	7	Ground/+12 VDC Return
4	Stereo Sync (TMDS Control Bit 3)	8	+ 12 VDC

Table 2-2: Pin Assignments for Optional 8-Contact Position Connector Interface

Note: TMDS Control Bit 0 is reserved for receiver PLL_SYNC.

3. Electrical Layer Specification

3.1 Transition Minimized Differential Signaling Interface

The TMDS interface is defined as a low voltage, low EMI, DC-balanced, signal skew tolerant, high speed, serial, differential data transmission scheme. The transmitter IC converts parallel video/graphics data from the host graphics controller and serializes the data, and transmits it over suitable transmission media up to 10 meters in length. The receiver converts the high speed serial data back to parallel data for use by the FPD timing interface logic.

The significance of this interface is that: (1) it only uses a small number of differential data pairs with all timing and control data embedded in data transmission, (2) it uses a transition minimized binary DC balanced coding for reliable, low-power, and high-speed data transmission, (3) it uses low-swing differential voltage which minimizes EMI, and (4) it can be implemented in low-cost scaleable CMOS technology available as a megacell or standard IC.

3.1.1 Overview

As the number of transactions from a variety of multimedia sources increases in desktop computing systems, reliable transmission of data at high-speed becomes essential. In particular, video data transmission between computer systems and flat panel displays (e.g., liquid crystal displays) needs higher speed interconnections for increasing bandwidth and video display color depth. Existing digital interconnection systems for such applications typically employ parallel data streams. As display resolutions and color depths increase the bandwidth requirements increase and the parallel interface suffers. The many parallel lines are noisy transmission lines which cause EMI radiation and unreliable data transmission. The large number of wires required for a parallel interface interfere each other making the video transmission difficult for long cable lengths. The TMDS data transmission system not only reduces the number of data channels required for high bandwidth data transmission, but also minimizes the EMI using-low swing differential voltage transmission with a new coding scheme for low power operation and simpler clocking methods. TMDS technology employs a DC balanced and transition minimized coding scheme for low power operation and a method of embedding timing and video control signals into the data streams. This further reduces the number of wires required and the attendant EMI radiation. TMDS technology can be applied to LCD's and other flat panel displays that require digital interfaces for reliable and low EMI radiation video transmission. In some remote display applications the distance between display and the host system can be as long as tens of meters. The transmission media can be fiber optics. Fiber optics is extremely tolerant to EMI susceptibility as compared to analog video signaling methods used for the CRT.

3.1.2 Logical Architecture

Below is a figure showing the block diagram of the TMDS transmitter with 8-bits of red, green, blue, and the various control signals. The transmitter outputs are coded, DC-balanced, high speed serial data streams and a reference clock.

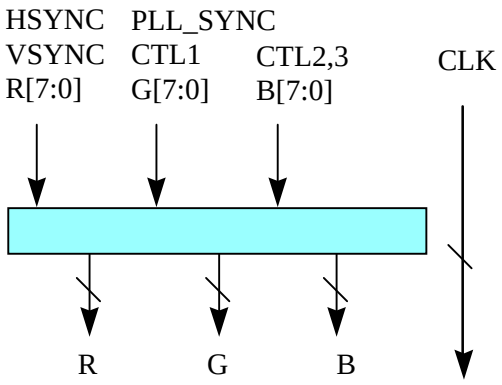


Figure 3-1: Simplified Block Diagram of an Interface with Clock and RGB

The TMDS transmission system is composed of three data lines and an accompanying reference clock line with a reduced differential logic swing and a DC-balanced data stream for transformer or capacitor coupling. Suitable signal transmission media can be either terminated wires, such as twin-axial cable or twisted pairs, or an optical fiber. In this case a video source provides the data stream to the TMDS transmitter IC which drives an amplifier for laser diode modulation. After the light signal passes through the fiber optic transmission media, a PIN receiver diode converts the light back to electrical signals which drive the TMDS receiver IC.

For the wire transmission case, the voltage swing is adjustable with 500 mV being the typical voltage swing. The 500 mV voltage swing is the single-ended signal voltage on one wire of the pair, the net signal on the wire pair is will be twice as large as the single-ended signal. The transmitter IC has an externally adjustable drive current level for the serial data stream. The VESA P&D and this specification suggest a default current drive of the maximum value of 12 mA. This ensures inter-operability for the largest number of transmitter and receiver combinations. For closed system applications, with low power consumption requirements and data transmission over short distances (e. g., a notebook computer), the transmitter IC drive level may be safely decreased. The TMDS transmission system as described uses a low voltage swing signal on only four terminated differential lines. The result is significantly reduced EMI radiation. A full parallel wire implementation radiates EMI because the non-terminated lines act as multiple antennas.

For unconditional FPDI-2 TMDS inter-operable TMDS transmission, the transmitter output drive current level should be set to the maximum of 12 mA. For limited-domain applications (e.g., notebooks) make the output current level adjustable so that the transmitter can accommodate various kinds of cable and receiver types with minimum power and EMI.

The voltage difference between AVCC (voltage supply to TMDS transmitter and receiver) and EXT_SWING (on TMDS transmitter only) pin determines the voltage swing of the differential signal pairs. Therefore, this adjustable low-voltage differential swing can be used for various cable lengths. A larger voltage swing can be used for longer cables, and a smaller voltage swing can be used for shorter cables. Sometimes larger voltage swings can cause noise on shorter cables due to transmission line effects. Therefore it is necessary to adjust the voltage swing accordingly to the length and type of the cable; the larger the voltage swing, the higher the power consumption and EMI of the system.

If the EXT_SWING pin is left unconnected, the internal voltage divider circuit will set the EXT_SWING pin at approximately 2.8 V when AVCC is at 3.3 V, producing approximately a 500 mV swing on the differential signal pairs. The differential voltage level swing for single ended systems is set approximately by the formula below:

$\mathbf{V_{SWING} = 0.5V \times (500\ \Omega / R_{EXT\_SWING})}$ where

V_{SWING} = Single Ended Differential voltage swing
R_{EXT_SWING} = External Resistor on EXT_SWING pin

R_{EXT_SWING}	Vs (Theoretical Calculation)
300 Ω	833 mV
400 Ω	625 mV
500 Ω	500 mV
600 Ω	417 mV
700 Ω	357 mV
800 Ω	313 mV
900 Ω	278 mV
1 KΩ	250 mV

Table 3-1: Theoretical Low-Voltage, Single-Ended Differential Swing Level Relative to R_{EXT_SWING}

As can be seen from the Figure 3-2, TMDS technology uses current drive to develop the low-voltage differential signal at the receiver side of the transmission line.

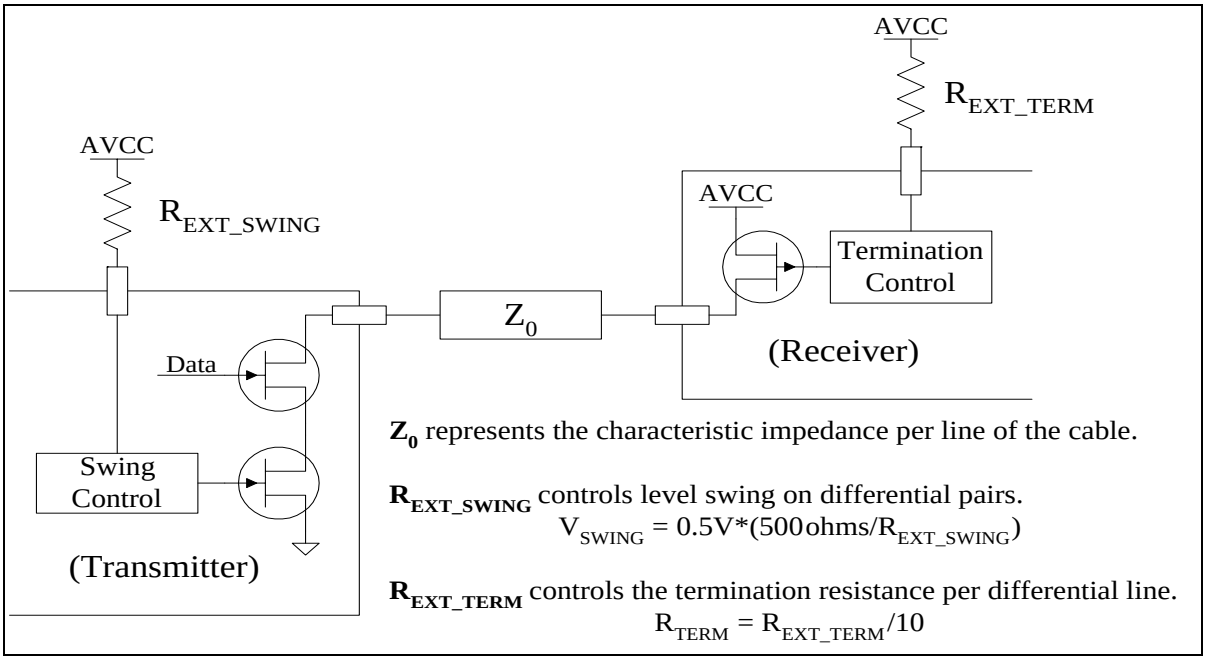
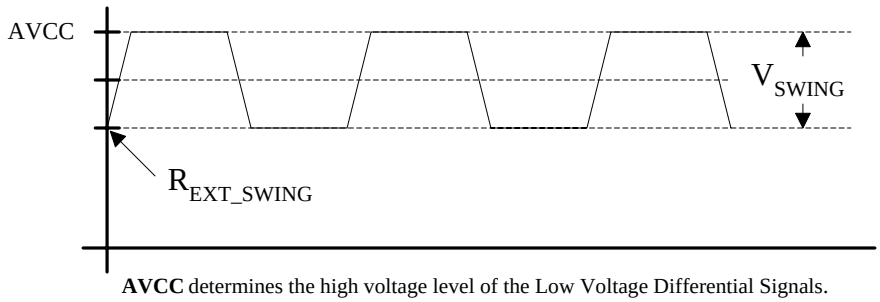


Figure 3-2: Transition Minimized Differential Voltage Swing Adjust



AVCC determines the high voltage level of the Low Voltage Differential Signals.

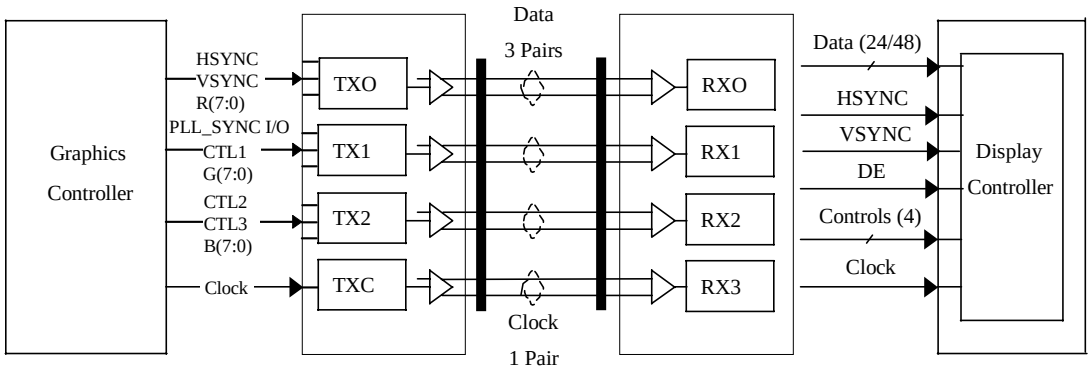
R_{EXT_SWING} determines the low voltage level of the Low Voltage Differential Signals. Therefore V_{SWING} is determined by

V_{SWING} = AVCC - (Voltage set by R_{EXT_SWING})

Figure 3-3: Single Ended Transition Minimized Differential Signal Adjustment

From Figure 3-3, it is evident that high voltage level of the low-voltage differential signals will be set by (AVCC), while the low voltage is adjustable with the low voltage level differential swing control circuit. Therefore, the low voltage differential voltage swing is adjustable by using a potentiometer (R_{EXT_SWING}) also illustrated.

Video signals are composed of three separate signals, typically RGB, along with two synchronization signals called HSYNC and VSYNC. Instead of having extra lines, these two SYNC signals are mixed with the RGB data in the encoder, thereby limiting the number of data pairs to three. The transition-controlled digital encoding will encode 8 bits of data, data enable (DE), and 2 bits of control signals. Control signals are allowed to change only during "blank" time when DE is low/inactive; keeping the levels of the control signals constant during active data area when DE is high.



Transition Minimized Differential Signals

Note: Each pair requires a current return, usually provided by a shield

Figure 3-4: System Environment Block Diagram Example

The TMDS system provides parallel interfaces to both the computer system display/graphics controller and the display devices. No modification to the existing system is required other than merely adding a TMDS transmitter and a TMDS receiver IC.

3.1.3 Summary

TMDS technology implements a high-speed video data transmission system capable of converting parallel video data stream and video display timing and control signals to three high-speed serial differential data pairs at speeds supporting high-resolution displays (e.g., 800x600 color pixels and above resolutions). In addition to enabling reliable and low EMI data transmission at high data transmission rates to support high resolution FPD's, a TMDS transmitter can be fabricated using scaleable CMOS technology. This technique lowers power consumption and makes the total silicon area small enough, such that it can be integrated into an ASIC as a megacell.

Shown below are samples of typical monitor update and refresh rates. These are general descriptions and are meant to denote general requirements. Other update and refresh rates are possible.

Addressability	*Frame Rate (Hz)*	*Pixel Clock (MHz)*	*Data Rate (Mbytes/s) Post Palette 4 bits/color*	*Data Rate (Mbytes/s) Post Palette 8 bits /color*
Update (Shadow Buffer in Monitor)				
640 x 480	60	25	37.5	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	30	23.59	35.38	70.77
1280 x 1024	30	40	60	120
2000 x 2000	30	120	180	360
1280 x 720	30	27.64	41.46	82.92
1920 x 1080	30	62.2	93.3	186.6
CRT Compatible Refresh Rates				
640 x 480	60	25	37.5	75
720 x 400	70	28	42	84
800 x 600	60	40	60	120
1024 x 768	60	65	97.5	195
1280 x 1024	60	112	168	336
1600 x 1200	75	250	375	750
2500 x 2000	75	384	575	1150
1280 x 720	60	77.5	116.25	232.5
1920 x 1080	30(Interlaced))	77.5	115.8	231.6

Table 3-2: Addressability Table

3.1.4 TMDS Transmitter

Note: This standard deals with the TMDS receiver mounted on the FPD module. This transmitter section, not part of this standard, is included for completeness only and does not constitute part of the FPDI-2 standard.

The transmitter is a serial link sharing a common clock. It accepts parallel data streams and converts them into serial data streams. The clock line does not bear the same frequency as the data rate on the transmission wire. Effective data transmission is 10 times the input clock frequency. One of the advantages of this scheme is power reduction.

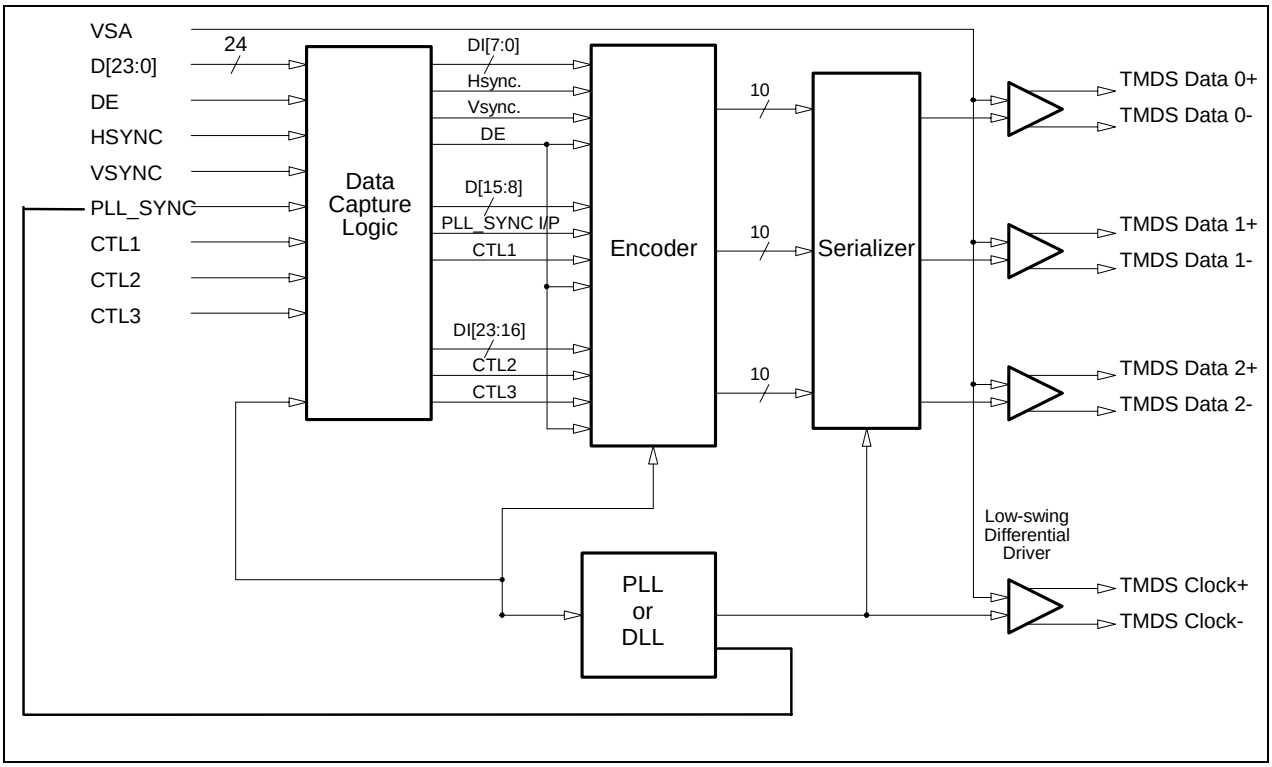


Figure 3-5: Video Transmitter IC Functional Block Diagram

Figure 3-5 shows a TMDS transmitter IC functional block diagram. The transmitter IC consists of a data capture logic block, data encoder block, serializer block, three high-speed differential data pair and differential clock line drivers. The encoder converts 8 bits of data into 10-bits of transition-minimized and DC-balanced data stream. The serializer takes 10 bit encoded data as an input and serializes it according to the differential data pair speed required for the display resolution. The differential data pair driver implements adjustable differential voltage swing drivers. It is an open drain driver which requires receiver-end termination with pull-up resistors matching the impedance of the interconnect system, as shown in Figure 3-6.

A TMDS interconnect system is composed of three data pairs and an accompanying clock pair with a reduced differential logic swing and a DC-balanced data stream for transformer or capacitor coupling. Signal transmission media can be either a terminated wires such as twinax cable or twisted pair or an optical fiber. In this case a driver and an amplifier for a laser diode and a PIN diode respectively are a signal load and a source for the video link.

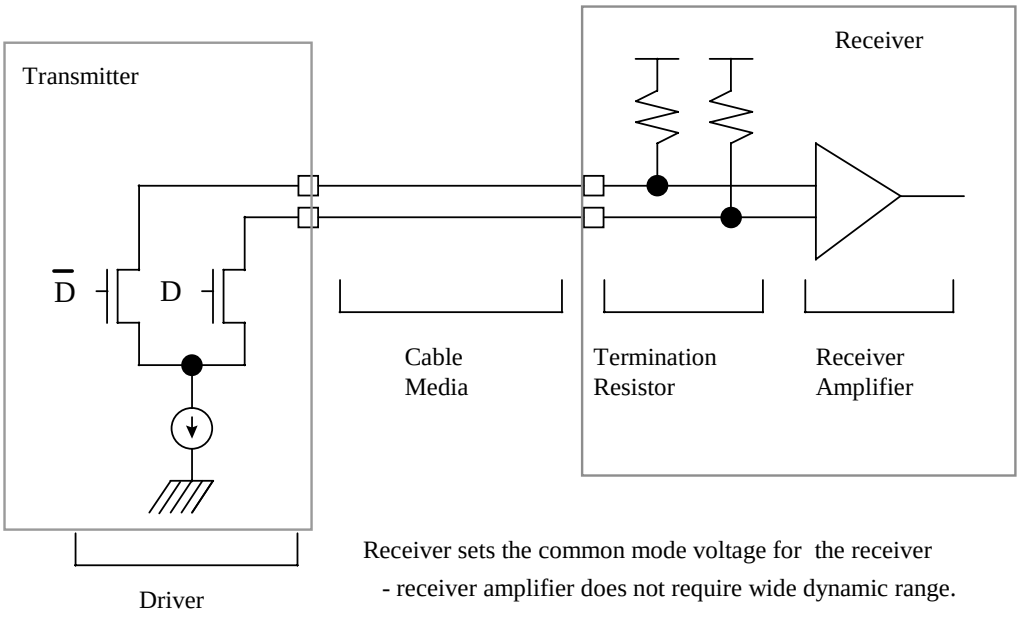


Figure 3-6: Typical CMOS Circuits for TMDS Driver

The voltage swing on the wire is adjustable but 1V is the typical differential voltage. Since its swing is differential on the wire, the net signal on the wire has a swing twice as large as the single-ended signal. Since a differential swing of 1 V is large enough to drive a receiver it might be possible to reduce the voltage swing depending on the quality and length of the wire without sacrificing its performance. In fact, since the voltage on the cable is developed by the current supplied by the receiver; with reduced swing, the power dissipation can be reduced. Also, with a larger characteristic impedance on the cable, it is possible to develop the same voltage with a reduced amount of current, further reducing the power. Therefore, it is very important to make the transmitter with an externally adjustable current level, in situations when a standard level is not used for maximum current reduction. Since the TMDS interconnect system uses a low-swing signal on only four terminated lines, there will be significantly reduced electromagnetic interference, (EMI) relative to fully parallel interfaces.

Video signals are composed of three separate signals, typically RGB, along with two synchronization signals called HSYNC and VSYNC. Instead of having extra lines, those two SYNC signals are mixed with the RGB data in the coder, thereby, limiting the number of data wires to three. As shown in Figure 3-5, each encoder unit will encode 8 bits of data, data enable (DE), and two bits of control signals. Three functionally identical encoders are used to transmit all data and control signals. Control signals are assumed to change only during “blank” time when DE is low/inactive; therefore, the levels of the control signals are assumed to be constant within the active data area when DE is high.

There are two ways to encode the control signals when DE is low. The first method uses edge transitions (rise/fall) of the control signals and the second method uses the levels (high/low) of control signals. TMDS encoding uses the latter, encoding levels of control signals. The proprietary encoding method guarantees transition-minimized and DC-balanced character sets for the data. Four special characters are used to encode the control signals. A total of 260 (256 in-band data sets and 4 out-of-band special character sets) 10-bit characters are required for each encoder as shown in the following table.

Data [7:0]	DE	Control 1	10 bit code
1 to 256	High	-	C_1-C_{256}
-	Low	Low	C_{257}
-	Low	Low	C_{258}
-	Low	High	C_{259}
-	Low	High	C_{260}

Table 3-3: Encoder Mapping for a Single Differential Data Pair

The encoder generates one of the four kinds of special characters according to the level of HSYNC and VSYNC (or 2-control inputs) when DE is LOW. When DE is high, 8-bit data is converted to 10-bit transition minimized and DC-balanced in-band data.

3.1.5 TMDS Receiver Summary

The receiver recovers the transmitter's data stream using the differential pixel clock provided with the three serial data streams. Since there is no assumption on the related timing between clock and three data lines, the receiver blindly oversamples the data with the multiphase clocks and digital logic extracts data in later stages in the digital domain. The multiphase clocks are generated in the PLL from the reference clock that is brought with the data lines. Since only one datum is selected as an output out of the three sampled data, only one sampler will be activated after correct timing is determined. The remaining two will be deactivated until the next timing adjustment is needed, resulting in power-saving. Since the three differential data pairs might have different line lengths, the correct sampling time will be different from differential data pair to differential data pair. The correct sampling time is individually obtained and correct word is assembled from three data to form a parallel data from the information of intermittent synchronizing patterns.

Figure 3-7 is a TMDS receiver functional block diagram. The TMDS receiver chip consists of three differential receiver circuits, a data recovery block, a decoder block, and panel interface logic. In normal application, the host graphics controller may use different clock frequencies for different modes, therefore, the receiver clock should normally be derived from the clock transmitted by the transmitter chip which goes to the TMDS Clock + and TMDS Clock - pins.

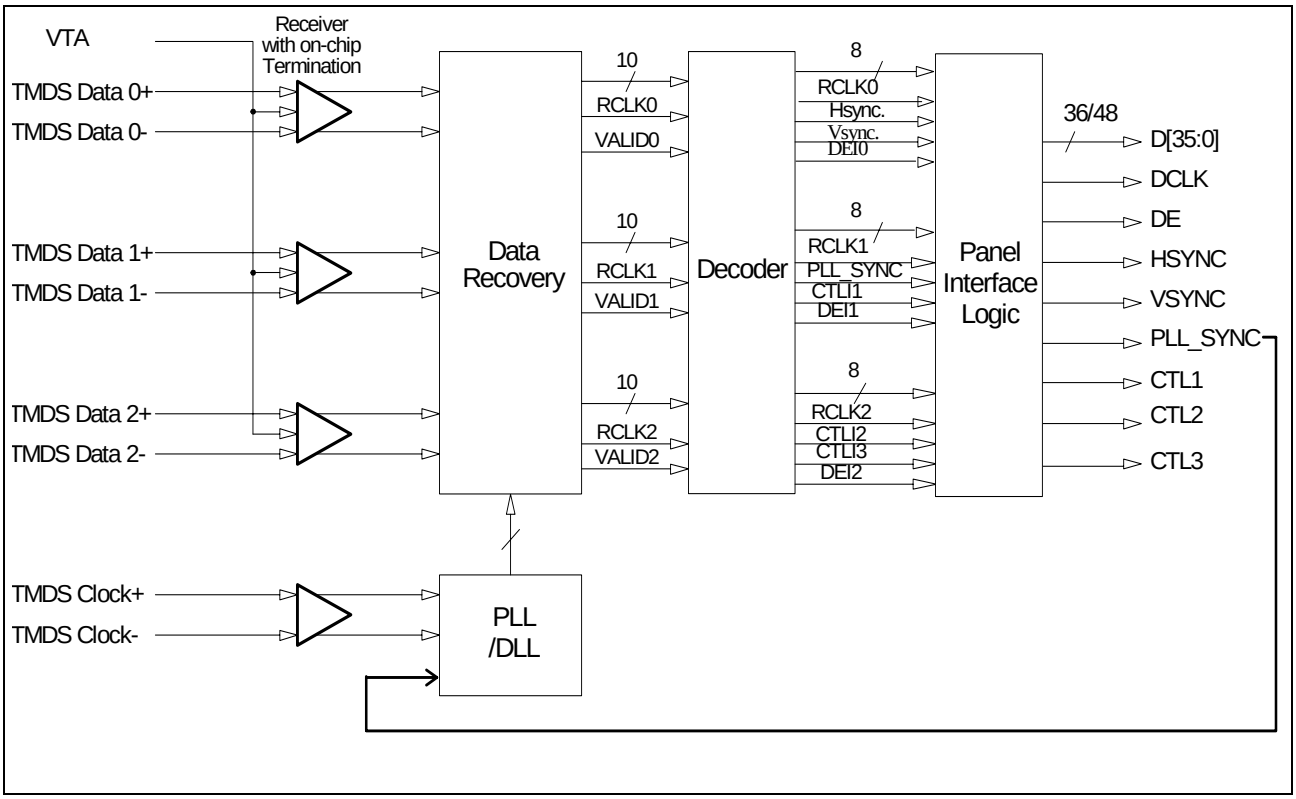


Figure 3-7: Video Receiver IC Functional Block Diagram

There can be inter-channel timing skew among the multiple channel data recovery block because the line length of different data transmission channel can be slightly different from differential data pair to differential data pair. The inter-channel timing skew can produce up to 1-cycle time mismatch.

The TMDS interface defines a logical architecture, an encoding scheme, and a scaleable physical interface based on a low-voltage differential swing current-mode circuit technology. Each color information is carried with an 8-bit wide differential data pair. Each differential data pair carries up to eight bits of data. Three control signals can be used for implementation-dependent or user-defined signals.

3.1.6 Relationship Between Controller's Output Data and Input Data Clock

The following vertical and horizontal timing diagrams for a typical flat panel display graphics controller demonstrates the relationship between the controller's output data (D[23:0]) and the transmitter interface input data clock (IDCK).

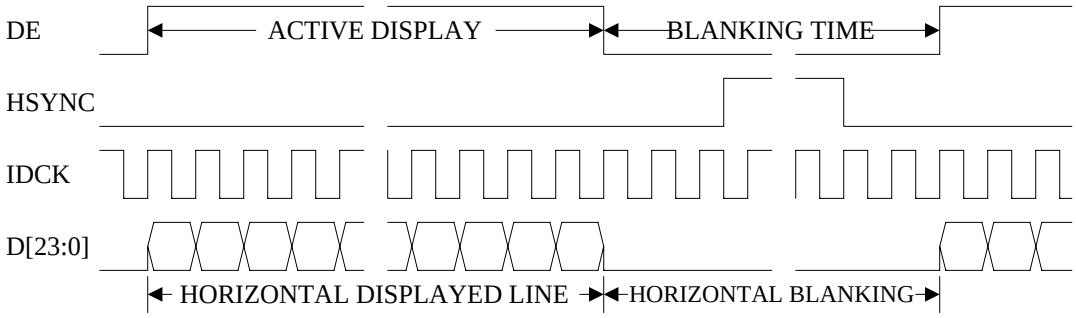


Figure 3-8: Horizontal Input Timing at Type B Interface

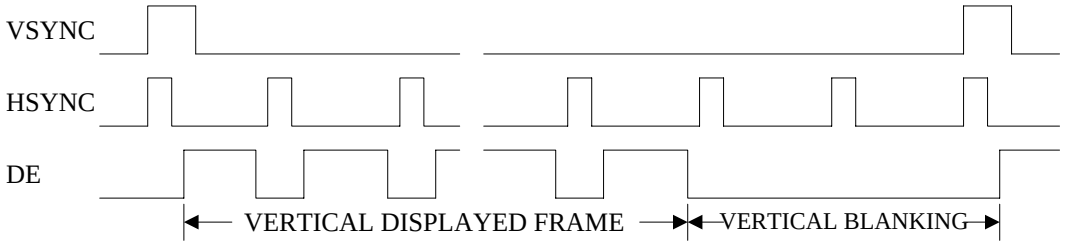


Figure 3-9: Vertical Input Timing at Type B Interface

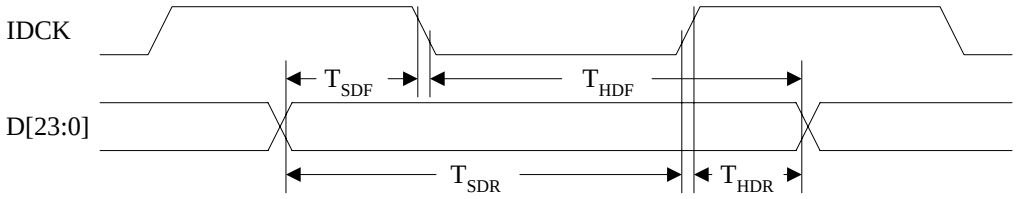


Figure 3-10: Input Data Timing with Respect to IDCK at Type B Interface

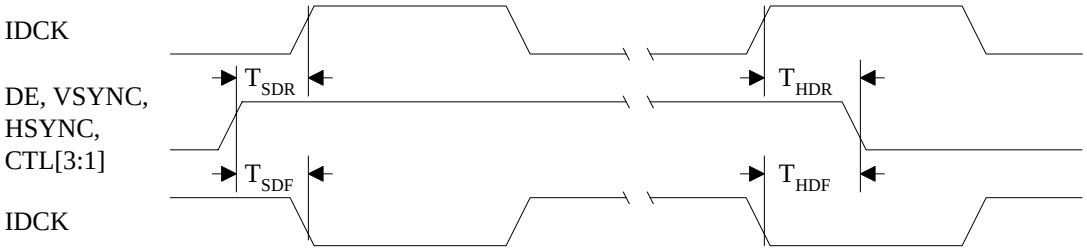


Figure 3-11: Control Signal Timing with Respect to IDCK at Type B Interface

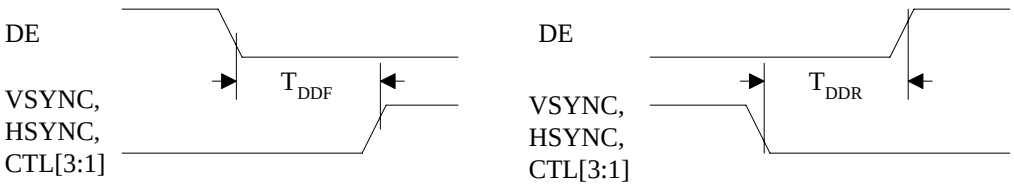


Figure 3-12: Control Signals with Respect to DE Timing

Signal Name	Type	Description
HSYNC	In	Horizontal Sync Input Control Signal
VSYNC	In	Vertical Sync Input Control Signal
PLL_SYNC	In	General Input Control Signal 0 reserved for PLL_SYNC
CTL1	In	General Input Control Signal 1
CTL2	In	General Input Control Signal 2
CTL3	In	General Input Control Signal 3
DE	In	Input Data Enable. This signal qualifies the active data area. DE is always required and must be high for active video time and low during blanking.
IDCK	In	Input Data clock. Maximum frequency is 160 MHz. Input data can be valid either on falling edge of IDCK or on rising edge of IDCK as selected by DEDGE pin. IDCK must be a continuous free running clock with a minimum 40/60 or maximum 60/40 duty cycle.
DEDGE	In	Data Latching Edge for input data. A low level indicates that input data (D[23:0]) must be latched on falling edge of IDCK while a high level (3.3V) indicates that input data must be latched on rising edge of IDCK.
CEDGE	In	Control Latching Edge for input data enable (DE) and control signals (HSYNC, VSYNC, CTL[3-0]). A low level indicates that input data enable and control signals must be latched on falling edge of IDCK while high level (3.3V) indicates that input data enable and control signals must be latched on rising edge of IDCK.
Data	In	Input data is synchronized with input data clock (IDCK). Data can be latched on the rising or falling edge of IDCK depending upon whether DEDGE is high or low respectively.

Table 3-4: Signal Name Description

The clock line does not bear the same frequency as the data rate on the transmission wire. A $1/10^{th}$ signal frequency of the input maximum parallel serial data rate is transmitted.

In the above diagram DE, HSYNC, and VSYNC signals are shown with positive polarity. DE must always have positive polarity, whereas HSYNC, VSYNC and other control signals (CTL[3:1]) can have either positive or negative polarity. DE must always be connected and must go low for a minimum of 10 IDCK cycles, even for DSTN panels. The interface relies on the polarity and timing of DE and not on the control signals.

DE signal is used to differentiate between “active” display areas and “non-active” display areas (“blank” time). The interface requires an active high Display Enable (DE) signal. There is no restriction on the polarity of the control signals; however, the change in polarity for the control signals is recognized only during “blank” time.

Input data D[23:0] and DE are normally generated on the rising edge of IDCK since most displays latch data on the falling edge of shift clock. For the interface, D[23:0] and DE can be latched on the rising or falling edge of IDCK

depending upon the setting of DEDGE and CEDGE respectively. The DEDGE pin controls the latching of data D[23:0]. When DEDGE is low, D[23:0] is latched using the falling edge of IDCK. When DEDGE is high, D[23:0] is latched using the rising edge of IDCK. The CEDGE pin controls the latching of control signals DE, HSYNC, VSYNC, CTL[3:1]. When CEDGE is low, DE and the other control signals are latched using the falling edge of IDCK. When CEDGE is high, DE and the other control signals are latched using the rising edge of IDCK.

The timing between D[23:0] and DE with respect to IDCK falling/rising edge, requires close attention. Timing considerations between the other control signals and IDCK are not as restrictive since the display timing requirements are relaxed.

For most display graphics controllers, D[23:0] and DE have the same or similar timing; therefore, DEDGE and CEDGE should to be set at the same level. However, if D[23:0] is to be latched using the rising edge of IDCK and DE using the falling edge of IDCK, then DE will be latched half a clock cycle earlier with respect to D[23:0]. Subsequently, DE and D[23:0] are synchronized at the output of the data capture logic.
IDCK must always be free running with nominally 50/50 duty cycle and less than 5% jitter, even for DSTN panels.

3.2 Transition-Controlled Digital Encoding and Signal Transmission

The encoder is required to encode eight bits of data during active display time, and DE plus two bits of control signals during "blank" time. The encode is required to generate 10-bit, DC-balanced and transition minimized codes during active display time. Control signals are assumed to change only during "blank" time when DE is low/inactive; therefore, the levels of the control signals are assumed to be constant during active data area when DE is high.

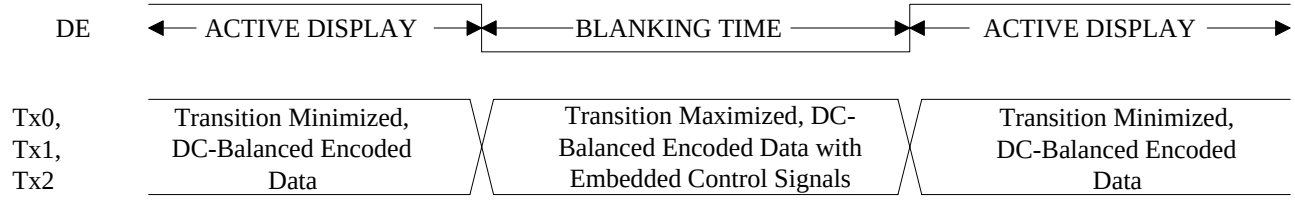


Figure 3-13: TMDS Interface Transition Minimization Timing Diagram

The encoding method guarantees transition-minimized DC-balanced 256 level data codes during active time during "blank" time, which supports high-speed, low-voltage differential, low power, and low EMI operation. The special characters are used for the level encoding of the control signals.

Encoded are eight bits of data, plus DE, plus two bits of control signals. The TMDS encoding method encodes the levels of control signals when DE is low. The encoding method guarantees the number of signal edge transitions in any eight bits of data are minimized to no more than three transitions and a DC-balanced character set is generated for the data. Four kinds of special characters are used for the level encoding of the control signals. A total of 260 (256 in-band data set and four, out-of-band special character set) 10-bit characters are conveyed for each encoded parallel data stream.

Data [7:0]	**DE**	**VSYNC**	**HSYNC**	**10 bit code**
1 to 256	High	-	-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 3-5: Encoded Data Components for TMDS Data 0 Differential Data Pair

Data [15:8]	DE	PLL_SYNC	CTL1	10 bit code
1 to 256	High	-	-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 3-6: Encoded Data Components for TMDS Data 1 Differential Data Pair

Data [24:16]	DE	CTL2	CTL3	10 bit code
1 to 256	High	-	-	C_1-C_{256}
-	Low	L	L	C_{257}
-	Low	L	H	C_{258}
-	Low	H	L	C_{259}
-	Low	H	H	C_{260}

Table 3-7: Encoded Data Components for TMDS Data 2 Differential Data Pair

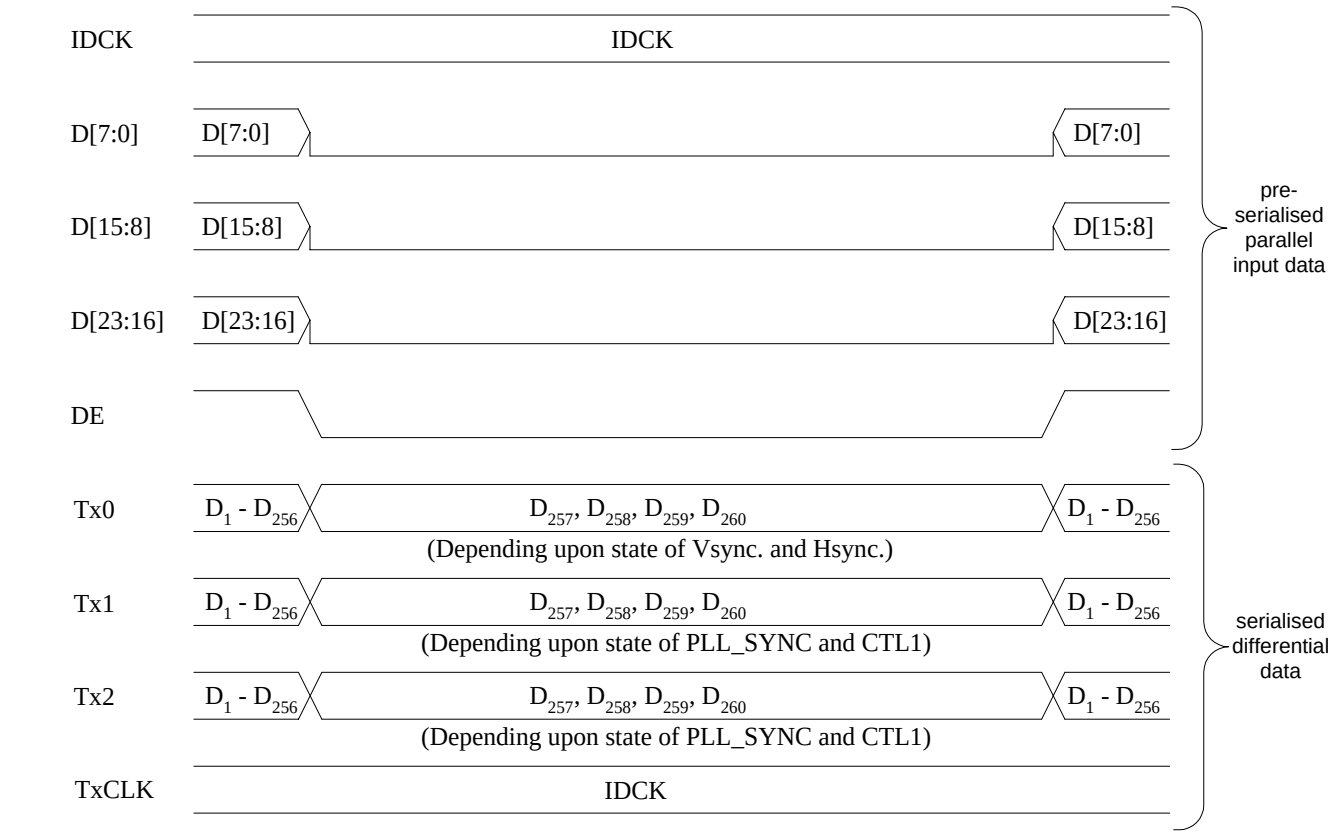


Figure 3-14: Encoded Timing Diagram for All Differential Data Pair

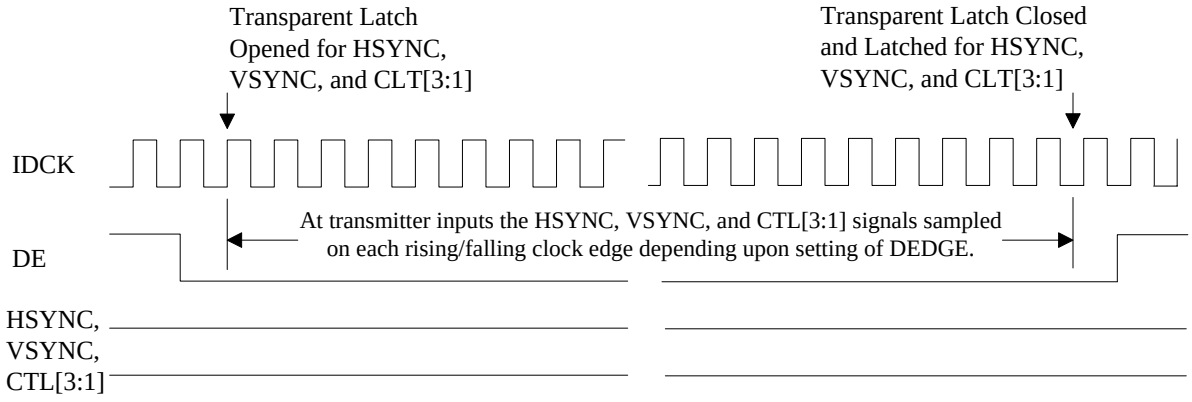


Figure 3-15: HSYNC, VSYNC, and CTL[3:1] Sampling Relative to Clock Edge

A compliant implementation must generate one of the four kinds of special characters according to the level of HSYNC and VSYNC (or 3 control inputs) when DE is low. When DE is high, eight-bit data is converted to ten-bit transition minimized and DC-balanced in-band data. Four kinds of special characters are used for the level encoding of the control signal.

A compliant implementation is required to generate the ten-bit DC-balanced codes. Control signals are assumed to change only during "blank" time when DE is low/inactive; therefore, the levels of the control signals are required to be constant during active data area when DE is high.

A compliant implementation is required to generate one of four kinds of special characters depending upon the level of HSYNC and VSYNC or Control [3:1], when DE is low. When DE is high, eight-bit data is converted to ten-bit coded RGB data in each of four channels at the transmitter.

4. Digital Data Formats

4.1 Summary Table

The TMDS link between the flat panel graphics controller and the flat panel display can be regarded more or less as a "pipe" i.e., whatever is driven by the graphics controller into the inputs of the transmitter will be entirely reproduced at the outputs of the receiver to which the flat panel is attached. This creates a need to ensure that the format of the data sent across the TMDS interface remain consistent so that differing combinations of graphics controllers and flat panels may be assembled without undue difficulty.

A graphics controller that is meant to be compliant with FPDI-2 must support all of the data formats summarized in Table 4-1 following. A flat panel display that is meant to be compliant with FPDI-2 need support only one data format, but it must be one of those summarized in Table 4-1.

Table 4-1 summarizes the standard data formats. The table lists monochrome dual-scan STN with eight-bits each to the upper and lower sub-panel, color single scan STN with single sixteen-bits, color dual scan STN with eight-bits each to the upper and lower sub-panel, color STN dual scan with twelve-bits each to the upper and lower sub-panel, color TFT with six-bits per primary color, and color TFT with eight-bits per primary color.

Bit Number	8-Over-8 Mono STN-DD	16-Bit Color STN-SS	8-Over-8 Color STN-DD	12-Over-12 Color STN-DD	18-Bit Color TFT	24-Bit Color TFT
0	UD7	R0	UR0	UR0	–	B0
1	UD6	G0	UG0	UG0	–	B1
2	UD5	B0	UB0	UB0	B0	B2
3	UD4	R1	UR1	LR0	B1	B3
4	UD3	G1	LR0	LG0	B2	B4
5	UD2	B1	LG0	LB0	B3	B5
6	UD1	R2	LB0	UR1	B4	B6
7	UD0	G2	LR1	UG1	B5	B7
8	LD7	B2	UG1	UB1	–	G0
9	LD6	R3	UB1	LR1	–	G1
10	LD5	G3	UR2	LG1	G0	G2
11	LD4	B3	UG2	LB1	G1	G3
12	LD3	R4	LG1	UR2	G2	G4
13	LD2	G4	LB1	UG2	G3	G5
14	LD1	B4	LR2	UB2	G4	G6
15	LD0	R5	LG2	LR2	G5	G7
16	–	SHFCLK	SHFCLK	LG2	–	R0
17	–	–	–	LB2	–	R1
18	–	–	–	UR3	R0	R2
19	–	–	–	UG3	R1	R3
20	–	–	–	UB3	R2	R4
21	–	–	–	LR3	R3	R5
22	–	–		LG3	R4	R6
23	–	–		LB3	R5	R7
Pixels per SHFCLK	16	16/3	16/3	8	1	1
Minimum Req'd for P&D			Yes	Yes	Yes	Yes

Table 4-1: Data Format Summary

4.2 Per Transfer Detail Tables

The following six pages provide tables and on-screen scan illustrations that show the pattern followed for the data in each of the six-above-listed data formats.

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	upper pixel 7	upper pixel 15	...
Bit 1	upper pixel 6	upper pixel 14	...
Bit 2	upper pixel 5	upper pixel 13	...
Bit 3	upper pixel 4	upper pixel 12	...
Bit 4	upper pixel 3	upper pixel 11	...
Bit 5	upper pixel 2	upper pixel 10	...
Bit 6	upper pixel 1	upper pixel 9	...
Bit 7	upper pixel 0	upper pixel 8	...
Bit 8	lower pixel 7	lower pixel 15	...
Bit 9	lower pixel 6	lower pixel 14	...
Bit 10	lower pixel 5	lower pixel 13	...
Bit 11	lower pixel 4	lower pixel 12	...
Bit 12	lower pixel 3	lower pixel 11	...
Bit 13	lower pixel 2	lower pixel 10	...
Bit 14	lower pixel 1	lower pixel 9	...
Bit 15	lower pixel 0	lower pixel 8	...
Bit 16			
Bit 17			
Bit 18			
Bit 19			
Bit 20			
Bit 21			
Bit 22			
Bit 23			

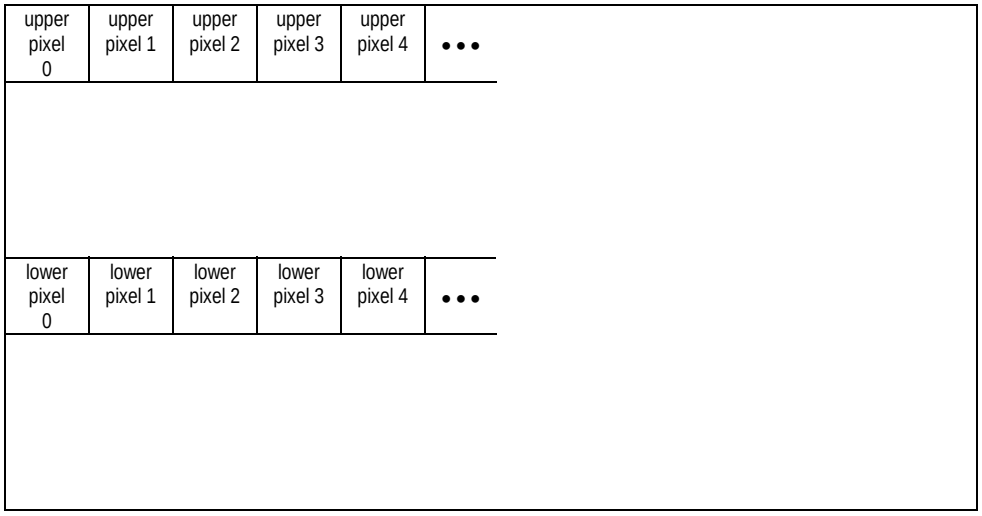


Table 4-2: Data Format for Monochrome, Dual-Scan STN with 8 bits each to Upper and Lower Sub-panel

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	
Bit 0	pixel 0 red	pixel 5 green	pixel 10 blue	...
Bit 1	pixel 0 green	pixel 5 blue	pixel 11 red	...
Bit 2	pixel 0 blue	pixel 6 red	pixel 11 green	...
Bit 3	pixel 1 red	pixel 6 green	pixel 11 blue	...
Bit 4	pixel 1 green	pixel 6 blue	pixel 12 red	...
Bit 5	pixel 1 blue	pixel 7 red	pixel 12 green	...
Bit 6	pixel 2 red	pixel 7 green	pixel 12 blue	...
Bit 7	pixel 2 green	pixel 7 blue	pixel 13 red	...
Bit 8	pixel 2 blue	pixel 8 red	pixel 13 green	...
Bit 9	pixel 3 red	pixel 8 green	pixel 13 blue	...
Bit 10	pixel 3 green	pixel 8 blue	pixel 14 red	...
Bit 11	pixel 3 blue	pixel 9 red	pixel 14 green	...
Bit 12	pixel 4 red	pixel 9 green	pixel 14 blue	...
Bit 13	pixel 4 green	pixel 9 blue	pixel 15 red	...
Bit 14	pixel 4 blue	pixel 10 red	pixel 15 green	...
Bit 15	pixel 5 red	pixel 10 green	pixel 15 blue	...
Bit 16				
Bit 17				
Bit 18				
Bit 19				
Bit 20				
Bit 21				
Bit 22				
Bit 23				

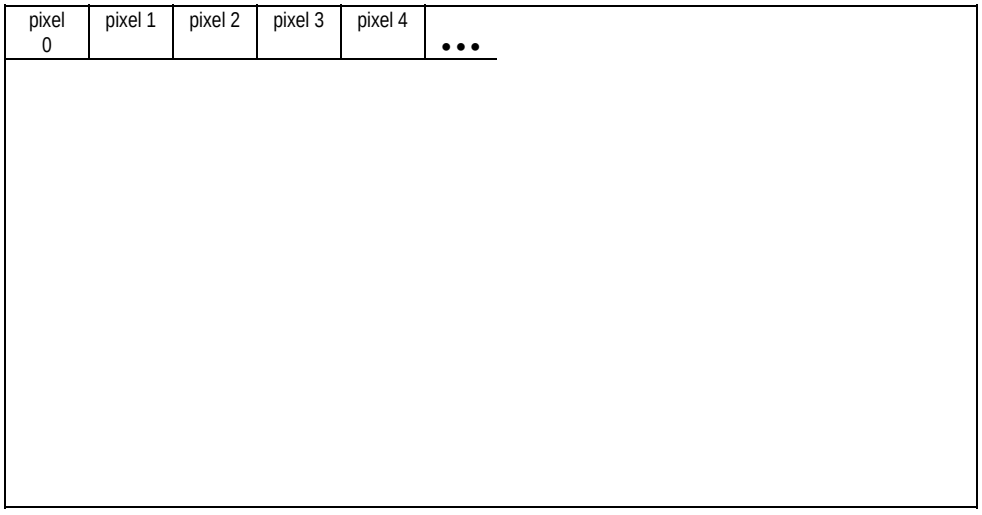


Table 4-3: Data Format for Color, Single-Scan STN with 16 bits

Bus Signal	1st Transfer	2nd Transfer	3rd Transfer	
Bit 0	upper pixel 0 red	upper pixel 2 blue	upper pixel 5 green	...
Bit 1	upper pixel 0 green	upper pixel 3 red	upper pixel 5 blue	...
Bit 2	upper pixel 0 blue	upper pixel 3 green	upper pixel 6 red	...
Bit 3	upper pixel 1 red	upper pixel 3 blue	upper pixel 6 green	...
Bit 4	lower pixel 0 red	lower pixel 2 blue	lower pixel 5 green	...
Bit 5	lower pixel 0 green	lower pixel 3 red	lower pixel 5 blue	...
Bit 6	lower pixel 0 blue	lower pixel 3 green	lower pixel 6 red	...
Bit 7	lower pixel 1 red	lower pixel 3 blue	lower pixel 6 green	...
Bit 8	upper pixel 1 green	upper pixel 4 red	upper pixel 6 blue	...
Bit 9	upper pixel 1 blue	upper pixel 4 green	upper pixel 7 red	...
Bit 10	upper pixel 2 red	upper pixel 4 blue	upper pixel 7 green	...
Bit 11	upper pixel 2 green	upper pixel 5 red	upper pixel 7 blue	...
Bit 12	lower pixel 1 green	lower pixel 4 red	lower pixel 6 blue	...
Bit 13	lower pixel 1 blue	lower pixel 4 green	lower pixel 7 red	...
Bit 14	lower pixel 2 red	lower pixel 4 blue	lower pixel 7 green	...
Bit 15	lower pixel 2 green	lower pixel 5 red	lower pixel 7 blue	...
Bit 16				
Bit 17				
Bit 18				
Bit 19				
Bit 20				
Bit 21				
Bit 22				
Bit 23				

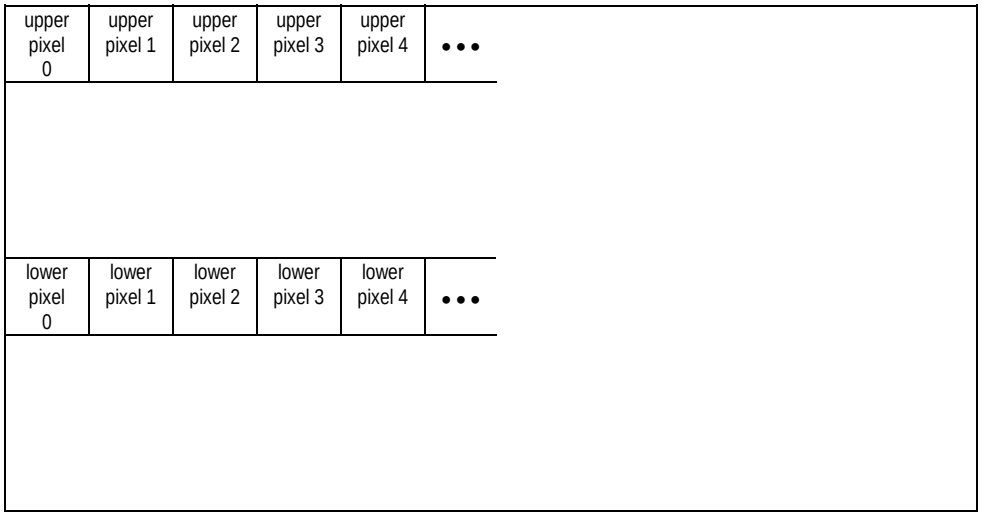


Table 4-4: Data Format for Color, Dual-Scan STN with 8 bits each to Upper and Lower Sub-panel

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	upper pixel 0 red	upper pixel 4 red	...
Bit 1	upper pixel 0 green	upper pixel 4 green	...
Bit 2	upper pixel 0 blue	upper pixel 4 blue	...
Bit 3	lower pixel 0 red	lower pixel 4 red	...
Bit 4	lower pixel 0 green	lower pixel 4 green	...
Bit 5	lower pixel 0 blue	lower pixel 4 blue	...
Bit 6	upper pixel 1 red	upper pixel 5 red	...
Bit 7	upper pixel 1 green	upper pixel 5 green	...
Bit 8	upper pixel 1 blue	upper pixel 5 blue	...
Bit 9	lower pixel 1 red	lower pixel 5 red	...
Bit 10	lower pixel 1 green	lower pixel 5 green	...
Bit 11	lower pixel 1 blue	lower pixel 5 blue	...
Bit 12	upper pixel 2 red	upper pixel 6 red	...
Bit 13	upper pixel 2 green	upper pixel 6 green	...
Bit 14	upper pixel 2 blue	upper pixel 6 blue	...
Bit 15	lower pixel 2 red	lower pixel 6 red	...
Bit 16	lower pixel 2 green	lower pixel 6 green	...
Bit 17	lower pixel 2 blue	lower pixel 6 blue	...
Bit 18	upper pixel 3 red	upper pixel 7 red	...
Bit 19	upper pixel 3 green	upper pixel 7 green	...
Bit 20	upper pixel 3 blue	upper pixel 7 blue	...
Bit 21	lower pixel 3 red	lower pixel 7 red	...
Bit 22	lower pixel 3 green	lower pixel 7 green	...
Bit 23	lower pixel 3 blue	lower pixel 7 blue	...

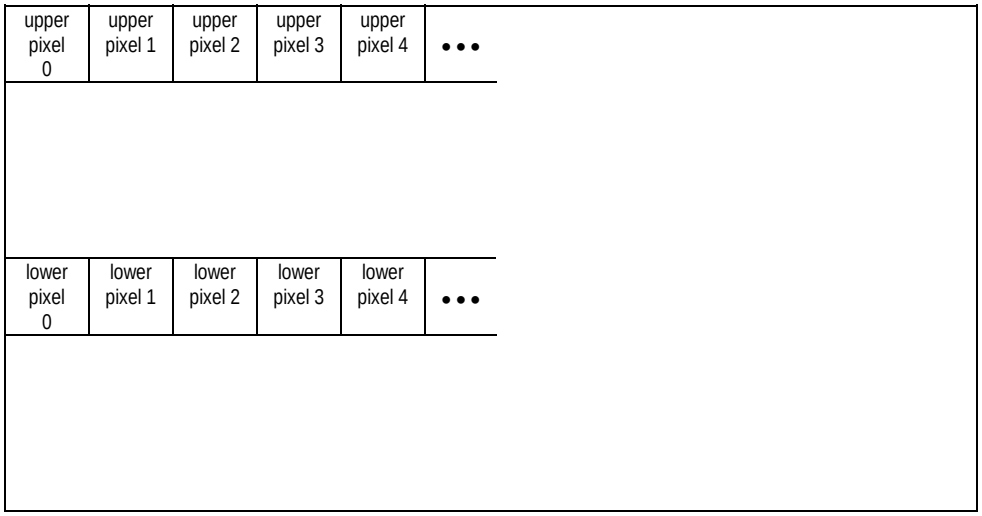


Table 4-5: Data Format for Color, Dual-Scan STN with 12 bits each to Upper and Lower Sub-panel

Bus Signal	1st Transfer	2nd Transfer	
Bit 0			
Bit 1			
Bit 2	pixel 0 blue bit 0	pixel 1 blue bit 0	...
Bit 3	pixel 0 blue bit 1	pixel 1 blue bit 1	...
Bit 4	pixel 0 blue bit 2	pixel 1 blue bit 2	...
Bit 5	pixel 0 blue bit 3	pixel 1 blue bit 3	...
Bit 6	pixel 0 blue bit 4	pixel 1 blue bit 4	...
Bit 7	pixel 0 blue bit 5	pixel 1 blue bit 5	...
Bit 8			
Bit 9			
Bit 10	pixel 0 green bit 0	pixel 1 green bit 0	...
Bit 11	pixel 0 green bit 1	pixel 1 green bit 1	...
Bit 12	pixel 0 green bit 2	pixel 1 green bit 2	...
Bit 13	pixel 0 green bit 3	pixel 1 green bit 3	...
Bit 14	pixel 0 green bit 4	pixel 1 green bit 4	...
Bit 15	pixel 0 green bit 5	pixel 1 green bit 5	...
Bit 16			
Bit 17			
Bit 18	pixel 0 red bit 0	pixel 1 red bit 0	...
Bit 19	pixel 0 red bit 1	pixel 1 red bit 1	...
Bit 20	pixel 0 red bit 2	pixel 1 red bit 2	...
Bit 21	pixel 0 red bit 3	pixel 1 red bit 3	...
Bit 22	pixel 0 red bit 4	pixel 1 red bit 4	...
Bit 23	pixel 0 red bit 5	pixel 1 red bit 5	...

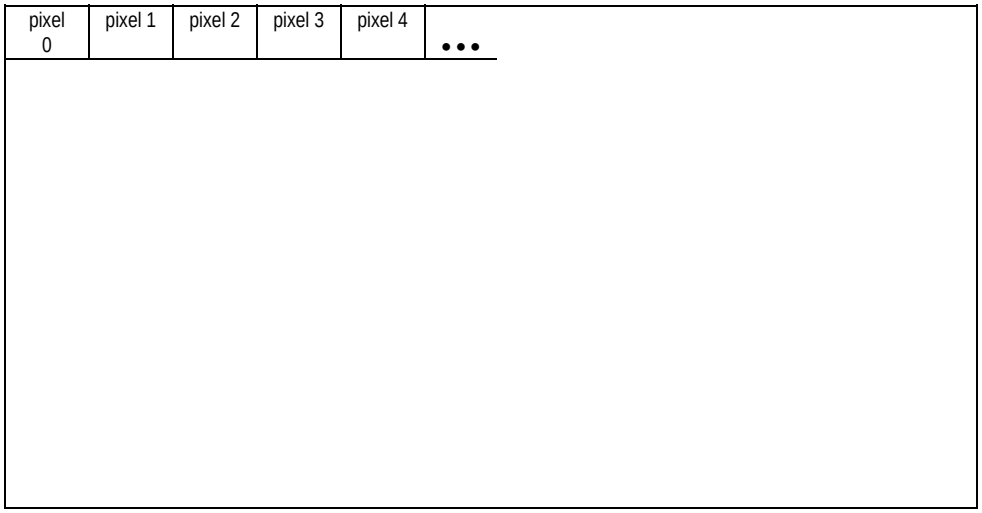


Table 4-6: Data Format for Color, TFT with 6 bits Per Primary Color

Bus Signal	1st Transfer	2nd Transfer	
Bit 0	pixel 0 blue bit 0	pixel 1 blue bit 0	...
Bit 1	pixel 0 blue bit 1	pixel 1 blue bit 1	...
Bit 2	pixel 0 blue bit 2	pixel 1 blue bit 2	...
Bit 3	pixel 0 blue bit 3	pixel 1 blue bit 3	...
Bit 4	pixel 0 blue bit 4	pixel 1 blue bit 4	...
Bit 5	pixel 0 blue bit 5	pixel 1 blue bit 5	...
Bit 6	pixel 0 blue bit 6	pixel 1 blue bit 6	...
Bit 7	pixel 0 blue bit 7	pixel 1 blue bit 7	...
Bit 8	pixel 0 green bit 0	pixel 1 green bit 0	...
Bit 9	pixel 0 green bit 1	pixel 1 green bit 1	...
Bit 10	pixel 0 green bit 2	pixel 1 green bit 2	...
Bit 11	pixel 0 green bit 3	pixel 1 green bit 3	...
Bit 12	pixel 0 green bit 4	pixel 1 green bit 4	...
Bit 13	pixel 0 green bit 5	pixel 1 green bit 5	...
Bit 14	pixel 0 green bit 6	pixel 1 green bit 6	...
Bit 15	pixel 0 green bit 7	pixel 1 green bit 7	...
Bit 16	pixel 0 red bit 0	pixel 1 red bit 0	...
Bit 17	pixel 0 red bit 1	pixel 1 red bit 1	...
Bit 18	pixel 0 red bit 2	pixel 1 red bit 2	...
Bit 19	pixel 0 red bit 3	pixel 1 red bit 3	...
Bit 20	pixel 0 red bit 4	pixel 1 red bit 4	...
Bit 21	pixel 0 red bit 5	pixel 1 red bit 5	...
Bit 22	pixel 0 red bit 6	pixel 1 red bit 6	...
Bit 23	pixel 0 red bit 7	pixel 1 red bit 7	...

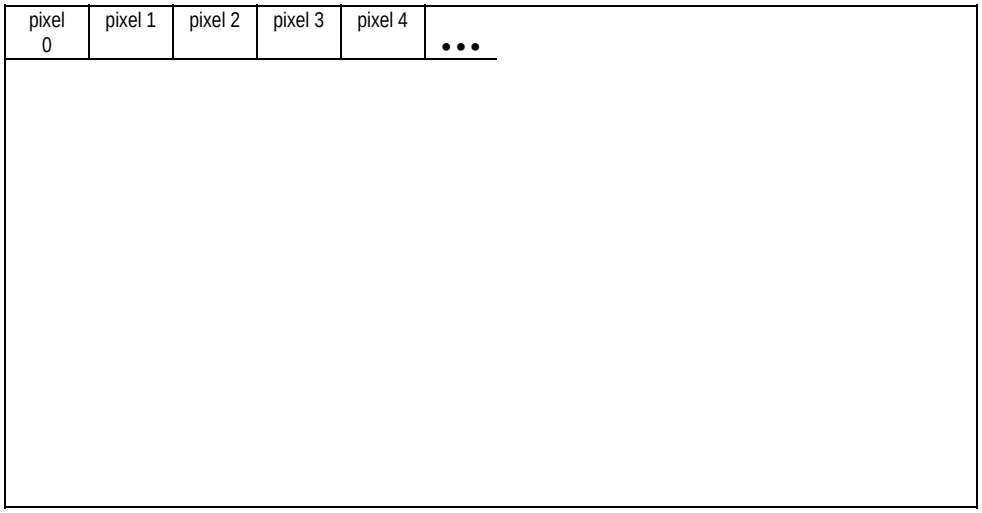


Table 4-7: Data Format for Color, TFT with eight bits per Primary Color

5. Initialization Control Communication

Implementation of initialization control is optional, but the connector interface pins defined for this function shall not be used for any other purpose.

If initialization control is implemented, then the DDC2 protocol defined in the VESA Display Data Channel (DDC), Version 3 Standard shall be used to transfer capability and configuration data from the FPD to the graphic sub-system.

The data consists of 256 bytes with a format defined in the VESA Extended Display Identification Data (EDID), Version 3, Standard.

DDC2 covers several protocol., This standard does not define a specific protocol.

- DDC2B Base level, allows graphic sub-system to request and receive EDID data.
- DDC2B+ Adds base level plus bi-directional communications capability.
- DDC2AB A full ACCESS.bus implementation.

6. Power Sequencing

6.1 Introduction

Two power sequencing cases are documented in this standard. For the notebook case, the power to the of the display is sequenced by the video/graphics subsystem. In this case the display power is cycled with the entire system. The second case is the monitor. In this case, the sequencing combinations are more complex since the host and monitor power may be power cycled at different times or even hot-plugged. The intent of this section is documentation of the signals and connector interface, while allow enough options for product differentiation at the FPD and monitor level.

6.2 Notebook Case

Figure 6-1 presents a block diagram of the manner in which a flat panel graphics controller would be interconnected with a flat panel. The graphics controller may have the TMDS transmitter either embedded or as a separate, discrete part.

Since use of a 256-byte, I^2C memory device to carry EDID data structure at address A6h describing the flat panel is optional, the graphics controller may or may not use this feature in order to learn of the display's characteristics. Note: information needed to correctly program the graphics controller for the particular flat panel may be contained elsewhere.

As with current flat panel notebook display interfacing practices, the graphics controller (or other logic operating under its influence) would be responsible for directly enabling and disabling the provision of both VDD1 and VDD2, VCONT and backlight power in the correct order with appropriate time delays. The control of these power supplies is not carried out through the TMDS interface.

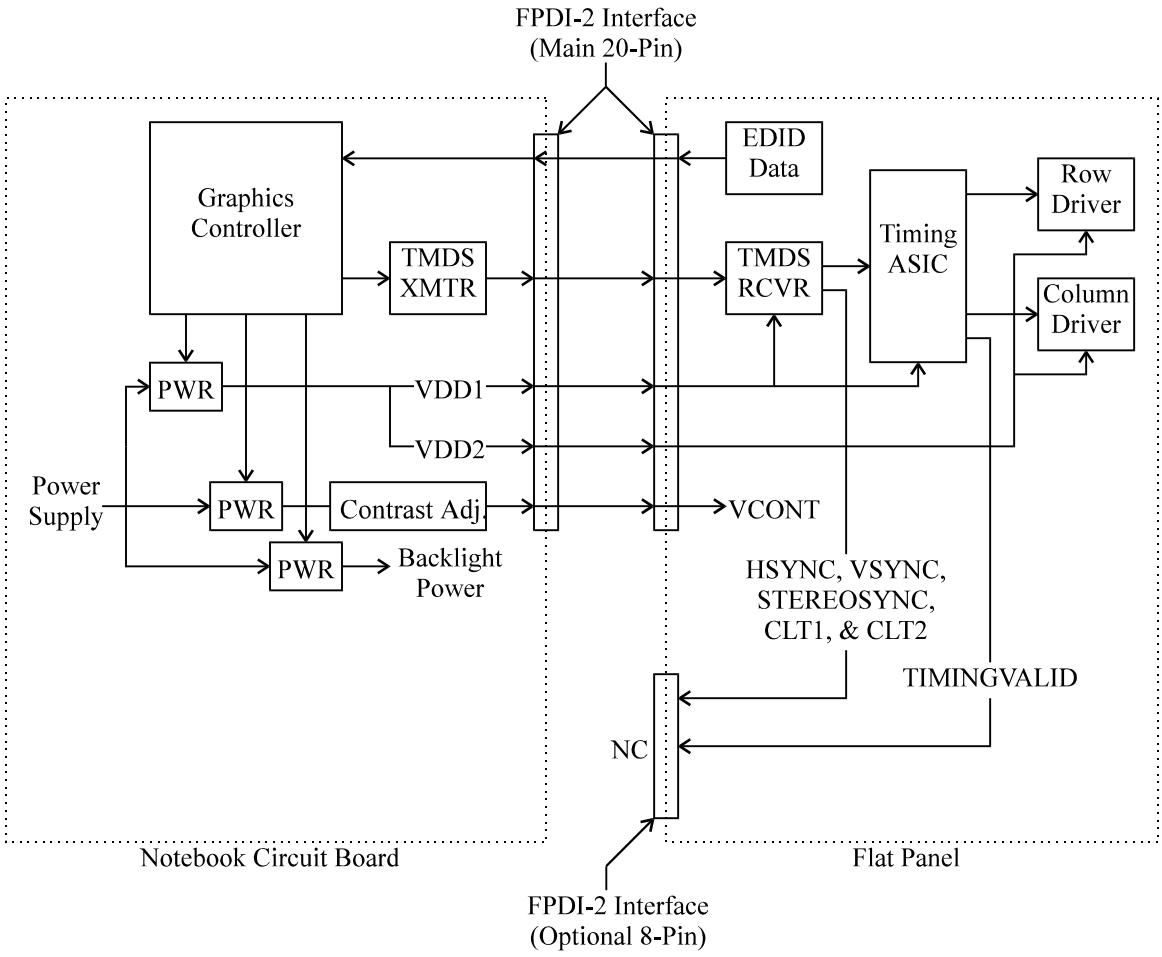
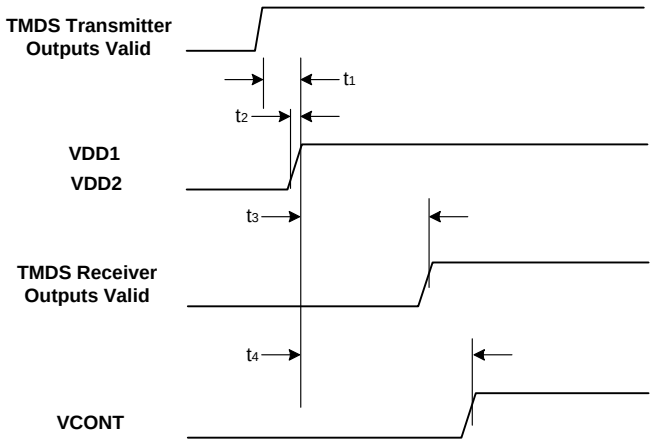
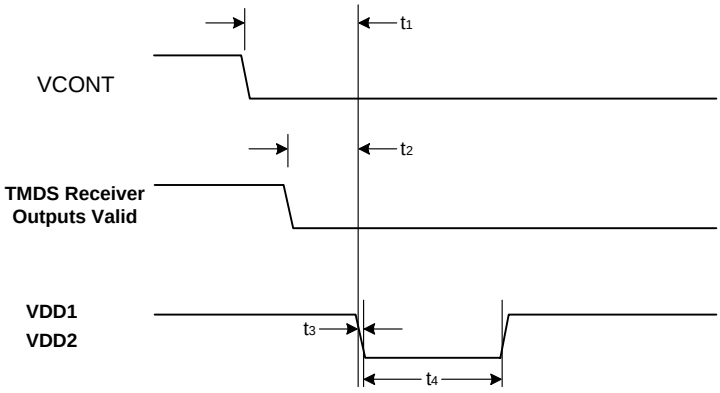


Figure 6-1: Block Diagram of Notebook Case



Symbol	Function	Min	Max	Unit
t1	TMDS Tx valid to VDD	0	∞	
t2	VDD rise time	0	40	ms
t3	VDD to TMDS Rx valid		10	ms
t4	VDD to VCONT	>0	∞	

Figure 6-2: Power-up Sequencing for the Notebook Case



Symbol	Function	Min	Max	Unit
t1	VCONT to VDD	>0	200	ms
t2	TMDS Rx valid to VDD	0	1000	ms
t3	VDD fall time		500	ms
t4	power retry	1000		ms

Figure 6-3: Power-down Sequencing for the Notebook Case

6.3 Monitor Case

Figure 6-4 presents a block diagram of the manner in which a flat panel that is compliant with FPDI-2 could be used to build a P&D-compliant monitor.

As shown in the figure, a circuit board with logic in addition to that already in place on the flat panel is interposed between the FPDI-2 interface of the flat panel and the P&D interface of the completed monitor. This circuit board's primary function is the control of the manner and timing by which power is supplied to the flat panel. A block of logic, referred to in the diagram as the "monitor logic" performs the work of responding to various actions taken by the host to which the monitor is attached, or to situations in which the monitor is hot-plugged into the host. This monitor logic could take any form, from a dedicated ASIC to a microcontroller, that performs these functions in addition to others.

As was the case with the flat panel graphics controller in the notebook scenario, the monitor logic would be responsible for directly enabling and disabling the provision of VDD1, VDD2, VCONT and backlight power in the correct order with appropriate time delays. The control of these power supplies is not carried out through the TMDS interface.

Since the 256-byte, I^2C memory device used to carry the EDID data structure resides at address A2h for P&D-compliant monitors, and not at the A6h address reserved for flat panels adhering to FPDI-2, it is likely that a separate memory device will be used.

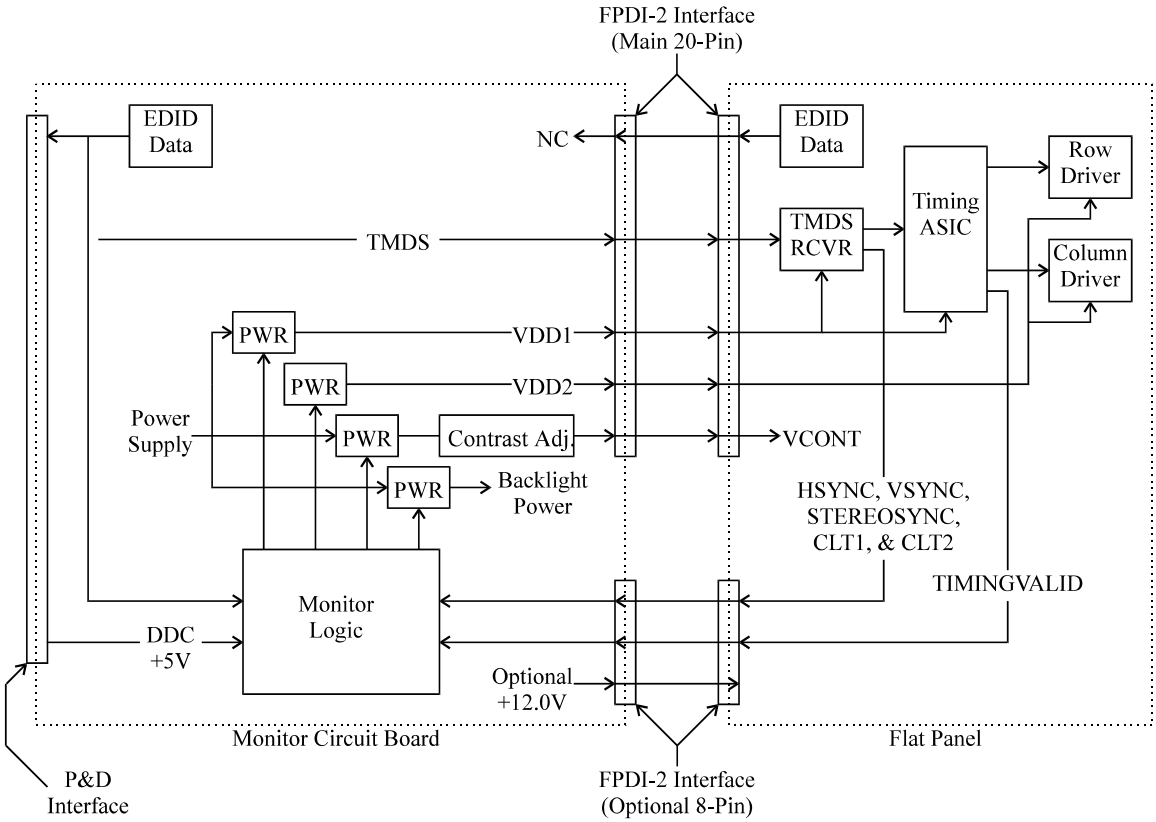


Figure 6-4: Block Diagram of Monitor Case

Figure 6-5 presents a flowchart of the sequence of actions taken by a P&D-compliant monitor based on a FPDI-2-compliant flat panel (i.e, the monitor case) when the monitor is connected to a power source. The monitor is required to provide a minimum +2.4 V on the Charge Power line of the P&D connector interface, at least when it has been turned on by the end user or whenever it has power from a continuous source such as an AC outlet. If the monitor supports DPMS, then it is expected that the monitor will default to being in the DPMS "off" state upon first being connected to a power source or turned on by the end-user.

The monitor logic would continuously watch the +5 VDC line received from the P&D connection to the host for the presence of +5 VDC. Presumably, this would mean that the monitor has just been hot-plugged to an active P&D-compliant host, or that the host has just been turned on by the end-user. The monitor logic would also continuously watch for when the host reads all 256 bytes of the monitor's EDID data structure at A2h. This would be taken as a sign that the host is, in fact, compliant with the P&D specification, and that the host should now be aware of the monitor's requirements. In response to the reading of the EDID data structure, the monitor logic would then supply VDD1 to the flat panel's TMDS receiver and timing ASIC.

Upon being powered up with VDD1, the flat panel's timing ASIC would wait end watch the incoming DCLK pulses, examining them to see that they are within an acceptable range of frequencies before driving the TIMINGVALID signal high. Although it is conceivable that the timing ASIC could also monitor HSYNC and VSYNC, it is highly recommended that the timing ASIC design place priority on examining DCLK, since this is the clock rate at which each pixel of data will be received by the panel. While continuing to check for the presence of +5.0V from the host, the monitor logic would wait until the flat panel's timing ASIC had driven TIMING VALID high before supplying VDD2 to the flat panel's row and column drivers and supplying the appropriate power to the flat panel's backlight, in the appropriate order and with the appropriate time delays. If the monitor is designed to support DPMS, then in normal operating mode the monitor logic would first watch the HSYNC and VSYNC signals from the TMDS receiver for indications of which of the four possible DPMS states it should switch to.

Throughout normal operation, the monitor logic would also continuously watch for either the cessation of DCLK, or the absence of +5 VDC. Should either of these happen, the monitor logic would power down the flat panel's backlight and the flat panel's row and column drivers (if they are not already powered down) and then power down the flat panel's TMDS receiver and timing ASIC -- essentially the equivalent of entering the DPMS "off" state. The monitor logic would then go back to waiting for +5.0 V to be reestablished and for the EDID data structure at A2h to be read again, before again supplying VDD1 to the flat panel's TMDS receiver and timing ASIC.

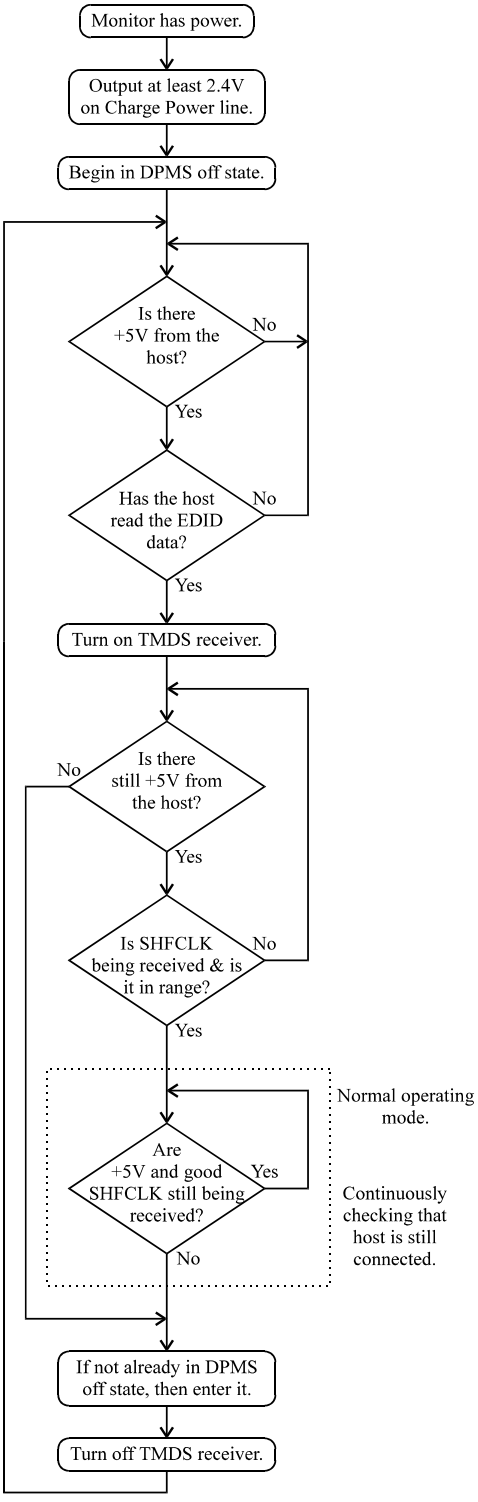


Figure 6-5: Power-Up and Hot-Plugging Flowchart for P&D-D (TMDS) Monitor

7. Connector Interface

7.1 Introduction

This section defines the standardized connector interfaces required on FPDI-2 flat panel displays. For reference, information is also provided for the mating interconnects.

The standardized connector interface required on the flat panel display is a receptacle connector with 20 contacts in a single row configuration, on a 1.25 mm centerline spacing. This connector has a plastic housing with pre-loaded contacts and is usually soldered to the flat panel display driver, printed circuit board, (PCB).
Mating interconnect options, to the standardized receptacle connector, include either a cabled plug connector or a flexible etched circuit (FEC). The cabled plug connector consists of a plastic housing which receives the snap-in tab contacts that have been terminated to discrete wires. The FEC interconnect eliminates the need for the plug connector and tab contacts. It is plugged directly into the standardized receptacle connector. Use of either interconnect option requires proper design of the discrete wire cable or FEC in order to comply with the performance requirements of this standard.

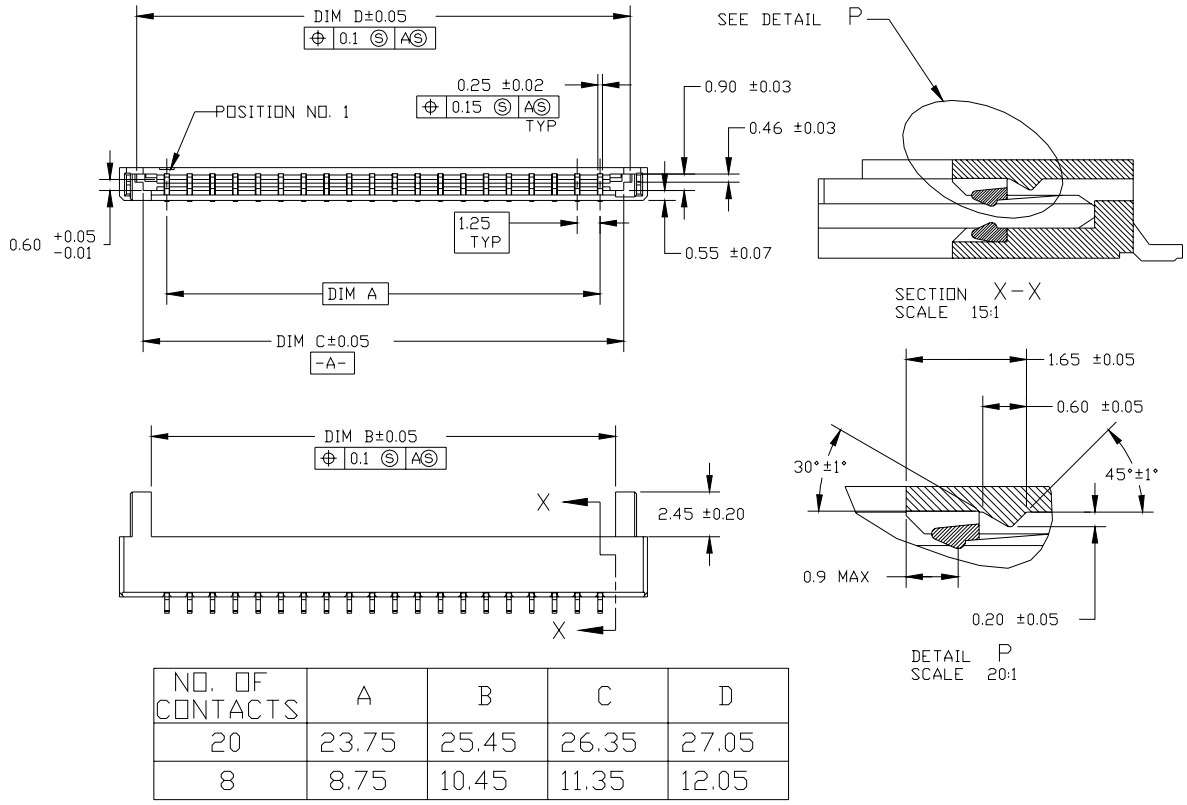
Monitor applications may require the use of an auxiliary connector for +12 VDC power, signals for hot-plugging and DPMS, user defined CTL1 and CTL1, and Stereo Sync. An 8-position connector from the 20-position connector family is illustrated throughout this section.

Dimensions, tolerances, and features which affect the inter-mateability of the standardized receptacle connector and contacts and are described in Figure 7.1 for both the 20-and the 8-position connectors. A PCB layout for the attachment of the receptacle connector to the flat panel circuit board is provided for reference in Figure 7.2. Similarly, the recommended plug connector and contact features are described in Figure 7.3. Figure 7.4 shows a recommended flexible etched circuit.

This specification also describes the connector interface pin assignments, performance characteristics, and requirements.

7.2 Receptacle Connector

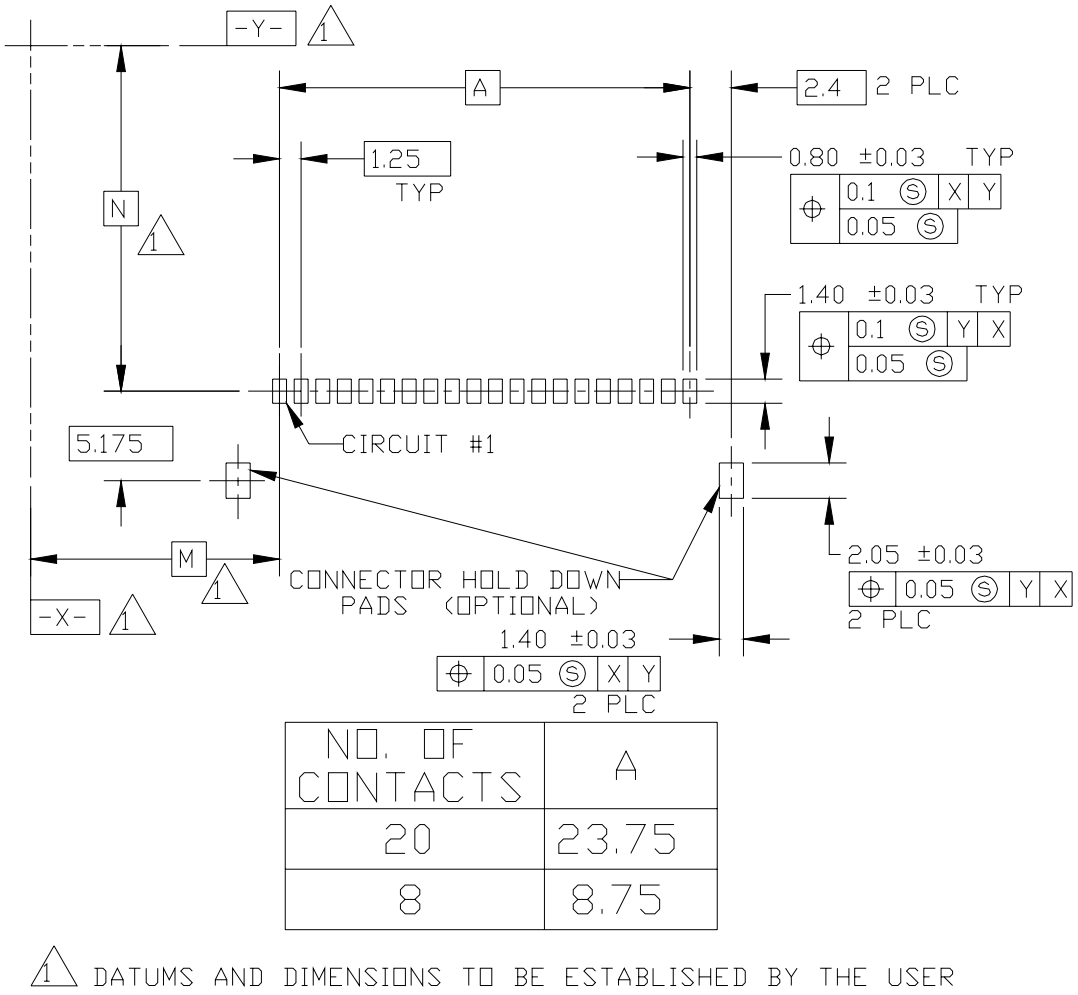
Figure 7.1 illustrates the mating interface of the receptacle connector, which is the controlling interface in this standard. Figure 7.2 illustrates the recommended PCB layout for the receptacle connector.



NO. OF CONTACTS	A	B	C	D
20	23.75	25.45	26.35	27.05
8	8.75	10.45	11.35	12.05

Figure 7-1: Receptacle Connector Mating Interface Defining Features

Notes:
1. Dimensions are in millimeters.
2. Dimensions and tolerances are per ASME Y14.5M - 1994.
3. Not to scale.



NO. OF CONTACTS	A
20	23.75
8	8.75

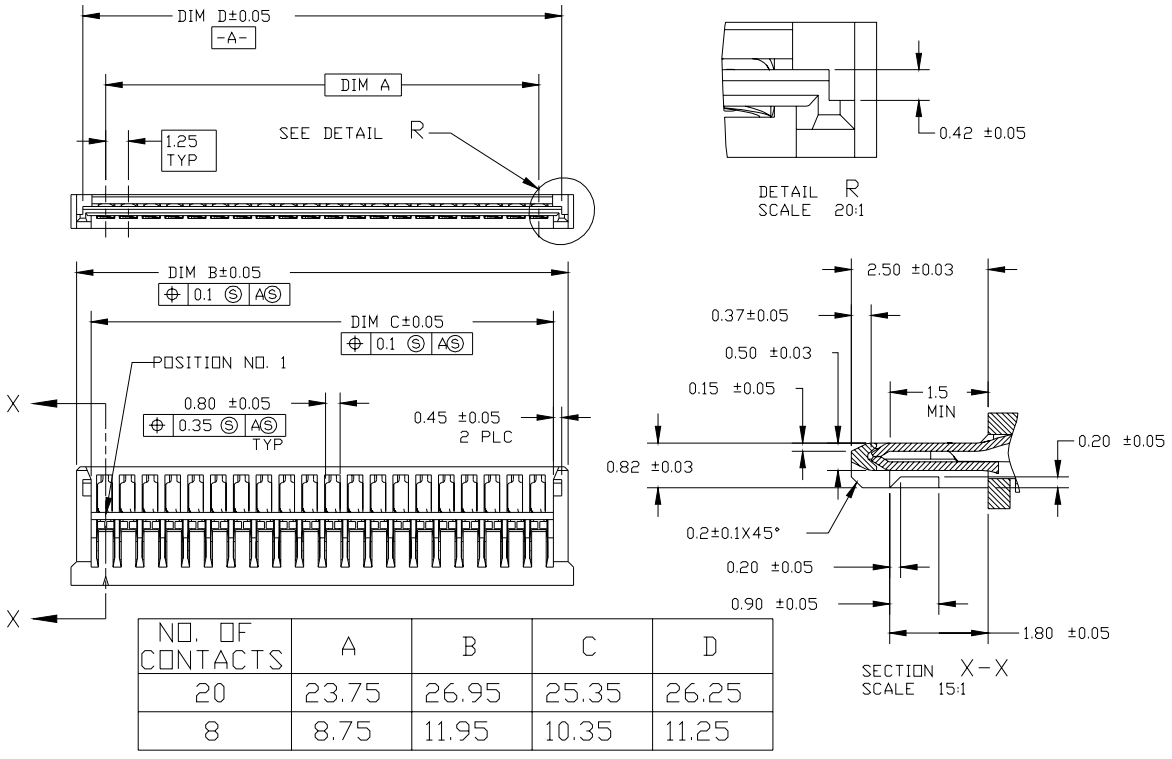
1 DATUMS AND DIMENSIONS TO BE ESTABLISHED BY THE USER

Figure 7-2 Recommended PCB Layout For The Receptacle Connector

Notes:
1. Dimensions are in millimeters.
2. Dimensions and tolerances are per ASME Y14.5M - 1994.
3. Not to scale.

7.3 Plug Connector

Figure 7.3 illustrates the mating interface features and dimensions of the plug connector, including the tab contacts.



NO. OF CONTACTS	A	B	C	D
20	23.75	26.95	25.35	26.25
8	8.75	11.95	10.35	11.25

Figure 7-3: Recommended Plug Connector Mating Interface Features (Contacts Installed in Housing for Clarity)

Notes:
1. Dimensions are in millimeters.
2. Dimensions and tolerances are per ASME Y14.5M - 1994.
3. Not to scale.

7.3.1 Alternate Transmission Media Termination

Termination of the tab contacts to wire may be varied to suit manufacturing processes. However, the end-product must meet the performance requirements of this Standard.

7.3.2 Recommended Flexible Etched Circuit Interconnection (Alternative to Plug)

As an alternative to using wire and wire terminations, FECs may be designed to plug into the standardized receptacle connector. The design of the FEC and backer board may vary, however, the overall assembly and mating interface must conform to the receptacle connector dimensional requirements and meet the performance requirements of this Standard. Figure 7.4 illustrates the recommended mating interface for the flexible etched circuit. Refer to Section 7.5 for recommended contact platings.

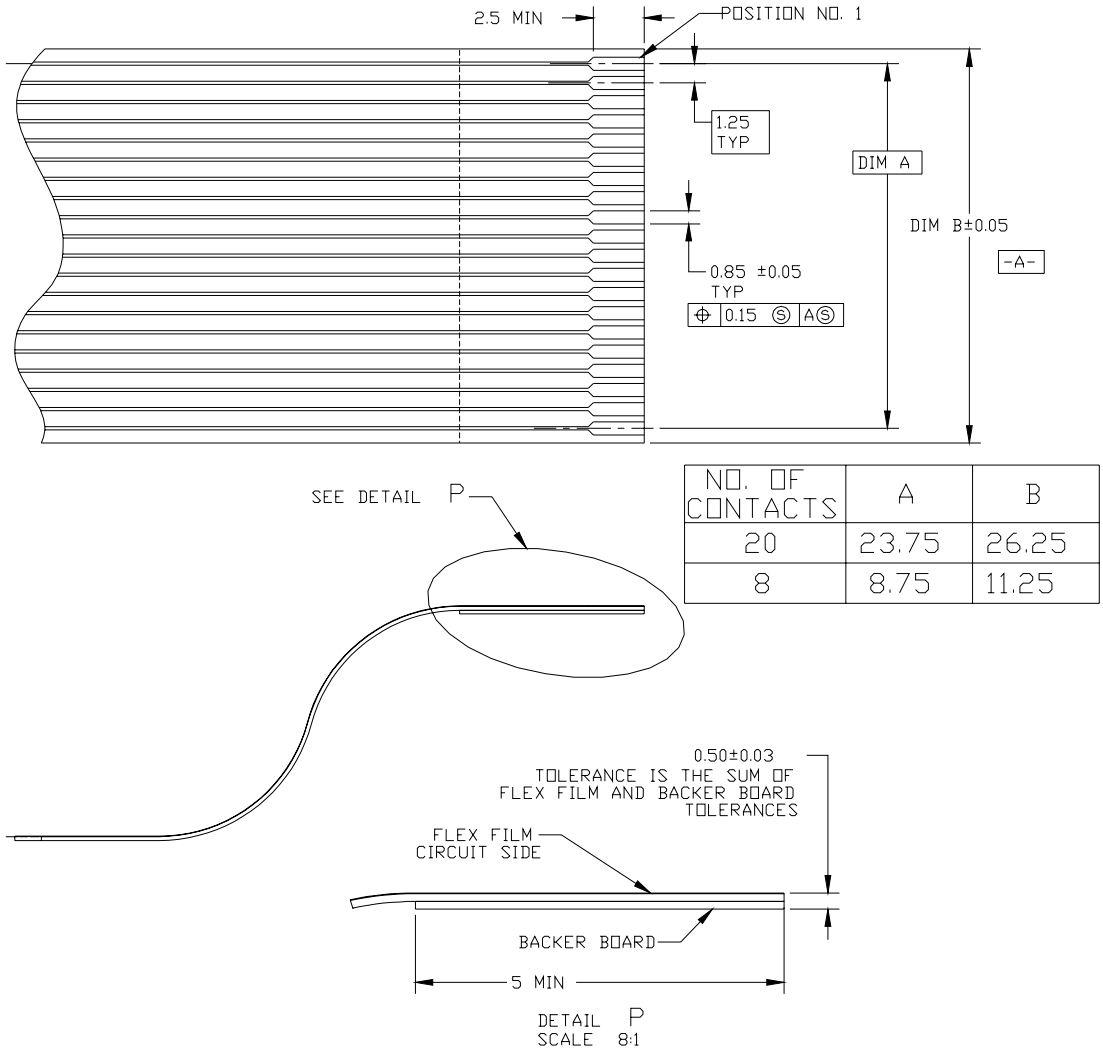


Figure 7-4: Recommended FEC Mating Interface Features

Notes:
1. Dimensions are in millimeters.
2. Dimensions and tolerances are per ASME Y14.5M - 1994.
3. Not to scale.

7.4 Recommended Contact Platings

The following electroplatings are most common.

Receptacle Contact: 0.25 micron minimum, tin, over 1.27 micron, minimum, nickel

Plug Tab Contact: 0.15 micron minimum, tin, over 1.27 micron, minimum, nickel

Other thicknesses and compositions may be used, providing they meet the performance requirements of this Standard. It is not acceptable to use gold or other metals known to be incompatible with tin.

7.5 Connector Performance Characteristics

This section summarizes the electrical, mechanical, and environment performance characteristics of the FPDI-2 connector. ANSI/EIA-364 Test Procedures and Conditions are noted, where applicable. Connector performance requirements are also noted for each test.

7.5.1 Electrical

7.5.1.1 Contact Resistance

Conditions:	ANSI/EIA 364-23A
Requirement:	20 mΩ, maximum, initial, per contact mated pair
Requirement:	40 mΩ, maximum, final, per contact mated pair
Requirement:	20 mΩ maximum, change, per contact mated pair

7.5.1.2 Contact Current Rating

Conditions:	ANSI/EIA-364-70
Requirement:	1.0 A, minimum per contact, terminated to 30 AWG wire

7.5.1.3 Dielectric Withstanding Voltage

Conditions:	ANSI/EIA 364-20 Method C
	Barometric pressure 685 to 785 mm Hg at Sea Level
	Unmated and un-mounted
Requirement:	500 VDC for 1 minute, minimum

7.5.1.4 Insulation Resistance

Conditions:	ANSI/EIA 364-21
	Unmated and un-mounted
	500 VDC for 1 minute
Requirement:	500 MΩ, minimum

7.5.1.5 Differential Impedance:

Conditions:	ANSI/EIA-364-67 [1]
	TDR method, normalized to 1ns rise-time
Requirement:	100 Ω, +/- 10%

7.5.1.6 Bandwidth:

Conditions:	Frequency Domain Measurement [2]
	Includes reflections, dielectric losses and skin effect losses
Requirement:	1.5 dB loss maximum @ 6 GHz

7.5.1.7 Crosstalk:

Conditions:	ANSI/EIA 364-90 [1]

Edge Rate = 250 ps at 1 volt
Requirement: Near End Crosstalk = 1.4 % maximum

7.5.2 Mechanical

7.5.2.1 Mechanical Shock

Conditions: ANSI/EIA 364-27 Condition A
3 shocks in 3 mutually perpendicular planes, 18 shocks total
50 G's half sine pulses, 11 ms duration
Requirement: No discontinuities > 1μs

7.5.2.2 Durability

Conditions: ANSI/EIA 364-09
Engage/Disengage at rate of 10 cycles per minute
Requirement: 30 cycles, minimum
Requirement: Contact resistance requirements of Section 7.5.1.1

7.5.2.3 Mating and Unmating Forces

Conditions: ANSI/EIA 364-13
Engage/Disengage at rate of 20 mm per minute
Requirement: Mating Force of 39 N, maximum
Requirement: Unmating Force of 7.8 N, minimum

7.5.3 Environmental

7.5.3.1 Operating Temperature Range

Conditions -30°C to +85°C

7.5.3.2 Thermal Shock

Conditions: ANSI/EIA 364-32 Condition I
5 cycles, -55 to +85 °C
Requirement: Contact resistance requirements of Section 7.5.1.1

7.5.3.3 Humidity, Steady State

Conditions: ANSI/EIA 364-31 Condition A, Method II
+40°C at 90-95% RH for 96 Hours
Requirement: Insulation Resistance > 250 MΩ
Requirement: Contact resistance requirements of Section 7.5.1.1

[1] At the time of preparation of this Standard, ANSI/EIA-364-67 and ANSI/EIA-364-90 have not been ratified, and are cited as the recommended test procedures. The impedance values are described in ohms as calculated from the "% reflection" as specified in ANSI/EIA-364-67.

[2] No current test procedure exists in ANSI/EIA-364 for bandwidth testing.

8. Compliance, Troubleshooting, Verification

8.1 System De-Bug on Differential Data Pairs

The following will allow the system designer to generate a reproducible (triggerable) pattern for system de-bug on the differential data pairs. With Data Enable (DE) low, the following out-of-band characters will be sent depending only on the sync characters. This requires the sync signals and DE be jumpered on the system designer's proto board. The patterns are independent of the 24-bit data bus into the transmitter.

Rx0 Differential Data Pair (e.g. blue):											
HSYNC	VSYNC	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1
Rx1 Differential Data Pair (e.g. green):											
PLL_SYNC	CTL1	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1
Rx2 Differential Data Pair (e.g. red):											
CTL2	CTL3	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9
0	0	0	0	1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1	0
1	1	1	1	0	1	0	1	0	1	0	1

Table 8-1: System Debug Patterns

Example: for DE = 0, VSYNC = 0, HSYNC = 0. Differential Data Pair Rx0 will cycle through the sequence 0010101011 repeatedly. The bit time will be the pixel clock period x10.

8.2 Signal Bandwidth Characteristics

P_{CLK}	f_o	x	f_c	Maximum Distributed Rise-Time
25	125 MHz	3	375 MHz	933 ps
40	200 MHz	3	600 MHz	583 ps
65	325 MHz	3	0.975 GHz	360 ps
112	560 MHz	3	1.68 GHz	208 ps
160	800 MHz	3	2.4 GHz	145 ps

Table 8-2: Distributed Transmission Path Bandwidth and Rise-Time

Note:
P_{clk} = Pixel Clock
f_o = frequency operation
x = harmonic order
f_c = cut-off frequency = $3f_o$
Rise-Time = $0.35/f_c$

8.3 Electrical Characteristics

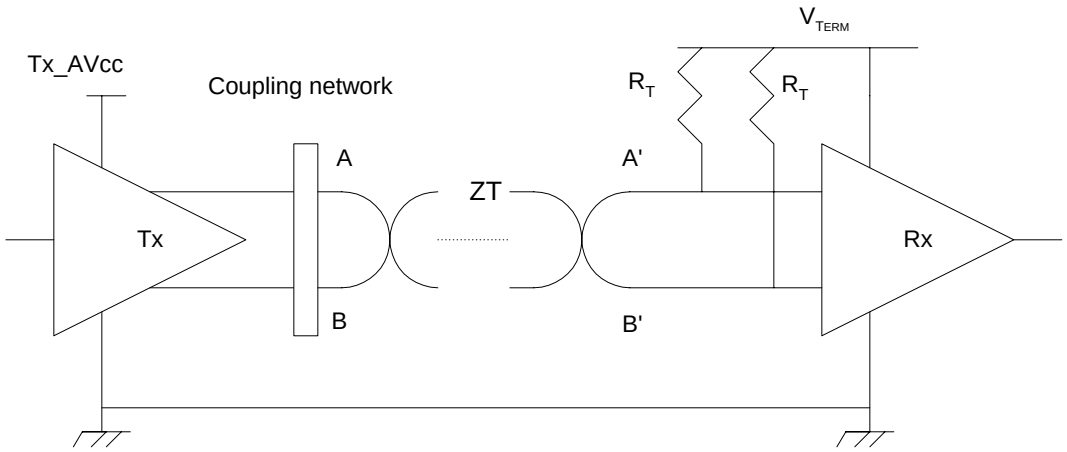


Figure 8-1: Differential Mode Impedance

Tx = Transmitter
Rx = Receiver
A = Transmitter interface point
A' = Receiver interface point
B = Transmitter interface point
B' = Receiver interface point
R_T = Termination Resistance
V_{TERM}= Termination Voltage

V_{TERM} = 3.3 V ± 5% and must be within 5% with respect to TX_ AV_{CC} (with direct coupling)
V_{TERM} = 3.3 V ± 5% (with capacitor coupling) (see Figure 8-5)
90 Ω < Z_T < 110 Ω (range of allowed differential mode impedance of the media.)
R_T = ½ Z_T
2 mA < I_{SINK} < 12 mA
100 mV < V_{SWING} < 600 mV single-ended with R_T = 50 Ω on A or B.

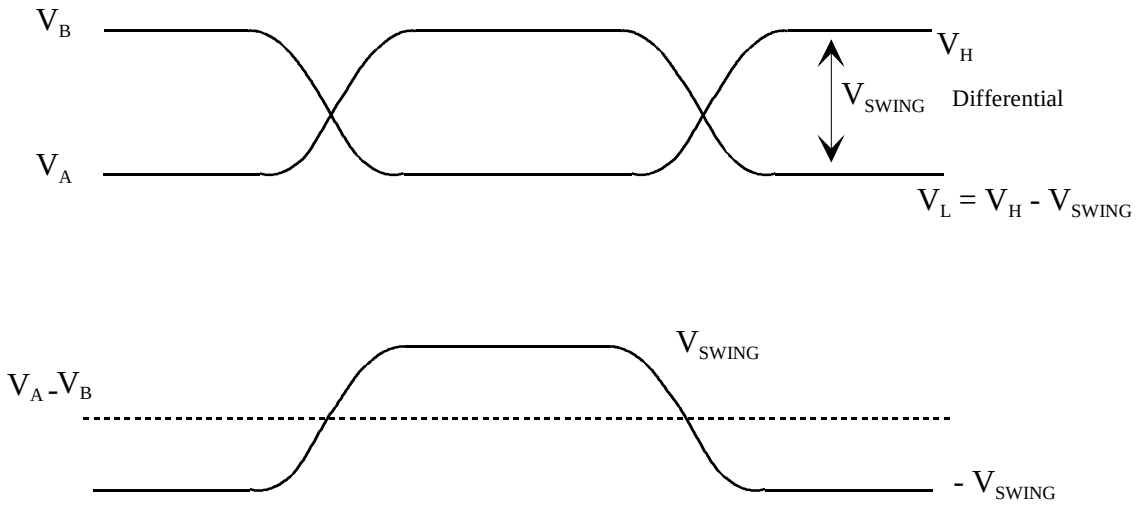


Figure 8-2: Signal Levels on Transmission Media

8.4 DC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak-to-peak amplitude	R_{LOAD} = 50 Ω	250		720	mV
V_{DOH}	Differential High-level Output Voltage			AVCC		V

Under normal operating conditions unless otherwise specified.

Table 8-3: Receiver Specifications for TMDS Input

8.5 Driver Output Levels

Driver output stage is a differential current switch with externally adjustable current. The range of adjustment is from 2 mA to 12 mA, depending on the length of the cable. The output impedance of the driver is dominant compared with the characteristic impedance of the interconnect media. Thus, the output current is not affected by the termination resistance. Impedance of the interconnect is 100 Ω with 10% tolerance. 50 Ω termination resistors with 10% tolerance are connected to the receiver supply voltage.

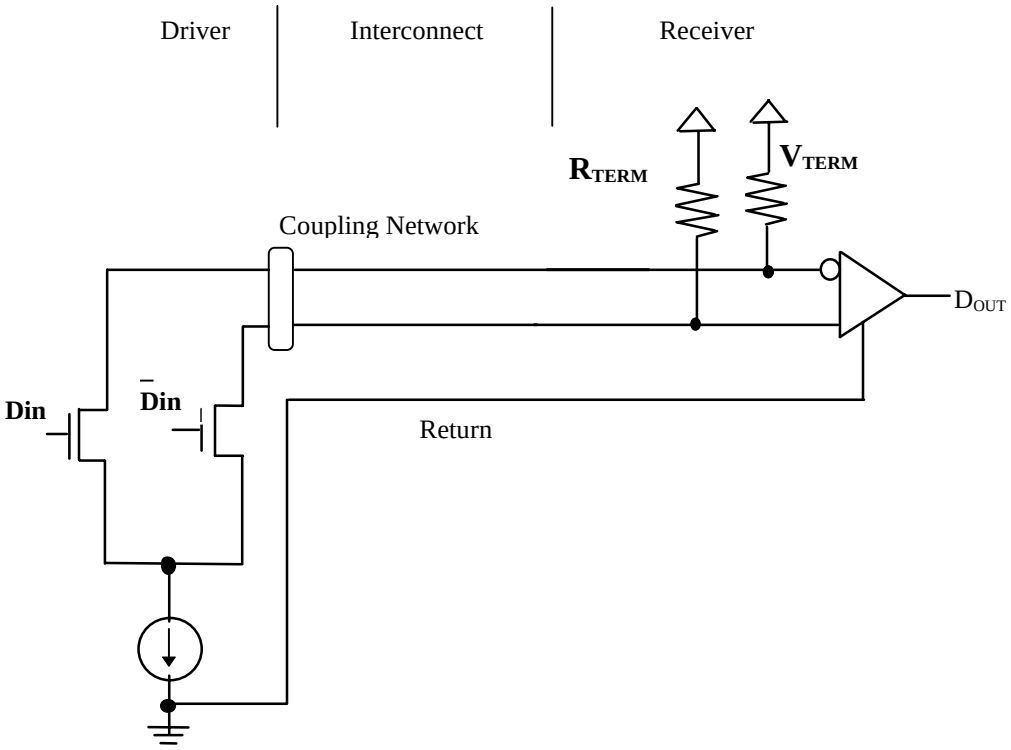


Figure 8-3: Driver and Receiver Circuit Model for One Differential Data Pair

Test Circuit Information: Din = High ; Din = Low
I_{OH} = fixed 12 mA for FPDI-2
When AV_{CC} is driven locally and when direct connection is made without AC-coupling, the two supply voltages must be within 10% of each other in addition to their individual tolerance of ± 10%. See Figure 2-4. For AC-coupling with capacitors, the two supplies can have their individual tolerance of ± 10%. Ground shield is shared in both cases. The recommended circuit is shown in Figure 2-5. In case of capacitor coupling, signaling current must be increased to give the same signal level in the receiver. The receiver needs to be able to resolve 100 mV differential input.

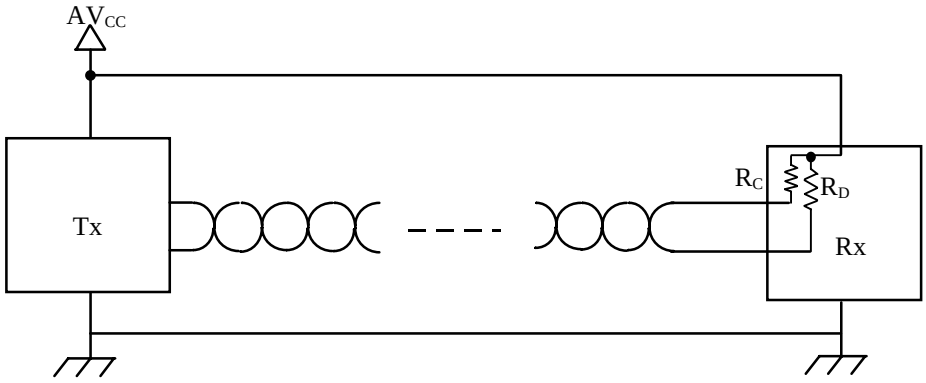


Figure 8-4: Direct Coupling for Notebook Case

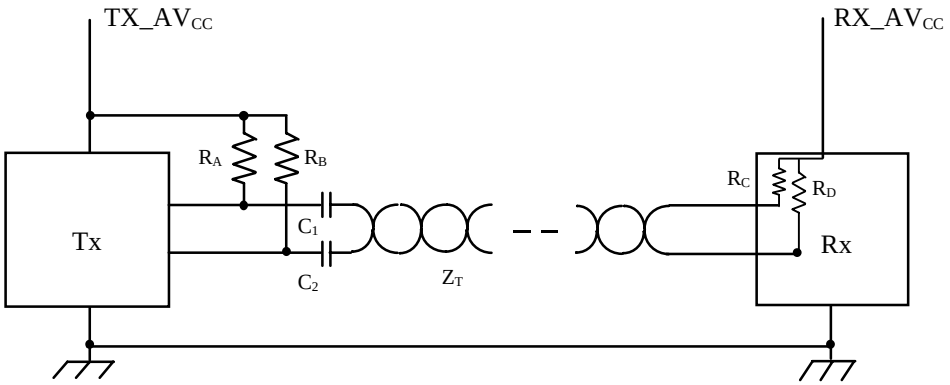


Figure 8-5: Capacitor - Coupled for Monitor Case

The purpose of R_A and R_B is to provide an average DC level on the Tx side. R_C and R_D provide on-chip termination. R_A and R_B provide source termination. Source termination reduces V_{SWING} on the cable, but improves signal integrity.

Component	25-65 MHz	65-112 MHz
Z_T	100 Ω	100 Ω
C_1	10 nf ± 20%[1]	10 nf ± 20%[1]
C_2	10 nf ± 20%[1]	10 nf ± 20%[1]
R_A	100 Ω	100 Ω
R_B	100 Ω	100 Ω
[1] Typical Part Number CE103Z2NV		

Table 8-4: Component Values for Figure 8-5

8.6 Signal Integrity

Maximum transmission rate is defined by the user depending on the application. In case of 800x600, 40 MHz dot clock is used. In case of 1024x768 and 1280x1024, 65 MHz and 112 MHz could be used. A bit time is one-tenth of a clock period. The duty cycle of the transmitted clock should be maintained close to 50% to remove DC component.

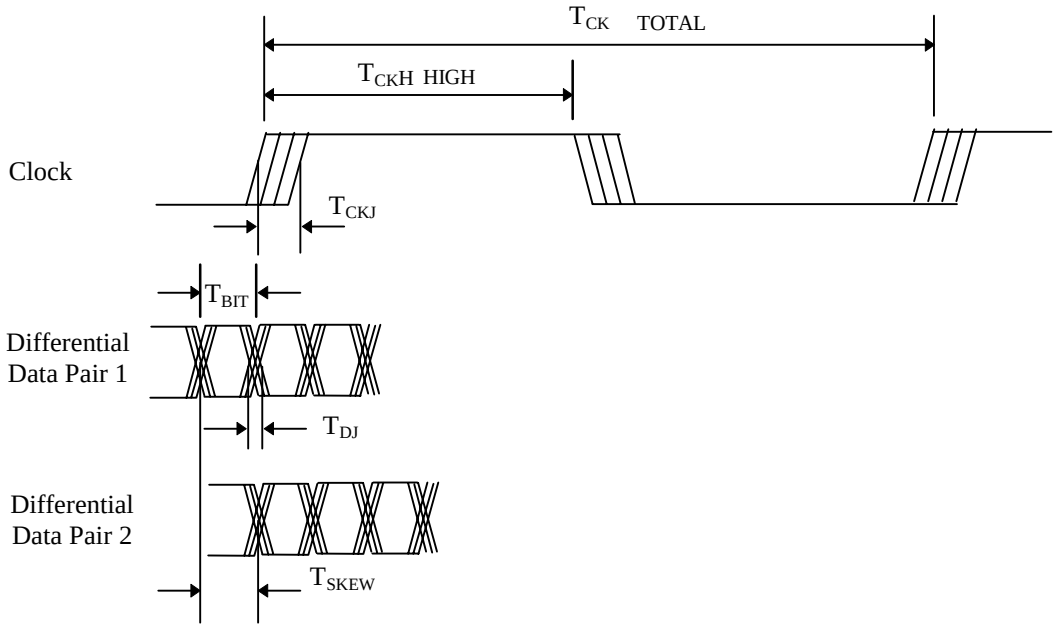


Figure 8-6: Timing Diagram for Jitter and Skew Specification

8.6.1 Jitter and Skew of Clock and Differential Data Pairs

The amount of jitter in the dot clock is allowed within 5% of the dot clock period. For differential data pair, 20% jitter, with respect to bit time, is allowed. The skew among the differential data pair is allowed within one pixel time. Skew between clock and data channels is allowed within one bit time.

Frequency of Pixel Clock	**25 MHz**	**40 MHz**	**65 MHz**	**112 MHz**	**160 MHz**
T_{CK} = Clock Period = 1/F	40 ns	25 ns	15.38 ns	8.929 ns	6.25 ns
T_{CKH} = Clock duty min/max	40/60	40/60	40/60	40/60	40/60
T_{CKJ} = Clock jitter = T_{CK} x 0.05	2 ns	1.25 ns	769 ps	446 ps	313 ps
T_{BIT} = Bit time = T_{CK} x 0.10	4 ns	2.5 ns	1.538 ns	892 ps	625 ps
T_{DJ} = Data jitter = T_{BIT} x 0.20	800 ps	500 ps	307.6 ps	178.4 ps	125 ps
T_{SKEW} = T_{BIT}	4 ns	2.5 ns	1.538 ns	892 ps	625 ps

Table 8-5: Signal Integrity Parameters

8.6.2 Eye Diagram Template

The reference points for all connections between transmitter and receiver are points S and R as shown in Figure 8-7.

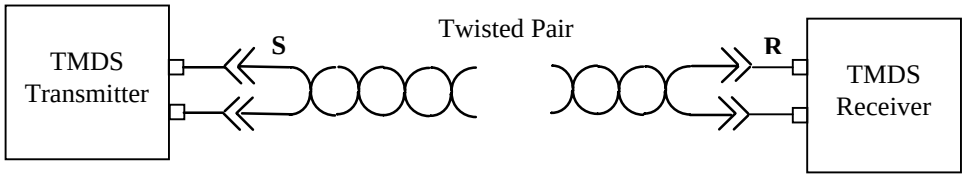


Figure 8-7: TMDS Connection

The output from the TMDS transmitter shall have the levels as specified in Section 2.4. The mask of the transmitter eye diagram, as measured at the input to the cable (point S) on two 50 Ω termination resistors, are given in Figure 8-8 and Table 8-6. The Y1 and Y2 amplitudes in Table 8-6 are set to allow overshoot and undershoots relative to the amplitudes of a logic 1 and logic 0.

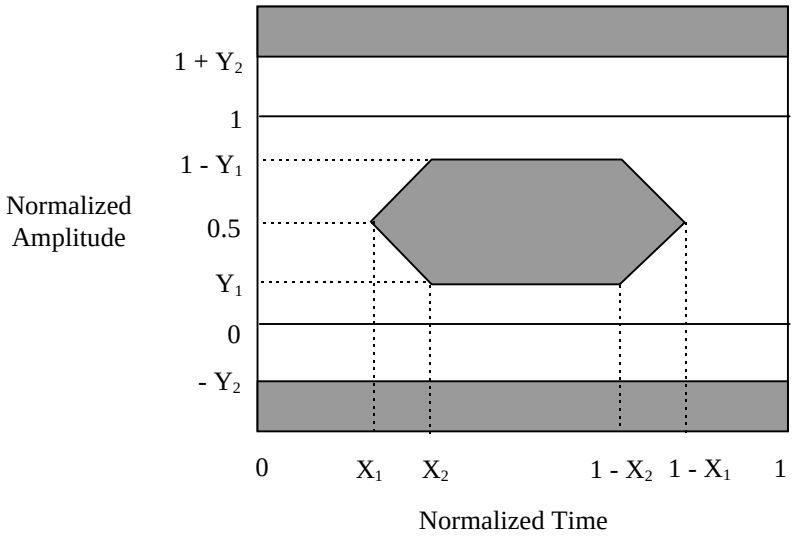


Figure 8-8: Eye Diagram Mask at Point S

DOT CLOCK FREQUENCY	X_1	X_2	Y_1	Y_2
25 MHz	0.15	0.25	0.20	0.20
40 MHz	0.15	0.25	0.20	0.20
65 MHz	0.20	0.30	0.20	0.20
112 MHz	0.20	0.30	0.20	0.20

Table 8-6: Eye Diagram Mask at Point S*

*** Preliminary**

The TMDS receiver terminates the link with an equivalent resistance of 100 Ω. The mask of the receiver eye diagram is given in Figure 8-9 and its specification in Table 8-7.

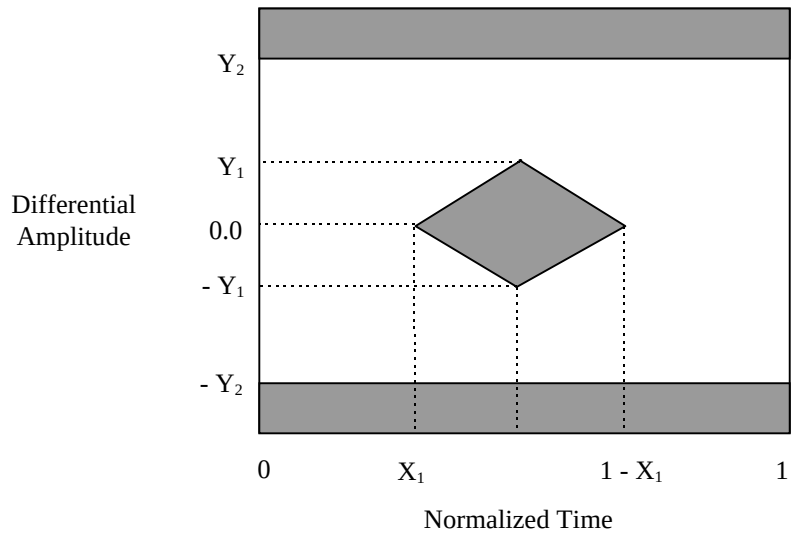


Figure 8-9: Eye Diagram Mask at Point R

DOT CLOCK FREQUENCY	X_1	Y_1	Y_2
25 MHz	0.30	100 mV	600 mV
40 MHz	0.30	100 mV	600 mV
65 MHz	0.30	100 mV	600 mV
112 MHz	0.30	100 mV	600 mV

Table 8-7: Eye Diagram Mask at Point R*

*** Preliminary**

8.7 AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Small Swing Low-to-High Transition Time	C_L = 5 pF	0.25	0.3	0.5	ns
S_{HLT}	Small Swing High-to-Low Transition Time	C_L = 5 pF	0.25	0.3	0.5	ns
D_{LHT}	Digital Output Low-to-High Transition Time (Data, DE, VSYNC, HSYNC, CTL[3:0])	C_L = 15 pF OVCC = 3.3 V	2.5	3.1	4.1	ns
		OVCC = 5.0 V	1.9	2.4	3.0	ns
	(ODCK)	C_L = 15 pF OVCC = 3.3 V	1.2	1.4	1.9	ns
		OVCC = 5.0 V	0.9	1.1	1.4	ns
D_{HLT}	Digital Output High-to-Low Transition Time (Data, DE, VSYNC, HSYNC, CTL[3:0])	C_L = 15 pF OVCC = 3.3 V, Data Out	1.1	1.9	2.6	ns
		OVCC = 5.0 V, Data Out	1.3	1.6	2.1	ns
	(ODCK)	C_L = 15 pF OVCC = 3.3 V, Clock Out	0.7	0.9	1.2	ns
		OVCC = 5.0 V, Clock Out	0.6	0.7	0.9	ns
T_{LPL}	PLL Locking Time				12	us
T_{UPL}	PLL Unlocking Time				1	us
T_{DPS}	Differential Pair Skew	1 Bit Time			5	%
T_{CCS}	Differential data pair-to-Differential data pair Skew				T_{CIP}	ns
T_{CIP}	IDCK Cycle Time		15		40	ns
T_{CIH}	IDCK High Time		0.4 T_{CIP}	0.5 T_{CIP}	0.6 T_{CIP}	ns
T_{CIL}	IDCK Low Time		0.4 T_{CIP}	0.5 T_{CIP}	0.6 T_{CIP}	ns
T_{IJIT}	IDCK Jitter	(0.05)x T_{CKJ}			1	ns
R_{CIP}	ODCK Cycle Time		15		40	ns
R_{CIH}	ODCK High Time		0.4 T_{CIP}	0.5 T_{CIP}	0.6 T_{CIP}	ns
R_{CIL}	ODCK Low Time		0.4 T_{CIP}	0.5 T_{CIP}	0.6 T_{CIP}	ns

Symbol	Parameter	Conditions	Min	Max	Unit
T_{SDF}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Setup Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	3		ns
T_{HDF}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Hold Time from IDCK falling edge	CEDGE = 0 DEDGE = 0	4		ns
T_{SDR}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Setup Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	4		ns
T_{HDR}	Data, DE, VSYNC, HSYNC, and CTL[3:0] Hold Time from IDCK rising edge	CEDGE = 1 DEDGE = 1	3		ns
T_{DDF}	VSYNC, HSYNC, and CTL[3:0] Delay from DE falling edge		T_{CIP}		ns
T_{DDR}	VSYNC, HSYNC, and CTL[3:0] Delay from DE rising edge		T_{CIP}		ns
T_{TRX}	Differential Clock Output delay from IDCK			5.8	ns
T_{HDE}	DE high time			8000 T_{CIP}	ns
T_{LDE}	DE low time		10 T_{CIP}		ns
T_{PH1}	PLL_SYNC Delay from VSYNC asserted (Phase 1)	SYNC_CONT = 1	T_{CIP}	3 T_{CIP}	ns
T_{PH2}	PLL_SYNC Delay from VSYNC asserted (Phase 2)	SYNC_CONT = 0	T_{CIP}	3 T_{CIP}	ns
T_{LPS}	PLL_SYNC Delay from VSYNC de-asserted		T_{CIP}	2 T_{CIP}	ns
T_{LPD}	Delay from PD Active to Outputs Disabled		4	6	ns
T_{HPD}	Delay from PD Inactive to Outputs enabled		4	6	ns

Table 8-8: AC Specifications

Note : All timing measured from 80% and 20% of waveform signal.

8.7.1 Timing Diagrams

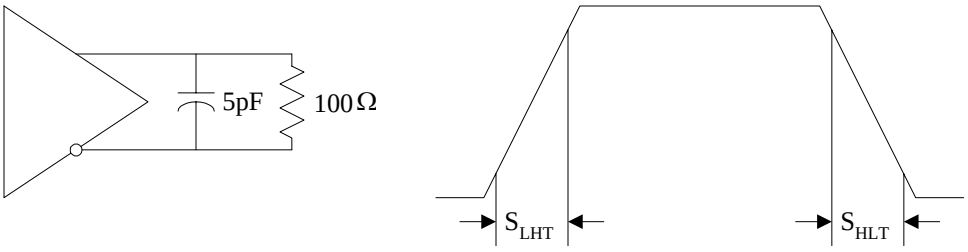


Figure 8-10. Transmitter Small Signal Transition Times

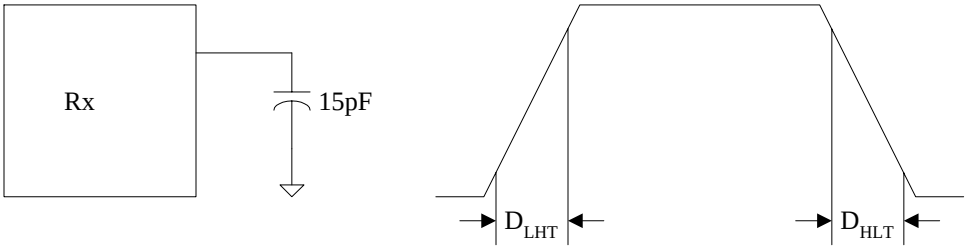


Figure 8-11. Receiver Digital Output Transition Times

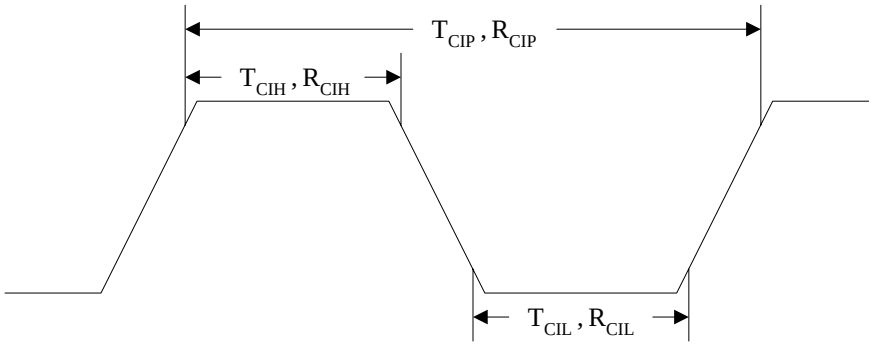


Figure 8-12. Transmitter/Receiver Clock Cycle/High/Low Times

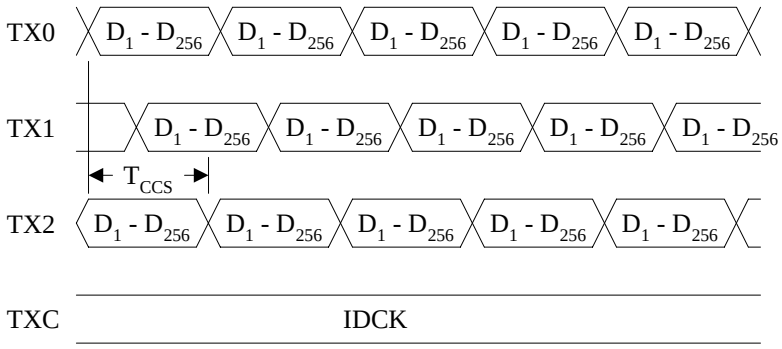


Figure 8-13. Differential Data Pair-to-Differential Data Pair Skew Timing

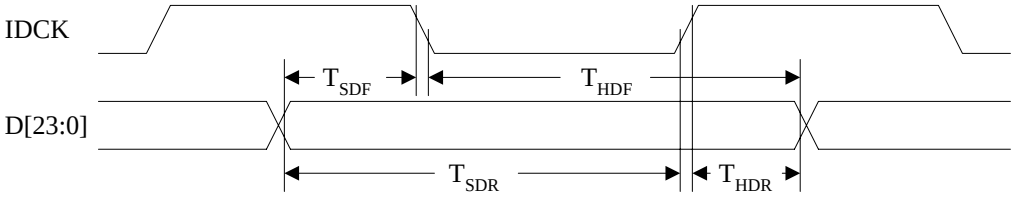


Figure 8-14. Input Data Setup/Hold Times to IDCK of Transmitter

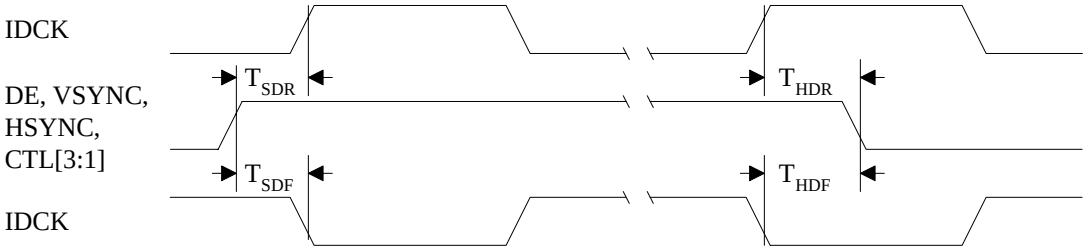


Figure 8-15. DE, VSYNC, HSYNC, and CTL[3:1] Setup/Hold Times to IDCK of Transmitter

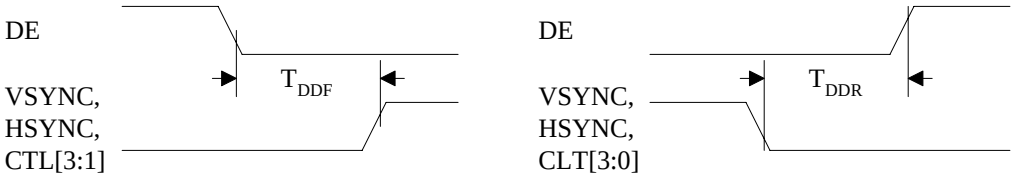


Figure 8-16. VSYNC, HSYNC, and CTL[3:1] Delay Times from DE of Transmitter

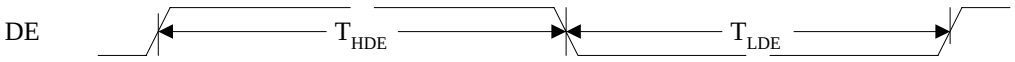


Figure 8-17. DE High/Low Times of Transmitter

Figure 8-18. PLL_SYNC Timing of Transmitter with SYNC_CONT = 1

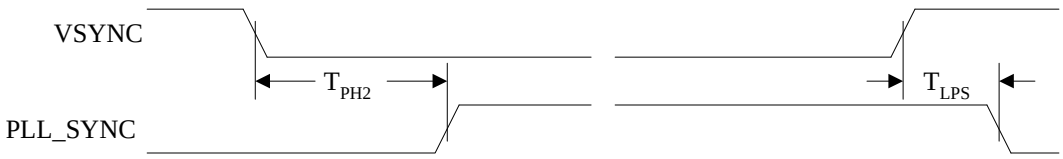


Figure 8-19. PLL_SYNC Timing of Transmitter with SYNC_CONT = 0

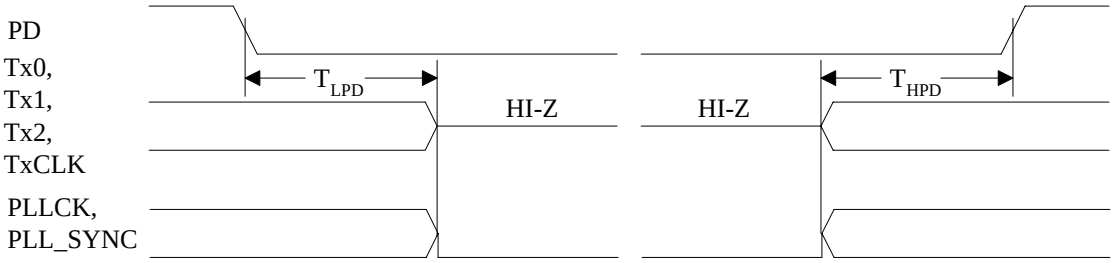


Figure 8-20. Output Signals Disabled/Enabled Timing from PD Active/Inactive from Transmitter

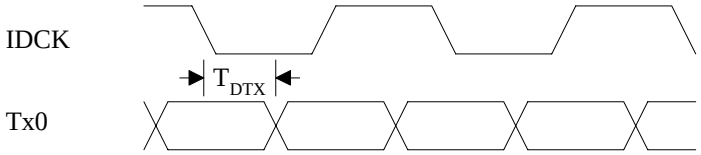


Figure 8-21. Differential Clock Delay from IDCK

8.8 Error Specification for TMDS Interface

Pixel Error Rate [1] 1 pixel error/2,000 frames (33 seconds)

HSYNC and VSYNC pulses are spread over a number of frames determined by the length of the pulse. The Pixel Error Rate is over one frame hence it is unlikely that a transmission error will affect more than a small percentage of the HSYNC or VSYNC pulse time.

8.9 Guidance for Display Controller Implementation

Line Error Rate [2] 1 pixel wide bit error/20,000 frames (5 min 33 seconds)
Full Frame Error Rate [3] 1 pixel wide bit error/200,000 frames (55 min 33 seconds)

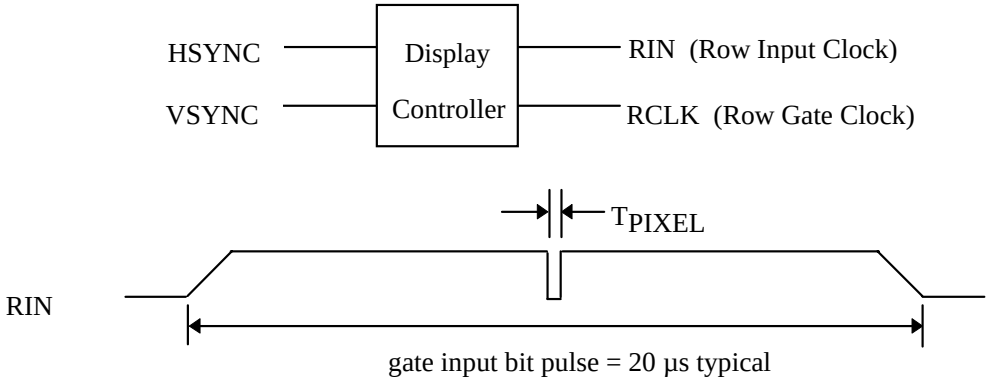


Figure 8-22: Line Error Rate

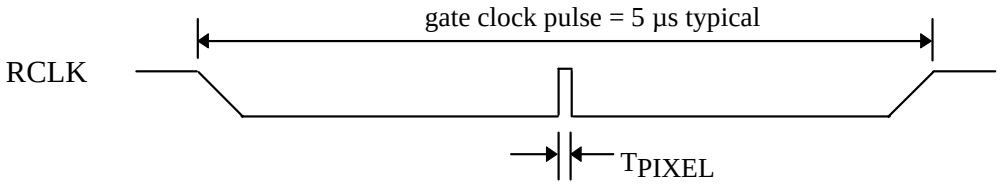


Figure 8-23: Full Frame Error Rate

Worst Case Effects:

[1] Pixel Error Rate results in single pixel off value.
[2] Line Error Rate Results in display error data on one line.
[3] Full Frame Error Rate results in one frame with random data displayed for the duration of refresh rate.

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