Video Electronics Standards Association

DisplayPort Panel Connector

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VESA DisplayPort Panel Connector Standard

Version 1.1
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Purpose

This specification shall serve as an alternative panel connector for various VESA panel standards. It defines the requirements for a standard DisplayPort connector for use in any standard panel that uses a 30-pin LVDS connector

Summary

This standard specifies connector mechanical dimensions as well as signal and data mapping for this connector.

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Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Table 1: Reference Documents

Source	Name	Version / Date
VESA	VESA DisplayPort Standard	Version 1.1 - March 19, 2007

Support

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product which incorporates any variant of DisplayPort, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

Fax: 408-957 9277, direct this note to Technical Support at VESA

Email: support@vesa.org

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Acknowledgements

This document would not have been possible without the efforts of the VESA Display Device Standards Committee's Monitor Panels Task Group. In particular, the following individuals and their companies contributed significant time and knowledge to this standard document.

Table 1 – Main Contributors

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Revision History

January 5, 2007 – Initial release of the standard

January 4, 2008 – Version 1.1 - Updated to specify position of pin 1 on the panel connector

1 Overview

1.1 Summary

This standard is provided as an adjunct to various VESA panel standards, extending those standards to embrace the VESA DisplayPort interface. The main Lanes configuration is taken from DP 1.1 to preserve the work that was done on the layout pattern for high speed signals. This standard is intended for display panels wanting to use the DisplayPort interface instead of LVDS. In case pin assignment of disagreement with original DisplayPort specification this specification takes precedence.

2 DisplayPort Panel Labeling Requirement

VESA Standard DisplayPort panels will use the same physical connector as VESA Standard LVDS panels (JAE FI-X30SSL-HF or equivalent). To ensure that VESA DisplayPort panels will not be accidentally connected to LVDS sources, panels conforming to this specification will prominently display a warning label or have an engraving in the chassis. Such warning labels or markings will be located as close to the panel's DisplayPort connector as practical.

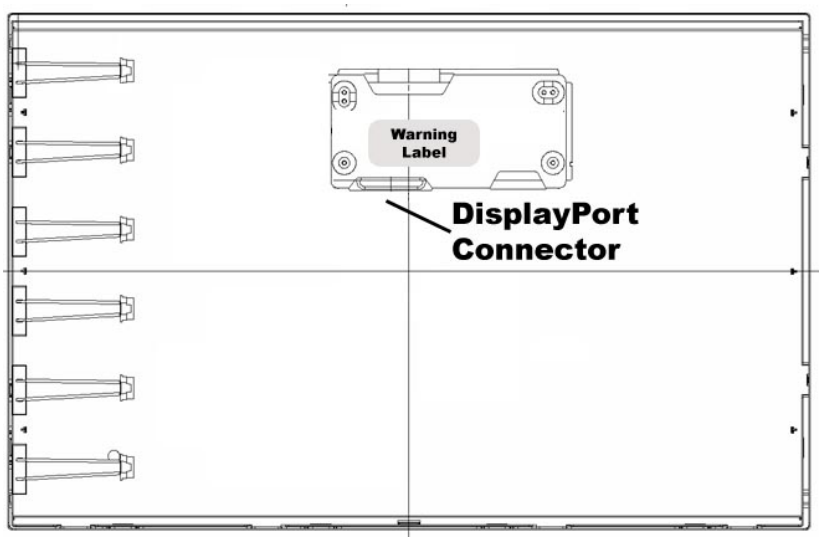


Figure 2-1: VESA DisplayPort Panel Showing Warning Label Affixed Near Connector

Figure 2-2: Example of a DisplayPort Label

3 Referencing Other VESA Standards

When referencing other VESA panel standards, please note that the panel layout illustrations in these standards are not consistent with respect to showing either all front or back views.

Therefore, care must be taken to ensure that you properly identify connector Pin 1 locations based on the call-out identifying the drawing orientation in the particular specification you are viewing.

4 DisplayPort Panel Connector

The DisplayPort internal panel connector is a 30-position, JAE FI-X-SSL or equivalent, cable-to-board, co-planar connector set. One side terminates the cable (Plug) and the other is attached to the PCB (Receptacle).

The connectors support up to four Main Link lanes (Lane 0 ~ Lane 3). In embedded connections, the cable connector assembly may support one, two, or four lanes depending on the bandwidth requirement of the application. For one-lane and two-lane Main Link configurations, the stuffing rule shall be as follows:

- When only two lanes are needed, Lane 0 and Lane 1 shall be populated while Lane 2 and Lane 3 are unpopulated.
- When only one lane is needed, Lane 0 shall be populated while Lanes 1, 2 and 3 are unpopulated.

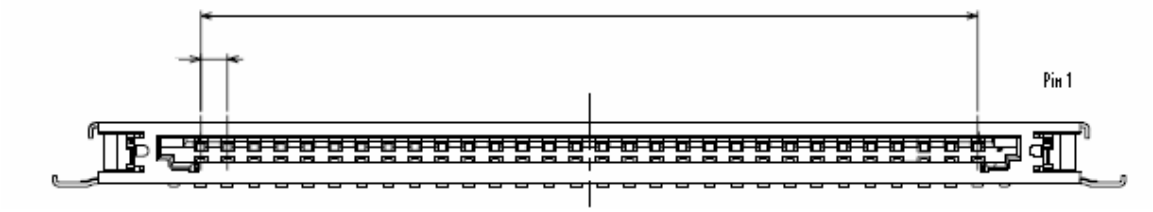
Only the panel TCON (timing controller) side of the connector is defined in this specification. While some cables may have the same connectors on both ends of the cable-connector assembly, others may have more pins for the source side (that is, the side of graphics processor, LCD controller, etc.) for LCD backlight control, for instance.

Table 4-1: DisplayPort Panel Connector Pin Assignment

Panel Standard Pin #	Pin Name	Pin Definition
Frame		Outer shell
1	Reserved	
2	LCDVCC	Power to LCD panel.
3	LCDVCC	
4	LCDVCC	
5	LCDVCC	
6		Power Return (Ground)
7		
8		
9		
10	Hot Plug Detect	Hot Plug Detect Optional
11	Reserved	
12	Reserved	
13	H_GND	High Speed (Main Link) Ground
14	ML_Lane 3(n)	'Complement' Signal-Main Link
15	ML_Lane 3(p)	'True' Signal-Main Link
16	H_GND	High Speed (Main Link) Ground
17	ML_Lane 2(n)	'Complement' Signal-Main Link
18	ML_Lane 2(p)	'True' Signal-Main Link
19	H_GND	High Speed (Main Link) Ground
20	ML_Lane 1(n)	'Complement' Signal-Main Link
21	ML_Lane 1(p)	'True' Signal-Main Link
22	H_GND	High Speed (Main Link) Ground
23	ML_Lane 0(n)	'Complement' Signal-Main Link
24	ML_Lane 0(p)	'True' Signal-Main Link
25	H_GND	High Speed (Main Link) Ground
26	AUX_CH (p)	'True' Signal – Auxiliary channel
27	AUX_CH (n)	'Complement' Signal – Auxiliary
28	H_GND	High Speed (Main Link) Ground
29	DP PWR Out	+3.3 PWR out
30	Reserved	
Frame		Outer shell

4.1 DisplayPort Panel Receptacle Connector

The figures below show the drawings of DisplayPort panel-side internal PCB receptacle connector and the recommended footprint layout, respectively. Pin 1 is declared on the right side as you face the connector. This will allow for straight ribbon cable connections with Pin 1 for the TX on the left hand side of the facing circuit board.



RX Signal Connector with Pin 1 designation shown

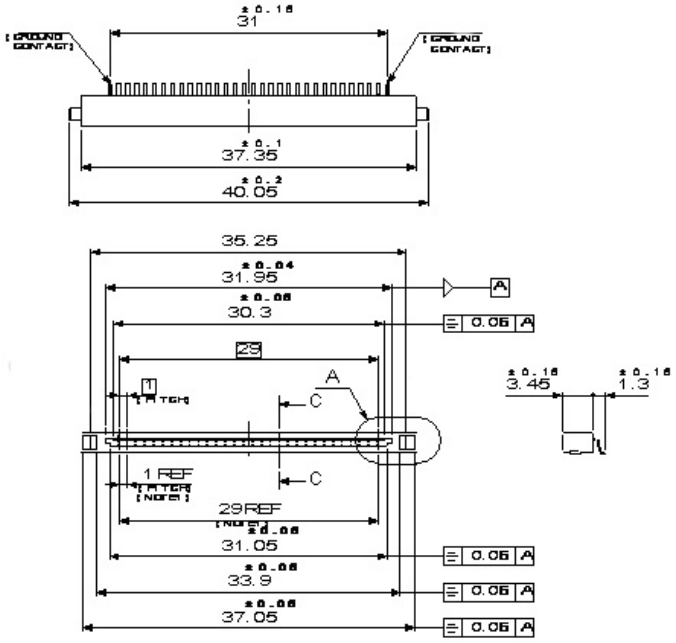


Figure 4-1: Panel PCB Mount Receptacle

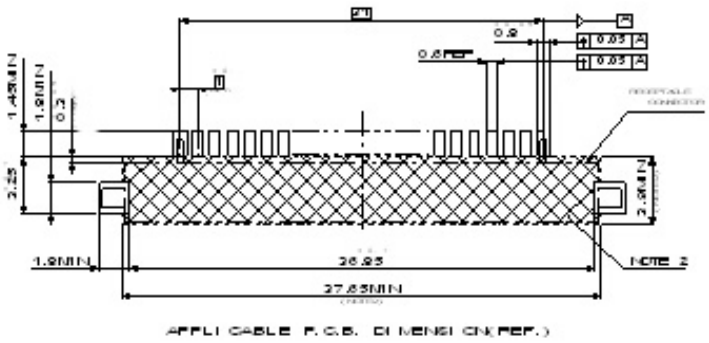


Figure 4-2: PCB Mount Connector Recommended Footprint Layout

4.2 DisplayPort Panel Mating Plug Connector

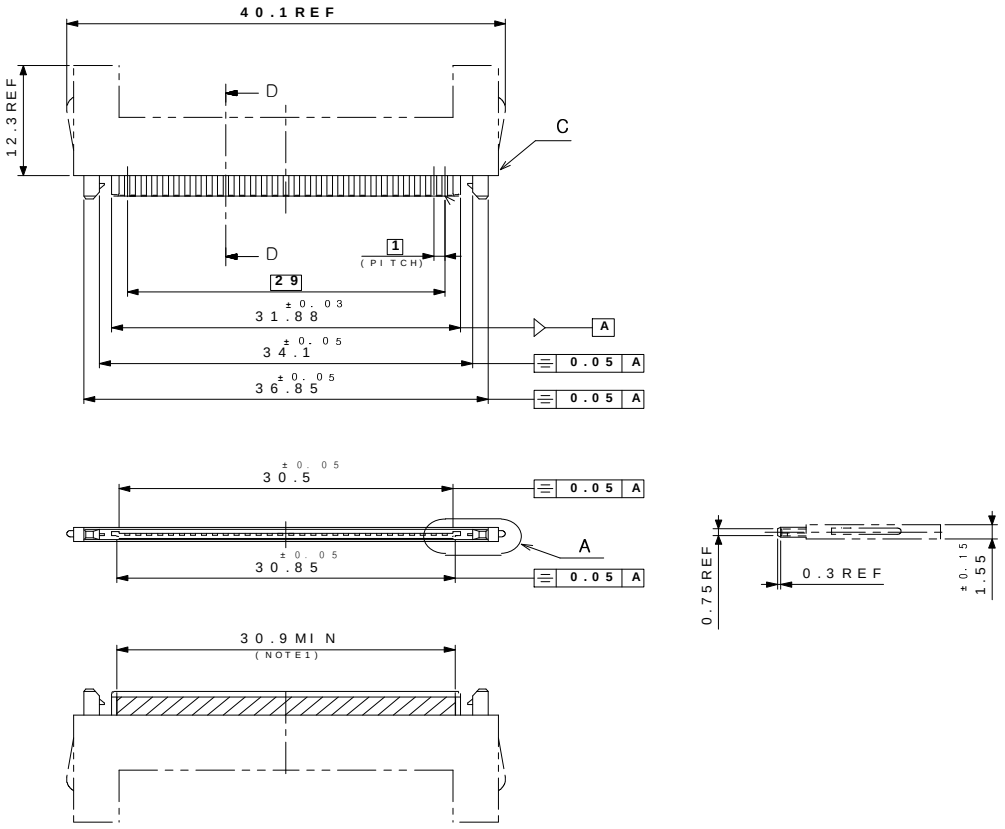


Figure 4-3: DisplayPort Panel Plug Connector

The Figures below show the contact and mechanical guide details of DisplayPort internal plug connector Contact and mechanical guide details

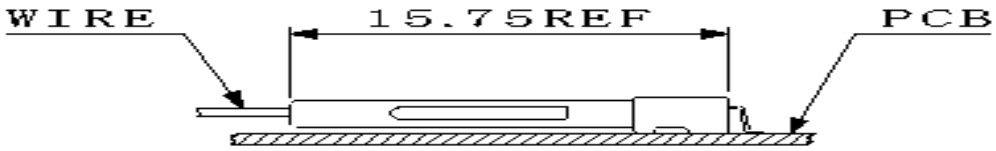


Figure 4-4: Plug and Receptacle Shown Mated

The table below describes the mechanical requirements of the DisplayPort panel connector.

Table 4-2: Panel Side Connector Electrical Requirements

Item	Test Condition	Requirement
Vibration (Random)	Frequency: 10Hz to 2000Hz Acceleration Vel. 30.38m/s^2 (3.1G) RMS. Action direction: In each of 3 mutually perpendicular planes. Duration: 15 minutes each sample. EIA-364-28, Test condition VII, test condition D.	100mA applied with no electrical discontinuity greater than 1µ sec.
Physical Shock	Sample should be mounted on the test jig as mounted on the PCB. Acceleration velocity 490m/s^2 or 50G. Waveform: half sine Duration:11 msec. Number of drops: 3 drops each to normal and reversed directions of X,Y and Z axis. Total 18 drops. EIA-364-27B method A	No electrical discontinuity greater than 1 µ sec. shall occur.
Durability (mating and unmating).	Number of cycles: 50 Automatic Cycling: 100 ± 50 cycles per hour EIA364-09C	R = 40mΩ Max. (Initially) ΔR = 20 mΩ Max. (Final)
Durabilty (preconditioning)	Number of cycles: 20 EIA-364-09C	No Physical Damage.
Connector Insertion Force	Operation speed :12.5mm/min Measure the force required to mate connector including the latching mechanism. EIA-364-13B	35N (2.55kgf) Max. per connector (30) pin
Connector Withdrawal Force	Operation speed :12.5mm/min Measure the force required to unmate connector excluding the latching mechanism. EIA-364-13B	5 N minimum to 25 N maximum (30) connector

The table below describes the electrical properties of the DisplayPort panel connector.

Table 4-3: DisplayPort Panel Connector Electrical Properties

Item	Test Condition	Requirment
Dielectric withstanding voltage	0.25 kVAC for 1 minute Test between adjacent circuits of unmated connectors. EIA364-20C	No creeping discharge or flashover shall occur. Current leakage : 0.5 mA Max.
Insulation Resistance	Impressed voltage 100 VDC Test between adjacent circuits of unmated connectors for 2 minutes. EIA-364-21C	100 MΩ Min (initial) 50 MΩ Min. (final)
Low Level Contact Resistance	Subject mated contacts assembled in housing measured by dry circuit 20mV maximum open circuit at 10 mA (EIA-364-23B)	R = 40mΩ Max. (initial) ΔR = 40mΩ Max. (final)
Temperature Rise	Measure temperature rise by energizing current EIA-364-70A method 1	30ºC max. under loaded rated current.

The table below lists DisplayPort panel connector environmental requirements

Table 4-4: DisplayPort Panel Connector Environmental Requirements

Item	Test Condition	Requirement
Humidity and Temperature Cycling	Cycle Mated connector,25ºC to 65ºC and 50% to 80% R.H. 10 cycles and 10 cycles of cold shock at -10ºC per EIA-364-31B method 4	Mating Condition: Contact Resistance: R = 80mΩ Max. (final) Unmating condition: Insulation resistance R = 50MΩ Min. (final) ΔR = 50MΩ Max.
Thermal Shock	Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes repeat for 10 cycles. EIA-364-32	R = 40mΩ minimum (initial) ΔR = 40mΩ Max. (final)
Temperature Life (heat age)	Submit mated connector to 105ºC for 168 hours. EIA-364-17B	R = 40mΩ Max. (initial) ΔR = 40mΩ Max. (final)
Temperature Life (preconditioning)	Submit mated connector to 105ºC for 92 hours. EIA-364-17B	No physical damage allowed