Video Electronics Standards Association

DisplayPort™ Link Layer Compliance Test Standard

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VESA DisplayPort™ Link Layer Compliance Test Standard

Version 1.0

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Purpose

The purpose of this document is to define a compliance test procedure and criteria (or masks) to maximize the interoperability of DisplayPort devices at the Link Layer and above.

Summary

This document specifies the DisplayPort Link Layer and above compliance tests for Source, Sink and Branch devices.

Preface

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Holder Name	Contact Information	Claims Known
AMD	Raymond Li (raymond.li@amd.com)	U.S. Patent Application: 60/895,645

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Revision History

September 14, 2007	Initial release of the standard

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1 Introduction

1.1 Scope of This Document

This document is intended for box-to-box connections. While this does not preclude the use of some or all of the specified equipment and/or test cases for embedded connections, this document does not make any attempt to fully cover the feature requirements of embedded connections or to limit the test cases to those features that are available in embedded systems.

This document is only intended to cover the DisplayPort Link Layer and above (see 'Introduction' for more information). The PHY layer is covered by the DisplayPort (PHY Layer) Compliance Test Specification.

The DisplayPort Link Layer Compliance Test Specification Version 1 will not include tests for DisplayPort secondary packets (including Audio Sample Packets) other than the mandatory MSA field. DisplayPort secondary packets will be covered in a future version of the DisplayPort Link Layer Compliance Test Specification.

1.2 DisplayPort Layers Covered in this Test Specification

DisplayPort has a layered, modular architecture as shown in Figure 1-1: Layered Architecture below to facilitate performance and feature extensibility. This document describes the compliance test specification for DisplayPort Link Layer and above.

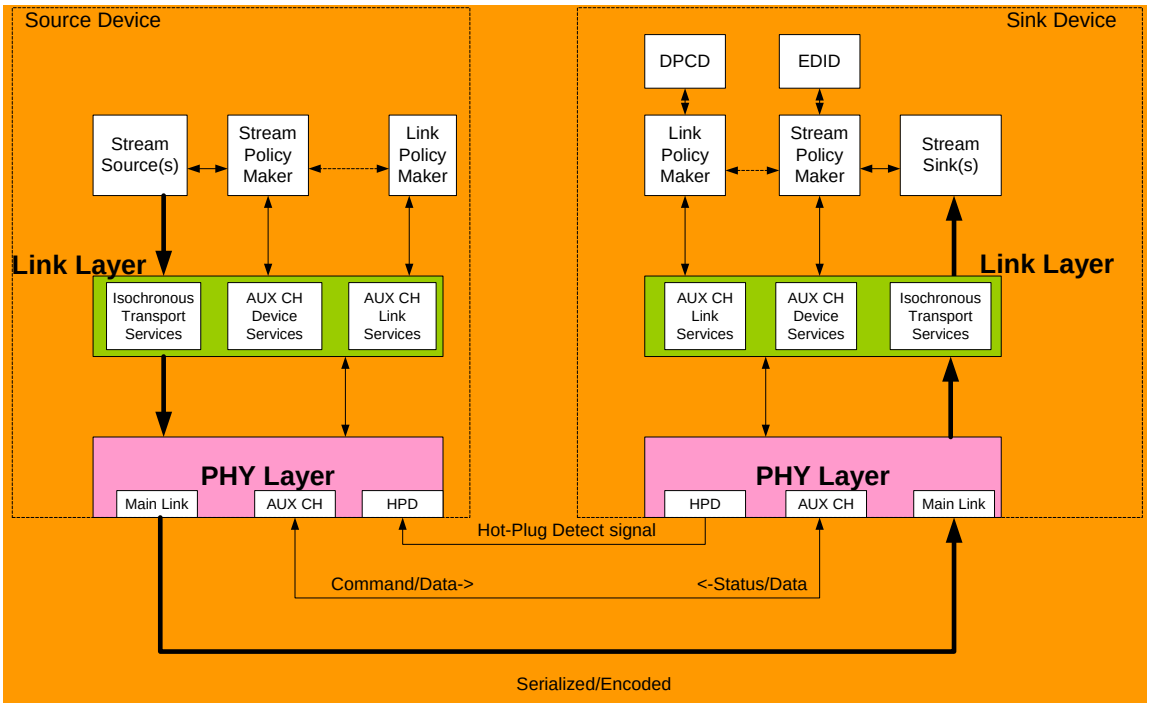

Figure 1-1: Layered Architecture

Link Layer provides Link/Device Services and Isochronous Transport Services as follows:

- Link and Device Services
    - Link Services are used for discovering, configuring, and maintaining the link. The AUX CH read/write access to DPCD (DisplayPort Configuration Data) field is used for these purposes.
    - Device Services support device-level applications such as EDID and MCCS access. Furthermore, Device Services may optionally include content protection.

Of these two, Link Services are to be tested in the DisplayPort compliance test. As far as Device Services are concerned, only I^2C-to-AUX CH streaming is tested.

- Isochronous Transport Services

  The Isochronous Transport Services map the video and audio streams onto the DisplayPort Main Link with a set of rules so that the streams can be properly reconstructed to the original format and time base in Sink Device. The Isochronous Transport Services provide for the following:

    1. Mapping of stream data to and from Main Link lanes
        - Packing/unpacking
        - Stuffing/un-stuffing
        - Framing/un-framing
        - Inter-lane skewing and de-skewing
    2. Stream clock recovery
    3. Insertion of Main Stream Attribute data

All of the Isochronous Transport Services functions above are tested in DisplayPort compliance test.

Source DUT is connected directly to Reference Sink Device. Sink DUT is connected directly to the Reference Source. Branch DUT (such as a cable extender) is connected to Reference Source and Sink Devices.

1.3 Organization of this Document

The DisplayPort Link Layer and Above Compliance Specification details the test procedures of Source, Sink and Branch Devices, and is organized into the following sections:

Section 1 – Introduction

This Section gives an overview of the DisplayPort architecture, and describes the Link Layer services that will be covered by the compliance testing.

Section 2 – Equipment for Compliance Test of Link Layer

This Section describes the test equipment that is used for the compliance testing – the Reference Source and Reference Sink, and their capabilities.

Section 3 – Compliance Test Operation

The compliance test operation Section describes the modes of operation, as well as a list of information that is required about the device under test. This Section also describes DPCD extensions to support automated compliance testing.

Section 4 – Source Device Test

The detailed test procedures for testing of Source devices are described in this Section.

Section 5 – Sink Device Test

The detailed test procedures for testing of Sink Devices are described in this Section.

Section 6 – Branch Device Test

The detailed test procedures for testing of Branch devices are described in this Section.

1.4 Acronyms

Acronym	Stands For:
bpc	Bits Per Component
bpp	Bits Per Pixel
CDR	Clock-to-Data Recovery
CEA	Consumer Electronics Association
CRC	Cyclic Redundancy Check
CVT	Coordinated Video Timing
DMT	Discrete Monitor Timing
DPCD	DisplayPort Configuration Data
DUT	Device Under Test
ECC	Error Correcting Code
EDID	Extended Display Identification Data
HPD	Hot Plug Detect line
IRQ_HPD	Interrupt Request sent over HPD line
lsb	least significant bit
Maud	M value for audio
MCCS	Monitor Command and Control Set
msb	most significant bit
Mvid	M value for video
Naud	N value for audio
Nvid	N value for video
VB-ID	Vertical Blanking ID
VESA	Video Electronics Standards Association

1.5 Glossary

Terminology	Definition
AUX CH	Half-duplex, bi-directional channel between DisplayPort transmitter and DisplayPort receiver. Consists of 1 differential pair transporting self-clocked data. The DisplayPort AUX CH supports a bandwidth of 1Mbps over DisplayPort link. DisplayPort Source Device is the master (also referred to as AUX CH Requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as AUX CH Replier) that replies to the AUX CH transaction initiated by the Requester.
Box-to-box connection	DisplayPort link between two boxes detachable by an end user. A DisplayPort cable-connector assembly for the box-to-box connection shall have four Main Link lanes.
bpc	Number of bits for each of R,G, B or Y, Cb, and Cr.
bpp	Number of bits for each pixel. For RGB and YCbCr444, the bpp value is 3x the bpc value. For YCbCr422, the bpp value is 2x the bpc value.
Branch Device	Devices located in between Root (Source Device) and Leaf (Sink Device). Those devices are: - Repeater Device, - DisplayPort-to-Legacy Converter, - Legacy-to-DisplayPort Converter, - Replicater Device, - Composite Device.
CEA range	Nominal zero intensity level at 16 for 24-bpp, 64 for 30-bpp, 256 for 36-bpp, and 1024 for 48-bpp. Maximum intensity level at maximum code value allowed for bit depth, namely, 235 for 24-bpp RGB, 940 for 30-bpp RGB, 3760 for 36-bpp RGB, and 15040 for 48-bpp RGB. Note that the RGB CEA range is defined for 24, 30, 36, 48 bpp RGB only, not for 18-bpp RGB.
DisplayPort receiver	Circuitry that receives the incoming DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in a device with DisplayPort Sink Function.
DisplayPort transmitter	Circuitry that transmits the DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH. Located in a device with DisplayPort Source Function.
DisplayPort Configuration Data (DPCD)	Mapped to the DisplayPort address space of DisplayPort Sink Device. DisplayPort Source Device reads the receiver capability and status of the DisplayPort link and the Sink Device from DPCD address. Furthermore, DisplayPort Source Device writes to the link configuration field of DPCD for configuring and initializing the link.
Down-spread	Spreading a clock frequency downward from a peak frequency.
Embedded connection	DisplayPort link within a box that is not to be detached by an end user. DisplayPort cable for the embedded connection may have one, two, or four Main Link lanes.
HPD	The HPD (Hot Plug Detect) line is used to indicate when a Sink device is connected and ready to accept AUX CH requests. A logic ‘1’ (high) on the HPD line indicates that the sink is connected. A logic ‘0’ (low) on the HPD line of duration greater than 2ms indicates that the Sink Device is disconnected or unable to accept AUX CH requests.
IRQ_HPD	Interrupt Request on HPD line. The HPD (Hot Plug Detect) line, which is used to indicate when a Sink Device is connected and ready to accept AUX CH requests, is also used by the Sink Device to send interrupt requests when in the connected (logic ‘1’ or ‘high’) state.

	The Sink Device issues IRQs (interrupt requests) to the Source device by generating low-going HPD pulses of 0.5ms ~ 1ms in duration. Upon detecting this "IRQ HPD pulse", Source device shall read link/sink status field of DPCD and take corrective action.
Idle Pattern	Link symbol pattern sent over the link when the link is active with no stream data being transmitted.
Link Layer	Server providing services as instructed/requested by the Stream-/Link-Policy Makers.
Link Policy Maker	Manages the link and is responsible for keeping the link synchronized. All DisplayPort Devices shall have Link Policy Maker.
Main Link	Uni-directional channel for isochronous stream transport from DisplayPort Source Device to DisplayPort Sink Device. Consists of 1, 2, or 4 lanes, or differential pairs. Supports 2 bit rates: 2.7Gbps per lane (referred to as "high bit rate") and 1.62Gbps per lane (referred to as "low bit rate" or "reduced bit rate").
Main Stream Attributes	Attributes describing the main video stream format in terms of geometry and color format. Inserted once per video frame during the video blanking period. Used by DisplayPort receiver for reconstructing the stream.
Root Device	Source Device, located at a root in a DisplayPort tree topology.
Secondary Data	Data transported over Main Link that are not main video stream data. Audio data and InfoFrame packet are examples.
Sink Device	Contains one Sink Function and at least one Rendering Function, and is a Leaf Device in a DisplayPort tree topology.
Sink Function	Sink functionality (reception of stream) of DisplayPort
Source Device	Contains one or more Source Functions and is a root in a DisplayPort tree topology.
Source Function	Source functionality (transmission of stream) of DisplayPort
Stream Clock	Used for transferring stream data into DisplayPort transmitter within DisplayPort Source Device or from DisplayPort receiver within DisplayPort Sink Device. Video and audio (optional) are likely to have separate stream clocks
Stream Clock Recovery	Operation of recovering the stream clock from the Link Symbol Clock.
Stream Policy Maker	Manages how to transport an isochronous stream.
Symbol	There are Data Symbols and Control Symbols. Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as "ANSI 8B/10B" in this document) before being transmitted over a link. In addition to data symbols, DisplayPort Version 1.1 defines nine Control Symbols for framing Data Symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).
Transfer unit (TU)	Used to carry main video stream data during its horizontal active period. TU has 64 symbols per lane (except for at the end of the horizontal active period), each consisting of active data symbols and fill symbols.
Trickle Power	Power for Sink Device that is sufficient to let Source device read EDID via AUX CH, but insufficient to enable Main Link and other Sink functions. For Sink to drive Hot Plug Detect (HPD) signal high, at least the trickle power must be present. The amount of power needed for the trickle power is Sink implementation specific.
VB-ID	Data symbol indicating whether the video stream is in vertical blanking interval, whether video stream is transported, and whether to mute audio.
VESA range	Nominal zero intensity level at code value zero. Maximum intensity level at maximum code value allowed for bit depth, Namely, 63 for 18-bpp RGB, 255 for 24-bpp RGB, 1023 for 30-bpp RGB, 4095 for 36-bpp RGB, and 65,535 for

	48-bpp RGB.
Video Horizontal Timing	Horizontal timing means video line timing. For example, horizontal period and horizontal sync pulse mean line period and line sync pulse, respectively.
Video Vertical Timing	Vertical timing means video frame (or field) timing. For example, vertical period and vertical sync pulse mean a frame (or field) period and a frame sync pulse, respectively. The terms, "horizontal" and "vertical", do not necessarily correspond to the physical orientation of a display device. For instance, a line may be oriented vertically on a "portrait" display.

1.6 References

Document	Version/revision	Date
CEA, A DTV Profile for Uncompressed High Speed Digital Interface	861-D	July 18, 2006
VESA, Enhanced Extended Display Identification Data Standard (E-EDID)	Release A, Rev. 2	September 25, 2006
VESA DisplayPort Standard	Version 1.1	March 19, 2007
VESA Enhanced Display Data Channel Standard (E-DDC)	Version 1.1	March 24, 2004
VESA DisplayPort PHY Compliance Test Standard	Version 1.0	(not yet published)
Video Demystified (by Keith Jack)	Fourth Edition	2005
ITU-R BT.709 Parameter values for the HDTV standards for production and international programme exchange	5	April 2002
ITU-R BT.601 Studio encoding parameters of digital television for standard 4:3 and wide screen 16:9 aspect ratios	5	October 1995

2 Equipment for Compliance Test of Link Layer and Above

This Section describes the equipment required for conducting the compliance test of DisplayPort Link Layer and above.

One or both of the following two pieces of equipment are required:

- Reference Sink (required for Source DUT, Branch DUT testing)
- Reference Source (required for Sink DUT, Branch DUT testing)

2.1 Reference Sink

Reference Sink, which is used for testing a Source or Branch DUT, shall have the following capabilities:

- Link Capabilities
    - Issue interrupt request (IRQ) by generating IRQ HPD pulse as needed.
    - Update the DPCD content on the fly as controlled by Reference Sink Control Tool.
    - Support 1, 2, 4 lane Main Link configurations as indicated in DPCD content
    - Support high bit rate (2.7Gbps per lane) and reduced bit rate (1.62Gbps per lane) as indicated in DPCD content.
        - Down-spread of 0.5% shall be also supported.
    - Support synchronous and asynchronous clock modes.
    - Implement some method of detection of active vs. inactive lanes
    - Implement some method to detect whether the link rate is the low bandwidth rate (162 MHz) or high bandwidth rate (270 MHz)
- Stream Sink Capabilities
    - Update the EDID content on the fly.
    - Support all the video formats specified in VESA DMT/CVT standards, CEA 861-D standard, and 1366x768 video format.
    - Support all the colorimetry formats and pixel bit depths specified in DisplayPort Version.1.1 specification (up to 48 bpp).
    - Support all the audio formats specified in DisplayPort Version 1.1.
    - Support the Sink Device requirement for visual-/audible-glitch-free operation upon stream format change as specified Section 5.2.3 of DisplayPort Standard Version 1.1.

The link/stream sink capabilities of Reference Sink shall be controlled by a control tool connected to it (called “Reference Sink Control Tool”).

The Reference Sink should not need to implement any complex analog measurements. For example, verification that the voltage swing and pre-emphasis on the differential pairs matches the values reported by the Source DUT is not required. The Reference Sink is required to detect whether the link bandwidth is ‘low’ or ‘high’ and whether the Source DUT has not enabled any of the channels it has reported are disabled. However, these checks do not have to be implemented in a sophistication fashion. For example, the Reference Sink could simply try to achieve CR lock on the lanes reported to be inactive and give an error if CR lock is achieved.

Note: For each video format, all of the colorimetry formats and pixel bit depths specified in DisplayPort Version 1.1 specification shall be supported.

2.2 Reference Source

Reference Source, which is used for testing a Sink or Branch DUT, shall have the following capabilities:

- Link Capabilities
    - Detect the status change of HPD signal and take appropriate corrective action.
    - Support 1, 2, 4 lane Main Link configurations
    - Support high bit rate (2.7Gbps) and reduced bit rate (1.62Gbps).
    - Support 0% and 0.5% down-spread.
    - Support synchronous and asynchronous clock modes.
    - Support all four levels of pre-emphasis and voltage swing
- Stream Source capabilities
    - Initiate one or multiple AUX CH transactions including DPCD read/write and EDID read).
    - Support all the video formats specified in VESA DMT/CVT standards and CEA 861-D standard and 1366x768 format.
    - Support adjustment of pixel rate via Source Control Tool.
    - Support all the colorimetry formats and color depths specified in DisplayPort Version 1.1 specification.
    - Support all the audio formats specified in DisplayPort Version 1.1 specification,
    - Support the source device requirement for visual-/audible-glitch-free operation upon stream format change as specified Section 5.1.3 of DisplayPort specification Version 1.1.

The link/stream source capabilities of Reference Source shall be controlled by a control tool connected to it (called “Reference Source Control Tool”).

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3 Compliance Test Operation

Two modes of test operation are possible:

1) Pass/fail mode – where only the final outcome of the test is logged

2) Debug mode – where final outcome, as well as any warnings and debug information, are logged.

Pass/fail criteria are listed at the end of each test. There are also intermediate conditions to be verified during the execution of a test which are listed within the test procedures. The test should attempt to continue even if certain test conditions are not met. These failing test conditions are logged as warnings in the debug mode operation.

The following notation is used for pass/fail/debug conditions:

- Checks listed as 'Pass/Fail' are used to determine the outcome of the tests
- Checks listed as 'Note/Warning' are for debug purposes only.
- For each step in the test case, as well as the 'Results' section, each check is numbered.
- 'Pass1' indicates that the first check for the current test step is a pass/fail check; there should be an associated 'Fail1'
- 'Note3' indicates that the third check for the current test step is a check for information purposes only; there should be an associated 'Warning1'

To pass compliance it will be necessary to train successfully at all supported lane counts and with sufficient bandwidth to allow all supported video modes. The compliance test should be carried out with a cable assembly that meets the high bit rate specification in order to prevent signal integrity problems from affecting the test results.

For Source Devices, fill in the following table (Table 3-1) prior to executing the DisplayPort Source Device Compliance tests (one for each device tested).

Table 3-1: Source Device Capability Question List

Question	Answer
1. What is the maximum lane count supported?	
2. What is the maximum link rate supported?	
3. Which video timings and color formats are supported?	
4. If there are no video timings and color formats listed in the answer to question 3 (for example, this is a fixed timing or embedded device), list the preferred timing here.	Device Preferred timing: Resolution: Refresh Rate: Color Format: Interlaced / Progressive: Blanking Mode:
5. Is the DPCD extension for device test automation (see following sections) supported?	
6. Is spread spectrum clocking supported?	
7. Is video format change without link re-training supported?	

For Sink DUTs, fill in the following table (Table 3-2) prior to executing the DisplayPort Sink DUT Compliance tests (one for each device tested).

Table 3-2: Sink Device Capability Question List

Question	Answer
1. What is the maximum lane count supported?	
2. What is the maximum link rate supported?	
3. Which video timings and color formats are supported?	
4. If there are no video timings and color formats listed in the answer to question 3 (for example, this is a fixed timing or embedded device), list the preferred timing here.	Device Preferred timing: Resolution: Refresh Rate: Color Format: Interlaced / Progressive: Blanking Mode:
5. Is the DPCD extension for device test automation (see following sections) supported?	
6. List Receiver Capability Field contents (12 bytes)	

For Branch DUTs, fill in the following table (Table 3-3) prior to executing the DisplayPort Branch DUT Compliance tests (one for each device tested).

Table 3-3: Branch Device Capability Question List

Question	Answer
1. What is the maximum lane count supported?	
2. What is the maximum link rate supported?	
3. Is this device a repeater, concentrator or replicater?	
Repeater, Concentrator and Replicater Capability Question List The following section applies to devices that answered 'yes' to question 3 above	
4. Is there a local timing reference present in the branch device?	
5. List Receiver Capability Field contents (12 bytes)	

3.1 DPCD Field for Source Device Test Automation

3.1.1 Background

Optional test automation features have been added to allow Source Device testing with minimal test operator intervention. Automated tests are initiated by the Reference Sink using the HPD interrupt mechanism, which causes a Source Device that supports test automation to read the DPCD Link Status field, detect that a test automation request has been issued, and respond to the request.

Because test automation is optional, a DisplayPort version 1.1 compliant Source Device is not required to support test automation or to respond to Reference Sink test automation requests without test operator intervention.

3.1.2 Testing of Source DUTs that do not Support Test Automation

Source DUTs that do not support test automation will require test operator intervention to respond to requests issued by the Reference Sink. The Reference Sink shall provide a Graphical User Interface (GUI) to issue the same requests that would otherwise be issued via the Source Device Test Automation interface. The optional test duration limit feature should be disabled to ensure that the test operator will have time to configure the Source DUT to carry out the requested test. Where possible the Reference Sink may continue the test case automatically once it receives the expected response from the Source Device; otherwise a 'continue' button is required to allow the test operator to indicate when the Reference Sink should proceed with the test.

For link training tests, the GUI must be used to allow the Reference Sink to request the start of link training and report the desired link rate and number of lanes.

For video format tests, the GUI must be used to allow the Reference Sink to request the desired video mode. The test operator will select the requested video format and press the 'continue' button, which will cause the sink to complete the test.

3.1.3 Testing of Source DUTs that Support Test Automation

For Source DUTs that support test automation, it should be possible to run the compliance suite without test operator intervention. The optional test duration limit feature may be enabled to ensure that all tests complete even if one or more test cases(s) hang. This feature limits the duration of any test case to one second.

3.1.4 Test Automation Details

To support test automation, a new interrupt is added to DEVICE_SERVICE_IRQ of DPCD in DisplayPort Specification Ver.1.1. The Reference Sink shall configure the DPCD test request field to indicate the test mode requested. To initiate a test mode, the Reference Sink shall set the TEST_REQ bit and toggle IRQ HPD pulse. There are three test modes defined for Link Layer Compliance Test:

1) Link training test mode, with TEST_LINK_TRAINING set to 1,

2) Test pattern generation, with TEST_PATTERN set to 1,

3) EDID read test mode, with TEST_EDID_READ set to 1.

Upon detecting IRQ HPD pulse, the Source DUT shall read the TEST_REQ bit of DPCD. If TEST_REQ is set to 1, the Source DUT shall read TEST_REQUEST to see which test mode is being requested.

If TEST_REQUEST.TEST_LINK_TRAINING = 1, a link training test is being requested. The Reference Sink populates the TEST_LANE_COUNT and TEST_LINK_RATE with the desired lane count and link rate respectively. The Source DUT shall read the TEST_LANE_COUNT and TEST_LINK_RATE fields, and begin link training at the requested lane count and link rate.

Note: It is assumed that the Reference Sink has knowledge of the lane count and link rates that are supported by the Source DUT.

If TEST_REQUEST.TEST_PATTERN = 1, a test pattern is being requested. The Source DUT shall read the test request field in DPCD (offset 00221h to 00234h) to determine if it can support the test mode requested by the Reference Sink.

The test request field (offset 00221h to 00224h) for test pattern request in DPCD is the same as the main stream attribute data, except:

- A test refresh rate is specified (instead of M and N values)
- Interlacing is specified
- Test ACK / NACK bit is defined

All the DPCD fields required to support this new interrupt are defined in Table 3-4.

If the test mode requested is supported, the Source DUT shall start transmitting the TEST_PATTERN in the test mode requested, and set the TEST_ACK bit in the TEST_RESPONSE register.

If the test mode requested is not supported, the Source DUT shall signal a negative acknowledgement by setting the TEST_NAK bit in the TEST_RESPONSE register.

The Source DUT must acknowledge the interrupt by writing to the TEST_RESPONSE register within 5 seconds of IRQ HPD pulse detect.

To indicate the end of the test mode, the Reference Sink shall generate an IRQ HPD pulse, and set TEST_REQUEST.TEST_PATTERN = 0.

If TEST_REQUEST.TEST_EDID_READ = 1, an EDID read test is being requested. The Source DUT shall read the EDID of the Reference Sink (including any EDID extension blocks), write the EDID checksum to TEST_EDID_CHECKSUM and set the TEST_RESPONSE.TEST_EDID_CHECKSUM_WRITE bit. The TEST_EDID_CHECKSUM will also reflect the checksum of the last EDID block that was read by the Source DUT. After the EDID read has completed, the Source DUT shall also send the color square test pattern.

Table 3-4: DPCD Field for Source Device Test Automation in DisplayPort Standard Ver.1.1

DisplayPort Address	Definition	Read/Write over AUX Ch.
00201h	DEVICE_SERVICE_IRQ_VECTOR Bit 0 = RESERVED for REMOTE_CONTROL_COMMAND_PENDING When this bit is set to 1, Source Device shall read the Device Services Field for REMOTE_CONTROL_COMMAND_ PASS_THROUGH. Bit 1 =AUTOMATED_TEST_REQUEST When this bit is set to 1, Source Device shall read Addresses 00218h - 0027Fh for requested link test. Bit 2 = CP_IRQ This bit is used by an optional content protection system. Bits 5:3 = RESERVED. Read all 0's.	Read only

	Bit 6 =SINK_SPECIFIC_IRQ Usage is vendor-specific. Bit 7 = RESERVED. Read 0.	
Test Request Field		
00218h	TEST_REQUEST Test requested by the Sink Device. All other values reserved. Bit 0 = TEST_LINK_TRAINING 0 = no link training test requested 1 = link training test requested. See TEST_LINK_RATE and TEST_LANE_COUNT for link rate and lane count requested respectively. Bit 1 = TEST_PATTERN 0 = no test pattern requested 1 = test pattern requested Bit 2 = TEST_EDID_READ 0 = no EDID read test requested 1 = EDID read test requested. Checksum of the last EDID block read is written to TEST_EDID_CHECKSUM. Source will also send color square test pattern. Bits 7:3 = RESERVED. Read all 0's.	Read only
00219h	TEST_LINK_RATE Bits 7:0 = TEST_LINK_RATE 06h = 1.62Gbps 0Ah = 2.7Gbps	Read only
00220h	TEST_LANE_COUNT Bits 4:0 = TEST_LANE_COUNT All other values reserved. 1h = one lane 2h = two lanes 4h = four lanes Bits 7:5 = RESERVED. Read all 0's.	Read only
00221h	TEST_PATTERN **Test pattern requested by the Sink Device** 01h = color ramps 02h = black and white vertical lines 03h = color square	Read only
00222h – 00223h	TEST_H_TOTAL Horizontal total of transmitted video stream in pixel count 00222h Bits7:0 = TEST_H_TOTAL Bits15:8 00223h Bits7:0 = TEST_H_TOTAL Bits7:0	Read only

00224h – 00225h	TEST_V_TOTAL Vertical total of transmitted video stream in line count 00224h Bits7:0 = TEST_V_TOTAL Bits15:8 00225h Bits7:0 = TEST_V_TOTAL Bits7:0	Read only
00226h – 00227h	TEST_H_START Horizontal active start from Hsync start in pixel count 00226h Bits7:0 = TEST_H_START Bits15:8 00227h Bits7:0 = TEST_H_START Bits7:0	Read only
00228h – 00229h	TEST_V_START Vertical active start from Vsync start in line count 00228h Bits7:0 = TEST_V_START Bits15:8 00229h Bits7:0 = TEST_V_START Bits7:0	Read only
0022Ah – 0022Bh	TEST_HSYNC Hsync width in pixel count 0022A Bit7 = TEST_HSYNC_POLARITY 0022A Bits6:0 = TEST_HSYNC_WIDTH Bits14:8 0022B Bits7:0 = TEST_HSYNC_WIDTH Bits7:0	Read only
0022Ch – 0022Dh	TEST_VSYNC Vsync width in line count 0022C Bit7 = TEST_VSYNC_POLARITY 0022C Bits6:0 = TEST_VSYNC_WIDTH Bits14:8 0022D Bits7:0 = TEST_VSYNC_WIDTH Bits7:0	Read only
0022Eh – 0022Fh	TEST_H_WIDTH Active video width in pixel count 0022Eh Bits7:0 = TEST_H_WIDTH Bits15:8 0022Fh Bits7:0 = TEST_H_WIDTH Bits7:0 E.g. 0x400 = 1024 active	Read only
00230h – 00231h	TEST_V_HEIGHT Active video height in line count 00230h Bits7:0 = TEST_V_HEIGHT Bits15:8 00231h Bits7:0 = TEST_V_HEIGHT Bits7:0 E.g. 0x300 = 768 active	Read only
00232h - 00233h	TEST_MISC 00232h Bits7:0 are the same definition as the miscellaneous field in the main stream attribute data (See DisplayPort Version 1.1 section 2.2.4, “Main Stream Attribute Data Transport”, p.64, “Miscellaneous”) 00232h Bit 0 = TEST_SYNCHRONOUS_CLOCK 0 = Link clock and stream clock asynchronous 1 = Link clock and stream clock synchronous 00232h Bits 2:1 = TEST_COLOR_FORMAT 00 = RGB 01 = YCbCr422 10 = YCbCr444 11 = Reserved	Read only

	00232h Bit 3 = TEST_DYNAMIC_RANGE 0 = VESA range (from 0 to the maximum) 1 = CEA range (as defined in CEA 861-D section 5 "Colorimetry") 00232h Bit 4 = TEST_YCBCR_COEFFICIENTS 0 = ITU601 (ITU-R BT.601-6, Section 3.5) 1 = ITU709 (ITU-R BT.709-5, Part 1 Section 6.10) 00232h Bits 7:5 = TEST_BIT_DEPTH Bit depth per color / component 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved 00233h Bit0 = TEST_REFRESH_DENOMINATOR 0 = 1 1 = 1.001 00233h Bit1 = TEST_INTERLACED 0 = non-interlaced 1 = interlaced 00233h Bits7:2 = RESERVED. Read all 0's.	
00234h	TEST_REFRESH_RATE_NUMERATOR Indicates the refresh rate requested by the Sink Device e.g. 60 = 60Hz numerator Refresh rate = TEST_REFRESH_RATE_NUMERATOR / TEST_REFRESH_RATE_DENOMINATOR	Read only
00235h – 0025Fh	RESERVED for test automation extensions	Reads all 0's
00260h	TEST_RESPONSE Bit 0 = TEST_ACK 0 = writing zero has no effect on TEST_REQ state 1 = positive acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to sink that source has started requested test mode. Bit 1 = TEST_NAK 0 = writing zero has no effect on TEST_REQ state 1 = negative acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to sink that source will not start requested test mode. Bit 2 = TEST_EDID_CHECKSUM_WRITE 0 = no write to TEST_EDID_CHECKSUM 1 = EDID checksum has been written to	Write

	TEST_EDID_CHECKSUM Bits 7:3 = RESERVED. Read all 0's.	
00261h	TEST_EDID_CHECKSUM In the TEST_EDID mode, the checksum of the last EDID block that was read is written here.	Write

Note: Support of this interrupt / DPCD test method is optional.

3.1.5 Test Pattern Definitions

Table 3-5 below shows the colorimetry formats that are supported by DisplayPort and which test pattern should be used for the compliance tests.

Table 3-5: Colorimetry Supported by Display Source DUT and Corresponding Test Patterns

Colorimetry Format	Bit-depth per pixel (bpp)	Bit-depth per component (bpc)	Dynamic Range	Test Pattern Used	Mandatory vs. Optional
RGB	18	6	VESA	Ramp	Mandatory
	24	8	VESA	Ramp	Mandatory
	30	10	VESA	Ramp	Optional
	36	12	VESA	Ramp	Optional
	48	16	VESA	Ramp	Optional
	24	8	CEA	Color square	Optional
	30	10	CEA	Color square	Optional
	36	12	CEA	Color square	Optional
	48	16	CEA	Color square	Optional
YCbCr422 (601 or 709 coefficients)	16	8	CEA	Color square	Mandatory if YCbCr supported
	20	10	CEA	Color square	Optional
	24	12	CEA	Color square	Optional
	32	16	CEA	Color square	Optional
YCbCr444 (601 or 709 coefficients)	24	8	CEA	Color square	Mandatory if YCbCr supported
	30	10	CEA	Color square	Optional
	36	12	CEA	Color square	Optional
	48	16	CEA	Color square	Optional

Note: This table is based upon the colorimetry support as outlined in the DisplayPort Standard.

The test data pattern can be generated in the Source DUT either in hardware or software, depending on the implementation of the Source DUT.

The test result is obtained by the Reference Sink automatically.

3.1.5.1 Color Ramp

When TEST_PATTERN = 0x1, the test data pattern used will consist of red, green, blue and white color ramps up, so visual anomalies can be seen easily. See Table 3-6.

Each color will be a ramp of 64 lines high, displayed sequentially (for example red, green, blue then white). Please see Table 3-6 below. For each line, the ramp is looped until the end of the line is reached. This is repeated until the end of the frame is reached. Note that the color ramp pattern is only defined for VESA dynamic range.

If there are two ramps defined, each ramp will be 32 lines high instead. See Figure 3-2.

Table 3-6: Color Ramp Test Pattern Definition

Colorimetry	Color Range (per color)	Thickness (lines)	Step size	Total Steps in Ramp
18 bpp RGB	0x00 -> 0x3F	64	0x1	64
24 bpp RGB	0x00 -> 0xFF	64	0x1	256
30 bpp RGB	Ramp 1: 0x180 -> 0x27F Ramp 2: 0x000 -> 0x3FC	32 32	0x1 0x4	256 256
36 bpp RGB	Fine ramp: 0x780 -> 0x87F Coarse ramp: 0x000 -> 0xFF0	32 32	0x1 0x10	256 256
48 bpp RGB	Fine ramp: 0x7F80 -> 0x807F Coarse ramp: 0x0000 -> 0xFF00	32 32	0x1 0x100	256 256

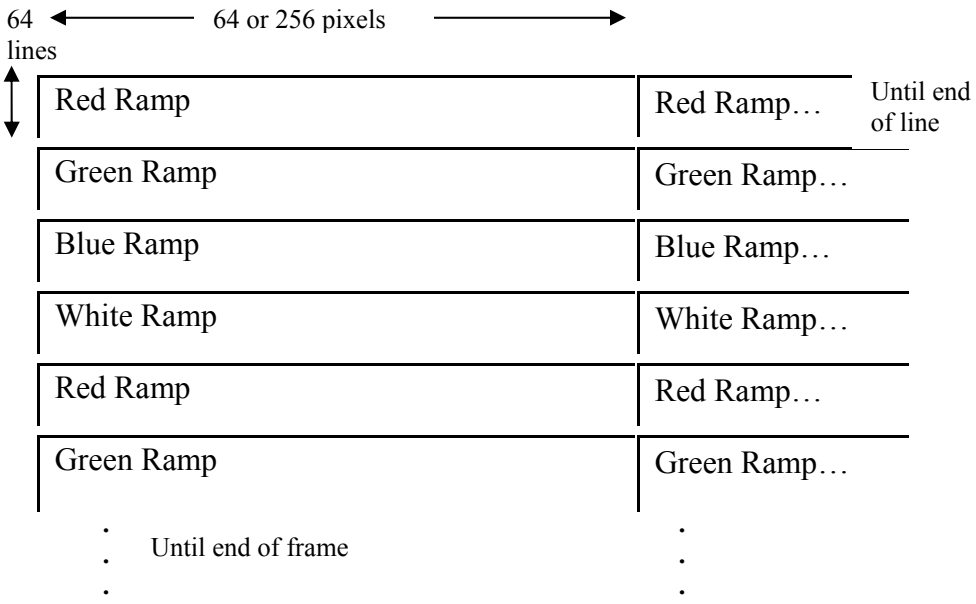

Figure 3-1: Color Ramp Test Pattern (One Ramp per Color)

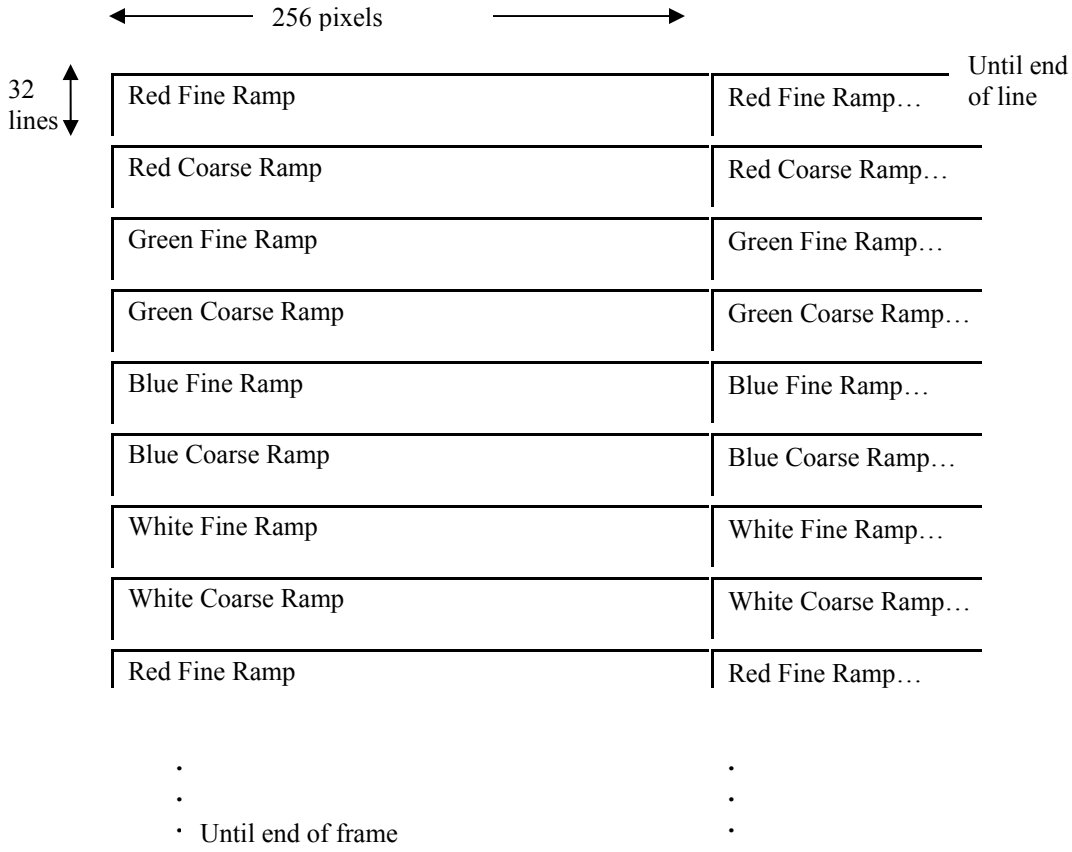

Figure 3-2: Color Ramp Test Pattern (Two Ramps per Color)

3.1.5.2 Black and White Vertical Lines

When TEST_PATTERN = 0x2, the black and white vertical line pattern is sent. This consists of alternating vertical lines of black and white, one pixel wide. Every line in the pattern is the same, alternating between black and white until the end of line is reached. **Note** that this pattern is defined only for VESA dynamic range. The black and white vertical line pattern is defined in Table 3-7.

Table 3-7: Black and White Vertical Lines

Colorimetry	Pattern specification
18 bpp RGB	R, G, B = 0x00 for 1 pixel R, G, B = 0x3F for 1 pixel
24 bpp RGB	R, G, B = 0x00 for 1 pixel R, G, B = 0xFF for 1 pixel
30 bpp RGB	R, G, B = 0x000 for 1 pixel R, G, B = 0x3FF for 1 pixel
36 bpp RGB	R, G, B = 0x000 for 1 pixel R, G, B = 0xFFF for 1 pixel
48 bpp RGB	R, G, B = 0x0000 for 1 pixel R, G, B = 0xFFFF for 1 pixel

3.1.5.3 Color Square

When TEST_PATTERN = 0x3, 100% color square test pattern is sent. The color square pattern consists of rows and columns of 64x64 pixel color squares. The first row is in this order: White, Yellow, Cyan, Green, Magenta, Red, Blue, and Black. This pattern is repeated horizontally.

The next row consists of 64x64 pixel color squares in the reverse order, but still with the Black square last: Blue, Red Magenta, Green, Cyan, Yellow, White, and Black.

This pattern is also repeated horizontally. These two row patterns are repeated vertically to the bottom of the frame. See Figure 3-3, Table 3-8, and Table 3-9 below.

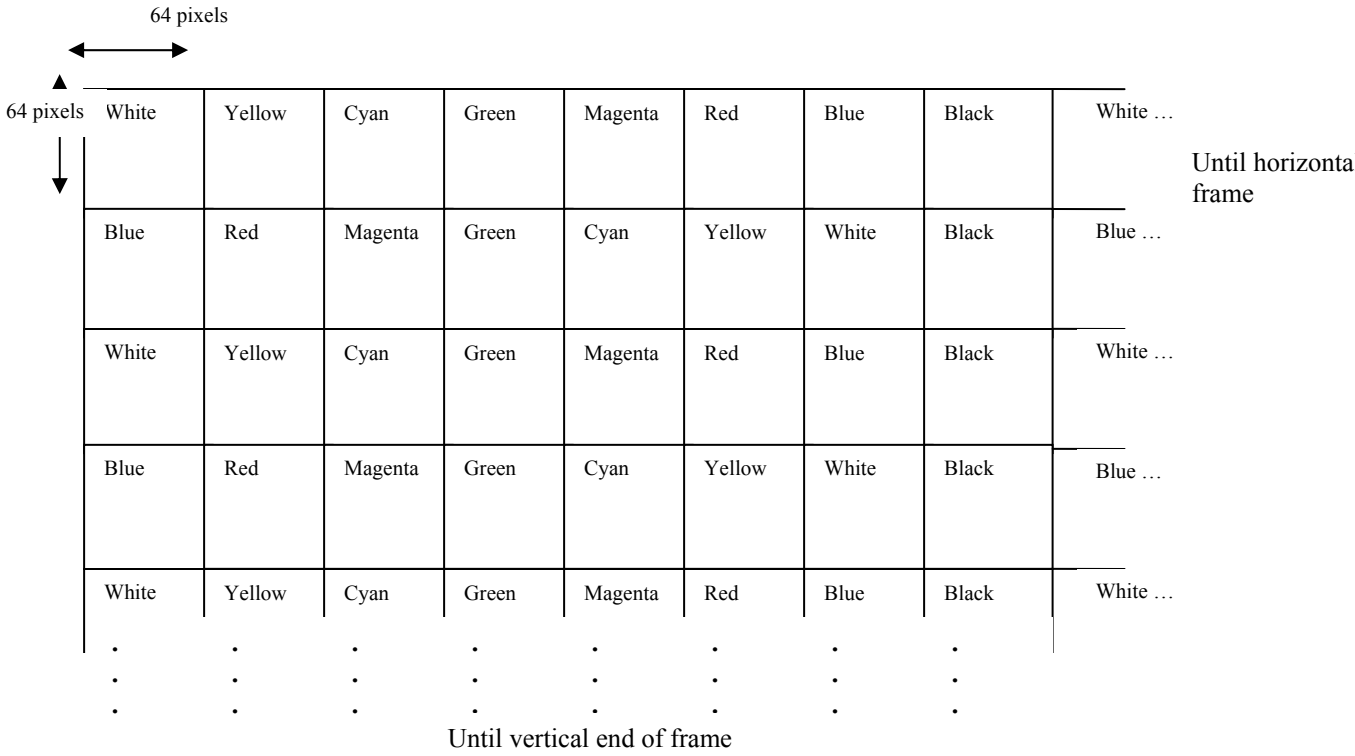

Figure 3-3: Color Square Test Pattern

Table 3-8: Color Square Definition in RGB

Colorimetry	Dynamic Range		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
18bpp RGB	VESA	R	63	63	0	0	63	63	0	0
		G	63	63	63	63	0	0	0	0
		B	63	0	63	0	63	0	63	0
24bpp RGB	VESA	R	255	255	0	0	255	255	0	0
		G	255	255	255	255	0	0	0	0
		B	255	0	255	0	255	0	255	0
24bpp RGB	CEA	R	235	235	16	16	235	235	16	16
		G	235	235	235	235	16	16	16	16
		B	235	16	235	16	235	16	235	16
30bpp RGB	VESA	R	1023	1023	0	0	1023	1023	0	0
		G	1023	1023	1023	1023	0	0	0	0
		B	1023	0	1023	0	1023	0	1023	0
30bpp RGB	CEA	R	940	940	64	64	940	940	64	64
		G	940	940	940	940	64	64	64	64
		B	940	64	940	64	940	64	940	64
36bpp RGB	VESA	R	4095	4095	0	0	4095	4095	0	0
		G	4095	4095	4095	4095	0	0	0	0
		B	4095	0	4095	0	4095	0	4095	0
36bpp RGB	CEA	R	3760	3760	256	256	3760	3760	256	256
		G	3760	3760	3760	3760	256	256	256	256
		B	3760	256	3760	256	3760	256	3760	256
48bpp RGB	VESA	R	65535	65535	0	0	65535	65535	0	0
		G	65535	65535	65535	65535	0	0	0	0
		B	65535	0	65535	0	65535	0	65535	0
48bpp RGB	CEA	R	60160	60160	4096	4096	60160	60160	4096	4096
		G	60160	60160	60160	60160	4096	4096	4096	4096
		B	60160	4096	60160	4096	60160	4096	60160	4096

Table 3-9: Color Square Definition in YCbCr

Colorimetry	Co-efficients		White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
8bpc YCbCr	601	Y	235	210	170	145	106	81	41	16
		Cb	128	16	166	54	202	90	240	128
		Cr	128	146	16	34	222	240	110	128
8bpcYCbCr	709	Y	235	219	188	173	78	63	32	16
		Cb	128	16	154	42	214	102	240	128
		Cr	128	138	16	26	230	240	118	128
10bpc YCbCr	601	Y	940	940	64	64	940	940	64	64
		Cb	940	940	940	940	64	64	64	64
		Cr	940	64	940	64	940	64	940	64
10bpc YCbCr	709	Y	940	840	678	578	426	326	164	64
		Cb	512	64	663	215	809	361	960	512
		Cr	512	585	64	137	887	960	439	512
12bpc YCbCr	601	Y	3760	3361	2712	2313	1703	1304	655	256
		Cb	2048	257	2651	860	3236	1445	3839	2048
		Cr	2048	2339	257	548	3548	3839	1757	2048
12bpc YCbCr	709	Y	3760	3508	3014	2761	1255	1002	508	256
		Cb	2048	257	2458	667	3429	1638	3839	2048
		Cr	2048	2213	257	422	3674	3839	1883	2048
16bpc YCbCr	601	Y	60160	53769	43397	37006	27250	20859	10487	4096
		Cb	32768	4119	42411	13762	51774	23125	61417	32768
		Cr	32768	37421	4119	8773	56763	61417	28115	32768
16bpc YCbCr	709	Y	60160	56123	48218	44182	20074	16038	8133	4096
		Cb	32768	4119	39327	10679	54857	26209	61417	32768
		Cr	32768	35403	4119	6754	58782	61417	30133	32768

Note: The RGB to YCbCr conversion equations are taken from "Video Demystified", Fourth Edition, by Keith Jack.

The following describes in further detail of the Color square generation:

---------- **example** ----------

Given:
HCount[8:0] : Horizontal position counter resets to 0x000 when DE (Data Enable)=0. Increments by one for each new pixel on a line while DE=1. Wraps back to 0x000 every 512 pixels on each line.
VCount[5:0] : Vertical position counter resets to 0x00 at each new frame (or top field). Increments by 1 at each DE falling edge for progressive modes, or by 2 for interlaced modes. Wraps back to 0x00 every 64 lines.

Color square pattern generator:

```
If VCount[5] == 0 Then
        SquareColor[2:0] <= HCount[8:6];
         // For lines 0-31 use top three bits of HCount to get color code
Else
        SquareColor[2:0] <= (not HCount[8:6]) – 1;
         // For lines 32-63 invert top three bits of HCount and subtract 1 to get color code
```

EndIf;

The output color can now be determined based upon the required color type (RGB or YCbCr) and dynamic range (CEA or VESA) and sample size (8, 10, 12, 16 bits/sample) and the above SquareColor[2:0] variable. The SquareColor is decoded as:
000 – White
001 – Yellow
010 – Cyan
011 – Green
100 – Magenta
101 – Red
110 – Blue
111 – Black
---------- **end of example** ----------

3.2 DPCD Field for Sink Device Test Automation

3.2.1 Background

Optional test automation features have been added to allow Sink DUT testing with minimal test operator intervention. Sink Device Test Automation allows the Reference Source to transmit standard test patterns with predefined CRC results computed using the CRC-16 LFSR described in this specification.

A Sink DUT that supports test automation internally computes the CRC and allows the Reference Source to read the CRC result through the Sink's DPCD. This allows the Reference Source to compare the Sink's computed CRC with the expected value, indicating whether the transmitted frame was received and decoded correctly.

Since the CRC is optional and only verifies that the video data was received correctly, the Reference Source must also provide a User Interface (UI) to allow the test operator to provide feedback indicating whether the transmitted image was displayed correctly for pass/fail. The UI will be used for Sink DUTs that do not support Sink Device Test Automation. The UI may optionally be used even for Sink DUTs that do support Sink Device Test Automation as an additional check to very that the image is displayed as expected.

Note: The visible image may be slightly modified by color space changes and / or dithering; this should not be considered a test failure unless the changes are major (i.e. pass / fail is somewhat subjective, but major image changes vs. the reference image should be considered a failure).

3.2.2 Testing of Sink DUTs that do not Support Sink Device Test Automation

For Sink DUTs that do not support Sink Device Test Automation, the visual check of the image will be the only method to verify that test patterns are displayed correctly.

3.2.3 Testing of Sink DUTs that Support Sink Device Test Automation

Sink DUTs that support Sink Device Test Automation may run the test sequences without test operator input; however, as noted above, the use of the optional test operator visual feedback mechanism will help to ensure that the image is received and displayed correctly.

3.2.4 Test Automation Details

To support test automation for the Sink DUT, a DPCD field is defined as shown in Table 3-10 below in DisplayPort Specification Ver.1.1. If this method is supported by the Sink DUT, the TEST_CRC_SUPPORTED bit in the TEST_SINK_MISC field shall be set to 1.

To start the test, the Reference Source will set the TEST_SINK_START bit in the TEST_SINK field. The Reference Source will send the test pattern, and calculate the expected CRC internally. The Sink DUT shall start calculating the CRC and storing them in the TEST_CRC_x_x fields. Each time the CRC values are updated, the TEST_CRC_COUNT is incremented. The CRC result is internally double buffered in the Sink DUT.

The Reference Source will read the TEST_CRC_x_x fields through the AUX channel, and compare those values to the internally calculated CRC values to determine if the Sink DUT has deconstructed the main stream properly.

To exit this test mode, the Reference Source will clear the TEST_SINK_START bit in the TEST_SINK field to terminate the test mode.

Table 3-10: DPCD Field for Sink Device Test Automation

DisplayPort Address	Definition	Read/Write over AUX Ch.
Test Request Field – Sink		
00240h-00241h	TEST_CRC_R_Cr Stores the 16 bit CRC value of the R or Cr component. 00240h bits 7:0 = CRC value bits 7:0 00241h bits 7:0 = CRC value bits 15:8	Read only
00242h-00243h	TEST_CRC_G_Y Stores the 16 bit CRC value of the G or Y component. 00242h bits 7:0 = CRC value bits 7:0 00243h bits 7:0 = CRC value bits 15:8	Read only
00244h-00245h	TEST_CRC_B_Cb Stores the 16 bit CRC value of the B or Cb component. 00244h bits 7:0 = CRC value bits 7:0 00245h bits 7:0 = CRC value bits 15:8	Read only
00246h	TEST_SINK_MISC Bits 3:0 = TEST_CRC_COUNT 4 bit wrap counter which increments each time the TEST_CRC_x_x are updated. Reset to 0 when TEST_SINK bit 0 = 0. Note: TEST_CRC_x_x are updated each frame, but the CRC result may be unchanged. The counter shall be incremented when TEST_CRC_x_x is updated, regardless of whether the CRC changed or not. Bit 5 = TEST_CRC_SUPPORTED 0 = CRC not supported by Sink Device 1 = CRC supported by Sink Device Bits 7:6 = Reserved	Read only
00270h	TEST_SINK Bit 0 = TEST_SINK_START 0 = Stop calculating CRC on next frame 1 = Start calculating CRC on next frame Bits7:1 = RESERVED. Read all 0's. Note: The CRC calculation is done on the entire frame. A 16 bit CRC is generated per color component, based on the following polynomial: $f(x) = x^{16} + x^{15} + x^2 + 1$. The CRC calculation is only done on active pixels. The lsb is shifted in first. For any color format that is less than 16 bits per component, zero-pad the lsb. The following is an example of the CRC-16 generation.	Write / Read

The CRC calculation is done on the entire frame. A 16 bit CRC is generated per color component, based on the following polynomial: f(x) = x^16 + x^15 + x^2 + 1. The CRC calculation is only done on active pixels. The msb is shifted in first. For any color format that is less than 16 bits per component, zero-pad the lsb.

The following is an example of the CRC-16 generation.

---------- **example** ----------

```
module crc16_16(
        // Outputs
        dout,
        // Inputs
        reset, clk, d, enable
        );

 // Inputs and Outputs
 input  [ 15: 0] d;
 input         clk;
 input         reset;
 input         enable;
 output [ 15: 0] dout;

 // Internal Signals
 reg    [ 15: 0] b;
 wire   [ 15: 0] dout;

 // Internal Assignments
 assign dout = b;

 // Define LFSR
 always @(posedge clk)
   begin
     if (reset)
       begin
         b <= 16'h0;
       end
     else
       begin
         if (enable)
           begin
             b[15] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^ b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[14]
                      ^ b[15] ^  d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^ d[ 8] ^ d[ 9] ^ d[10] ^ d[11]
                       ^ d[12] ^ d[14] ^ d[15];
             b[14] <= b[12] ^ b[13] ^ d[12] ^ d[13];
             b[13] <= b[11] ^ b[12] ^ d[11] ^ d[12];
             b[12] <= b[10] ^ b[11] ^ d[10] ^ d[11];
             b[11] <= b[ 9] ^ b[10] ^ d[ 9] ^ d[10];
             b[10] <= b[ 8] ^ b[ 9] ^ d[ 8] ^ d[ 9];
             b[ 9] <= b[ 7] ^ b[ 8] ^ d[ 7] ^ d[ 8];
             b[ 8] <= b[ 6] ^ b[ 7] ^ d[ 6] ^ d[ 7];
             b[ 7] <= b[ 5] ^ b[ 6] ^ d[ 5] ^ d[ 6];
             b[ 6] <= b[ 4] ^ b[ 5] ^ d[ 4] ^ d[ 5];
             b[ 5] <= b[ 3] ^ b[ 4] ^ d[ 3] ^ d[ 4];
             b[ 4] <= b[ 2] ^ b[ 3] ^ d[ 2] ^ d[ 3];
```

```
            b[ 3] <= b[ 1] ^ b[ 2] ^ b[15] ^ d[ 1] ^ d[ 2] ^ d[15];
            b[ 2] <= b[ 0] ^ b[ 1] ^ b[14] ^ d[ 0] ^ d[ 1] ^ d[14];
            b[ 1] <= b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^ b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13] ^ b[14]
                     ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^ d[ 8] ^ d[ 9] ^ d[10] ^ d[11] ^ d[12] ^ d[13]
                     ^ d[14];
            b[ 0] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^ b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13]
                     ^  b[15] ^  d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^ d[ 8] ^ d[ 9] ^ d[10] ^ d[11]
                     ^ d[12] ^ d[13] ^ d[15];
          end
        end
    end
endmodule
```

---------- **end of example** ----------

Note: Support of this DPCD extension method is optional.

4 Source Device Tests

This section describes the compliance test procedures for Source DUTs. Figure 4-1 below shows the setup for Source Device testing.

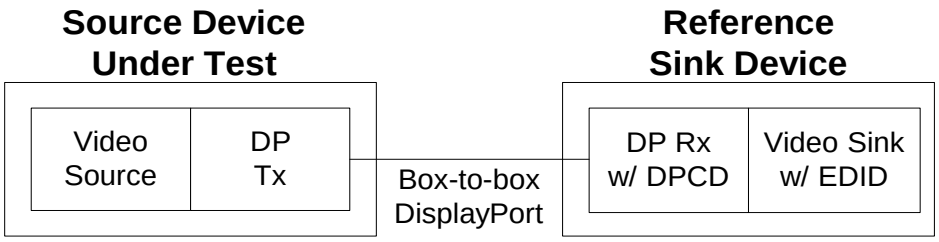

Figure 4-1: Source Device Compliance Test Setup for Link Layer and Above

4.1 Source Device Compliance Test Assertions (Informative)

During Source Device test execution, some assertions can be implemented to verify that the Source DUT is following the DisplayPort protocol. The following assertions may be added:

Aux Channel Requests:

- Verify that minimum duration preamble occurs during Aux-CH SYNC
- Verify that Aux request has START pattern immediately after SYNC
- Verify that Aux request ends with STOP
- Verify that the number of bits between SYNC and STOP is a multiple of 8
- Verify that Aux Request Command (CMD) is valid
- Verify that for writes, the number of write bytes matches the LENGTH field
- Verify that the Source DUT does not indicate illegal voltage swing / pre-emphasis combinations on any active lane via DPCD TRAINING_LANEx_SET fields

Main Link:

- Verify that after the Source DUT indicates that link training is complete by writing TRAINING_PATTERN_SET to 00h, all active lanes transition from Training Pattern 2 to BS-Idle pattern.
- Verify that whenever BS-Idle pattern is transmitted, Source DUT sends at least 5 BS-Idle patterns before enabling video stream

4.2 Source Device Services Test Procedures

In Source Device Services Tests, Aux wake, Aux retry, EDID reads and DPCD reads are verified.

4.2.1 Aux Reads after HPD Connect

The following test cases verify Aux reads on Hot Plug Connect

4.2.1.1 Source DUT Retry on No-Reply During Aux Read after Hot Plug Event

This test checks that the Source DUT retries Aux requests on HPD connect if the sink does not initially reply.

Test Procedure:

1. Reference Sink sets up EDID with one block of data (128 bytes).
2. Reference Sink asserts HPD. If one second test duration feature is selected, start one second timer.
3. Wait until the Source DUT issues an Aux request. Reference Sink does not send any reply to Aux request.
4. Wait until the Source DUT issues another Aux request. Reference Sink does not send any reply to Aux request. Verify that Reference Source waits at least 400us after completion of previous request before sending a new request.

   Pass1: Time between end of previous request and start of current request is at least 400us
   Fail1: Time between end of previous request and start of current request is less than 400us
5. Wait until the Source DUT issues another Aux request. Reference Sink replies to Aux request. Verify that Reference Source waits at least 400us after completion of previous request before sending a new request.

   Pass1: Time between end of previous request and start of current request is at least 400us
   Fail1: Time between end of previous request and start of current request is less than 400us
6. Verify that the Source DUT reads the entire EDID block through AUX CH (Note: Source DUT may issue other Aux transactions in addition to EDID read; this should not be treated as a failure).

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout of test duration limit timer or by user

Pass2: All pass / fail checks in test steps passed
Fail2: One or more pass / fail check(s) in test steps failed.

4.2.1.2 Source Retry on Invalid Reply During Aux Read after Hot Plug Event

This test checks that the Source DUT retries after receiving an invalid Aux response after a Hot Plug event.

Test Procedure:

1. Reference Sink sets up EDID with one block of data (128 bytes).
2. Reference Sink asserts HPD. If one second test duration feature is selected, start one second timer.
3. Wait until the Source DUT issues an Aux request. Reference Sink sends a partial Aux reply (Aux SYNC + some number of bits, but no Aux STOP).
4. Wait until the Source DUT issues another Aux request. Reference Sink replies to Aux request. Verify that the Source DUT waits at least 400us after completion of previous request before sending a new request.

   Pass1: Time between end of previous request and start of current request is at least 400us
   Fail1: Time between end of previous request and start of current request is less than 400us
5. Verify that the Source DUT reads the entire EDID block through AUX CH (**Note**: Source DUT may issue other Aux transactions in addition to EDID read; this should not be treated as a failure).

Result:

This test passes if all pass/fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout of test duration limit timer or by user

Pass2: All pass / fail checks in test steps passed
Fail2: One or more pass / fail check(s) in test steps failed.

4.2.2 EDID and DPCD Reads

Note that Source DUT may initiate EDID read transaction anytime when HPD signal is high. It is not the intention of these tests to fully verify EDID compliance and functionality.

All test cases begin with the HPD signal de-asserted, so assertion of HPD will signify a connect event.

4.2.2.1 EDID Read upon Hot Plug Event

This test checks that the Source DUT reads the EDID from the Reference Sink upon a Hot Plug event.

Test Procedure:

1. Reference Sink sets up EDID with one block of data (128 bytes).
2. Reference Sink asserts HPD. If one second test duration feature is selected, start one second timer.
3. Verify that the Source DUT reads the entire EDID block through AUX CH.

Result:

This test fails if the Source DUT does not read the entire EDID block through AUX CH before transmission of the main video stream, or if test times out or is interrupted by test operator.

4.2.2.2 DPCD Receiver Capability Read upon Hot Plug Event

This test checks that the Source DUT reads the DPCD Receiver Capability field from the Reference Sink upon a Hot Plug event.

Test Procedure:

1. Reference Sink asserts HPD. If one second test duration feature is selected, start one second timer.

2. Verify that the Source DUT reads the DPCD Receiver Capability field (DPCD: 0000h:000Bh) through AUX CH.

Result:

This test fails if the Source DUT does not read the entire EDID block through AUX CH before link training, test timeout or test operator interrupt.

4.2.2.3 EDID Read

This test checks that the Source DUT reads the EDID from the Reference Sink correctly and transmits the main video stream using the preferred timing.

Test Procedure:

1. Reference Sink sets up EDID with one block of data (128 bytes) with a preferred timing defined (no other timings are to be defined). Use a video timing listed in Table 3-1: Source Device Capability Question List.
2. Reference Sink sets TEST_REQUEST.TEST_EDID_READ = 1.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends test request via GUI. If one second test duration feature is selected, start one second timer.
4. Verify that the Source DUT reads the entire EDID block through AUX CH.
5. Verify that the TEST_RESPONSE.TEST_EDID_CHECKSUM_WRITE = 1, and verify that the TEST_EDID_CHECKSUM field matches the checksum in the Reference Sink EDID.
6. Verify that the Source DUT transmits main stream with main video stream attribute data set to match either the preferred timing indicated in the EDID of the Reference Sink or the fail-safe mode (640x480).

Result:

This test fails if the Source DUT does not read the entire EDID block through AUX CH before transmission of the main video stream, test timeout or interrupt by test operator. This test also fails if the Source DUT does not transmit the main video stream using the preferred timing or the fail-safe mode.

4.2.2.4 EDID Absence Detection

This test checks that when no EDID information is available, the Source DUT will transmit the main video stream using the fail-safe mode.

Test Procedure:

1. Reference Sink sets TEST_REQUEST.TEST_EDID_READ = 1.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends test request via GUI. If one second test duration feature is selected, start one second timer.
3. Reference Sink sends an AUX CH NACK when an EDID read is issued by the Source DUT (AUX CH read to address A0).

Note: The Source DUT may retry the EDID read multiple times.

4. Reference Sink keeps SINK_STATUS in DPCD = 0 until the Source DUT transmits main stream with main video stream attribute data set to indicate fail-safe mode (VGA 640x480 at 60Hz, with RGB 18bpp).

Note: The Source DUT may try a set of implementation specific fall-back modes before defaulting to the fail-safe mode.

Result:

This test fails if the Source DUT does not read EDID through AUX CH before transmission of the main video stream, test timeout or interrupt by test operator. This test also fails if the Source DUT does not transmit the main video using the fail-safe mode.

4.2.2.5 EDID Corruption Detection

This test checks that when EDID information is corrupted, the Source DUT will transmit the main video stream using the fail-safe mode.

Test Procedure:

1. Reference Sink sets up EDID with incorrect checksum.
2. Reference Sink sets TEST_REQUEST.TEST_EDID_READ = 1.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends test request via GUI. If one second test duration feature is selected, start one second timer.
4. Verify that the Source DUT reads the entire EDID block (128 bytes) over the AUX CH.

Note: The Source DUT may retry the EDID read multiple times. The Source may choose to write the incorrect checksum to the TEST_EDID_CHECKSUM, but is not required.

Reference Sink keeps SINK_STATUS in DPCD = 0 until the Source DUT transmits main stream with main video stream attribute data set to indicate fail-safe mode (VGA 640x480 at 60Hz, with RGB 18bpp).

Note: The Source DUT may try a set of implementation specific fall-back modes before defaulting to the fail-safe mode.

Result:

This test fails if the Source DUT does not read the entire EDID block through AUX CH before transmission of the main video stream, test timeout or interrupt by test operator. This test also fails if the Source DUT does not transmit the main video using the fail-safe mode.

4.3 Source Device Link Services Test Procedures

The following two items shall be tested:

- Link Training
- Link Maintenance

4.3.1 Link Training

DisplayPort Link Training is described in section 3.5.1.3 of the DisplayPort 1.1 Standard. Figure 2-36 'Link Training State' shows the overall link training sequence. Figures 3-11 'Clock Recovery Sequence of Link Training' and 3-12 'Channel Equalization Sequence of Link Training' show the details of the two phases of link training.

This set of tests verifies that the Source DUT can successfully complete link training on the DisplayPort main link for all lane counts and link rates supported. These tests also check the correct operation of the link training state machine in the Source DUT.

Note: Link training is initiated by the Source DUT by writing TRAINING_PATTERN_SET to 01h, and terminated by the Source DUT by writing TRAININIG_PATTERN_SET to 00h. In the following test cases,

if TRAINING_PATTERN_SET is written to 00h at any time after the Source DUT initiates link training and prior to the test step where a write of TRAINING_PATTERN_SET to 00h is expected, the test shall skip to the Result state and report that link training failed, with the failure cause being 'Training Terminated by Source'.

4.3.1.1 Successful Link Training Upon Hot Plug Detect

Test Procedure:

Note: In this test case, the Source DUT can choose to train the link to any lane count it supports, and any link rate that it supports.

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate. Set MAX_LINK_RATE = 0Ah (270 MHz) and MAX_LANE_COUNT = 04h (4 lanes)).
2. Reference Sink asserts HPD. HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
3. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.

   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1**:** CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lanes {lanes that do not have TP2}

7. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

   Note1: Equalization succeeded on all active lanes
   Warning1: Equalization failed on lanes {lanes that failed equalization}
   Note2: Symbol lock succeeded on all active lanes.
   Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
   Pass3 (2 and 4 lane cases only): All lanes are properly skewed
   Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N
   (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though are not specified in this test.

8. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

   Note1: Link training timer ≤ 10 ms
   Warning1: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully (report even if training exceeds 10 ms time constraint)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks within the test steps succeeded
Fail3: One or more checks within the test steps failed

4.3.1.2 Successful Link Training at All Supported Lane Counts and Link Speeds

This test is repeated for all lane counts and link rates up to the maximum supported by the Source DUT.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the lane count and link rate currently under test. For example, for test 1a in Table 4-1, Reference Sink will advertise MAX_LINK_RATE = 06h and MAX_LANE_COUNT = 1h in its DPCD Receiver Capability Field.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to request lane count and link rate currently under test. For example, for test 1a in Table 4-1, Reference Sink will set TEST_LINK_RATE = 06h and TEST_LANE_COUNT = 1h in its DPCD Test Request Field.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to the expected values.

   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and at least 100us after link training begins.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR

LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

6. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

7. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lanes {lanes that do not have TP2}

8. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

   Note1: Equalization succeeded on all active lanes
   Warning1: Equalization failed on lanes (lanes that failed equalization)
   Note2: Symbol lock succeeded on all active lanes.
   Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
   Pass3 (2 and 4 lane cases only): All lanes are properly skewed
   Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

9. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

   Note1: Link training timer ≤ 10 ms
   Warning1: Link training timer > 10 ms

Result:

This test passes if all pass/fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step (report which test step the test was in when interrupted)

Pass2: Link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:

LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET

Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Link training completed successfully at target link rate and lane count
Target LINK_BW = K, Actual LINK_BW = K
Target LANE_COUNT = X, Actual LANE_COUNT = X

Fail3: Link training did not complete successfully at target link rate or lane count
Target LINK_BW = K, Actual LINK_BW = L (L not= K)
Target LANE_COUNT = X, Actual LANE_COUNT = Y (Y not= X)

Pass4: All pass/fail checks within the test steps succeeded
Fail4: One or more pass/fail checks with the test steps failed

Table 4-1:Link Training Test Cases

Link speed\lane count	**1 MAX_LANE_COUNT = 1h**	**2 MAX_LANE_COUNT = 2h**	**4 MAX_LANE_COUNT = 4h**
1.62Gbps MAX_LINK_RATE = 06h	1a	1b	1c
2.7Gbps MAX_LINK_RATE = 0Ah	1d	1e	1f

4.3.1.3 Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate supported by the Source DUT.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to the maximum lane count and link rate supported by the Source DUT.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to the expected values.

   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah

Pass3: LANE_COUNT_SET = {1,2 or 4}
Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4

5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and at least 100us after link training begins.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

6. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

7. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.VOLTAGE_SWING_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

8. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding

lanes that have voltage swing adjustment flagged as complete)
Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

9. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.VOLTAGE_SWING_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes excluding those that have voltage swing adjustment flagged as complete.
10. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

    Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

Note: Support of fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

11. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
12. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all any active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
13. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

    Pass1: CR lock achieved for all active lanes.
    Fail1: CR lock failed for lane(s) {lanes which failed CR lock)
14. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

Pass1: Training Pattern 2 detected on all active lanes
Fail1: Training Pattern 2 not detected on lanes {report active lanes without TP2}

15. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 or 4 lane cases only): All lanes are properly skewed
    Fail3 (2 or 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N
    (N = 0 .. 2, M not= 2)

Note: multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

16. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks within the test steps succeeded
Fail3: One or more checks within the test steps failed

4.3.1.4 Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing

Note: Support of 2.7Gbps link rate is optional. This test is skipped if the test operator has reported that Source DUT supports a maximum link rate of 1.62Gbps.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate supported by the Source DUT.

2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to the maximum lane count and link rate supported by the Source DUT.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 0Ah
   Fail2: LINK_BW_SET not= 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
6. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
7. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting

ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

8. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

9. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

10. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this test step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

    Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (repeat for x = 0 .. N, N = highest active lane, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (report for x = 0 .. N, N = any active lane that has VOLTAGE SWING SET not= 01b and does not have voltage swing adjustment flagged as complete)

Note: Support for fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

11. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

12. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)

Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)
Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete).

13. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
14. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Increment voltage swing iteration counter.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = YYb (YY = last requested voltage swing; check all active lanes)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= YYb (YY = last requested voltage swing; check all active lanes)
15. Repeat step 14 (including pass/fail checks) until sink writes LINK_BW_SET.
16. Verify that the Source DUT sets the LINK_BW_SET to 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iterations at high link bandwidth
    Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations
    Pass1: LINK_BW_SET = 06h
    Fail1: LINK_BW_SET not= 06h
    Pass2: Training Pattern 1 detected on all enabled lanes when LINK_BW_SET is written
    Fail2: Training Pattern 1 not sent on lanes {report lanes without TP1} when LINK_BW_SET is written
    Pass3: link rate = 1.62 Gbps
    Fail3: link rate not= 1.62 Gbps
17. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though are not specified in this test.

18. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {lanes without TP2}
19. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is

complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

Note1: Equalization succeeded on all active lanes
Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
Note2: Symbol lock succeeded on all active lanes
Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
Pass3 (2 and 4 lane cases only): All lanes are properly skewed
Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

20. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: All pass/fail checks succeeded
Fail4: One or more checks failed

4.3.1.5 Successful Link Training to a Lower Link Rate #2: - Iterate at Minimum Voltage Swing

Note: Support of 2.7Gbps link rate is optional. This test is skipped if the test operator has reported that Source DUT supports a maximum link rate of 1.62Gbps.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate supported by the Source DUT.

2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to the maximum lane count and link rate supported by the Source DUT.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 0Ah
   Fail2: LINK_BW_SET not= 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
6. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

7. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
8. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Increment voltage swing iteration counter.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)
9. Repeat step 8 (including pass/fail checks) until sink writes LINK_BW_SET.
10. Verify that the Source DUT sets the LINK_BW_SET to 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

    Pass1: Iteration counter = 5, indicating Source initiated training at low link bandwidth after five iterations at high link bandwidth.
    Fail1: Iteration counter not= 5, indicating Source initiated training at low link bandwidth after an incorrect number of iterations.

    Pass1: LINK_BW_SET = 06h
    Fail1: LINK_BW_SET not= 06h
    Pass2: Training Pattern 1 detected on all enabled lanes when LINK_BW_SET is written
    Fail2: Training Pattern 1 not sent on lanes {report lanes without TP1} when LINK_BW_SET is written
    Pass3: link rate = 1.62 Gbps
    Fail3: link rate not= 1.62 Gbps

11. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

12. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {lanes without TP2}
13. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

Note1: Equalization succeeded on all active lanes
Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
Note2: Symbol lock succeeded on all active lanes
Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
Pass3 (2 and 4 lane cases only): All lanes are properly skewed
Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

14. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: All pass/fail checks succeeded
Fail4: One or more checks failed

4.3.1.6 Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate supported by the Source DUT.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to the maximum lane count and link rate supported by the Source DUT.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.

4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
6. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

7. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}
8. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-

emphasis adjustment as complete for that lane after completion of this test step and do not make any further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 15.

Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes)
Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes)

9. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 01b for all active lanes that do not have pre-emphasis flagged as complete.
10. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this test step and do not make further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 15.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis flagged as complete)
11. Reference Sink keeps sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 10b for all active lanes that do not have pre-emphasis flagged as complete.
12. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this test step and do not make further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 15.

    Pass1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 10b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 10b (check all active lanes, excluding those that have pre-emphasis flagged as complete)

Note: Support for third pre-emphasis level (in addition to zero setting) is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

13. Reference Sink keeps sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 11b for all active lanes that do not have pre-emphasis flagged as complete.

14. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (check all active lanes, excluding those that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding those that have pre-emphasis flagged as complete)

15. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 and 4 lane cases only): All lanes are properly skewed
    Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

16. Wait until the Source DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step (report which test step the test was in when interrupted)

Pass2: Link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks succeeded
Fail3: One or more checks failed

4.3.1.7 Successful Link Training at Lower Link Rate due to Loss of Symbol Lock During Channel Equalization Sequence

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count and link rate supported by the Source DUT.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT and TEST_LINK_RATE to the maximum lane count and link rate supported by the Source DUT.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

6. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

7. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}

8. Reference Sink clears LANEx_CR_DONE bits in DPCD Link/Sink Status Field to indicate a loss of symbol lock.

9. If Source DUT only supports 1.62Gbps link rate or has already reduced link rate to 1.62 Gbps, wait until the Source DUT terminates the link training by writing 00h to TRAINING_PATTERN_SET in the DPCD Link Configuration Field. Stop the link training timer and proceed to 'Result'. If Source DUT supports 2.7Gbps link rate and has achieved CR lock on all lanes at 2.7 Gbps, proceed with the remainder of the test.

   Pass1 (only if link rate is already 1.62 Gbps): TRAINING_PATTERN_SET = 00h
   Fail1 (only if link rate is already 1.62 Gbps): TRAINING_PATTERN_SET not= 00h

10. Wait until the Source DUT writes to LINK_BW_SET. Verify that the Source DUT sets LINK_BW_SET to 06h to attempt link training at the lower link rate by going through the Clock Recovery sequence again.

    Pass1: LINK_BW_SET = 06h
    Fail1: LINK_BW_SET not= 06h

11. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE SWING SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes.

    Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
    Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
    Pass2: VOLTAGE SWING SET = 00b
    Fail2: VOLTAGE SWING SET not= 00b
    Pass3: PRE-EMPHASIS_SET = 00b
    Fail3: PRE-EMPHASIS_SET not= 00b

12. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Pass1: CR lock succeeded on all active lanes
    Fail1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

13. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field, and that the Source DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}

14. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Source DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 or 4 lane cases only): All lanes are properly skewed
    Fail3 (2 or 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N
    (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

15. Wait until the Source DUT writes a 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2 (only if link rate was 2.7 Gbps in step 9, allowing continuation of test): Link training completed successfully
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2 (only if link rate was 2.7 Gbps in step 9, allowing continuation of test): Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks within the test steps succeeded
Fail3: One or more checks within the test steps failed

4.3.1.8 Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count supported by the Source DUT and 1.62Gbps link rate.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT to the maximum lane count supported by the Source DUT and TEST_LINK_RATE to 1.62Gbps link rate.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
6. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

7. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
8. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
9. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
10. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this test step, and do not make further adjustments or checks on that lane until step 13. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 13.

    Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

Note: Support for fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

11. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
12. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)
Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

13. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
14. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. Increment voltage swing iteration counter. Repeat step 14 until Source DUT writes to TRAINING_PATTERN_SET; when Source DUT writes to TRAINING_PATTERN_SET, skip forward to step 15.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)
15. Verify that the Source DUT writes 00h to TRAINING_PATTERN_SET to terminate link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iteration at high link bandwidth.
    Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after an incorrect number of iterations.
    Pass2: TRAINING_PATTERN_SET = 00h
    Fail2: TRAINING_PATTERN_SET not= 00h
    Pass3: Link training timer ≤ 10 ms
    Fail3: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step (report which test step the test was in when interrupted)

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

4.3.1.9 Unsuccessful Link Training at Lower Link Rate #2: - Iterate at Minimum Voltage Swing

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count supported by the Source DUT and 1.62Gbps link rate.

2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT to the maximum lane count supported by the Source DUT and TEST_LINK_RATE to 1.62Gbps link rate.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
6. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
7. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
8. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active

lanes. Increment voltage swing iteration counter. Repeat step 8 until Source DUT writes to TRAINING_PATTERN_SET; when Source DUT writes to TRAINING_PATTERN_SET, skip forward to step 9.

Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)

9. Verify that the Source DUT writes 00h to TRAINING_PATTERN_SET to terminate link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

   Pass1: Iteration counter = 5, indicating Source initiated training at low link bandwidth after five iterations at high link bandwidth
   Fail1: Iteration counter not= 5, indicating Source initiated training at low link bandwidth after an incorrect number of iterations
   Pass2: TRAINING_PATTERN_SET = 00h
   Fail2: TRAINING_PATTERN_SET not= 00h
   Pass3: Link training timer ≤ 10 ms
   Fail3: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

4.3.1.10 Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the maximum lane count supported by the Source DUT and 1.62Gbps link rate.
2. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT to the maximum lane count supported by the Source DUT and TEST_LINK_RATE to 1.62Gbps link rate.
3. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test. Reference Sink also sends link training request via GUI. If one second test duration feature is selected, start one second timer.
4. Wait until the Source DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 5 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h

Pass3: LANE_COUNT_SET = {1,2 or 4}
Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4

5. Wait until the Source DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Source DUT transmits training pattern 1 on all active lanes. Verify that the Source DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

6. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

7. Wait until the Source DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field, and that the Source DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lanes {active lanes without TP2}

8. Verify that TRAINNIG_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. Set the equalization iteration counter to 1. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 15.

   Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (for x = 0 .. N, N = max active lane)

Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (for x = 0 .. N, N = any active lane that has MAX_PRE-EMPHASIS_REACHED = 1)

9. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 01b for all active lanes.
10. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 2. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS REACHED = 1 for all active lanes, proceed to step 15.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
11. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 10b for all active lanes.
12. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 3. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 15. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS REACHED = 1 for all active lanes, proceed to step 15.

    Pass1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

Note: Support of third pre-emphasis level is optional. Do not fail if sink indicates that it does not support PRE-EMPHASIS_SET = 11b by setting MAX_PRE-EMPHASIS_REACHED=1 on this iteration.

13. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 11b for all lanes.
14. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 4. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes.

Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

15. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared. LANEx_CR_DONE bits in DPCD Link/Sink Status Field remain set.
16. Wait until the Source DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes. Repeat step 16 until Source DUT writes to TRAINING_PATTERN_SET; when Source DUT writes to TRAINING_PATTERN_SET, skip forward to step 17.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
17. Verify that the Source DUT terminates link training by writing TRAINING_PATTERN_SET to 00h. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iterations at high link bandwidth.
    Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after an incorrect number of iterations.
    Pass2: TRAINING_PATTERN_SET = 00h
    Fail2: TRAINING_PATTERN_SET not= 00h
    Pass3: Link training timer ≤ 10 ms
    Fail3: Link training timer > 10 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

4.3.1.11 Lane Count Reduction

Test Procedure:

Note: This test is skipped if the Source DUT only supports one lane.

The test begins with the DisplayPort main link already trained and active, to the maximum number of lanes supported by the Source DUT, and running at 1.62Gbps link rate.

Test Procedure:

1. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT to one lane and TEST_LINK_RATE to 1.62Gbps link rate.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends link training request via GUI. HPD signal remains asserted for the remainder of the test.
3. Verify that the Source DUT transmits idle pattern on all lanes.
4. Verify that the Source DUT writes 01h to LANE_COUNT_SET, and that it disables (stops transmission) on all lanes other than lane 0.
5. Check that the Source DUT continues to send idle pattern on lane 0. The Source DUT may instead do a full re-training of the link with the new lane count (report this as a warning).
6. Reference Sink keeps LANEx_CR_DONE, LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK set for lane 0, and clear for all other lanes. INTERLANE_ALIGNED_DONE remains set.
7. Verify that the Source DUT sends at least 5 BS-idle patterns on lane 0.

Result:

This test fails if one or more of the checks listed in the test steps fails.

4.3.1.12 Lane Count Increase

Test Procedure:

Note: This test is skipped if the Source DUT only supports one lane. The DisplayPort main link is already trained and active, using one lane, and running at 1.62Gbps link rate before this test is executed.

1. Reference Sink sets TEST_REQUEST.TEST_LINK_TRAINING = 1, and TEST_LANE_COUNT to maximum number of lanes supported by the Source DUT and TEST_LINK_RATE to 1.62Gbps link rate.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD signal remains asserted for the remainder of the test.
3. Verify that the Source DUT disables all lanes (stop transmission).
4. Verify that the Source DUT writes the new lane count (maximum number of lanes supported by Source DUT) to LANE_COUNT_SET.
5. Continue the rest of the link training (go to step 4 of test 4.3.1.2).

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully (report even if training exceeds 10 ms time constraint or did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Link training completed successfully at one lane, 1.62Gbps
Fail3: Link training did not complete successfully at one lane, 1.62Gbps
Target LINK_BW = 1.62 Gb/s, Actual LINK_BW = 2.7 Gb/s
Target LANE_COUNT = 1, Actual LANE_COUNT = X

Pass4: All pass/fail checks within the test steps succeeded
Fail4: One or more pass/fail checks with the test steps failed

4.3.2 Link Maintenance

This set of tests check that the Source DUT does the appropriate action when an interrupt is signaled by IRQ HPD pulse.

Note: These tests all begin with the DisplayPort main link already trained to the maximum number of lanes supported by the Source DUT. The link maintenance tests can be done at either link rate.

4.3.2.1 Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock

This test case verifies re-training by the Source DUT after Reference Sink reports loss of symbol lock. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.
This test is repeated separately for each lane.

Test Procedure:

1. Reference Sink clears the LANEx_SYMBOL_LOCKED bit of DPCD Link Status field to indicate a loss of symbol lock, and sets the LINK_STATUS_UPDATED bit.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD remains asserted for the remainder of the test. Start Link Status Read Timer.
3. Wait until the Source DUT reads DPCD Link Status field (Aux read of address 0200h). Stop the Link Status Read timer. Verify that the Source DUT read addresses 0200h – 0205h. Verify that the Link Status read occurred within 100ms of the rising edge of HPD.

   Pass1: Source DUT read DPCD addresses 0200h – 0205h
   Fail1: Source DUT did not read DPCD addresses 0200h – 0205h
   Pass2: Link Status Read started link status read within 100 ms
   Fail2: Link Status Read did not start within 100 ms
4. Carry out steps 4-8 of test 4.3.1.1 ‘Successful Link Training Upon Hot Plug Detect’ to re-train the link.
5. Verify that the Source DUT transitions from Training Pattern 2 to Idle Pattern, and that Source DUT sends at least 5 BS-Idle Pattern on all active lanes.

   Pass1: Transition from TP2 to Idle Pattern detected on all active lanes

Fail1: Transition from TP2 to Idle Pattern not detected on lane(s) {active lanes where transition was not detected}
Pass2: Valid Idle Pattern detected on all active lanes
Fail2: Valid Idle Pattern not detected on lanes {active lanes without valid Idle Pattern}
Pass3: At least 5 BS-Idle Pattern detected on all active lanes
Fail3: N BS-Idle Pattern detected for on lane M {repeat for all active lanes M that have N < 5}

Result:

This test passes if all of the pass/fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully (report even if training exceeds 10 ms time constraint)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass4: LANE_COUNT_SET = original LANE_COUNT_SET
Fail4: LANE_COUNT_SET not= original LANE_COUNT_SET

Pass5: LINK_BW_SET = original LINK_BW_SET
Fail5: LINK_BW_SET not= original LINK_BW_SET

Pass6: All pass / fail checks within test steps passed
Fail6: One or more pass / fail check(s) within test steps failed

4.3.2.2 Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock

This test case verifies re-training by the Source DUT after Sink reports loss of clock recovery lock. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.

This test is repeated separately for each lane.

Other than step 1, this test case is identical to test 4.3.2.1 ‘Successful Link Re-training after IRQ HPD Pulse Due to Loss of Symbol Lock’.

Test Procedure:

1. Reference Sink clears the LANEx_CR_DONE bits of DPCD Link Status field to indicate a loss of clock recovery lock, and sets the LINK_STATUS_UPDATED bit.
2. Go to step 2 of test 4.3.2.1.

Result:

See ‘Result’ section of test 4.3.2.1

4.3.2.3 Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

Note: This test is skipped if the Source DUT supports the maximum of one lane

This test case verifies re-training by the Source DUT after Sink reports loss of inter-lane alignment lock. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.

Other than step 1, this test case is identical to test 4.3.2.1 'Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock'.

Test Procedure:

1. Reference Sink clears the INTERLANE_ALIGN_DONE bit of DPCD Link Status field to indicate a loss of inter-lane alignment lock and sets the LINK_STATUS_UPDATED bit.
2. Go to step 2 of test 4.3.2.1.

Result:

See 'Result' section of test 4.3.2.1

4.3.2.4 No link re-training required after IRQ HPD pulse

Test Procedure:

1. Reference Sink keeps LANEx_SYMBOL_LOCKED, LANEx_CR_DONE and INTERLANE_ALIGN_DONE bits of DPCD Link Status field set.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD remains asserted for the remainder of the test. Start Link Status Read timer (Reference Sink does not indicate any errors).
3. Wait until the Source DUT reads DPCD Link Status field (Aux read of address 0200h). Stop the Link Status Read timer. Verify that the Source DUT read addresses 0200h – 0205h. Verify that the Link Status read occurred within 100ms of the rising edge of HPD.

   Pass1: Source DUT read DPCD addresses 0200h – 0205h
   Fail1: Source DUT did not read DPCD addresses 0200h – 0205h
   Pass2: Link Status Read started link status read within 100 ms
   Fail2: Link Status Read did not start within 100 ms
4. Monitor AUX CH and main link activity for 10 ms. Verify that the Source DUT does not re-initiate link training (does not write to TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field) during 10 ms interval. Verify that the Source DUT continues to transmit BS-Idle pattern or active video stream.

   Pass1: Source DUT does not write to TRAINING_PATTERN_SET
   Fail1: Source DUT writes to TRAINING_PATTERN_SET
   Pass2: BS-Idle or active video stream being transmitted on the main link
   Fail2: No BS-Idle or active video stream on the main link

Result:

This test passes if all pass / fail checks below pass

Pass1: Test completed successfully
Fail1: Test was manually interrupted

Pass2: All pass/fail checks within test steps succeeded
Fail2: One or more checks within test steps failed

4.4 Source Isochronous Transport Services Test Procedures

In Source Isochronous Transport Services Test, Main Stream data mapping capability, including the generation of Main Stream Attribute packet, shall be tested.

4.4.1 Main Stream Data Mapping

This set of tests check the main stream data mapping capability of the DisplayPort main link. Data mapping is further broken down into two parts: 1) bus steering – the mapping of pixel to a lane, and 2) data packing and stuffing into transfer units (TU). It is not the intention of this test to cover the interoperability of all video timings and color formats.

Note: The test procedures assume that the interrupt / DPCD test method is used. If this method is not available, some other vendor specific or manual method will be required.

For fixed timing Source DUTs (for example, embedded devices) which only support one video timing, the Pixel data steering test shall be executed at the supported timing. The other tests in this section shall be skipped.

4.4.1.1 Pixel Data Steering

This test also checks that the dynamic range bit in the main stream attribute data is set properly.

For fixed timing Source DUTs, execute this test at the supported video timing.

Test Procedure:

1. Set the DisplayPort main link to 1.62Gbps data rate, and one lane.

   Note: This test should be repeated for all lane widths supported by the Source DUT.

2. Reference Sink sets test video timing to use VGA 640x480 @ 60Hz in the test request field of DPCD.
3. Reference Sink sets the test color format in test request field of DPCD. This test is repeated for all color formats supported by the Source DUT. Please refer to Table 3-5 for the list of color formats supported in DisplayPort.
4. Reference Sink sets the TEST_REQ bit, sets TEST_REQUEST.TEST_PATTERN = 1 and requests a test pattern (the test pattern used for each color format is listed in Table 3-5).
5. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms).
6. Reference Sink reads the TEST_RESPONSE register after 5s. If the TEST_RESPONSE.TEST_NAK = 1, the test mode is not supported by the Source DUT and terminate test. This is a test failure if the colorimetry currently under test is mandatory. If the TEST_RESPONSE.TEST_ACK is set, proceed with remainder of the test.
7. Verify that the test data pattern is received properly at the Reference Sink.

Result:

This test fails if Reference Sink indicates an error in the test data pattern received. This test also fails if the Source DUT does not support the mandatory colorimetries.

4.4.1.2 Main Stream Data Packing and Stuffing – Least Packed TU

This tests the main stream data packing and stuffing in the case where a transfer unit (TU) is the least packed with data symbols.

Note: This test is skipped for a fixed timing Source DUT.

Test Procedure:

1. Set the DisplayPort main link to maximum number of lanes supported by Source DUT, and 2.7Gbps if supported (1.62Gbps if only low link rate is supported).
2. Reference Sink sets the color format to use 18-bpp RGB with VESA dynamic range in test request field of DPCD.

Note: If YCbCr is supported, use 16-bpp YCbCr422 instead.

3. Reference Sink sets the video timing to use VGA 640x480 @ 60Hz in test request field of DPCD.
4. Reference Sink sets the TEST_REQ bit, sets TEST_REQUEST.TEST_PATTERN = 1, and requests a test pattern (the test pattern used for each color format is listed in Table 3-5).
5. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms).
6. Reference Sink reads the TEST_RESPONSE register after 5s. If the TEST_RESPONSE.TEST_NAK is set, the test mode is not supported by the Source DUT and terminate test. If the TEST_RESPONSE.TEST_ACK is set, proceed with remainder of the test.
7. Verify that the test data pattern is received properly at the Reference Sink.

Result:

This test fails if Reference Sink indicates an error in the test data pattern received. This test also fails if Source DUT does not support the fail-safe mode.

4.4.1.3 Main Stream Data Packing and Stuffing – Most Packed TU

This tests the main stream data packing and stuffing in the case where a transfer unit (TU) is the most packed with data symbols.

Note: This test is skipped for a fixed timing Source DUT.

Test Procedure:

1. Set the DisplayPort main link to use low link rate.
2. Set the DisplayPort main link to use 1 lane lane count, and video mode according to Table 4-2.

Note: This test is repeated for all lane counts supported by the Source DUT. For consumer Source DUTs, please refer to Table 4-3.

3. Reference Sink sets test color format according to Table 4-2 in test request field of DPCD. Start with the mode that will result in the highest packing ratio.
4. Reference Sink sets test video timing according to Table 4-2 in test request field of DPCD.
5. Reference Sink sets the TEST_REQ bit, sets TEST_REQUEST.TEST_PATTERN = 1, and requests a test pattern (the test pattern used for each color format is listed in Table 3-5)
6. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms).
7. Reference Sink reads the TEST_RESPONSE register after 5s.
8. If the TEST_RESPONSE.TEST_NAK is set, the test mode is not supported by the Source DUT. Go back to Step 3, and go to the next highly packed mode in Table 3-5. If all the modes in Table 3-5 have been tried, terminate test.
9. If the TEST_RESPONSE.TEST_ACK is set, proceed with remainder of the test.
10. Verify that the test data pattern is received properly at the Reference Sink.

Result:

This test fails if Reference Sink indicates an error in the test data pattern received.

Table 4-2: Main Stream Data Packing and Stuffing – Most Packed Modes for PC

Lane Count	Standard	H Res	V Res	Refresh Rate (Hz)	Interlaced / Progressive	Blanking Mode	bpp	Packing Ratio
1	CVT	1280	800	60	Progressive	Reduced	18	99%
1	DMT	1280	768	60	Progressive	Reduced	18	95%
1	DMT	800	600	60.317	Progressive	Normal	30	93%
1	DMT	1024	768	60	Progressive	Normal	18	90%
2	DMT	1280	1024	60	Progressive	Normal	24	100%
2	DMT	1280	960	60	Progressive	Normal	24	100%
2	DMT	1360	768	60	Progressive	Normal	30	99%
2	CVT	1200	800	60	Progressive	Normal	30	97%
2	DMT	1400	1050	60	Progressive	Reduced	24	94%
2	DMT	1280	768	60	Progressive	Normal	30	92%
2	CVT	1600	1200	60	Progressive	Reduced	18	90%
4	CVT	2048	1536	60	Progressive	Reduced	24	97%
4	DMT	1792	1344	60	Progressive	Normal	24	95%
4	DMT	1600	1200	60	Progressive	Normal	30	94%

Note: Spread spectrum clocking is not used.

Table 4-3: Main Stream Data Packing and Stuffing – Most Packed Modes for Consumers

Lane Count	Standard	H Res	V Res	Refresh Rate (Hz)	Interlaced / Progressive	bpp	Packing Ratio
1	CEA	1440	480	59.94	Progressive	24	100%
2	CEA	1920	1080	50 59.94 60	Interlaced	30	86%
4	CEA	1920	1080	60	Progressive	40	86%

Note: Spread spectrum clocking is not used. For 2 and 4 lanes, use a lower bpp if 30bpp is not supported.

4.4.2 Main Video Stream Format Change Handling

The required behavior of Source DUT upon the main video stream format change is defined in Section 5.l.3 of DisplayPort Specification Version 1.1. This test case verifies that the Source DUT complies with the format change requirement.

Note: A Source DUT may optionally choose to always re-train the link when carrying out a format change. This test case is skipped for Source DUTs that do not support format changes without link re-training, as reported in Table 3-1: Source Device Capability Question List.

Note: This test is skipped for a fixed timing Source DUT.

Test Procedure:

1. Set the DisplayPort main link to 1.62Gbps data rate, and one lane.
2. Reference Sink sets the color format to use 18-bpp RGB with VESA dynamic range in test request field of DPCD.
3. Reference Sink sets the video timing to use VGA 640x480 @ 60Hz in test request field of DPCD.
4. Reference Sink sets the TEST_REQ bit, sets TEST_REQUEST.TEST_PATTERN = 1, and requests a test pattern (ramp pattern).
5. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends test request (color format, video timing, test pattern) via a GUI.
6. Reference Sink reads the TEST_RESPONSE register after 5s. If the TEST_RESPONSE.TEST_NAK is set, Reference Sink waits for user input to allow the test to proceed. If the TEST_RESPONSE.TEST_ACK is set, proceed with remainder of the test.
7. Verify that the test data pattern is received properly at the Reference Sink.
8. Reference Sink sets the color format to use 24-bpp RGB with VESA dynamic range in test request field of DPCD.
9. Reference Sink sets the TEST_REQ bit, sets TEST_REQUEST.TEST_PATTERN = 1, and requests a test pattern (ramp pattern).
10. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). Reference Sink also sends test request (color format, video timing, test pattern) via a GUI.
11. Reference Sink reads the TEST_RESPONSE register after 5s. If the TEST_RESPONSE.TEST_NAK is set, Reference Sink waits for user input to allow the test to proceed. If the TEST_RESPONSE.TEST_ACK is set, proceed with remainder of the test.
12. Verify that the Source DUT repeats the idle pattern at least 5 times before inserting the new Main Stream Attributes.
13. Verify that the test data pattern is received properly in the new main stream video format at the Reference Sink.

Result:

This test fails if Reference Sink indicates an error in the test data pattern received. This test also fails if Source DUT does not support the fail-safe mode.

5 Sink Device Tests

This section describes the compliance test procedures for Sink DUTs. Figure 5-1 below shows the setup for the Sink Device test.

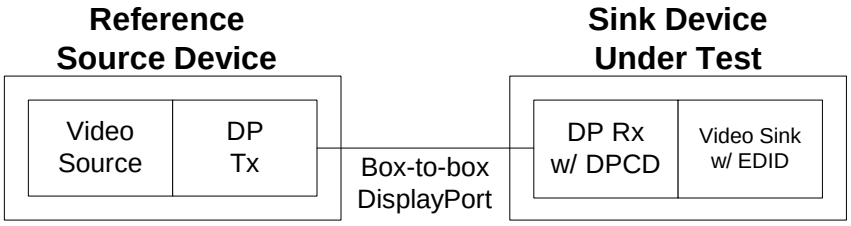

Figure 5-1: Sink Device Compliance Test Setup for Link Layer and Above

5.1 Sink Device Compliance Test Assertions (Informative)

During Sink Device test execution, some assertions can be implemented to verify that the Sink DUT is following the DisplayPort protocol. The following assertions may be added:

Aux Channel Replies:

- Verify that minimum duration preamble occurs during Aux-CH SYNC
- Verify that Aux request has START pattern immediately after SYNC
- Verify that Aux request ends with STOP
- Verify that the number of bits between SYNC and STOP is a multiple of 8
- Verify that Aux Reply Command (CMD) is valid
- Verify that for reads, the number of read bytes (returned from Sink to Source) matches the Request LENGTH field
- Verify that the Aux Reply always begins within 400us of the end of an Aux Request (no-reply is allowed, but if there is a reply it must not commence later than 400us after the request)
- The number of Aux Request retries before an Aux reply is received exceeds three

Hot Plug Detect Line:

- Verify that the Hot Plug Detect interrupt duration is between 500 and 1000 us
- Verify that the Sink DUT does not request illegal voltage swing / pre-emphasis combinations on any active lane via the DPCD ADJUST_REQUEST_LANEx fields

5.2 Sink Device Services Test Procedures

In Sink Device Services Tests, the following Sink capabilities shall be tested:

- DisplayPort Auxiliary Channel Reply Protocol And Data
- Send EDID data in reply to EDID read transaction via DisplayPort Auxiliary Channel

Note: The Source DUT may initiate EDID read transaction anytime when HPD signal is high.

5.2.1 Auxiliary Channel Protocol

This set of tests verifies that the Sink DUT responds correctly to aux channel read and write requests. Both native aux and I2C over aux transactions are covered. These tests shall be run with the main link off, to ensure that Sink DUT will not be issuing IRQ HPD requests.

The declared Receiver Capability Field contents will be compared against the values read back in these test cases.

5.2.1.1 Read One Byte from Valid DPCD Address

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   90-00-00-00h (native aux read from address 0000h, 1 byte)
   (This reads the first Receiver Capability byte)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, return to step 2. If reply is Aux ACK, proceed to step 4. If reply is not Aux DEFER or Aux ACK, exit test.

   Aux Defer is as follows:
   20h
   (1 byte - Native Aux Defer)

   Aux ACK is as follows:
   00-R0h
   (2 bytes - Native Aux ACK plus one read byte)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass2: Reply is Aux DEFER or Aux ACK
   Fail2: Reply is not Aux DEFER or Aux ACK

4. Verify reply data.

   Pass1: Read byte R0 matches first byte of Sink DUT's Receiver Capabilities
   Fail1: Read byte R0 does not match first byte of Sink DUT's Receiver Capabilities

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

5.2.1.2 Read Twelve Bytes from Valid DPCD Address

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Set parameter X to zero.
3. Reference Source computes the remaining number of bytes to fetch:
   REQ_LEN = (12 - X - 1)
   and start address:
   REQ_ADDRESS = X
4. Reference Source sends the following Aux request:
   90-00-REQ_ADDRESS-REQ_LEN (native aux read of (12 - X) bytes from address (00h + X))
   (This reads the 12-byte Receiver Capability field, skipping bytes that were previously read)
5. Wait for Aux reply. If reply isn't received within 400us, return to step 3. Check reply. If reply is unintelligible (received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, return to step 3. If reply is Aux ACK, proceed to step 5. If reply is not Aux DEFER or Aux ACK, exit test.

   Aux DEFER is as follows:
   20h
   (1 byte - Native Aux Defer)

   Aux ACK is as follows:
   00h-{RBN[7:0]}
   (Native Aux ACK + (1..REQ_LEN) Read Bytes)

   Pass1: Valid reply command (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Invalid reply command
   (all the checks below are done only if valid reply is received and is not a Defer)
   Info: print Defer retry counter
   Pass2: Native Aux ACK received
   Fail2: some other Aux reply command received (print bytes)
   Pass3: 1 <= REPLY_BYTE_COUNT <= REQ_LEN + 1
   Fail3: REPLY_BYTE_COUNT = 0 OR REPLY_BYTE_COUNT > REQ_LEN + 1
6. Increment X for each read byte received (i.e. all reply bytes excluding the first byte). Compute REPLY_BYTE_COUNT = X - REQ_ADDRESS. If X < 12, return to step 2. Otherwise proceed to step 6.

7. Check reply.

   Pass1: Read bytes R0-R11 match Sink DUT's Receiver Capabilities fields
   Fail1: Read bytes R0-R11 do not match Sink DUT's Receiver Capabilities fields

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within the test steps passed
Fail2: One or more check(s) within the test steps failed

5.2.1.3 Write One Byte to Valid DPCD Address

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   80-01-00-00-06h (native aux write to address 0100h, 1 byte)
   (This writes LINK_BW_SET to 06h)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER or Aux NACK, return to step 2. If reply is Aux ACK, proceed to step 4.

   Aux DEFER is as follows:
   20h
   (Native Aux Defer)

   Aux NACK is as follows:
   01-00h
   (Native Aux NACK, 0 bytes written)

   Aux ACK is as follows:
   00h
   (Native Aux ACK)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass2: Reply is Aux DEFER, Aux NACK or Aux ACK
   Fail2: Reply is not Aux DEFER, Aux NACK or Aux ACK
4. Read back one byte at address 0100h, using procedure from test case 5.2.1.1, 'Read One Byte From Valid DPCD Address'. Verify that data read matches data written.

   Pass1: Read byte = 06h
   Fail1: Read byte not= 06h

Result:

This test passes if all of the pass / fail checks below pass

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within the test steps passed
Fail2: One or more check(s) within the test steps failed

5.2.1.4 Write Nine Bytes to Valid DPCD Addresses

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Set parameter N to zero. Set WRITE_DATA[9] to {0A, 84, 7C, 3F, 3F, 3F, 3F, 11, 01}. The WRITE_DATA array is used to set the following DPCD parameters: (LINK_BW_SET = 0Ah, LANE_COUNT_SET = 04h, ENHANCED_FRAME_EN = 1, TRAINING_PATTERN_SET = 0, LINK_QUAL_PATTERN_SET = 3, RECOVERED_CLOCK_OUT_EN = 1, SCRAMBLING_DISABLE = 1, SYMBOL_ERROR_COUNT_SEL = 1, VOLTAGE SWING SET = 3 for all lanes, MAX_SWING_REACHED = 1 for all lanes, PRE-EMPHASIS_SET = 3 for all lanes, MAX_PRE-EMPHASIS_REACHED = 1 for all lanes, MODULATION_FREQ = 1, SPREAD_AMP = 1, MAIN_LINK_CHANNEL_CODING_SET = 1)
3. Reference Source computes the remaining number of bytes to write:
   REQ_LEN = (9 - N - 1)
   and start address:
   REQ_ADDRESS = 100h + N
4. Reference Source sends the following Aux request:
   80-REQ_ADDRESS[15:8]-REQ_ADDRESS[7:0]-REQ_LEN-{WRITE_DATA[N] .. WRITE_DATA[N+REQ_LEN]
   (native aux write to address REQ_ADDRESS .. REQ_ADDRESS + REQ_LEN, data = WRITE_DATA(N .. N+REQ_LEN))
5. Wait for Aux reply. If reply isn't received within 400us, return to step 3. Check reply. If reply is unintelligible (received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, return to step 3. If reply is Aux NACK, proceed to step 5. If reply is Aux ACK, proceed to step 6. If reply is not Aux DEFER, Aux NACK or Aux ACK, exit test.

   Aux Defer is as follows:
   20h
   (1 byte - Native Aux Defer)

   Aux NACK is as follows:
   10b-BYTES_WRITTEN[7:0]
   (Native Aux NACK, number of bytes written = 0 .. REQ_LEN-1)

   Aux ACK is as follows:
   00h
   (Native Aux ACK)

Pass1: Valid reply command (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
Fail1: Invalid reply command
(all the checks below are done only if valid reply is received and is not a Defer)
Info: print Defer retry counter
Pass2: Native Aux ACK received
Fail2: some other Aux reply command received (print bytes)

6. Increment N by BYES_WRITTEN. Return to step 2.
7. Read back nine bytes at address 0100h, using procedure from test case 5.2.1.2, 'Read 12 Bytes From Valid DPCD Address'. Verify that read data matches write data.

   Pass1: Read bytes = 0A-84-7C-3F-3F-3F-3F-11-01h
   Fail1: Read bytes not= 0A-84-7C-3F-3F-3F-3F-11-01h

Result:

This test passes if all of the pass / fail checks below pass

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within the test steps passed
Fail2: One or more check(s) within the test steps failed

5.2.1.5 Write Nine Bytes to Read-Only DPCD Address

This test case verifies that the Sink DUT NACKs a write to a read-only DPCD address.

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   80-02-02-09-00-11-22-33-44-55-66-77-88-99
   (native aux write to address 0202h – 020Bh)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (ex - received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, return to step 2. If reply is Aux NACK, test is complete. If reply is not Aux DEFER or Aux NACK, exit test.

   Aux Defer is as follows:
   20h
   (Native Aux Defer)

   Aux NACK reply is as follows:
   10h
   (Native Aux NACK, no length field)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received

Pass2: Reply is Aux DEFER or Aux NACK
Fail2: Reply is not Aux DEFER or Aux NACK

Result:

This test passes if all of the pass/fail checks below pass

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within the test steps passed
Fail2: One or more check(s) within the test steps failed

5.2.1.6 Write EDID Offset (One Byte I^2C-Over-Aux Write)

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   00-00-50-00-00
   (Write one byte to I2C address 101|0000 (EDID offset), data = 0, MOT bit = 0)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, return to step 2. If reply is Aux ACK, proceed to step 4. If reply is not Aux DEFER or Aux ACK, exit test.

   Aux DEFER is as follows:
   20h
   (Native Aux Defer)

   Aux ACK is as follows:
   IJKLb-MNOPb-{BYTES_WRITTEN[7:0]}
   (KL = 00: Aux ACK, IJ = I2C Reply Command Field, MNOP = 0000b, BYTES_WRITTEN may or may not be present)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass6: Reply is Aux DEFER or Aux ACK
   Fail6: Reply is not Aux DEFER or Aux ACK
4. If BYTES_WRITTEN is present and equal to 0, issue status update request (below) and return to step 3. Otherwise, test is complete.

   Status update request for previous write command:
   20-00-50
   (Status Update Request flag = 1, same I2C address)

   Pass1: BYTES_WRITTEN=0 or BYTES_WRITTEN not present
   Fail1: BYTES_WRITTEN present and not= 0

Result:

This test passes if all of the pass / fail checks below pass

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within the test steps passed
Fail2: One or more check(s) within the test steps failed

5.2.1.7 Read One EDID Byte (One Byte I2C-Over-Aux Read)

This test case verifies that the Sink DUT responds correctly to a one byte I2C-Over-Aux read.

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   10-00-50-00
   (Read one byte from I2C address 101|0000 (EDID offset), MOT bit = 0)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (ex - received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux Defer, return to step 2. If reply is Aux ACK, proceed to step 4. If reply is not Aux DEFER, Aux NACK or Aux ACK, exit test.

   Aux DEFER is as follows:
   20h
   (Native Aux Defer)

   Aux ACK is as follows:
   IJKLb-MNOPb-{RB0}
   (KL == 00b (Aux ACK), IJ = I2C Reply Command Field, MNOP=0000b, {RB} = Read Byte)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass2: Reply is Aux DEFER or Aux ACK as defined above
   Fail2: Reply is not Aux DEFER, or Aux ACK as defined above
4. Sink should have terminated the I2C transaction after returning the requested amount of data because MOT=0 (however this cannot be verified by the Reference Source), so test is complete.

Result:

This test passes if all of the pass / fail checks below pass

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

5.2.1.8 EDID Read (1 Byte I2C-Over-Aux Segment Write, 1 Byte I²C-Over-Aux Offset Write, 128 Byte I²C-Over-Aux Read)

This test case should be repeated for all EDID segments, starting with segment 0. If the segment 0 write is NACK'd, do not attempt to read other segments.

This test case verifies that the Sink DUT responds correctly to an E-DDC read request, and returns exactly the expected amount of data.

The E-DDC read request consists of the following DDC transaction implemented using the I2C-Over-Aux protocol:

S-0x60-A/NA-SP-A/NA-SR-0xA0-A-0x00-A-SR-0xA1-A-RB0-A-...-RB127-NA-P
(S = START, SR = repeat START, 60 = E-DDC Segment address, SP = Segment Pointer, A0/A1 = E-DDC address, A=Ack, NA = Nack, RBx = Read Byte x, P = STOP)

Test Procedure:

1. Start one second timer. Timer is mandatory for this test case; test will fail if it is not completed within this interval.
2. Reference Source sends the following Aux request:
   40-00-30-00-SP
   (Write one byte to I2C address 011|0000 (EDID Segment), data = SP (Segment Pointer), MOT bit = 1)
3. Wait for Aux reply. If reply isn't received within 400us, return to step 2. Check reply. If reply is unintelligible (ex - received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, Aux NACK, return to step 2. If reply is Aux ACK, proceed to step 4. If reply command is not Aux DEFER, Aux NACK or Aux ACK, exit test.

   Aux DEFER reply is as follows:
   20h
   (Aux Defer)

   Aux NACK is as follows:
   10-00h
   (Aux NACK + bytes written = 0)

   Aux ACK is as follows:
   If I2C over aux command was accepted by sink, Aux reply should be as follows:
   IJKLb-MNOPb-{BYTES_WRITTEN[7:0]}
   (KL == 00b (Aux ACK), IJ = I2C Reply Command Field, MNOP=0000b, BYTES_WRITTEN may or may not be present)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass2: Reply is Aux DEFER, Aux NACK or Aux ACK as defined above
   Fail2: Reply is not Aux DEFER, Aux NACK or Aux ACK as defined above
   Pass3: Number of reply bytes = 1 or 2
   Fail3: More than 2 reply bytes
4. Check I2C Reply Command Field.
   If I2C Reply Command Field = 11b (invalid), fail and exit test. If I2C Reply Command Field = 01b

(I2C NACK), this means that the EDID ROM attached to the sink does not support E-DDC, which is not an error – proceed to step 6. If reply command is 00-01 (native Aux ACK, I2C-Over-Aux ACK, 1 byte written) the write has completed successfully – proceed to step 6.
If reply command = 20h (I2C DEFER), issue the following status update request and return to step 3:
60-00-30
(Status update request for previous write command, keeping MOT bit and address unchanged)

Pass1: I2C Reply Command Field = 00b (ACK) or 10b (DEFER) or 01b (NACK)
Fail1: I2C Reply Command Field = 11b (invalid)
Pass2: I2C Reply Command Field = ACK and BYTES_WRITTEN not present OR
I2C Reply Command Field = NACK and (BYTES_WRITTEN not present or BYTES_WRITTEN = 00h)
I2C Reply Command Field = DEFER and BYTES_WRITTEN not present
Fail2: I2C Reply Command Field = ACK and (BYTES_WRITTEN present) OR
I2C Reply Command Field = NACK and (BYTES_WRITTEN > 00h) OR
I2C Reply Command Field = DEFER and BYTES_WRITTEN present

5. Reference Source sends the following Aux request (should result in repeat START):
40-00-50-00-00
(Write one byte to I2C address 101|0000 (EDID Offset), data (offset)=0, MOT bit = 1)

6. Wait for Aux reply, check reply. If reply is unintelligible (ex - received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER, Aux NACK or there is no reply, return to step 5. If reply is Aux ACK, proceed to step 7. If reply command is not Aux DEFER, Aux NACK or Aux ACK, exit test.

   Aux DEFER reply is as follows:
   20h (1 byte - Aux Defer)

   Aux NACK is as follows:
   10-00h (Aux NACK + bytes written = 0)

   Aux ACK is as follows:
   If I2C over aux command was accepted by sink, Aux reply should be as follows:
   IJKLb-MNOPb-{BYTES_WRITTEN[7:0]}
   (KL == 00b (Aux ACK), IJ = I2C Reply Command Field, MNOP=0000b, BYTES_WRITTEN may or may not be present)

   Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
   Fail1: Unintelligible Reply command received
   Pass2: Reply is Aux DEFER, Aux NACK or Aux ACK as defined above
   Fail2: Reply is not Aux DEFER, Aux NACK or Aux ACK as defined above
   Pass3: Number of reply bytes = 1 or 2
   Fail3: More than 2 reply bytes

7. Check I2C Reply Command Field.
   If I2C Reply Command Field = 11b (invalid), fail and exit test. If I2C Reply Command Field = 01b (I2C NACK), this means that the there is no response to the DDC address – exit test. If reply is 00-01 (native Aux ACK, I2C-Over-Aux ACK, 1 byte written) the write has completed successfully – proceed to step 8.

If reply command = 20h (I2C DEFER), issue the following status update request and return to step 3:
60-00-50
(Status update request for previous write command, keeping MOT bit and address unchanged)

Pass1: I2C Reply Command Field = 00b (ACK) or 10b (DEFER) or 01b (NACK)
Fail1: I2C Reply Command Field = 11b (invalid)
Pass2: I2C Reply Command Field = ACK and BYTES_WRITTEN not present OR
I2C Reply Command Field = DEFER and BYTES_WRITTEN not present
Fail2: I2C Reply Command Field = ACK and (BYTES_WRITTEN present) OR
I2C Reply Command Field = NACK OR
I2C Reply Command Field = DEFER and BYTES_WRITTEN present

8. Set parameter N, index of read bytes returned, to zero.
9. Compute the remaining number of bytes to fetch:
   REQ_LEN = MIN(16, (128 - N - 1))
10. Reference Source sends the following Aux request (should result in repeat START):
    50-00-50-REQ_LEN
    (Read REQ_LEN bytes from I2C address 101|0000 (EDID Offset), data (offset)=0, MOT bit = 1)
11. Wait for Aux reply, check reply. If reply is unintelligible (ex - received SYNC preamble but no STOP, number of bits isn't a multiple of 8, more than maximum number of bytes allowed in a DisplayPort Aux reply, etc), exit test. If reply is Aux DEFER or there is no reply, return to step 10. If reply is Aux ACK, proceed to step 12. If reply command is not Aux DEFER or Aux ACK, exit test.

    Aux DEFER reply is as follows:
    20h (1 byte - Aux Defer)

    Aux ACK is as follows:
    If I2C over aux command was accepted by sink, Aux reply should be as follows:
    IJKLb-MNOPb-{RB}
    (KL == 00b (Aux ACK), IJ = I2C Reply Command Field, MNOP=0000b, {RB} = 1-16 Read Bytes)

    Pass1: Intelligible Reply command received (received valid SYNC preamble, STOP, 8*K bits for integer K, not too many reply bytes)
    Fail1: Unintelligible Reply command received
    Pass2: Reply is Aux DEFER or Aux ACK as defined above
    Fail2: Reply is not Aux DEFER, or Aux ACK as defined above
12. Push read bytes {RB} into EDID FIFO. Increment N by the number of bytes returned. If N >= 128, proceed to step 13 otherwise return to step 10.
13. Verify that exactly 128 bytes were received. Verify EDID checksums.

    Pass1: EDID checksums are valid
    Fail1: EDID checksums are invalid
14. Send Address-only request with MOT bit cleared to terminate the transaction.
    01-00-50

    Pass1: N = 128
    Fail1: N > 128

Result:

This test passes if all pass / fail checks below pass

Pass1: Test completed normally
Fail1: Test was terminated by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

5.2.1.9 Illegal Aux Request Syntax

1. Reference Source starts sending the following Aux request, but terminates somewhere in the middle of the request and tristates is aux differential output without sending STOP pattern.
   80-02-02-09-00-11-22-33-44-55-66-77-88-99
   (native aux write to address 0202h – 020Bh)
2. Reference Source enables its aux receive logic, waits for 1 us after sending the request, and verifies that the Reference Sink does not send a reply (i.e. that there is no switching activity detected on the aux differential pair).

Result:
This test passes if no Aux channel reply is detected. This test fails if an Aux channel reply is detected.

5.2.2 EDID Read

This test checks that the Sink DUT responds to an EDID read over the AUX CH, when EDID read is interleaved with DPCD reads.

Test Procedure:

1. Reference Source initiates EDID read over the AUX CH.
2. Reference Source will interleave EDID read transactions with reads to link status field in DPCD.
3. Verify that the Sink DUT returns the entire EDID block.
4. Verify that the checksum of the first EDID block is correct.
5. Reference Source reads the EDID extension blocks (if defined).
6. Verify that the Sink DUT returns the entire EDID extension block(s).
7. Verify that the checksum of the EDID extension block(s) is correct.

Result:

This test fails if the Sink DUT does not respond to EDID read over AUX CH, or if checksum of any EDID block is incorrect.

5.3 Sink Device Link Services Test Procedures

The following two items shall be tested:

- Link Training
- Link Maintenance

5.3.1 Link Training

DisplayPort Link Training is described in section 3.5.1.3 of the DisplayPort 1.1 Standard. Figure 2-36 ‘Link Training State’ shows the overall link training sequence. Figures 3-11 ‘Clock Recovery Sequence of Link

Training' and 3-12 'Channel Equalization Sequence of Link Training' show the details of the two phases of link training.

This set of tests verifies that the Sink DUT can successfully complete link training on the DisplayPort main link for all lane counts and link rates supported. These tests also check the correct operation of the link training state machine in the Sink DUT.

5.3.1.1 Successful Link Training at All Supported Lane Counts and Link Speeds

This test is repeated for all lane counts and link rates up to the maximum supported by the Sink DUT.

Test Procedure:

1. Verify that HPD is asserted. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.
   If one second test duration feature is selected, start one second timer.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
2. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field.
3. Reference Source writes to LANE_COUNT_SET in DPCD to set the desired lane count.
4. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field. Start the link training timer.
5. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 6. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 5. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, switch to low link rate if at high link rate; if already at low link rate fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Warning2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} while at high link rate; switching to low link rate
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
7. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 8. If LANEx_CR_DONE = 0 for any active lane, switch to low link rate if not already at low link rate; otherwise fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 switch to low link rate if not already at low link rate and repeat step 5, otherwise fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 7.

   Note1: Equalization succeeded on all active lanes
   Warning1: Equalization failed on lanes {lanes that failed equalization}
   Note2: Symbol lock succeeded on all active lanes.
   Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
   Note3: Inter-lane alignment succeeded on all active lanes.
   Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0} while at high link rate; switching to low link rate
   Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
   Pass5: N iterations at test step 7; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
   Warning5: N iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
   Warning5: 5 iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} while at high link rate; switching to low link rate
   Fail5: 5 iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

8. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
9. Verify that the Sink DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

   Pass1: HPD not de-asserted between steps 1 and 8
   Fail1: HPD de-asserted between steps 1 and 8
10. Reference Source sends the idle pattern on all lanes.
11. Verify that link training has been completed in 10ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

12. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test passes if all pass / fail checks below pass. This test fails if the DisplayPort main link is not trained to the proper lane count, or link is not active with Reference Source sending idle pattern.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Link training completed successfully at target link rate and lane count
Target LINK_BW = K, Actual LINK_BW = K
Target LANE_COUNT = X, Actual LANE_COUNT = X
Fail3: Link training did not complete successfully at target link rate or lane count
Target LINK_BW = K, Actual LINK_BW = L (L not= K)
Target LANE_COUNT = X, Actual LANE_COUNT = Y (Y not= X)

Pass4: All pass/fail checks within the test steps succeeded
Fail4: One or more pass/fail checks with the test steps failed

5.3.1.2 Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence

The objective of this test is to verify that when it is unable to achieve clock recovery lock, the Sink DUT requests voltage swing adjustments as specified in the DisplayPort specification. To achieve this, the Reference Source forces the first phase of link training to fail at all settings other than the highest differential voltage swing by not sending any transmitted signal.

Once the Sink DUT has requested all of the required voltage swing settings, the Reference Source sends a valid signal to provide an opportunity for the Sink DUT to achieve clock recovery lock. However, this only gives only one opportunity at one combination of pre-emphasis and differential voltage swing for the Sink DUT to achieve lock. Because this test case makes successful completion of link training more difficult and because the objective of this test case is completed before the end of the clock recovery phase of link training, this test does not fail if clock recovery lock is not achieved at the maximum differential voltage swing. If clock recovery lock is successful but the subsequent link training steps fail, the test will fail.

Note: 'Active lane' in this test case refers to any lane that is reported as active due to the 'MAX_LANE_COUNT' setting. This includes lanes that are shut off to cause clock recovery lock to fail.

Test Procedure:

1. Verify that HPD is asserted. HPD should remain asserted for remainder of the test. If HPD is de-asserted at any time during the test, exit test.
   If one second test duration feature is selected, start one second timer.

Pass1: HPD is asserted
Fail1: HPD is not asserted

2. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field. Reference Source will attempt to train the link at the low link rate.
3. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Sink DUT.
4. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and with pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. The intention here is to not allow the Sink DUT to achieve clock recovery lock, so Reference Source leaves the transmitters on all active lanes disabled. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field. Start the link training timer.
5. After 100us, Reference Source reads DPCD Link/Sink Status Field. LANEx_CR_DONE bits should be cleared. Reference Source reads DPCD ADJUST_REQUEST_LANEx {x=0_1, 2_3} for all active lanes. The Sink DUT must request adjustments to the differential voltage swing and / or pre-emphasis levels. Differential voltage swing increase requests must be made within 5 iterations until TRAINING_LANEx_SET.MAX_SWING_REACHED is asserted. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx = 11b for any active lane, set TRAINING_LANEx_SET.VOLTAGE_SWING_LANEx = 11b, set TRAINING_LANEx_SET.MAX_SWING_REACHED = 1, transmit training pattern 1 on that lane, and flag that lane's voltage swing adjustment sequence as complete. If all active lanes are flagged as complete, proceed to step 6. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx remains unchanged for 5 iterations any lane not flagged as complete, fail and exit test. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx not= 11b for any active lane, adjust pre-emphasis and / or voltage swing as requested in ADJUST_REQUEST_LANEx and repeat step 5.

   Pass1: LANEx_CR_DONE = 0 for all active lanes not flagged as complete
   Fail1: LANEx_CR_DONE = 1 for any active lane not flagged as complete
   Pass2: LANEx_CR_DONE = 1 for all active lanes flagged as complete
   Fail2: LANEx_CR_DONE = 0 for any active lane flagged as complete
   Pass3: VOLTAGE_SWING_LANEx unchanged or incremented {repeat for all active lanes}
   Fail3: VOLTAGE_SWING_LANEx decremented {repeat for all active lanes}
   Note4: M iterations at VOLTAGE_SWING_LANEx= N
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Fail4: 5 iterations at VOLTAGE_SWING_LANEx = N
   {N = {0,1,2}, repeat for all active lanes}

Note: A reference cable is used to connect the Reference Source and the Sink DUT so it is expected that the Sink DUT will achieve CR lock with the maximum voltage swing. However, the test will only give a warning and not fail if CR lock fails.

6. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field. If these bits are set, Clock Recovery sequence is complete; proceed to step 8. If these bits are not set, exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

7. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
8. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 9. If LANEx_CR_DONE = 0 for any active lane, switch to low link rate if not already at low link rate; otherwise fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5, switch to low link rate if not already at low link rate, carry out step 5 from test 5.3.1.1, and continue from step 6 of this test case; otherwise fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 8.

   Note1: Equalization succeeded on all active lanes
   Warning1: Equalization failed on lanes {lanes that failed equalization}
   Note2: Symbol lock succeeded on all active lanes.
   Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
   Note3: Inter-lane alignment succeeded on all active lanes.
   Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0} while at high link rate; switching to low link rate
   Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
   Pass5: N iterations at test step 7; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
   Warning5: N iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
   Warning5: 5 iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} while at high link rate; switching to low link rate
   Fail5: 5 iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

9. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
10. Verify that the Sink DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 1 and 9
    Fail1: HPD de-asserted between steps 1 and 9
11. Reference Source sends the idle pattern on all lanes.
12. Verify that link training has been completed in 10ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

13. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more pass/fail checks with the test steps failed

5.3.1.3 Successful Link Training to a Lower Link Rate Due To Clock Recovery Lock Failure During Clock Recovery Sequence

The objective of this test is to verify that after a clock recovery lock failure, it is possible to train the Sink DUT to the low link rate. To achieve this, the Reference Source forces the first phase of link training to fail at the high link rate by not sending any transmitted signal.

Note: Support of the high (2.7Gbps) link rate is optional. This test is skipped if the test operator has reported that Sink DUT supports only the low (1.62Gbps) link rate.
Note: 'Active lane' in this test case refers to any lane that is reported as active due to the 'MAX_LANE_COUNT' setting. This includes lanes that are shut off to cause clock recovery lock to fail.

Test Procedure:

1. Verify that HPD is asserted. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test. If one second test duration feature is selected, start one second timer.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted

2. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field.

3. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Sink DUT.

4. Reference Source starts with minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and with pre-emphasis disabled (TRAINING_LANEx_SET.PRE_EMPHASIS_SET = 00b) on all active lanes. The intention here is to not allow the Sink DUT to achieve clock recovery lock, so Reference Source leaves the transmitters on all active lanes disabled. Start the link training timer.

5. After 100us, Reference Source reads DPCD Link/Sink Status Field. LANEx_CR_DONE bits should be cleared. Reference Source reads DPCD ADJUST_REQUEST_LANEx {x=0_1, 2_3} for all active lanes. The Sink DUT must request adjustments to the differential voltage swing and / or pre-emphasis levels. Differential voltage swing increase requests must be made within 5 iterations until TRAINING_LANEx_SET.MAX_SWING_REACHED is asserted. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx = 11b for any active lane, set TRAINING_LANEx_SET.VOLTAGE_SWING_LANEx = 11b, set TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 and flag that lane's voltage swing adjustment sequence as complete. If all active lanes are flagged as complete, proceed to step 6. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx remains unchanged for 5 iterations any

lane not flagged as complete, fail and exit test. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx not= 11b for any active lane, adjust pre-emphasis and / or voltage swing as requested in ADJUST_REQUEST_LANEx and repeat step 5.

Pass1: LANEx_CR_DONE = 0 for all active lanes
Fail1: LANEx_CR_DONE = 1 for any active lane
Pass2: VOLTAGE_SWING_LANEx unchanged or incremented {repeat for all active lanes}
Fail2: VOLTAGE_SWING_LANEx decremented {repeat for all active lanes}
Note3: M iterations at VOLTAGE_SWING_LANEx= N
{N = {0,1,2}, M < 5, repeat all active lanes}
Fail3: 5 iterations at VOLTAGE_SWING_LANEx = N
{N = {0,1,2}, repeat for all active lanes}

6. Reference Source writes LINK_BW_SET byte of DPCD = 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.
7. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field.
8. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 9. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 8. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

9. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
10. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 11. If LANEx_CR_DONE = 0 for any active lane, fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 10.

Note1: Equalization succeeded on all active lanes
Warning1: Equalization failed on lanes {lanes that failed equalization}
Note2: Symbol lock succeeded on all active lanes.
Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
Note3: Inter-lane alignment succeeded on all active lanes.
Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
Note4: LANEx_CR_DONE = 1 for all active lanes
Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
Pass5: N iterations at test step 7; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
Warning5: N iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
Fail5: 5 iterations at test step 7; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

11. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
12. Verify that the Sink DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 1 and 12
    Fail1: HPD de-asserted between steps 1 and 12
13. Reference Source sends the idle pattern on all lanes.
14. Verify that link training has been completed in 10ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms
15. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test passes if all pass / fail checks below pass. This test fails if the DisplayPort main link is not trained to the proper lane count, or link is not active with Reference Source sending idle pattern.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks within the test steps succeeded
Fail3: One or more pass/fail checks with the test steps failed

5.3.1.4 Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence

The objective of this test is to verify that when it is unable to achieve Symbol, Equalization and Inter-lane Alignment lock the Sink DUT requests voltage swing and or pre-emphasis adjustments to attempt to achieve lock. To force a failure of the above-mentioned locks, the Reference Source forces the second phase of link training to fail for four iterations by transmitting the wrong training pattern.

After four iterations, the Reference Source gives the Sink DUT an opportunity to achieve lock by transmitting training pattern 2. However, this only gives one opportunity at one combination of pre-emphasis and differential voltage swing for the Sink DUT to achieve lock. Because this test case makes successful completion of link training more difficult and because the objective of this test case is completed before the end of the equalization phase of link training, this test does not fail if equalization, symbol lock and inter-lane alignment lock do not complete successfully. If equalization, symbol lock and inter-lane alignment lock are successful but subsequent link training steps fail, the test will fail.

Test Procedure:

1. Verify that HPD is asserted. HPD should remain asserted for remainder of the test. If HPD is de-asserted at any time during the test, exit test.
   If one second test duration feature is selected, start one second timer.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
2. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field.
3. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Sink DUT.
4. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field. Start the link training timer.
5. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 6. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 5. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, switch to low link rate if at high link rate; if already at low link rate fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Warning2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} while at high link rate;

switching to low link rate
Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
{N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Reference Source continues to transmit training pattern 1 on all active lanes. The intention here is to not allow the Sink DUT to complete Channel Equalization. Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
7. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. For each lane, LANEx_CR_DONE may remain set, but all of the other bits should be cleared. If any of LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK and INTERLANE_ALIGN_DONE is set, fail and exit test. The Sink DUT should request a change in pre-emphasis and/or differential voltage swing within 5 iterations. After four iterations at this test step, proceed to step 8.

   Pass1: Equalization failed on all active lanes (expected)
   Fail1: False equalization success reported on lanes {lanes that passed equalization}
   Pass2: Symbol lock failed on all active lanes (expected)
   Fail2: False symbol lock success reported on lanes {lanes that passed symbol lock}
   Pass3: Inter-lane alignment failed on all active lanes (expected)
   Fail3: False inter-lane alignment success reported on lanes {lanes that passed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}
   Pass3: (check only on fourth iteration) Sink DUT requested at least one adjustment to pre-emphasis or differential voltage swing
   Fail3: (check only on fourth iteration) Sink DUT did not request any adjustments to pre-emphasis or differential voltage swing
8. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
9. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If LANEx_CR_DONE = 0 for any active lane, exit test. If one or more of the other bits is/are not set, exit test.

   Note1: Equalization succeeded on all active lanes
   Warning1: Equalization failed on lanes {lanes that failed equalization}
   Note2: Symbol lock succeeded on all active lanes.
   Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
   Note3: Inter-lane alignment succeeded on all active lanes.
   Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
   Note5: Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}

Warning5: Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} – terminating link training

10. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
11. Verify that the Sink DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 1 and 10
    Fail1: HPD de-asserted between steps 1 and 10
12. Reference Source sends the idle pattern on all lanes.
13. Verify that link training has been completed in 10ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms
14. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more pass/fail checks with the test steps failed

5.3.1.5 Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence

The objective of this test is to verify that after an equalization sequence failure, it is possible to train the Sink DUT to the low link rate. To achieve this, the Reference Source forces the second phase of link training to fail at the high link rate by sending the wrong training pattern.
Successful Clock Recovery lock at the high link rate is mandatory for this test. The test will fail if Clock Recovery lock fails at the high link rate because it prevents completion of the test case.
Note: Support of the high (2.7Gbps) link rate is optional. This test is skipped if the test operator has reported that Sink DUT supports only the low (1.62Gbps) link rate.

Test Procedure:

1. Verify that HPD is asserted. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test. If one second test duration feature is selected, start one second timer.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
2. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field.
3. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Sink DUT.

4. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field. Start the link training timer.
5. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 6. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 5. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} – aborting test due to failure to achieve clock recovery lock at high link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Reference Source continues to transmit training pattern 1 on all active lanes. The intention here is to not allow the Sink DUT to complete Channel Equalization. Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.
7. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. For each lane, LANEx_CR_DONE may remain set, but all of the other bits should be cleared. If any of LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK and INTERLANE_ALIGN_DONE is set, fail and exit test. The Sink DUT should request a change in pre-emphasis and/or differential voltage swing within 5 iterations. After five iterations at this test step, proceed to step 8.

   Pass1: Equalization failed on all active lanes (expected)
   Fail1: False equalization success reported on lanes {lanes that passed equalization}
   Pass2: Symbol lock failed on all active lanes (expected)
   Fail2: False symbol lock success reported on lanes {lanes that passed symbol lock}
   Pass3: Inter-lane alignment failed on all active lanes (expected)
   Fail3: False inter-lane alignment success reported on lanes {lanes that passed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}
   Pass3: (check only on fifth iteration) Sink DUT requested at least one adjustment to pre-emphasis or differential voltage swing
   Fail3: (check only on fifth iteration) Sink DUT did not request any adjustments to pre-emphasis or differential voltage swing
8. Reference Source writes LINK_BW_SET byte of DPCD = 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

9. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Sink DUT DPCD Link Configuration Field.

10. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 11. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 10. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
    Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2}, M < 5, repeat for all active lanes}
    Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

11. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field.

12. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 13. If LANEx_CR_DONE = 0 for any active lane, fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 12.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Note3: Inter-lane alignment succeeded on all active lanes.
    Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
    Note4: LANEx_CR_DONE = 1 for all active lanes
    Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
    Pass5: N iterations at test step 12; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
    Warning5: N iterations at test step 12; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
    Fail5: 5 iterations at test step 12; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

13. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Sink DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
14. Verify that the Sink DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 1 and 12
    Fail1: HPD de-asserted between steps 1 and 12
15. Reference Source sends the idle pattern on all lanes.
16. Verify that link training has been completed in 10ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms
17. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test passes if all pass / fail checks below pass. This test fails if the DisplayPort main link is not trained to the proper lane count, or link is not active with Reference Source sending idle pattern.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Link training completed successfully
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: All pass/fail checks within the test steps succeeded
Fail3: One or more pass/fail checks with the test steps failed

5.3.1.6 Lane Count Reduction

Test Procedure:

Note: This test is skipped if the Sink DUT only supports one lane.

1. Set the DisplayPort main link to 1.62Gbps data rate, and the maximum number of lanes supported by the Sink DUT.
2. Reference Source carries out link training (see steps 4-11 of test 5.3.1.1), and transmits idle pattern on all lanes.
3. Reference Source writes 0x1 to the LANE_COUNT_SET field in DPCD.
4. Reference Source continues to transmit idle pattern on lane 0, and disables all other lanes.

5. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test fails if the DisplayPort main link is not active at 1 lane and 1.62Gbps with Sink DUT locked to the idle pattern.

5.3.1.7 Lane Count Increase

Test Procedure:

Note: This test is skipped if the Sink DUT only supports one lane.

1. Set the DisplayPort main link to 1.62Gbps data rate, and one lane.
2. Reference Source carries out link training (see steps 4-11 of test 5.3.1.1), and transmits idle pattern on all lanes.
3. Reference Source stops transmission on all lanes.
4. Reference Source writes 0x2 (if maximum number of lanes supported by Sink DUT is 2 lanes), or 0x4 (if Sink DUT supports up to 4 lanes) to the LANE_COUNT_SET field in DPCD.
5. Reference Source carries out link training (see steps 4-11 of test 5.3.1.1).
6. Verify that the Sink DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

Result:

This test fails if the DisplayPort main link is trained to the maximum lane count at 1.62Gbps with Sink DUT locked to the idle pattern.

5.3.2 Link Maintenance

This set of tests check that the Sink DUT carries out the appropriate action when there is a loss of link (loss of symbol lock, loss of clock recovery lock, or loss of inter-lane alignment lock).

These test cases shall begin with the DisplayPort main link already trained, and lane count set to the maximum number of lanes supported by the Sink DUT. The link maintenance tests can be done at either link rate.

5.3.2.1 IRQ_HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock

The objective of this test is to force the Sink DUT to report loss of symbol lock and clock recovery lock using the HPD interrupt and link status reporting mechanism. This test begins with the main link already trained.

Test Procedure:

1. Reference Source stops transmitting the idle pattern. Reference Source stops transmission and parks the differential symbols. The intent is to force loss of symbol lock and clock recovery lock.
2. Verify that the Sink DUT transmits an IRQ_HPD pulse (low pulse between 0.5ms – 1ms).
3. Reference Source reads Link Status registers, and verifies that the LANEx_SYMBOL_LOCKED and LANEx_CR_DONE bits are cleared, and the LINK_STATUS_UPDATED bit is set.
4. Reference Source re-trains the main link with the same settings and verifies that training completes successfully (see steps 4-12 of test 5.3.1.1).

Result:

This test fails if the Sink DUT does not toggle IRQ HPD pulse, clear the LANEx_SYMBOL_LOCKED and LANEx_CR_DONE bits and set the LINK_STATUS_UPDATED bit in DPCD.
This test fails if the main link re-training does not complete successfully.

5.3.2.2 IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

The objective of this test is to force the Sink DUT to report loss inter-lane alignment using the HPD interrupt and link status reporting mechanism.

Test Procedure:

Note: This test is skipped if the Sink DUT supports the maximum of one lane.

1. Reference Source disables inter-lane skew.
2. Verify that the Sink DUT toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms).
3. Verify that the INTERLANE_ALIGN_DONE bit is cleared and LINK_STATUS_UPDATED bit is set in DPCD.
4. Reference Source re-trains the main link with the same settings and verifies that training completes successfully (see steps 4-12 of test 5.3.1.1).

Result:

This test fails if the Sink DUT does not toggle IRQ HPD pulse, clear the INTERLANE_ALIGN_DONE bit and set the LINK_STATUS_UPDATED bit in DPCD.
This test fails if the main link re-training does not complete successfully.

5.4 Sink Isochronous Transport Services Test Procedures

In Sink Isochronous Transport Services Test, capability of Sink DUT of re-constructing the original main video stream shall be tested.

5.4.1 Main Video Stream Reconstruction

This set of tests check the main video stream reconstruction capability of the DisplayPort main link. Main video stream reconstruction is further broken down into two parts 1) pixel steering – the reconstruction from stream data into pixels, and 2) data unpacking and unstuffing. It is not the intention of this test to cover the interoperability of all video timings and color formats.

Note that the test procedures assume that the DPCD extension method is used. If this method is not available, some other vendor specific or manual method will be required.

For fixed timing Sink DUTs (for example, embedded devices) which only support one video timing, execute the Pixel data reconstruction test at the supported timing. The other tests in this section are skipped.

5.4.1.1 Pixel data reconstruction

Note: For fixed timing Sink DUTs, execute this test at the supported video timing.

Test Procedure:

1. Set the DisplayPort main link to 1.62Gbps data rate, and one lane.

   Note: This test should be repeated for all lane widths supported by the Sink DUT.

2. Reference Source sends the test pattern at VGA 640x480 @60Hz. If this mode is not supported, execute the test at the EDID definition of preferred timing of the Sink DUT.

3. This test is repeated for all color formats supported by the Sink DUT. Please refer to Table 3-5 for the list of color formats supported in DisplayPort and the test pattern that is used.
4. Reference Source reads the TEST_CRC_SUPPORTED bit.
5. If TEST_CRC_SUPPORTED is 0, skip steps 6-10. In this case the DPCD extension method is not supported by the Sink DUT, and the displayed test pattern must be checked visually for pass / fail by the test operator. If TEST_CRC_SUPPORTED is 1, the DPCD extension method is supported; continue on to step 6.
6. Reference Source sets the TEST_SINK_START bit in DPCD.
7. Reference Source reads the TEST_CRC_COUNT field. Wait until the TEST_CRC_COUNT field is greater than zero so the CRC results are valid.
8. Reference Source reads the TEST_CRC_x_x fields.
9. Verify that the TEST_CRC_x_x fields are equal to the Reference Source's internal CRC calculations.
10. Reference Source clears the TEST_SINK_START bit in DPCD.

Result:

This test fails if the TEST_CRC_x_x read from the Sink DUT do not match the CRC calculated by the Reference Source, or if the test operator reports that the visual check failed

5.4.1.2 Main Stream Data Unpacking and Unstuffing – Least Packed TU

This tests the main stream data unpacking and unstuffing in the case where a transfer unit (TU) is the least packed with data symbols.

Note: This test is skipped for a fixed timing Sink DUT.

Test Procedure:

1. Set the DisplayPort main link to maximum number of lanes supported by the Sink DUT, and 2.7Gbps if supported (1.62Gbps if only low link rate is supported).
2. Reference Source sends the test pattern at VGA 640x480 @60Hz, 18-bpp RGB with VESA dynamic range. If this mode is not supported, execute the test at the EDID definition of preferred timing of the Sink DUT. Please refer to Table 3-5 for the test pattern that is used.
3. Reference Source reads the TEST_CRC_SUPPORTED bit.
4. If TEST_CRC_SUPPORTED is 0, skip steps 5-9. In this case the DPCD extension method is not supported by the Sink DUT, and the displayed test pattern must be checked visually for pass / fail by the test operator. If TEST_CRC_SUPPORTED is 1, the DPCD extension method is supported; continue on to step 5.
5. Reference Source sets the TEST_SINK_START bit in DPCD.
6. Reference Source reads the TEST_CRC_COUNT field. Wait until the TEST_CRC_COUNT field is greater than zero so the CRC results are valid.
7. Reference Source reads the TEST_CRC_x_x fields.
8. Verify that the TEST_CRC_x_x fields are equal to the Reference Source's internal CRC calculations.
9. Reference Source clears the TEST_SINK_START bit in DPCD.

Result:

This test fails if the TEST_CRC_x_x read from the Sink DUT do not match the CRC calculated by the Reference Source, or if the test operator reports that the visual check failed.

5.4.1.3 Main Stream Data Unpacking and Unstuffing – Most Packed TU

This tests the main stream data packing and stuffing in the case where a transfer unit (TU) is the most packed with data symbols.

Note: This test is skipped for a fixed timing Sink DUT.

Test Procedure:

1. Set the DisplayPort main link to use low link rate.
2. Set the DisplayPort main link to use 1 lane lane count, video mode as specified by Table 4-2.

Note: This test is repeated for all lane counts supported by the Sink DUT. For consumer Sink DUTs, please refer to Table 4-3.

3. Reference Source sends the test pattern. Please refer to Table 3-5 for the test pattern that is used.
4. Reference Source reads the TEST_CRC_SUPPORTED bit.
5. If TEST_CRC_SUPPORTED is 0, skip steps 6-10. In this case the DPCD extension method is not supported by the Sink DUT, and the displayed test pattern must be checked visually for pass / fail by the test operator. If TEST_CRC_SUPPORTED is 1, the DPCD test automation method is supported; continue on to step 6.
6. Reference Source sets the TEST_SINK_START bit in DPCD.
7. Reference Source reads the TEST_CRC_COUNT field. Wait until the TEST_CRC_COUNT field is greater than zero so the CRC results are valid.
8. Reference Source reads the TEST_CRC_x_x fields.
9. Verify that the TEST_CRC_x_x fields are equal to the Reference Source's internal CRC calculations.
10. Reference Source clears the TEST_SINK_START bit in DPCD.

Result:

This test fails if the TEST_CRC_x_x read from the Sink DUT do not match the CRC calculated by the Reference Source, or if the test operator reports that the visual check failed.

5.4.2 Main Video Stream Format Change Handling

The required behavior of Sink DUT upon the main video stream format change is defined in Section 5.2.3 of DisplayPort Standard Version.1.1. Whether Sink DUT complies with the requirement is tested in this test.

Note: This test is skipped for a fixed timing Sink DUT.

Test Procedure:

1. Set the DisplayPort main link to 1.62Gbps data rate, and one lane.
2. Reference Source sends the ramp test pattern at VGA 640x480 @60Hz, 18-bpp RGB with VESA dynamic range (any bpp supported by the Sink DUT can be used here).
3. Reference Source reads the TEST_CRC_SUPPORTED bit.

4. If TEST_CRC_SUPPORTED is 0, skip steps 5-9. In this case the DPCD extension method is not supported by the Sink DUT, and the displayed test pattern must be checked visually for pass / fail by the test operator. If TEST_CRC_SUPPORTED is 1, the DPCD extension method is supported; continue on to step 5.
5. Reference Source sets the TEST_SINK_START bit in DPCD.
6. Reference Source reads the TEST_CRC_COUNT field. Wait until the TEST_CRC_COUNT field is greater than zero so the CRC results are valid.
7. Reference Source reads the TEST_CRC_x_x fields.
8. Verify that the TEST_CRC_x_x fields are equal to the Reference Source's internal CRC calculations.
9. Reference Source clears the TEST_SINK_START bit in DPCD.
10. Reference Source sends the idle pattern 5 times.
11. Reference Source sends the test pattern at the new main video stream format (the EDID definition of preferred timing of the Sink DUT).
12. If TEST_CRC_SUPPORTED is 0, skip steps 13-17. In this case the DPCD extension method is not supported by the Sink DUT, and the displayed test pattern must be checked visually for pass / fail by the test operator. If TEST_CRC_SUPPORTED is 1, the DPCD extension method is supported; continue on to step 13.
13. Reference Source sets the TEST_SINK_START bit in DPCD.
14. Reference Source reads the TEST_CRC_COUNT field. Wait until the TEST_CRC_COUNT field is greater than zero so the CRC results are valid.
15. Reference Source reads the TEST_CRC_x_x fields.
16. Verify that the TEST_CRC_x_x fields are equal to the Reference Source's internal CRC calculations.
17. Reference Source clears the TEST_SINK_START bit in DPCD.

Result:

This test fails if the TEST_CRC_x_x values read from the Sink DUT do not match the CRCs calculated by the Reference Source, or if the test operator reports that either visual check failed.

6 Branch Device Tests

This section describes the compliance test specification for Branch DUTs, Legacy to DisplayPort converters and DisplayPort to Legacy converters.

As shown in the figures below, Reference Source and Reference Sink Devices are used for testing Branch DUTs. It is assumed that the Reference Source and Reference Sink can communicate with each other during the testing. The method of communication between the Reference Source and Reference Sink Devices is specific to the Reference Device implementation.

- For Converters, only the DisplayPort link is tested.
- For Concentrators and Replicaters, only Port 0 is tested.

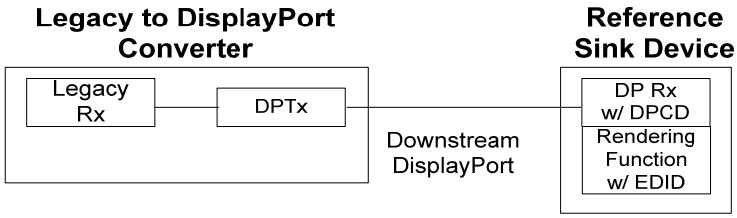

Figure 6-1: Legacy to DisplayPort Converter Compliance Test Setup

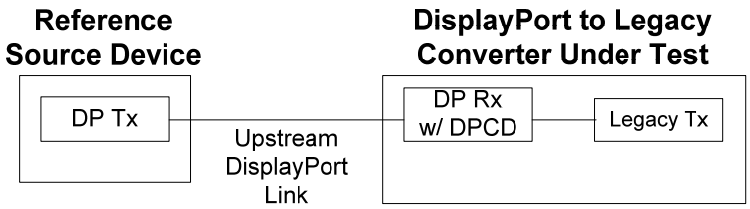

Figure 6-2: DisplayPort to Legacy Converter Compliance Test Setup

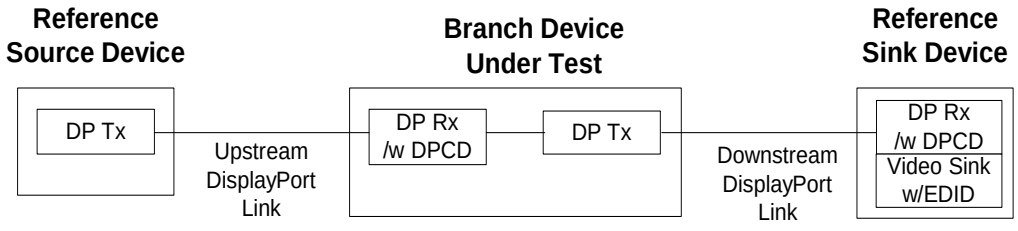

Figure 6-3: Branch Device (Repeater, Concentrator, Replicater) Compliance Test Setup

6.1 Branch Device Compliance Test Assertions (Informative)

During Branch Device test execution, some assertions can be implemented to verify that the Branch DUT is following the DisplayPort protocol. The following assertions may be added:

Aux Channel Requests (Downstream Link):

- Verify that minimum duration preamble occurs during Aux-CH SYNC
- Verify that Aux request has START pattern immediately after SYNC
- Verify that Aux request ends with STOP
- Verify that the number of bits between SYNC and STOP is a multiple of 8
- Verify that Aux Request Command (CMD) is valid
- Verify that for writes, the number of write bytes matches the LENGTH field
- Verify that the Branch DUT does not indicate illegal voltage swing / pre-emphasis combinations on any downstream link active lane via DPCD TRAINING_LANEx_SET fields

Main Link (Downstream):

- Verify that after the Brancu DUT indicates that downstream link training is complete by writing TRAINING_PATTERN_SET to 00h, all downstream active lanes transition from Training Pattern 2 to BS-Idle pattern.
- Verify that whenever BS-Idle pattern is transmitted on the downstream link, Branch DUT sends at least 5 BS-Idle patterns before enabling video stream

Aux Channel Replies (Upstream Link):

- Verify that minimum duration preamble occurs during Aux-CH SYNC
- Verify that Aux request has START pattern immediately after SYNC
- Verify that Aux request ends with STOP
- Verify that the number of bits between SYNC and STOP is a multiple of 8
- Verify that Aux Reply Command (CMD) is valid
- Verify that for reads, the number of read bytes (returned from Sink to Source) matches the Request LENGTH field
- Verify that the Aux Reply always begins within 400us of the end of an Aux Request (no-reply is allowed, but if there is a reply it must not commence later than 400us after the request)
- The number of Aux Request retries before an Aux reply is received exceeds three

Hot Plug Detect Line:

- Verify that the Hot Plug Detect interrupt duration is between 500 and 1000 us
- Verify that the Branch DUT does not request illegal voltage swing / pre-emphasis combinations on any upstream link active lane via the DPCD ADJUST_REQUEST_LANEx fields

6.2 Branch Device Services Test Procedures

In Branch Device Services Tests, Aux wake, Aux retry, EDID reads and DPCD reads are verified.

The Branch DUT shall forward Aux transactions to its downstream device.

The following DisplayPort Tx capabilities shall be tested:

- Read and interpret EDID in Reference Sink via AUX CH read transaction

The following DisplayPort Rx capabilities shall be tested:

- Send EDID data in reply to EDID read transaction via AUX CH.

Note: The DisplayPort Tx may initiate EDID read transaction anytime when HPD signal is high. It is not the intention of these tests to fully verify EDID compliance and functionality.

6.2.1 Auxiliary Channel Protocol

This set of tests verifies that the Branch DUT responds correctly to aux channel read and write requests. Both native aux and I2C over aux transactions are covered. These tests shall be run with the main link off, to ensure that Branch DUT will not be issuing IRQ_HPD requests.

Except where otherwise stated, the Reference Sink will use its default Receiver Capabilities (which must indicate support for DisplayPort Revision 1.1, up to 2.7 Gbps, 4 lanes, 0.5% downspread supported), so as to allow the Branch DUT to declare its maximum lane count / link rate capabilities.

The declared Receiver Capability Field contents will be compared against the values read back in these test cases.

6.2.1.1 Read One Byte from Valid DPCD Address

This test case is based on Sink DUT case 5.2.1.1, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-4 of Sink DUT case 5.2.1.1.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.2 Read Twelve Bytes from Valid DPCD Address

This test case is based on to Sink DUT case 5.2.1.2, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-6 of Sink DUT case 5.2.1.2.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.3 Write One Byte to Valid DPCD Address

This test case is based on Sink DUT case 5.2.1.3, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-4 of Sink DUT case 5.2.1.3.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.4 Write Nine Bytes to Valid DPCD Addresses

This test case is based on Sink DUT case 5.2.1.4, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-6 of Sink DUT case 5.2.1.4.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.5 Write Nine Bytes to Read-Only DPCD Address

This test case is based on Sink DUT case 5.2.1.5, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-3 of Sink DUT case 5.2.1.5.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.6 Write EDID Offset (One Byte I^2C-Over-Aux Write)

This test case is based on Sink DUT case 5.2.1.6, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-4 of Sink DUT case 5.2.1.6.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.7 Read One EDID Byte (One Byte I2C-Over-Aux Read)

This test case is based on Sink DUT case 5.2.1.7, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-4 of Sink DUT case 5.2.1.7.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.8 EDID Read (1 Byte I2C-Over-Aux Segment Write, 1 Byte I²C-Over-Aux Offset Write, 128 Byte I²C-Over-Aux Read)

This test case is based on Sink DUT case 5.2.1.8, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-14 of Sink DUT case 5.2.1.8.

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.1.9 Illegal Aux Request Syntax

This test case is identical to Sink DUT case 5.2.1.9, but with 'Sink DUT' replaced by 'Branch DUT'.

6.2.1.10 Update Receiver Capabilities Field Based on Downstream Device Receiver Capabilities

The objective of this test case is to verify that the Branch DUT updates its Receiver Capabilities based on the Reference Sink's Receiver Capabilities.

In this test case, the Reference Sink sets its MAX_LINK_RATE field (DPCD:00001h) to 06h indicating that only the 1.62Gbps link rate is supported, and sets its MAX_LANE_COUNT field (DPCD:00002h) to 01h indicating that it only supports one lane.

This test case is based on Sink DUT case 5.2.1.2, but with 'Sink DUT' replaced by 'Branch DUT'.

Test Procedure:

1. Reference Sink de-asserts HPD for more that 2ms to signify a disconnect, then re-asserts HPD. If one second test duration feature is selected, start one second timer.
2. Reference Source waits for de-assertion and re-assertion of HPD by Branch DUT.
3. Carry out steps 2-5 of Sink DUT case 5.2.1.2.
4. Check reply.

   Pass1: Read bytes R0 and R3-R11 match Branch DUT's Receiver Capabilities fields;
   Fail1: Read bytes R0 and R3-R11 do not match Branch DUT's Receiver Capabilities fields
   Pass2: Read byte R1 = 06h
   Fail2: Read byte R1 not= 06h
   Pass3: Read byte R2 = 01h
   Fail3: Read byte R2 not= 01h

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed normally
Fail1: Test was interrupted by timeout or by test operator

Pass2: All pass / fail checks within test steps passed
Fail2: One or more check(s) within test steps failed

6.2.2 Aux Reads after HPD Connect

The following test cases verify Aux reads on Hot Plug Connect

6.2.2.1 Branch DUT Retry on No-Reply During Aux Read after Hot Plug Event

This test case is identical to Source DUT test case 4.2.1.1, but with 'Source DUT' replaced by 'Branch DUT'.

6.2.2.2 Source Retry on Invalid Reply During Aux Read after Hot Plug Event

This test case is identical to Source DUT test case 4.2.1.2.

6.2.3 EDID and DPCD Reads

For Concentrator and Replicater Branch DUTs, the lowest port number to which a Reference Sink is connected is used for testing.

All test cases begin with the Reference Sink's HPD signal de-asserted, so assertion of HPD will signify a connect event.

6.2.3.1 EDID Read upon Hot Plug Event

Test Procedure:

1. Reference Sink sets up EDID with one block of data (128 bytes).
2. Reference Sink asserts HPD. If one second test duration feature is selected, start one second timer.
3. Verify that the Branch DUT asserts HPD upstream within 1ms.
4. Reference Source initiates EDID read over the AUX CH. Reference Source interleaves reads of DPCD link status field.
5. Verify that the Branch DUT downstream port reads the entire EDID block through the downstream AUX CH.
6. Verify that the Branch DUT returns the entire EDID block through the upstream AUX CH.
7. Reference Source verifies that the checksum of the EDID block is correct, and that the received EDID data matches the EDID data in the Reference Sink.

Result:

This test fails if the Branch DUT does not respond to the EDID read on the upstream AUX CH by reading the EDID on the downstream AUX CH, if the EDID checksum is incorrect, or if the EDID data received by the Reference Source does not match the EDID data in the Reference Sink.

6.2.3.2 DPCD Receiver Capability Read upon Hot Plug Event

This test case is identical to Source DUT test case 4.2.2.2, but with 'Source DUT' replaced by 'Branch DUT'.

6.3 Branch Device Link Services Test Procedures

The following two items shall be tested:

- Link Training
- Link Maintenance

6.3.1 Legacy-to-DisplayPort Converter Link Training

The Legacy-to-DisplayPort converter contains a DisplayPort transmitter like a DisplayPort Source device. Please refer to Section 4.3.1 for the link training tests. The assumption is that no legacy device is required to be connected when executing the link training tests.

6.3.2 DisplayPort-to-Legacy Converter Link Training

The DisplayPort-to-Legacy converter contains a DisplayPort Rx like a DisplayPort Sink Device. Please refer to Section 5.3.1. The assumption is that no legacy device is required to be connected when executing the link training tests.

6.3.3 Repeater Link Training

DisplayPort Link Training is described in section 3.5.1.3 of the DisplayPort 1.1 specification. Figure 2-36 'Link Training State' shows the overall link training sequence. Figures 3-11 'Clock Recovery Sequence of Link Training' and 3-12 'Channel Equalization Sequence of Link Training' show the details of the two phases of link training**.**

This set of tests verifies that the Branch DUT can successfully complete link training on the upstream and downstream DisplayPort main links for all lane counts and link rates. These tests also check the correct operation of the link training state machines in the Branch DUT.

6.3.3.1 Successful Link Training at all Supported Lane Counts and Link Speeds

Note: A repeater device is required to support 4 main link lanes and 2.7Gbps link rate.

Note: This test is repeated for all lane counts and link rates up to the maximum supported by the Branch DUT. Please refer to Table 4-1.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise the lane count and link rate currently under test, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Reference Source verifies that the Branch DUT asserts HPD upstream within 1ms. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.

   Pass1: HPD asserted within 1ms
   Fail1: HPD not asserted within 1ms
3. Reference Source reads the SINK_COUNT byte in the Branch DUT DPCD link/sink status field and verifies that the value is 1.

Pass1: SINK_COUNT = 1
Fail1: SINK_COUNT not= 1

4. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the Branch DUT DPCD receiver capability field and verifies that these have been updated by the Branch DUT to the values advertised by the Reference Sink. Start the link training timer.

   Pass1: MAX_LINK_RATE = value from Reference Sink
   Fail1: MAX_LINK_RATE not= value from Reference Sink
   Pass2: MAX_LANE_COUNT = value from Reference Sink
   Fail2: MAX_LANE_COUNT not= value from Reference Sink

Upstream Link Training: This portion of the test verifies the upstream link training between the Reference Source and the DisplayPort receiver on the Branch DUT.

5. Reference Source writes to LANE_COUNT_SET in DPCD to set the desired lane count.
6. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field. Start the upstream link training timer.
7. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 8. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 7. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, switch to low link rate if at high link rate; if already at low link rate fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Warning2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} while at high link rate; switching to low link rate
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

   Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

8. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.
9. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization

sequence is complete; proceed to step 10. If LANEx_CR_DONE = 0 for any active lane, switch to low link rate if not already at low link rate; otherwise fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 switch to low link rate if not already at low link rate and repeat step 7, otherwise fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 9.

Note1: Equalization succeeded on all active lanes
Warning1: Equalization failed on lanes {lanes that failed equalization}
Note2: Symbol lock succeeded on all active lanes.
Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
Note3: Inter-lane alignment succeeded on all active lanes.
Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
Note4: LANEx_CR_DONE = 1 for all active lanes
Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0} while at high link rate; switching to low link rate
Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
Pass5: N iterations at test step 9; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
Warning5: N iterations at test step 9; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
Warning5: 5 iterations at test step 9; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} while at high link rate; switching to low link rate
Fail5: 5 iterations at test step 9; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

10. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the upstream link training timer.
11. Verify that the Branch DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 3 and 12
    Fail1: HPD de-asserted between steps 3 and 12
12. Reference Source sends the idle pattern on all lanes.
13. Verify that upstream link training has been completed in 10ms or less.

    Note1: Upstream link training timer ≤ 10 ms
    Warning1: Upstream link training timer > 10 ms
14. Verify that the Branch DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

End of Upstream Link Training

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

15. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 16 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to the expected values.

    Pass1: LINK_BW_SET and LANE_COUNT_SET written
    Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
    Pass2: LINK_BW_SET = 06h or 0Ah
    Fail2: LINK_BW_SET not= 06h or 0Ah
    Pass3: LANE_COUNT_SET = {1,2 or 4}
    Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4

16. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and at least 100us after link training begins.

    Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
    Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
    Pass2: VOLTAGE SWING SET = 00b
    Fail2: VOLTAGE SWING SET not= 00b
    Pass3: PRE-EMPHASIS_SET = 00b
    Fail3: PRE-EMPHASIS_SET not= 00b
    Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
    Fail4: LINK_BW_SET = Y (Y not= X)
    Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
        LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
        LANE_COUNT_SET=4, lanes1-4 are enabled
    Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
        LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
        LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

17. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

18. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lanes {lanes that do not have TP2}

19. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Pass3 (2 and 4 lane cases only): All lanes are properly skewed
    Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

Note: If the downstream link is trained to the low link rate when the upstream link is trained to the high link rate, the Branch DUT needs to report this to the Reference Source and retrain the upstream link, though this is not specified in this test.

20. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer.
21. Verify that the downstream link training completed in 10 ms or less.

    Note1: Downstream link training timer ≤ 10 ms
    Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

22. Once upstream and downstream link training sequences are complete, stop the link training timer.
23. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

24. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)

Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET

Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Upstream ink training completed successfully at target link rate and lane count
Target LINK_BW = K, Actual LINK_BW = K
Target LANE_COUNT = X, Actual LANE_COUNT = X

Fail3: Upstream ink training did not complete successfully at target link rate or lane count
Target LINK_BW = K, Actual LINK_BW = L (L not= K)
Target LANE_COUNT = X, Actual LANE_COUNT = Y (Y not= X)

Pass4: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET

Fail4: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: Downstream link training completed successfully at target link rate and lane count
Target LINK_BW = K, Actual LINK_BW = K
Target LANE_COUNT = X, Actual LANE_COUNT = X

Fail5: Downstream link training did not complete successfully at target link rate or lane count
Target LINK_BW = K, Actual LINK_BW = L (L not= K)
Target LANE_COUNT = X, Actual LANE_COUNT = Y (Y not= X)

Pass6: All pass/fail checks within the test steps succeeded
Fail6: One or more pass/fail checks with the test steps failed

6.3.3.2 Successful Link Training with Request of Higher Differential Swing during Clock Recovery Sequence on Upstream Link

The objective of this test is to verify that when it is unable to achieve clock recovery lock on the upstream link, the Branch DUT requests voltage swing adjustments as specified in the DisplayPort specification. To achieve this, the Reference Source forces the first phase of link training to fail at all settings other than the highest differential voltage swing by not sending any transmitted signal.

Once the Branch DUT has requested all of the required voltage swing settings, the Reference Source sends a valid signal to provide an opportunity for the Branch DUT to achieve clock recovery lock. However, this only gives only one opportunity at one combination of pre-emphasis and differential voltage swing for the Branch DUT to achieve lock. Because this test case makes successful completion of link training more difficult and because the objective of this test case is completed before the end of the clock recovery phase of link training, this test does not fail if clock recovery lock is not achieved at the maximum differential voltage swing. If clock recovery lock is successful but the subsequent link training steps fail, the test will fail.

Note: 'Active lane' in this test case refers to any lane that is reported as active due to the 'MAX_LANE_COUNT' setting. This includes lanes that are shut off to cause clock recovery lock to fail.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and low (1.62 Gbps) link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Reference Source verifies that the Branch DUT asserts HPD upstream within 1ms. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
3. Reference Source reads the SINK_COUNT byte in the Branch DUT DPCD link/sink status field and verifies that the value is 1.

   Pass1: SINK_COUNT = 1
   Fail1: SINK_COUNT not= 1
4. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field. Reference Source will attempt to train the link at the low link rate. Start the link training timer.

Upstream Link Training: This portion of the test verifies the upstream link training between the Reference Source and the DisplayPort receiver on the Branch DUT.

5. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Branch DUT.
6. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and with pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. The intention here is to not allow the Branch DUT to achieve clock recovery lock, so Reference Source leaves the transmitters on all active lanes disabled. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field. Start the upstream link training timer.
7. After 100us, Reference Source reads DPCD Link/Sink Status Field. LANEx_CR_DONE bits should be cleared. Reference Source reads DPCD ADJUST_REQUEST_LANEx {x=0_1, 2_3} for all active lanes. The Branch DUT must request adjustments to the differential voltage swing and / or pre-emphasis levels. Differential voltage swing increase requests must be made within 5 iterations until TRAINING_LANEx_SET.MAX_SWING_REACHED is asserted. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx = 11b for any active lane, set TRAINING_LANEx_SET.VOLTAGE_SWING_LANEx = 11b, set TRAINING_LANEx_SET.MAX_SWING_REACHED = 1, transmit training pattern 1 on that lane, and flag that lane's voltage swing adjustment sequence as complete. If all active lanes are flagged as complete, proceed to step 8. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx remains unchanged for 5 iterations any lane not flagged as complete, fail and exit test. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx not= 11b for any active lane, adjust pre-emphasis and / or voltage swing as requested in ADJUST_REQUEST_LANEx and repeat step 7.

   Pass1: LANEx_CR_DONE = 0 for all active lanes not flagged as complete
   Fail1: LANEx_CR_DONE = 1 for any active lane not flagged as complete
   Pass2: LANEx_CR_DONE = 1 for all active lanes flagged as complete
   Fail2: LANEx_CR_DONE = 0 for any active lane flagged as complete
   Pass3: VOLTAGE_SWING_LANEx unchanged or incremented {repeat for all active lanes}

Fail3: VOLTAGE_SWING_LANEx decremented {repeat for all active lanes}
Note4: M iterations at VOLTAGE_SWING_LANEx= N
{N = {0,1,2}, M < 5, repeat for all active lanes}
Fail4: 5 iterations at VOLTAGE_SWING_LANEx = N
{N = {0,1,2}, repeat for all active lanes}

Note: A reference cable is used to connect the Reference Source and the Branch DUT so it is expected that the Branch DUT will achieve CR lock with the maximum voltage swing. However, the test will only give a warning and not fail if CR lock fails.

8. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field. If these bits are set, Clock Recovery sequence is complete; proceed to step 8. If these bits are not set, exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

9. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.

10. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 11. If LANEx_CR_DONE = 0 for any active lane, switch to low link rate if not already at low link rate; otherwise fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5, switch to low link rate if not already at low link rate, carry out step 7 from test 0, and continue from step 8 of this test case; otherwise fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 10.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Note3: Inter-lane alignment succeeded on all active lanes.
    Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
    Note4: LANEx_CR_DONE = 1 for all active lanes
    Warnig4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0} while at high link rate; switching to low link rate
    Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
    Pass5: N iterations at test step 10; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
    Warning5: N iterations at test step 10; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
    Warning5: 5 iterations at test step 10; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} while at high link rate; switching to low link rate
    Fail5: 5 iterations at test step 10; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

11. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the upstream link training timer.
12. Verify that the Branch DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 2 and 11
    Fail1: HPD de-asserted between steps 2 and 11
13. Reference Source sends the idle pattern on all lanes.
14. Verify that upstream link training has been completed in 10ms or less.

    Note1: Upstream link training timer ≤ 10 ms
    Warning1: Upstream link training timer > 10 ms
15. Verify that the Branch DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

End of Upstream Link Training

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

16. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 17 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to the expected values.

    Pass1: LINK_BW_SET and LANE_COUNT_SET written
    Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
    Pass2: LINK_BW_SET = 06h or 0Ah
    Fail2: LINK_BW_SET not= 06h or 0Ah
    Pass3: LANE_COUNT_SET = {1,2 or 4}
    Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
17. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and at least 100us after link training begins.

    Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
    Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
    Pass2: VOLTAGE SWING SET = 00b

Fail2: VOLTAGE SWING SET not= 00b
Pass3: PRE-EMPHASIS_SET = 00b
Fail3: PRE-EMPHASIS_SET not= 00b
Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
Fail4: LINK_BW_SET = Y (Y not= X)
Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

18. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

19. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lanes {lanes that do not have TP2}

20. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Pass3 (2 and 4 lane cases only): All lanes are properly skewed
    Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

Note: If the downstream link is trained to the low link rate when the upstream link is trained to the high link rate, the Branch DUT needs to report this to the Reference Source and retrain the upstream link, though this is not specified in this test.

21. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer.

22. Verify that the downstream link training completed in 10 ms or less.

Note1: Downstream link training timer ≤ 10 ms
Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

23. Once upstream and downstream link training are complete, stop the link training timer.
24. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms
25. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail3: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass4: All pass/fail checks within the test steps succeeded
Fail4: One or more pass/fail checks with the test steps failed

6.3.3.3 Successful Link Training to a Lower Link Rate Due to Error on the Upstream Port

The objective of this test is to verify that after a clock recovery lock failure on the upstream link, it is possible to train the Branch DUT to the low link rate. To achieve this, the Reference Source forces the first phase of link training to fail at the high link rate by not sending any transmitted signal.

Note: Support of the high (2.7Gbps) link rate is optional. This test is skipped if the test operator has reported that Branch DUT supports only the low (1.62Gbps) link rate.

Note: 'Active lane' in this test case refers to any lane that is reported as active due to the 'MAX_LANE_COUNT' setting. This includes lanes that are shut off to cause clock recovery lock to fail.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Reference Source verifies that the Branch DUT asserts HPD upstream within 1ms. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
3. Reference Source reads the SINK_COUNT byte in the Branch DUT DPCD link/sink status field and verifies that the value is 1.

   Pass1: SINK_COUNT = 1
   Fail1: SINK_COUNT not= 1
4. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field. Reference Source will attempt to train the link at the low link rate. Start the link training timer.

Upstream Link Training: This portion of the test verifies the upstream link training between the Reference Source and the DisplayPort receiver on the Branch DUT.

5. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Branch DUT.
6. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and with pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. The intention here is to not allow the Branch DUT to achieve clock recovery lock, so Reference Source leaves the transmitters on all active lanes disabled. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field. Start the upstream link training timer.
7. After 100us, Reference Source reads DPCD Link/Sink Status Field. LANEx_CR_DONE bits should be cleared. Reference Source reads DPCD ADJUST_REQUEST_LANEx {x=0_1, 2_3} for all active lanes. The Branch DUT must request adjustments to the differential voltage swing and / or pre-emphasis levels. Differential voltage swing increase requests must be made within 5 iterations until TRAINING_LANEx_SET.MAX_SWING_REACHED is asserted. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx = 11b for any active lane, set TRAINING_LANEx_SET.VOLTAGE_SWING_LANEx = 11b, set TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 and flag that lane's voltage swing adjustment sequence as complete. If all active lanes are flagged as complete, proceed to step 8. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx remains unchanged for 5 iterations any lane not flagged as complete, fail and exit test. If ADJUST_REQUEST_LANEx.VOLTAGE_SWING_LANEx not= 11b for any active lane, adjust pre-emphasis and / or voltage swing as requested in ADJUST_REQUEST_LANEx and repeat step 7.

Pass1: LANEx_CR_DONE = 0 for all active lanes
Fail1: LANEx_CR_DONE = 1 for any active lane
Pass2: VOLTAGE_SWING_LANEx unchanged or incremented {repeat for all active lanes}
Fail2: VOLTAGE_SWING_LANEx decremented {repeat for all active lanes}
Note3: M iterations at VOLTAGE_SWING_LANEx= N
{N = {0,1,2}, M < 5, repeat all active lanes}
Fail3: 5 iterations at VOLTAGE_SWING_LANEx = N
{N = {0,1,2}, repeat for all active lanes}

8. Reference Source writes LINK_BW_SET byte of DPCD = 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.
9. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field.
10. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 9. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 8. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
    Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2}, M < 5, repeat for all active lanes}
    Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

11. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.
12. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 13. If LANEx_CR_DONE = 0 for any active lane, fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 12.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.

Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
Note3: Inter-lane alignment succeeded on all active lanes.
Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
Note4: LANEx_CR_DONE = 1 for all active lanes
Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
Pass5: N iterations at test step 12; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
Warning5: N iterations at test step 12; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
Fail5: 5 iterations at test step 12; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

13. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer.
14. Verify that the Branch DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 2 and 13
    Fail1: HPD de-asserted between steps 2 and 13
15. Reference Source sends the idle pattern on all lanes.
16. Verify that upstream link training has been completed in 10ms or less.

    Note1: Upstream link training timer ≤ 10 ms
    Warning1: Upstream link training timer > 10 ms
17. Verify that the Branch DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

End of Upstream Link Training

18. Follow steps 15 to 24 from test 0 for the training of the downstream port and verification of the entire link.

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Upstream ink training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Upstream ink training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail4: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: Downstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail5: Downstream link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass6: All pass/fail checks within the test steps succeeded
Fail6: One or more pass/fail checks with the test steps failed

6.3.3.4 Successful Link Training with Request of a Change to Pre-emphasis And/Or Voltage Swing Setting during Channel Equalization Sequence on Upstream Port

The objective of this test is to verify that when it is unable to achieve Symbol, Equalization and Inter-lane Alignment lock on its upstream link, the Branch DUT requests voltage swing and / or pre-emphasis adjustments to attempt to achieve lock. To force a failure of the above-mentioned locks, the Reference Source forces the second phase of link training to fail for four iterations by transmitting the wrong training pattern.

After four iterations, the Reference Source gives the Branch DUT an opportunity to achieve lock by transmitting training pattern 2. However, this only gives one opportunity at one combination of pre-emphasis and differential voltage swing for the Branch DUT to achieve lock. Because this test case makes successful completion of link training more difficult and because the objective of this test case is completed before the end of the equalization phase of link training, this test does not fail if equalization, symbol lock and inter-lane alignment lock do not complete successfully. If equalization, symbol lock and inter-lane alignment lock are successful but subsequent link training steps fail, the test will fail.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Reference Source verifies that the Branch DUT asserts HPD upstream within 1ms. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
3. Reference Source reads the SINK_COUNT byte in the Branch DUT DPCD link/sink status field and verifies that the value is 1.

Pass1: SINK_COUNT = 1
Fail1: SINK_COUNT not= 1

4. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field. Reference Source will attempt to train the link at the low link rate. Start the link training timer.

Upstream Link Training: This portion of the test verifies the upstream link training between the Reference Source and the DisplayPort receiver on the Branch DUT.

5. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Branch DUT.
6. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field. Start the upstream link training timer.
7. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 8. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 7. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, switch to low link rate if at high link rate; if already at low link rate fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Warning2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} while at high link rate; switching to low link rate
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

   Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

8. Reference Source continues to transmit training pattern 1 on all active lanes. The intention here is to not allow the Branch DUT to complete Channel Equalization. Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.
9. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. For each lane, LANEx_CR_DONE may remain set, but all of the other bits should be cleared. If any of LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK and INTERLANE_ALIGN_DONE is set, fail and exit test. The Branch DUT should request a change in pre-emphasis and/or differential voltage swing within 5 iterations. After four iterations at this test step, proceed to step 10.

   Pass1: Equalization failed on all active lanes (expected)

Fail1: False equalization success reported on lanes {lanes that passed equalization}
Pass2: Symbol lock failed on all active lanes (expected)
Fail2: False symbol lock success reported on lanes {lanes that passed symbol lock}
Pass3: Inter-lane alignment failed on all active lanes (expected)
Fail3: False inter-lane alignment success reported on lanes {lanes that passed symbol lock}
Note4: LANEx_CR_DONE = 1 for all active lanes
Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}
Pass3: (check only on fourth iteration) Branch DUT requested at least one adjustment to pre-emphasis or differential voltage swing
Fail3: (check only on fourth iteration) Branch DUT did not request any adjustments to pre-emphasis or differential voltage swing

10. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.
11. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If LANEx_CR_DONE = 0 for any active lane, exit test. If one or more of the other bits is/are not set, exit test.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Note3: Inter-lane alignment succeeded on all active lanes.
    Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
    Note4: LANEx_CR_DONE = 1 for all active lanes
    Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
    Note5: Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
    Warning5: Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes} – terminating link training
12. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the upstream link training timer.
13. Verify that the Branch DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 2 and 12
    Fail1: HPD de-asserted between steps 2 and 12
14. Reference Source sends the idle pattern on all lanes.
15. Verify that upstream link training has been completed in 10ms or less.

    Note1: Upstream link training timer ≤ 10 ms
    Warning1: Upstream link training timer > 10 ms
16. Verify that the Branch DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

End of Upstream Link Training

17. Follow steps 15 to 24 from test 0 for the training of the downstream port and verification of the entire link.

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more pass/fail checks with the test steps failed

6.3.3.5 Successful Link Training at Lower Link Rate due to Loss of Symbol lock during Channel Equalization Sequence on the Upstream Port

The objective of this test is to verify that after an equalization sequence failure on the upstream port, it is possible to train the Branch DUT to the low link rate. To achieve this, the Reference Source forces the second phase of link training to fail at the high link rate by sending the wrong training pattern. Successful Clock Recovery lock at the high link rate is mandatory for this test. The test will fail if Clock Recovery lock fails at the high link rate because it prevents completion of the test case.
Note: Support of the high (2.7Gbps) link rate is optional. This test is skipped if the test operator has reported that Branch DUT supports only the low (1.62Gbps) link rate.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Reference Source verifies that the Branch DUT asserts HPD upstream within 1ms. HPD should remain asserted for the remainder of the test. If HPD is de-asserted at any time during the test, exit test.

   Pass1: HPD is asserted
   Fail1: HPD is not asserted
3. Reference Source reads the SINK_COUNT byte in the Branch DUT DPCD link/sink status field and verifies that the value is 1.

   Pass1: SINK_COUNT = 1
   Fail1: SINK_COUNT not= 1
4. Reference Source reads the MAX_LINK_RATE and MAX_LANE_COUNT from the DPCD receiver capability field. Reference Source will attempt to train the link at the low link rate. Start the link training timer.

Upstream Link Training: This portion of the test verifies the upstream link training between the Reference Source and the DisplayPort receiver on the Branch DUT.

5. Reference Source writes to LANE_COUNT_SET in DPCD to set the lane count to the maximum supported by the Branch DUT.
6. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled

(TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field. Start the upstream link training timer.

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

7. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 8. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 7. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
   Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2}, M < 5, repeat for all active lanes}
   Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
   {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes} – aborting test due to failure to achieve clock recovery lock at high link rate

8. Reference Source continues to transmit training pattern 1 on all active lanes. The intention here is to not allow the Branch DUT to complete Channel Equalization. Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.

9. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. For each lane, LANEx_CR_DONE may remain set, but all of the other bits should be cleared. If any of LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK and INTERLANE_ALIGN_DONE is set, fail and exit test. The Branch DUT should request a change in pre-emphasis and/or differential voltage swing within 5 iterations. After five iterations at this test step, proceed to step 10.

   Pass1: Equalization failed on all active lanes (expected)
   Fail1: False equalization success reported on lanes {lanes that passed equalization}
   Pass2: Symbol lock failed on all active lanes (expected)
   Fail2: False symbol lock success reported on lanes {lanes that passed symbol lock}
   Pass3: Inter-lane alignment failed on all active lanes (expected)
   Fail3: False inter-lane alignment success reported on lanes {lanes that passed symbol lock}
   Note4: LANEx_CR_DONE = 1 for all active lanes
   Warning4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}
   Pass3: (check only on fifth iteration) Branch DUT requested at least one adjustment to pre-emphasis or differential voltage swing
   Fail3: (check only on fifth iteration) Branch DUT did not request any adjustments to pre-emphasis or differential voltage swing

10. Reference Source writes LINK_BW_SET byte of DPCD = 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

11. Reference Source starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled

(TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Reference Source transmits training pattern 1 on all active lanes. Reference Source writes 01h to the TRAINING_PATTERN_SET byte in the Branch DUT DPCD Link Configuration Field.

12. After 100us, Reference Source reads LANEx_CR_DONE bits in DPCD Link/Sink Status Field for all active lanes. If these bits are all set, Clock Recovery sequence is complete; proceed to step 11. If one or more of these bits is/are not set, Reference Source reads the DPCD ADJUST_REQUEST_LANEx (x= 0_1, 2_3) registers for the affected lane(s), updates the voltage swing and / or pre-emphasis as requested, and repeats step 10. If VOLTAGE_SWING_SET=00b, 01b or 10b for five iterations without CR lock on any lane, or if VOLTAGE_SWING_SET=11b for 1 iteration without CR lock on any lane, fail and exit test.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}
    Note2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2}, M < 5, repeat for all active lanes}
    Fail2: M iterations without CR lock at VOLTAGE_SWING_SET = N on lane X
    {N = {0,1,2,3}, M = 5 if N = 0..2, M = 1 if N = 3, repeat for all active lanes}, and already at low link rate

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

13. Reference Source transmits training pattern 2 on all active lanes, with two link symbol inter-lane skew between adjacent lanes (inter-lane skew does not apply for lane count = 1). Reference Source writes 02h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field.

14. After 400us, Reference Source checks the LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, INTERLANE_ALIGN_DONE and LANEx_CR_DONE bits in the DPCD Link/Sink Status Field for all active lanes. If all of these bits are set, the Channel Equalization sequence is complete; proceed to step 15. If LANEx_CR_DONE = 0 for any active lane, fail and exit test. If one or more of the other bits is/are not set, check the number of times this test step has been repeated. If number is greater than 5 fail and exit test. Reference Source reads ADJUST_REQUEST_LANEx (x=0_1, 2_3) for all active lanes and updates pre-emphasis and / or voltage swing levels as requested; repeat step 14.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lanes {lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes.
    Warning2: Symbol lock failed on lanes {lanes that failed symbol lock}
    Note3: Inter-lane alignment succeeded on all active lanes.
    Warning3: Inter-lane alignment failed on lanes {lanes that failed symbol lock}
    Note4: LANEx_CR_DONE = 1 for all active lanes
    Fail4: LANEx_CR_DONE = 0 for lane(s) {lane(s) with CR_DONE=0}, and already at low link rate – terminating link training
    Pass5: N iterations at test step 14; Equalization, Symbol Lock and Inter-lane align lock succeeded for Lane X {repeat for all active lanes}
    Warning5: N iterations at test step 14; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {N < 5; repeat for all active lanes}
    Fail5: 5 iterations at test step 14; Lane X {Equalization, Symbol Lock, Inter-lane align lock} flags not set. {repeat for all active lanes}, and already at low link rate – terminating link training

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

15. Reference Source writes 00h to the TRAINING_PATTERN_SET byte of Branch DUT DPCD Link Configuration Field to indicate the end of the link training. Stop the upstream link training timer.
16. Verify that the Branch DUT has not de-asserted HPD during the time link training is taking place (when TRAINING_PATTERN_SET is non-zero).

    Pass1: HPD not de-asserted between steps 2 and 15
    Fail1: HPD de-asserted between steps 2 and 15

18. Reference Source sends the idle pattern on all lanes.
19. Verify that upstream link training has been completed in 10ms or less.

    Note1: Upstream link training timer ≤ 10 ms
    Warning1: Upstream link training timer > 10 ms

20. Verify that the Branch DUT has not cleared the LANEx_SYMBOL_LOCK bit, and has not set the LINK_STATUS_UPDATED bit in DPCD for at least 500us.

End of Upstream Link Training

21. Follow steps 15 to 24 from test 0 for the training of the downstream port and verification of the entire link.

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Upstream ink training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Upstream ink training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail4: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: Downstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail5: Downstream link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass6: All pass/fail checks within the test steps succeeded
Fail6: One or more pass/fail checks with the test steps failed

6.3.3.6 Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence on the Downstream Link

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to the expected values.

   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and at least 100us after link training begins.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)

Fail4: LINK_BW_SET = Y (Y not= X)
Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

6. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.VOLTAGE_SWING_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

7. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

8. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.VOLTAGE_SWING_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes excluding those that have voltage swing adjustment flagged as complete.

9. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (check all active lanes, excluding

lanes that have voltage swing adjustment flagged as complete)
Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

Note: Support of fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

10. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
11. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all any active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
12. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

    Pass1: CR lock achieved for all active lanes.
    Fail1: CR lock failed for lane(s) {lanes which failed CR lock)
13. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lanes {report active lanes without TP2}
14. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 or 4 lane cases only): All lanes are properly skewed
    Fail3 (2 or 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

15. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Note1: Downstream link training timer ≤ 10 ms
    Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

16. Once upstream and downstream link training sequences are complete, stop the link training timer.
17. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

18. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate

Result:

This test passes if all pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail3: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: All pass/fail checks within the test steps succeeded
Fail5: One or more pass/fail checks with the test steps failed

6.3.3.7 Successful Link Training to a Lower Link Rate due to Error on Downstream Port #1: Iterate at Maximum Voltage Swing

Note: Support of 2.7Gbps link rate is optional. This test is skipped if the test operator has reported that the Branch DUT supports a maximum link rate of 1.62Gbps.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 0Ah
   Fail2: LINK_BW_SET not= 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
5. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

6. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
7. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Increment voltage swing iteration counter.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)
8. Repeat step 7 (including pass/fail checks) until sink writes LINK_BW_SET.
9. Verify that the Branch DUT sets the LINK_BW_SET to 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

   Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iterations at high link bandwidth
   Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations
   Pass1: LINK_BW_SET = 06h
   Fail1: LINK_BW_SET not= 06h
   Pass2: Training Pattern 1 detected on all enabled lanes when LINK_BW_SET is written
   Fail2: Training Pattern 1 not sent on lanes {report lanes without TP1} when LINK_BW_SET is written
   Pass3: link rate = 1.62 Gbps
   Fail3: link rate not= 1.62 Gbps
10. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

11. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {lanes without TP2}
12. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

Note1: Equalization succeeded on all active lanes
Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
Note2: Symbol lock succeeded on all active lanes
Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
Pass3 (2 and 4 lane cases only): All lanes are properly skewed
Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

13. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Note1: Downstream link training timer ≤ 10 ms
    Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

14. Once upstream and downstream link training sequences are complete, stop the link training timer.
15. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

16. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Upstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: Downsteam link training completed successfully (report even if training result did not match target link rate and lane count)
Report downstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail4: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: Downstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail5: Downstream link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass6: All pass/fail checks succeeded
Fail6: One or more checks failed

6.3.3.8 Successful Link Training to a Lower Link Rate due to Error on Downstream Port #2: Iterate at Minimum Voltage Swing

Note: Support of 2.7Gbps link rate is optional. This test is skipped if the test operator has reported that the Branch DUT supports a maximum link rate of 1.62Gbps.

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 0Ah
   Fail2: LINK_BW_SET not= 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written

Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
Pass2: VOLTAGE SWING SET = 00b
Fail2: VOLTAGE SWING SET not= 00b
Pass3: PRE-EMPHASIS_SET = 00b
Fail3: PRE-EMPHASIS_SET not= 00b
Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
Fail4: LINK_BW_SET = Y (Y not= X)
Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

6. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

7. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

8. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

9. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that

TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this test step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (repeat for x = 0 .. N, N = highest active lane, excluding lanes that have voltage swing adjustment flagged as complete)
Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (report for x = 0 .. N, N = any active lane that has VOLTAGE SWING SET not= 01b and does not have voltage swing adjustment flagged as complete)

Note: Support for fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

10. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
11. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete).
12. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
13. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Increment voltage swing iteration counter.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = YYb (YY = last requested voltage swing; check all active lanes)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= YYb (YY = last requested voltage swing; check all active lanes)
14. Repeat step 13 (including pass/fail checks) until sink writes LINK_BW_SET.
15. Verify that the Branch DUT sets the LINK_BW_SET to 06h to attempt link training at the lower link rate, and transmits training pattern 1 at 1.62Gbps.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iterations at high link bandwidth

Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations
Pass1: LINK_BW_SET = 06h
Fail1: LINK_BW_SET not= 06h
Pass2: Training Pattern 1 detected on all enabled lanes when LINK_BW_SET is written
Fail2: Training Pattern 1 not sent on lanes {report lanes without TP1} when LINK_BW_SET is written
Pass3: link rate = 1.62 Gbps
Fail3: link rate not= 1.62 Gbps

16. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Note1: CR lock succeeded on all active lanes
    Warning1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

17. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {lanes without TP2}

18. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 and 4 lane cases only): All lanes are properly skewed
    Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

19. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Note1: Downstream link training timer ≤ 10 ms
    Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

20. Once upstream and downstream link training sequences are complete, stop the link training timer.

21. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

22. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Link training failed (report this if failure of any test step causes test to abort)

Pass3: Upstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail3: Upstream link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass4: Downsteam link training completed successfully (report even if training result did not match target link rate and lane count)
Report downstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail4: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass5: Downstream link training completed successfully at target link rate
LINK_BW = 1.62Gbps
Fail5: Downstream link training did not complete successfully at target link rate
LINK_BW not= 1.62Gbps

Pass6: All pass/fail checks succeeded
Fail6: One or more checks failed

6.3.3.9 Successful Link Training with Request of a Higher Pre-emphasis Setting during Channel Equalization Sequence in Downstream Link

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
5. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}

7. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this test step and do not make any further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes)

8. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 01b for all active lanes that do not have pre-emphasis flagged as complete.

9. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this test step and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis flagged as complete)

10. Reference Sink keeps sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 10b for all active lanes that do not have pre-emphasis flagged as complete.

11. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this test step and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 12.

    Pass1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 10b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

Fail1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 10b (check all active lanes, excluding those that have pre-emphasis flagged as complete)

Note: Support for third pre-emphasis level (in addition to zero setting) is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

12. Reference Sink keeps sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 11b for all active lanes that do not have pre-emphasis flagged as complete.
13. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (check all active lanes, excluding those that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding those that have pre-emphasis flagged as complete)
14. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}
    Note2: Symbol lock succeeded on all active lanes
    Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
    Pass3 (2 and 4 lane cases only): All lanes are properly skewed
    Fail3: (2 and 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

15. Wait until the Branch DUT writes 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the link training timer. Verify that link training completed in 10 ms or less.

    Note1: Link training timer ≤ 10 ms
    Warning1: Link training timer > 10 ms

End of Downstream Link Training

16. Once upstream and downstream link training sequences are complete, stop the link training timer.
17. Verify that the total link training time is 20ms or less.

Note1: Link training timer ≤ 20 ms
Warning1: Link training timer > 20 ms

18. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all of the pass/fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report downstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail3: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass4: All pass/fail checks succeeded
Fail4: One or more checks failed

6.3.3.10 Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence in Downstream Link

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h or 0Ah
   Fail2: LINK_BW_SET not= 06h or 0Ah
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
   LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
   LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled
5. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}
7. Reference Sink clears LANEx_CR_DONE bits in DPCD Link/Sink Status Field to indicate a loss of symbol lock.

8. If Branch DUT only supports 1.62Gbps link rate or has already reduced link rate to 1.62 Gbps, wait until the Branch DUT terminates the link training by writing 00h to TRAINING_PATTERN_SET in the DPCD Link Configuration Field. Stop the link training timer and proceed to 'Result'. If Branch DUT supports 2.7Gbps link rate and has achieved CR lock on all lanes at 2.7 Gbps, proceed with the remainder of the test.

   Pass1 (only if link rate is already 1.62 Gbps): TRAINING_PATTERN_SET = 00h
   Fail1 (only if link rate is already 1.62 Gbps): TRAINING_PATTERN_SET not= 00h

9. Wait until the Branch DUT writes to LINK_BW_SET. Verify that the Branch DUT sets LINK_BW_SET to 06h to attempt link training at the lower link rate by going through the Clock Recovery sequence again.

   Pass1: LINK_BW_SET = 06h
   Fail1: LINK_BW_SET not= 06h

10. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE SWING SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes.

    Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
    Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
    Pass2: VOLTAGE SWING SET = 00b
    Fail2: VOLTAGE SWING SET not= 00b
    Pass3: PRE-EMPHASIS_SET = 00b
    Fail3: PRE-EMPHASIS_SET not= 00b

11. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved at the lower link rate, and within 100us of the start of the current link training iteration.

    Pass1: CR lock succeeded on all active lanes
    Fail1: CR lock failed on lane(s) {report lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

12. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field, and that the Branch DUT transmits training pattern 2 on all active lanes.

    Pass1: Training Pattern 2 detected on all active lanes
    Fail1: Training Pattern 2 not detected on lane(s) {active lanes without TP2}

13. Reference Sink sets LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field after channel equalization is complete and verifies that Branch DUT is transmitting with 2 link symbol inter-lane skew between adjacent lanes (for all lane counts greater than one). LANEx_CR_DONE bits in DPCD Link/Sink Status Field also remain set.

    Note1: Equalization succeeded on all active lanes
    Warning1: Equalization failed on lane(s) {report lanes that failed equalization}

Note2: Symbol lock succeeded on all active lanes
Warning2: Symbol lock failed on lane(s) {report lanes that did not achieve symbol lock}
Pass3 (2 or 4 lane cases only): All lanes are properly skewed
Fail3 (2 or 4 lane cases only): Lane N+1 is skewed by M link symbols relative to lane N (N = 0 .. 2, M not= 2)

Note: Multiple iterations through the Channel Equalization sequence with adjustment of pre-emphasis setting are possible if required, though not specified in this test.

14. Wait until the Branch DUT writes a 00h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field to indicate the end of the link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Note1: Downstream link training timer ≤ 10 ms
    Warning1: Downstream link training timer > 10 ms

End of Downstream Link Training

15. Once upstream and downstream link training sequences are complete, stop the link training timer.
16. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

17. Verify that the upstream link and the downstream link of the Branch DUT are trained to the same lane count and link rate.

    Pass1: Upstream link rate = Downstream link rate
    Fail1: Upstream link rate not= Downstream link rate
    Pass2: Upstream lane count = Downstream lane count
    Fail2: Upstream lane count not= Downstream lane count

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Upstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report upstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Upstream link training failed (report this if failure of any test step causes test to abort)

Pass3: Downstream link training completed successfully (report even if training result did not match target link rate and lane count)
Report downstream link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET

PRE-EMPHASIS_SET
Fail3: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass4: All pass/fail checks succeeded
Fail4: One or more checks failed

6.3.3.11 Unsuccessful Link Training at Lower Link Rate Due to Failure on Downstream Link #1: Iterate at Maximum Voltage Swing

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and low (1.62 Gbps) link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
   LANE_COUNT_SET=4, lanes1-4 are enabled
   Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR

LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

6. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 01b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

7. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 01b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

8. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 10b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.

9. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for any active lane, flag voltage swing adjustment as complete for that lane after completion of this test step, and do not make further adjustments or checks on that lane until step 12. If TRAINING_LANEx_SET.MAX_SWING_REACHED = 1 for all active lanes, proceed to step 12.

   Pass1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 10b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)

Note: Support for fourth voltage swing level is optional. Do not fail if sink indicates that it does not support VOLTAGE SWING SET=11b by setting MAX_SWING_REACHED=1 on this iteration.

10. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared and requests an increase of differential voltage swing by setting the ADJUST_REQUEST_LANEx_x.DRIVE_CURRENT_LANEx = 11b in the DPCD Link/Sink Status Field for all active lanes that do not have voltage swing adjustment flagged as complete.
11. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have voltage swing adjustment flagged as complete.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 11b (check all active lanes, excluding those that have voltage swing adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 11b (check all active lanes, excluding lanes that have voltage swing adjustment flagged as complete)
12. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.
13. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. Increment voltage swing iteration counter. Repeat step 13 until Branch DUT writes to TRAINING_PATTERN_SET; when Branch DUT writes to TRAINING_PATTERN_SET, skip forward to step 14.

    Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
    Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
    Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
    Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)
14. Verify that the Branch DUT writes 00h to TRAINING_PATTERN_SET to terminate downstream link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iteration at high link bandwidth.
    Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations.
    Pass2: TRAINING_PATTERN_SET = 00h
    Fail2: TRAINING_PATTERN_SET not= 00h
    Pass3: Downstream link training timer ≤ 10 ms
    Fail3: Downstream link training timer > 10 ms

End of Downstream Link Training

15. Verify that the Branch DUT de-asserts HPD upstream.
16. Once downstream link training sequence is complete and upstream link training sequence is complete or upstream HPD de-asserted, stop the link training timer.
17. Verify that the total link training time is 20ms or less.

Note1: Link training timer ≤ 20 ms
Warning1: Link training timer > 20 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

6.3.3.12 Unsuccessful Link Training at Lower Link Rate Due to Failure on Downstream Link #2: Iterate at Minimum Voltage Swing

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and low (1.62 Gbps) link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b

Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
Fail4: LINK_BW_SET = Y (Y not= X)
Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR
LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)

6. Reference Sink keeps LANEx_CR_DONE bit in DPCD Link/Sink Status Field cleared; this results in a request for another iteration with the same voltage swing settings. Set voltage swing iteration counter to 1.

7. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes. Verify that TRAINING_LANEx_SET.MAX_SWING_REACHED = 0 for all active lanes. Increment voltage swing iteration counter. Repeat step 7 until Branch DUT writes to TRAINING_PATTERN_SET; when Branch DUT writes to TRAINING_PATTERN_SET, skip forward to step 8.

   Pass1: TRAINING_LANEx_SET.MAX_SWING_REACHED=0 (check all active lanes)
   Fail1: TRAINING_LANEx_SET.MAX_SWING_REACHED=1 (check all active lanes)
   Pass2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b (check all active lanes)
   Fail2: TRAINING_LANEx_SET.VOLTAGE_SWING_SET not= 00b (check all active lanes)

8. Verify that the Branch DUT writes 00h to TRAINING_PATTERN_SET to terminate downstream link training. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

   Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iteration at high link bandwidth.
   Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations.
   Pass2: TRAINING_PATTERN_SET = 00h
   Fail2: TRAINING_PATTERN_SET not= 00h
   Pass3: Downstream link training timer ≤ 10 ms
   Fail3: Downstream link training timer > 10 ms

End of Downstream Link Training

9. Verify that the Branch DUT de-asserts HPD upstream.

10. Once downstream link training sequence is complete and upstream link training sequence is complete or upstream HPD de-asserted, stop the link training timer.

11. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

6.3.3.13 Unsuccessful Link Training due to Failure with Channel Equalization Sequence (loop count > 5) on Downstream Port

Test Procedure:

1. Reference Sink sets up receiver capability field in DPCD to advertise maximum lane count and low (1.62 Gbps) link rate, and asserts HPD. HPD signal remains asserted for the remainder of the test. If one second test duration feature is selected, start one second timer.
2. Follow steps 2 to 14 of test 0 to train the upstream link.

Downstream Link Training: This portion of the test verifies the downstream link training between the DisplayPort transmitter on the Branch DUT and the Reference Sink. It is not required that the Branch DUT wait until the upstream link training is finished before starting downstream link training if the Branch DUT has a local timing reference.

3. Wait until the Branch DUT writes to the LINK_BW_SET and LANE_COUNT_SET fields. Skip forward to step 4 if TRAINING_PATTERN_SET is written to 01h before this test step is complete. Verify that LINK_BW_SET and LANE_COUNT_SET are written to legitimate values.
   Pass1: LINK_BW_SET and LANE_COUNT_SET written
   Fail1: TRAINING_PATTERN_SET written to 01h before LINK_BW_SET and / LANE_COUNT_SET
   Pass2: LINK_BW_SET = 06h
   Fail2: LINK_BW_SET not= 06h
   Pass3: LANE_COUNT_SET = {1,2 or 4}
   Fail3: LANE_COUNT_SET = 0 OR LANE_COUNT_SET = 3 OR LANE_COUNT_SET > 4
4. Wait until the Branch DUT writes 01h to the TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field. Start the downstream link training timer. Verify that the Branch DUT transmits training pattern 1 on all active lanes. Verify that the Branch DUT starts with the minimum differential voltage swing (TRAINING_LANEx_SET.VOLTAGE_SWING_SET = 00b) and pre-emphasis disabled (TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 00b) on all active lanes. Verify that LINK_BW_SET matches the actual link bandwidth, and that LANE_COUNT_SET matches the number of active lanes.

   Pass1: Training Pattern 1 detected on all enabled lanes when TRAINING_PATTERN_SET is written
   Fail1: Training Pattern 1 not sent on lanes {report lanes without TP1} when TRAINING_PATTERN_SET is written
   Pass2: VOLTAGE SWING SET = 00b
   Fail2: VOLTAGE SWING SET not= 00b
   Pass3: PRE-EMPHASIS_SET = 00b
   Fail3: PRE-EMPHASIS_SET not= 00b
   Pass4: LINK_BW_SET = X (X = 06h if link rate = 1.62 Gbps, X = 0Ah if link rate = 2.7 Gbps)
   Fail4: LINK_BW_SET = Y (Y not= X)
   Pass5: LANE_COUNT_SET=1, lane 1 is enabled and lanes 2-4 are disabled OR
   LANE_COUNT_SET=2, lanes 1-2 are enabled and lanes 3-4 are disabled OR

LANE_COUNT_SET=4, lanes1-4 are enabled
Fail5: LANE_COUNT_SET=1 but lane 1 is disabled or any of lanes 2-4 are enabled OR
LANE_COUNT_SET=2 but lane 1 or 2 is disabled or lane 3 or 4 is enable OR
LANE_COUNT_SET=4 but one or more of lanes 1-4 is disabled

5. Reference Sink sets LANEx_CR_DONE bits in DPCD Link/Sink Status Field after CR lock is achieved, and within 100us of the start of the current link training iteration.

   Note1: CR lock succeeded on all active lanes
   Warning1: CR lock failed on lane(s) {lanes that did not achieve CR lock}

Note: Multiple iterations through the Clock Recovery sequence with adjustment of drive strength are possible if required, though not specified in this test.

6. Wait until the Branch DUT writes 02h to the TRAINING_PATTERN_SET byte of Reference Sink DPCD Link Configuration Field, and that the Branch DUT transmits training pattern 2 on all active lanes.

   Pass1: Training Pattern 2 detected on all active lanes
   Fail1: Training Pattern 2 not detected on lanes {active lanes without TP2}

7. Verify that TRAINNIG_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. Set the equalization iteration counter to 1. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane and do not make further adjustments or checks on that lane until step 14. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes, proceed to step 14.

   Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 (for x = 0 .. N, N = max active lane)
   Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 (for x = 0 .. N, N = any active lane that has MAX_PRE-EMPHASIS_REACHED = 1)

8. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 01b for all active lanes.

9. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 2. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 0 for all active lanes. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 14. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS REACHED = 1 for all active lanes, proceed to step 14.

   Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
   Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

10. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 10b for all active lanes.
11. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 3. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for any active lane, flag pre-emphasis adjustment as complete for that lane after completion of this step, and do not make further adjustments or checks on that lane until step 14. If TRAINING_LANEx_SET.MAX_PRE-EMPHASIS REACHED = 1 for all active lanes, proceed to step 14.

    Pass1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 01b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

Note: Support of third pre-emphasis level is optional. Do not fail if sink indicates that it does not support PRE-EMPHASIS_SET = 11b by setting MAX_PRE-EMPHASIS_REACHED=1 on this iteration.

12. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared, and sets ADJUST_REQUEST_LANEx_x.PRE-EMPHASIS_LANEx = 11b for all lanes.
13. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter to 4. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
14. Reference Sink keeps LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK, and INTERLANE_ALIGN_DONE in the DPCD Link/Sink Status Field cleared. LANEx_CR_DONE bits in DPCD Link/Sink Status Field remain set.
15. Wait until the Branch DUT writes to DPCD registers TRAINING_LANEx_SET (0103h .. 0106h) for all active lanes that do not have pre-emphasis adjustment flagged as complete. Increment the equalization iteration counter. Verify that TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED = 1 for all active lanes. Repeat step 15 until Branch DUT writes to TRAINING_PATTERN_SET; when Branch DUT writes to TRAINING_PATTERN_SET, skip forward to step 16.

    Pass1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=1 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Fail1: TRAINING_LANEx_SET.MAX_PRE-EMPHASIS_REACHED=0 (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)
    Pass2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET = 11b (check all active lanes, excluding

lanes that have pre-emphasis adjustment flagged as complete)
Fail2: TRAINING_LANEx_SET.PRE-EMPHASIS_SET not= 11b (check all active lanes, excluding lanes that have pre-emphasis adjustment flagged as complete)

16. Verify that the Branch DUT terminates downstream link training by writing TRAINING_PATTERN_SET to 00h. Stop the downstream link training timer. Verify that downstream link training completed in 10 ms or less.

    Pass1: Iteration counter = 1, indicating Source initiated training at low link bandwidth after one iterations at high link bandwidth.
    Fail1: Iteration counter not= 1, indicating Source initiated training at low link bandwidth after a incorrect number of iterations.
    Pass2: TRAINING_PATTERN_SET = 00h
    Fail2: TRAINING_PATTERN_SET not= 00h
    Pass3: Downstream link training timer ≤ 10 ms
    Fail3: Downstream link training timer > 10 ms

End of Downstream Link Training

17. Verify that the Branch DUT de-asserts HPD upstream.
18. Once downstream link training sequence is complete and upstream link training sequence is complete or upstream HPD de-asserted, stop the link training timer.
19. Verify that the total link training time is 20ms or less.

    Note1: Link training timer ≤ 20 ms
    Warning1: Link training timer > 20 ms

Result:

This test passes if all of the pass / fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: All pass/fail checks within the test steps succeeded
Fail2: One or more checks within the test steps failed

6.3.3.14 Lame Count Reduction

The test begins with the DisplayPort main link already trained and active, to the maximum number of lanes supported by the Branch DUT, and running at the 1.62Gbps link rate.

Test Procedure:

1. Reference Source writes 0x1 to the LANE_COUNT_SET field in DPCD of Branch DUT.
2. Reference Source continues to transmit idle pattern on lane 0, and disables all other lanes.
3. Verify that the Branch DUT has not cleared the LANE0_CR_DONE, LANE0_CHANNEL_EQ_DONE, LANE0_SYMBOL_LOCK bits for at least 500us.
4. Verify that the Branch DUT writes 0x1 to the LANE_COUNT_SET field in DPCD of Reference Sink.
5. Check that the Branch DUT continues to send idle pattern on lane 0 of its downstream link. The Branch DUT may instead do a full re-training of the downstream link with the new lane count (report this as a warning).
6. Verify that the Branch DUT sends at least 5 BS-idle patterns on lane 0 of its downstream port, and disables all other lanes.

Result:

This test fails if the upstream and downstream DisplayPort links are not active at 1 lane and 1.62Gbps link rate, or the links are not active with the Branch DUT upstream port locked to the idle pattern, and Branch DUT downstream port sending the idle pattern.

6.3.3.15 Lane Count Increase

The test begins with the DisplayPort main link already trained and transmitting the BS-Idle pattern, configured with one lane running at the 1.62Gbps link rate.
Note: Since DisplayPort repeaters must support four lanes, this test case assumes that the Branch DUT supports four lanes.

Test Procedure:

1. Reference Source stops transmission on all lanes.
2. Reference Source writes 0x4 to the LANE_COUNT_SET field in DPCD.
3. Reference Source continues with link training (go to step 4 of test 0).

Result:

This test fails if the upstream and downstream DisplayPort links are not active at a lane count of four and 1.62Gbps link rate, or the links are not active with the Branch DUT upstream port locked to the idle pattern, and Branch DUT downstream port sending the idle pattern.

6.3.4 Concentrator Link Training

The link training tests for a Concentrator Branch DUT are the same as for the Repeater, with the tests run using the upstream port 0 of the Concentrator. Please refer to section 6.3.3 for Concentrator Link Training tests.

6.3.5 Replicater Link Training

The link training tests for a Replicater Branch DUT are the same as for the Repeater, with the tests run using the downstream port 0 of the Replicater. Please refer to Section 6.3.3 for Replicater Link Training tests.

6.3.6 Upstream Link Maintenance

This set of tests check that the upstream port of the Branch DUT does the appropriate action when there is a loss of link (loss of symbol lock, loss of clock recovery lock, or loss of inter-lane alignment lock).

Note: The upstream DisplayPort main link is already trained and active, to the maximum number of lanes supported by the Branch DUT before the link maintenance tests are executed. The link maintenance tests can be done at either link rate. These tests are essentially the same as the link maintenance tests for the DisplayPort Sink DUT.

Note that these tests are not run for a Legacy-to-DisplayPort converter since it does not have a DisplayPort receiver on its upstream port.

6.3.6.1 IRQ HPD Pulse due to Loss of Symbol Lock and Clock Recovery Lock

Test Procedure:

1. Reference Source stops transmitting the idle pattern. The intention is to force the Branch DUT to symbol lock.
2. Verify that the Branch DUT toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms) within 20 ms after its detection of the downstream HPD pulse.

Note: This test can continue to configure the main link again, but is not necessary.

3. Verify that the LANEx_SYMBOL_LOCKED and LANEx_CR_DONE bits are cleared, and the LINK_STATUS_UPDATED bit is set.
4. For a repeater, concentrator or replicater Branch DUT, verify that the Branch DUT disables the downstream port if there is no local timing reference.

Result:

This test fails if the Branch DUT does not toggle IRQ HPD pulse, clear the LANEx_SYMBOL_LOCKED and LANEx_CR_DONE bits and set the LINK_STATUS_UPDATED bit in DPCD.

6.3.6.2 IRQ HPD Pulse due to Loss of Inter-lane Alignment Lock

Test Procedure:

Note: This test is skipped if the Branch DUT supports the maximum of one lane.

1. Reference Source stops transmitting the idle pattern with 2 link symbol inter-skew between adjacent lanes. The intention is to force the Branch DUT to lose inter-lane alignment lock.
2. Verify that the Branch DUT toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms) within 20 ms after its detection of the downstream HPD pulse..

Note: This test can continue to configure the main link again, but is not necessary.

3. Verify that the INTERLANE_ALIGN_DONE bit is cleared and LINK_STATUS_UPDATED bit is set in DPCD.

Result:

This test fails if the Branch DUT does not toggle IRQ HPD pulse, clear the INTERLANE_ALIGN_DONE bit and set the LINK_STATUS_UPDATED bit in DPCD.

6.3.7 Downstream Link Maintenance

This set of tests check that the downstream port of the Branch DUT does the appropriate action when an interrupt is signaled by IRQ HPD pulse.

Note: These tests all begin with the DisplayPort main link already trained to the maximum number of lanes supported by the Branch DUT. The link maintenance tests can be done at either link rate.

Also note that these tests are not run for a DisplayPort-to-Legacy converter since it does not have a DisplayPort transmitter on its downstream port.

6.3.7.1 Successful Link Re-training after IRQ HPD Pulse due to Loss of Symbol Lock on Downstream Link

This test case verifies re-training by the Branch DUT after Reference Sink reports loss of symbol lock on the downstream link. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.
This test is repeated separately for each lane.

Test Procedure:

1. Reference Sink clears the LANEx_SYMBOL_LOCKED bit of DPCD Link Status field to indicate a loss of symbol lock, and sets the LINK_STATUS_UPDATED bit.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD remains asserted for the remainder of the test. Start Link Status Read Timer.
3. Wait until the Branch DUT reads DPCD Link Status field (Aux read of address 0200h). Stop the Link Status Read timer. Verify that the Branch DUT read addresses 0200h – 0205h. Verify that the Link Status read occurred within 100ms of the rising edge of HPD.

   Pass1: Branch DUT read DPCD addresses 0200h – 0205h
   Fail1: Branch DUT did not read DPCD addresses 0200h – 0205h
   Pass2: Link Status Read started link status read within 100 ms
   Fail2: Link Status Read did not start within 100 ms
4. Carry out steps 16-21 of test 0 to re-train the downstream link.
5. Verify that the Branch DUT transitions from Training Pattern 2 to Idle Pattern, and that Branch DUT sends at least 5 BS-Idle Pattern on all active lanes.

   Pass1: Transition from TP2 to Idle Pattern detected on all active lanes
   Fail1: Transition from TP2 to Idle Pattern not detected on lane(s) {active lanes where transition was not detected}
   Pass2: Valid Idle Pattern detected on all active lanes
   Fail2: Valid Idle Pattern not detected on lanes {active lanes without valid Idle Pattern}
   Pass3: At least 5 BS-Idle Pattern detected on all active lanes
   Fail3: N BS-Idle Pattern detected for on lane M {repeat for all active lanes M that have N < 5}

Result:

This test passes if all of the pass/fail checks below pass.

Pass1: Test completed successfully
Fail1: Test was manually interrupted OR Test timer expired during step {report which test step the test was in when interrupted}

Pass2: Downstream link training completed successfully (report even if training exceeds 10 ms time constraint)
Report link training results:
LINK_BW_SET
LANE_COUNT_SET
VOLTAGE SWING SET
PRE-EMPHASIS_SET
Fail2: Downstream link training failed (report this if failure of any test step causes test to abort)

Pass4: LANE_COUNT_SET = original LANE_COUNT_SET
Fail4: LANE_COUNT_SET not= original LANE_COUNT_SET

Pass5: LINK_BW_SET = original LINK_BW_SET
Fail5: LINK_BW_SET not= original LINK_BW_SET

Pass6: All pass / fail checks within test steps passed
Fail6: One or more pass / fail check(s) within test steps failed

6.3.7.2 Successful Link Re-training after IRQ HPD Pulse due to Loss of Clock Recovery Lock on Downstream Link

This test case verifies re-training by the Branch DUT after Sink reports loss of clock recovery lock. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.

This test is repeated separately for each lane.

Other than step 1, this test case is identical to test 6.3.7.1 'Successful Link Re-training after IRQ HPD Pulse Due to Loss of Symbol Lock'.

Test Procedure:

1. Reference Sink clears the LANEx_CR_DONE bits of DPCD Link Status field to indicate a loss of clock recovery lock, and sets the LINK_STATUS_UPDATED bit.
2. Go to step 2 of test 6.3.7.1.

Result:

See 'Result' section of test 6.3.7.1

6.3.7.3 Successful Link Re-training after IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock on Downstream Link

This test case verifies re-training by the Branch DUT after Sink reports loss of inter-lane alignment lock. It is expected that the lane count and link bandwidth will be unchanged after link re-training, because the line conditions have not changed.

Other than step 1, this test case is identical to test 6.3.7.1 'Successful Link Re-training after IRQ HPD Pulse Due to Loss of Symbol Lock'.

Test Procedure:

1. Reference Sink clears the INTERLANE_ALIGN_DONE bit of DPCD Link Status field to indicate a loss of inter-lane alignment lock and sets the LINK_STATUS_UPDATED bit.
2. Go to step 2 of test 6.3.7.1.

Result:

See ‘Result’ section of test 6.3.7.1

6.3.7.4 No Link Re-training Required after IRQ HPD Pulse

Test Procedure:

1. Reference Sink keeps LANEx_SYMBOL_LOCKED, LANEx_CR_DONE and INTERLANE_ALIGN_DONE bits of DPCD Link Status field set.
2. Reference Sink toggles IRQ HPD pulse (low pulse between 0.5ms – 1ms). HPD remains asserted for the remainder of the test. Start Link Status Read timer.
3. Wait until the Branch DUT reads DPCD Link Status field (Aux read of address 0200h). Stop the Link Status Read timer. Verify that the Branch DUT read addresses 0200h – 0205h. Verify that the Link Status read occurred within 100ms of the rising edge of HPD.

   Pass1: Branch DUT read DPCD addresses 0200h – 0205h
   Fail1: Branch DUT did not read DPCD addresses 0200h – 0205h
   Pass2: Link Status Read started link status read within 100 ms
   Fail2: Link Status Read did not start within 100 ms
4. Monitor downstream AUX CH and main link activity for 10 ms. Verify that the Branch DUT does not re-initiate link training (does not write to TRAINING_PATTERN_SET byte in the Reference Sink DPCD Link Configuration Field) during 10 ms interval. Verify that the Branch DUT continues to transmit BS-Idle pattern or active video stream.

   Pass1: Branch DUT does not write to TRAINING_PATTERN_SET
   Fail1: Branch DUT writes to TRAINING_PATTERN_SET
   Pass2: BS-Idle or active video stream being transmitted on the downstream main link
   Fail2: No BS-Idle or active video stream on the downstream main link

Result:

This test passes if all pass/fail checks below pass

Pass1: Test completed successfully
Fail1: Test was manually interrupted

Pass2: All pass/fail checks within test steps succeeded
Fail2: One or more checks within test steps failed

6.4 Branch Device Isochronous Transport Services Test Procedures

In the Branch Device Isochronous Transport Services Test, the capability of the Branch DUT to transmit a main stream from its upstream port to its downstream port is tested.

6.4.1 Main Video Stream Transmission

Note: This test is run on Repeater, Concentrator and Replicater Branch DUTs only. For concentrator and replicater Branch DUTs, port 0 is used for testing.

Test Procedure:

1. Set the DisplayPort upstream and downstream link to the maximum link rate and lane count.
2. Reference Source transmits the color bar test pattern. This can be done at any resolution and display timing.

3. Reference Sink verifies that the color bar test pattern has been received properly at the chosen resolution and display timing.

Result:

This test fails if the color bar test pattern is not received properly at the Reference Sink.