82562EZ(EX)/82540EM Dual Footprint LOM Design Guide

Application Note (AP-434)

Networking Silicon

Notice: This document contains information on products in the design phase of development. Product features and specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

Revision 1.0
August 2002

Revision History

Revision	Revision Date	Description
0.75	Jan 2002	**Preliminary Draft**
0.80	August 2002	Revised Pin assignments: E1, E12, G5, G6, G13, H5, H6, H7, H8, H11, J5, J6, J7, J8, J9, J10, J11, K5, K6, K7, K8, K9, K10, K11, L4, L5, L9, L10.
1.0	April 2003	Remoned confidential (secret) status. Section 1.0. Added product ordering codes.

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Contents

1.0 Introduction

The 82540EM Gigabit Ethernet Controller and the 82562EZ/EX Fast Ethernet Controller are both manufactured in a footprint compatible 15mm x 15mm, 196-ball grid array package. Many of the critical signal pin locations on the 82540EM are identical to signals on the 82562EZ/EX allowing designers to create a single design that accommodates both parts. Because the usage of some pins on the 82540EM differ from the usage on the 82562EZ, the two parts are not referred to as "pin compatible". The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with either part to maximize value while matching your customers' performance needs.

1.1 Scope of this Design Guide

This application note identifies the design differences between the 82540EM and 82562EZ(EX). The table in Section 2.0 shows the stuffing (population) options for the two parts.

For other necessary design collateral, please see “Reference Documents” (Section 1.2).

1.2 Reference Documents

This application note assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82540EM Datasheet, Intel Corporation
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet, Intel Corporation
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers
- 82559 Fast Ethernet Controllers Timing Device Selection Guide, AP-419, Intel Corporation

1.3 Product Codes

The following table summarizes the product ordering codes for the 82562EZ, 82562EX, and 82540EM.

Table 1. Product Ordering Codes

Device	Product Code
82562EZ	DA82562EZ
82562EM	DA82562EM
82540EM	RC82540EM

2.0 Pin Number to Signal Mapping with Population Options

Table 2 below shows the pin names for both controllers and the corresponding shared ball reference value. Note that the 82540EM pin name in the 82540EM Datasheet/Design guide is slightly different from the signal name on the reference schematic. The datasheet/design guide signal names maintain consistency with the 64-bit gigabit controller naming convention, while the schematic names follow the conventions used by our engineers on their design tools.

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 1 of 6)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
					82540EM	82562EZ(EX)	
A1	NC	NC	NC				
A2	PCI_SERR_N	NC	PCI_SERR_N		PCI_SERR_N	PCI_SERR_N	
A3	3.3V	3.3V	3.3V				
A4	PCI_IDSEL	NC	PCI_IDSEL		PCI_IDSEL	PCI_IDSEL	
A5	PCI_AD[25]	NC	PCI_AD[25]		PCI_AD[25]	PCI_AD[25]	
A6	PCI_PME_N	NC	PCI_PME_N		PCI_PME_N	PCI_PME_N	
A7	3.3V	3.3V	3.3V				
A8	PCI_AD[30]	NC	AD[30]		PCI_AD[30]	PCI_AD[30]	
A9	LAN_PWR_GOOD	NC	LAN_PWR_GOOD		Supervisor IC	No stuff	
A10	SMB_CLK	NC	SMB_CLK		SMB_CLK		
A11	3.3V	3.3V	3.3V				
A12	LINK_UP_N	LINK_UP_N	LINK_UP_N	x	LINK LED	LINK LED	Same signal - different names.
A13	TEST_MAC_DM	TEST_EN	TEST_TESTEN	x	Pull-down	Pull-down	May have LAN Disable logic for Kinnereth.
A14	NC	NC	NC				
B1	PCI_AD[22]	NC	AD[22]		PCI_AD[22]	PCI_AD[22]	
B2	PCI_AD[23]	NC	AD[23]		PCI_AD[23]	PCI_AD[23]	
B3	VSS	VSS	VSS				
B4	PCI_AD[24]	NC	AD[24]		PCI_AD[24]	PCI_AD[24]	
B5	PCI_AD[26]	NC	AD[26]		PCI_AD[26]	PCI_AD[26]	
B6	PCI_AD[27]	NC	AD[27]		PCI_AD[27]	PCI_AD[27]	
B7	VSS	VSS	VSS				
B8	PCI_AD[31]	NC	AD[31]		PCI_AD[31]	PCI_AD[31]	
B9	PCI_RST_N	NC	PCI_RST_N		PCI_RST_N	PCI_RST_N	
B10	SMB_ALERT_N	NC	SMB_ALERT_N		SMB_ALERT_N	SMB_ALERT_N	Need a Weak Pull-High
B11	LINK100_N	SPEED_LED	LINK100_N		LED	LED	Same signal - different names.

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 2 of 6) (Continued)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
B12	LINK1000_N	TOUT	LINK1000_N	x	LED	No stuff	Testability output for Kinnereth
B13	CTRL_25	RBIAS100	CTRL_25_RBIAS100		Pwr Regulator	619 pull-down	
B14	PHY REF	RBIAS10	PHYREF_RBIAS10		2.49K pull-down	549 pull-down	
C1	PCI_AD[21]	NC	AD[21]		PCI_AD[21]	PCI_AD[21]	
C2	M66EN	NC	M66EN		PCI M66EN	No stuff	
C3	PCI_REQ_N	NC	PCI_REQ_N		PCI_REQ_N	PCI_REQ_N	
C4	PCI_CBE_N[3]	NC	PCI_CBE_N[3]		PCI_CBE_N[3]	PCI_CBE_N[3]	
C5	APM_WAKEUP	NC	APM_WAKEUP		WOL	WOL	
C6	PCI_AD[28]	NC	AD[28]		PCI_AD[28]	PCI_AD[28]	
C7	PCI_AD[29]	NC	AD[29]		PCI_AD[29]	PCI_AD[29]	
C8	NC	NC	NC		No stuff	No stuff	
C9	SMB_DAT	NC	SMB_DAT		SMB_DAT	SMB_DAT	
C10	VSS	VSS	VSS				
C11	ACTIVITY_N	ACT_LED	ACTIVITY_N		LED	LED	Same signal - different names.
C12	VSS	VSS	VSS		VSS	VSS	
C13	MDI_PLUS[0]	TX_PLUS	MDI_0+		MDI	MDI	
C14	MDI_MINUS[0]	TX_MINUS	MDI_0-		MDI	MDI	
D1	PCI_AD[18]	NC	AD[18]		PCI_AD[18]	PCI_AD[18]	
D2	PCI_AD[19]	NC	AD[19]		PCI_AD[19]	PCI_AD[19]	
D3	PCI_AD[20]	NC	AD[20]		PCI_AD[20]	PCI_AD[20]	
D4	ALT_CLK125	VSS	RESERVED_GND_VSS		VSS	VSS	
D5	VSS	VSS	VSS				
D6	VSS	VSS	VSS				
D7	VSS	VSS	VSS				
D8	VSS	VSS	VSS				
D9	2.5V	NC	2.5V		2.5V	No stuff	Non-populated for 82562EZ
D10	NC	ISOL_EXEC	NC	x	NC	NC	May have LAN Disable for Kinnereth.
D11	2.5V	NC	2.5V		2.5V	No stuff	
D12	NC	ISOL_TI	NC	x	NC	NC	May have LAN Disable for Kinnereth.
D13	VSS	VSS	VSS	x	VSS		
D14	NC	ISOL_TCK	NC	x	NC	NC	May have LAN Disable for Kinnereth.
E1	3.3V	3.3V	3.3V				
E2	VSS	VSS	VSS				
E3	PCI_AD[17]	NC	AD[17]		PCI_AD[17]	PCI_AD[17]	
E4	VSS	VSS	VSS				

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 3 of 6) (Continued)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
E5	VSS	VSS	VSS				
E6	VSS	VSS	VSS				
E7	VSS	VSS	VSS				
E8	VSS	VSS	VSS				
E9	VSS	VSS	VSS				
E10	VSS	VSS	VSS				
E11	NC	VCCT	NC		1.5V	3.3V	
E12	NC	VCCT	NC		1.5V	3.3V	
E13	MDI_PLUS[1]	RX_PLUS	MDI_1+		MDI	MDI	
E14	MDI_MINUS[1]	RX_MINUS	MDI_1-		MDI	MDI	
F1	PCI_IRDY_N	NC	PCI_IRDY_N		PCI_IRDY_N	PCI_IRDY_N	
F2	PCI_FRAME_N	NC	PCI_FRAME_N		PCI_FRAME_N	PCI_FRAME_N	
F3	PCI_CBE_N[2]	NC	C/BE[2]		PCI_CBE_N[2]	PCI_CBE_N[2]	
F4	VSS	VSS	VSS				
F5	VSS	VSS	VSS				
F6	VSS	VSS	VSS				
F7	VSS	VSS	VSS				
F8	VSS	VSS	VSS				
F9	VSS	VSS	VSS				
F10	VSS	VSS	VSS				
F11	VSS	VSS	VSS				
F12	PHY_TSTPT	NC	RESERVED_NC		NC	NC	
F13	MDI_PLUS[2]	NC	MDI_2+		Magnetics	No stuff	
F14	MDI_MINUS[2]	NC	MDI_2-		Magnetics	No stuff	
G1	PCI_CLK	NC	PCI_CLK		PCI_CLK	PCI_CLK	
G2	VIO	NC	VIO		VIO	VIO	
G3	PCI_TRDY_N	NC	PCI_TRDY_N		PCI_TRDY_N	PCI_TRDY_N	
G4	PCI_ZP	NC	PCI_ZP		Pull-down	No stuff	
G5	RSVD	VCCR	1.5V		1.5V	3.3V	
G6	RSVD	3.3V	1.5V		1.5V	3.3V	
G7	VSS	VSS	VSS				
G8	VSS	VSS	VSS				
G9	VSS	VSS	VSS				
G10	VSS	VSS	VSS				
G11	VSS	VSS	VSS				
G12	2.5V	NC	2.5V		2.5V	No stuff	
G13	NC	3.3V	1.5V		1.5V	3.3V	
G14	VSS	VSS	VSS				
H1	PCI_STOP_N	NC	PCI_STOP_N		PCI_STOP_N	PCI_STOP_N	
H2	PCI_INTA_N	NC	PCI_INTA_N		PCI_INTA_N	PCI_INTA_N	

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 4 of 6) (Continued)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
H3	PCI_DEVSEL_N	NC	PCI_DEVSEL_N		PCI_DEVSEL_N	PCI_DEVSEL_N	
H4	PCI_ZN	NC	PCI_ZN		Pull-up	No stuff	
H5	RSVD	VCCR	1.5V		1.5V	3.3V	
H6	RSVD	3.3V	1.5V		1.5V	3.3V	
H7	RSVD	3.3V	1.5V		1.5V	3.3V	
H8	RSVD	3.3V	1.5V		1.5V	3.3V	
H9	VSS	VSS	VSS				
H10	VSS	VSS	VSS				
H11	RSVD	NC	1.5V		1.5V	3.3V	
H12	HSDACN	NC	RESERVED_NC		NC		
H13	MDI_PLUS[3]	NC	MDI_3+		Magnetics		
H14	MDI_MINUS[3]	NC	MDI_3-		Magnetics		
J1	PCI_PAR	NC	PCI_PAR		PCI_PAR	PCI_PAR	
J2	PCI_PERR_N	NC	PCI_PERR_N		PCI_PERR_N	PCI_PERR_N	
J3	PCI_GNT_N	NC	PCI_GNT_N		PCI_GNT_N	PCI_GNT_N	
J4	NC	NC	NC				
J5	RSVD	VCCR	1.5V		1.5V	3.3V	
J6	RSVDV	3.3V	1.5V		1.5V	3.3V	
J7	RSVD	3.3V	1.5V		1.5V	3.3V	
J8	RSVD	3.3V	1.5V		1.5V	3.3V	
J9	RSVD	3.3V	1.5V		1.5V	3.3V	
J10	RSVD	3.3V	1.5V		1.5V	3.3V	
J11	RSVD	NC	1.5V		1.5V	3.3V	
J12	AUX_PWR	NC	AUX_PWR		AUX_PWR	AUX_PWR	
J13	HSDACP	NC	RESERVED_NC1		NC	NC	
J14	XTAL2	XTAL2	XTAL2	x	XTAL2	XTAL2	
K1	PCI_AD[16]	NC	AD[16]		PCI_AD[16]	PCI_AD[16]	
K2	VSS	VSS	VSS				
K3	3.3V	3.3V	3.3V				
K4	3.3V	3.3V	3.3V				
K5	RSVD	3.3V	1.5V		1.5V	3.3V	
K6	RSVD	3.3V	1.5V		1.5V	3.3V	
K7	RSVD	3.3V	1.5V		1.5V	3.3V	
K8	RSVD	3.3V	1.5V		1.5V	3.3V	
K9	RSVD	3.3V	1.5V		1.5V	3.3V	
K10	RSVD	3.3V	1.5V		1.5V	3.3V	
K11	RSVD	3.3V	1.5V		1.5V	3.3V	
K12	VSS	VSS	VSS				
K13	3.3V	3.3V	3.3V				
K14	XTAL1	XTAL1	XTAL1	x	XTAL1	XTAL1	

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 5 of 6) (Continued)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
L1	PCI_AD[14]	NC	AD[14]		PCI_AD[14]	PCI_AD[14]	
L2	PCI_AD[15]	NC	AD[15]		PCI_AD[15]	PCI_AD[15]	
L3	PCI_CBE_N[1]	NC	PCI_C/BE_N[1]		PCI_CBE_N[1]	PCI_CBE_N[1]	
L4	RSVD	3.3V	1.5V		1.5V	3.3V	
L5	RSVD	3.3V	1.5V		1.5V	3.3V	
L6	VSS	VSS	VSS				
L7	CLK_BYP_N	ADV10	RESERVED-ADV10	x	NC	NC	
L8	2.5V	NC	2.5V		2.5V	No stuff	
L9	RSVD	3.3V	1.5V		1.5V	3.3V	
L10	RSVD	3.3V	1.5V		1.5V	3.3V	
L11	VSS	VSS	VSS				
L12	JTAG_TMS	NC	JTAG_TMS		NC	NC	
L13	JTAG_TRST_N	JTXD[1]	JTAG_TRST_N	x	PLC	PLC	ICH drives this signal low. TRST needs to be grounded to disable JTAG.
L14	JTAG_TCK	JTXD[2]	JTAG_TCK	x	PLC	PLC	ICH drives this signal low. TCK needs to be biased.
M1	PCI_AD[11]	NC	AD[11]		PCI_AD[11]	PCI_AD[11]	
M2	PCI_AD[12]	NC	AD[12]		PCI_AD[12]	PCI_AD[12]	
M3	PCI_AD[13]	NC	AD[13]		PCI_AD[13]	PCI_AD[13]	
M4	PCI_CBE_N[0]	NC	CBE_N[0]		PCI_CBE_N[0]	PCI_CBE_N[0]	
M5	PCI_AD[5]	NC	AD[5]		PCI_AD[5]	PCI_AD[5]	
M6	VSS	VSS	VSS				
M7	PCI_AD[1]	NC	AD[1]		PCI_AD[1]	PCI_AD[1]	
M8	CLK_VIEW	NC	RESERVED_CLK_NC		NC	NC	
M9	FLSH_CE_N	NC	FLSH_CE_N		NC	NC	
M10	EESK	NC	EESK		EESK	EESK	If EE from ICH and Kenai is shared, a zero ohm pop is required b/c ICH drives this in reset.
M11	FLSH_SI	NC	FLSH_SI		NC	NC	
M12	SDP[7]	JRXD[2]	SDP[7]	x	PLC	PLC	ICH expects this signal to be high or undriven.
M13	JTAG_TDI	JRSTSYNC	JTAG_TDI	x	PLC	PLC	ICH expects this signal to be high
M14	JTAG_TDO	JTXD[0]	JTAG_TDO	x	PLC	PLC	ICH expects this signal to be low
N1	VSS	VSS	VSS				
N2	PCI_AD[10]	NC	AD[10]		PCI_AD[10]	PCI_AD[10]	
N3	PCI_AD[9]	NC	AD[9]		PCI_AD[9]	PCI_AD[9]	

Table 2. Pin out comparison table for 82540EM and 82562EZ(EX) (Sheet 6 of 6) (Continued)

Pin Out	82540EM Pin Name	82562EZ/EX Pin Name	Schematic Pin Name	K	Population Option		Comments
N4	PCI_AD[7]	NC	AD[7]		PCI_AD[7]	PCI_AD[7]	
N5	PCI_AD[4]	NC	AD[4]		PCI_AD[4]	PCI_AD[4]	
N6	3.3V	3.3V	3.3V				
N7	PCI_AD[0]	NC	AD[0]		PCI_AD[0]	PCI_AD[0]	
N8	3.3V	3.3V	3.3V				
N9	FLSH_SCK	NC	FLSH_SCK		NC	NC	
N10	EE_DO	NC	EE_DO		EEDO	EEDO	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
N11	NC	NC	NC		No stuff	No stuff	
N12	VSS	VSS	VSS				
N13	SDP[6]	JRXD[1]	SDP[6]	x	PLC	PLC	ICH expects this signal to be high or undriven.
N14	SDP[0]	JCLK	SDP[0]	x	PLC	PLC	ICH expects this signal to be low or undriven.
P1	NC	NC	NC				
P2	3.3V	3.3V	3.3V				
P3	PCI_AD[8]	NC	AD[8]		PCI_AD[8]	PCI_AD[8]	
P4	PCI_AD[6]	NC	AD[6]		PCI_AD[6]	PCI_AD[6]	
P5	PCI_AD[3]	NC	AD[3]		PCI_AD[3]	PCI_AD[3]	
P6	PCI_AD[2]	NC	AD[2]		PCI_AD[2]	PCI_AD[2]	
P7	EE_CS	NC	EE_CS		EECS	EECS	If EE from ICH and Kenai is shared, a zero ohm pop is required b/c ICH drives this in reset.
P8	VSS	VSS	VSS				
P9	FLSH_SO	NC	FLSH_SO		NC	NC	
P10	EE_DI	NC	EE_DI		EEDI	EEDI	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
P11	CTRL_15	NC	CTRL_15		Pwr Regulator	No stuff	
P12	3.3V	3.3V	3.3V				
P13	SDP[1]	JRXD[0]	SDP[1]	x	PLC	PLC	ICH expects this signal to be high or undriven.
P14	NC	NC	NC				

3.0 PCB Routing Guidelines

3.1 Critical Dimensions for Discrete Magnetic Module and RJ45

There are four critical dimensions that must be considered during the layout phase of an 82540EM and 82562EZ LAN On Motherboard implementation. These dimensions are identified in Figure 1 as A, B, C and D.

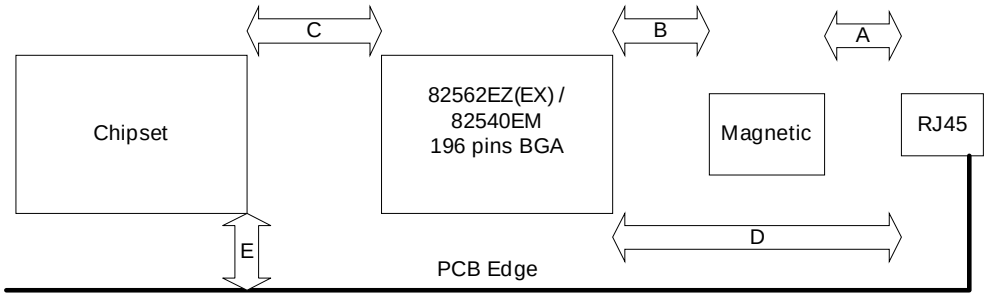


Figure 1. Critical Dimensions for 82562EZ(EX) and 82540EM Component Placement

3.1.1 Distance A: Magnetic to RJ45

The distance labeled “A” in Figure 1 should be given highest priority in board layout. The distance between the magnetic and RJ45 should be less than 1 inch of separation. The following trace characteristics are important and should be observed.

- Differential Impedance: The differential impedance should be 100 ohm. The single ended trace impedance will be approximately 50 ohm; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions.

3.1.2 Distance B: LAN Controller to Magnetic

The distance labeled “B” should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through the traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces.

3.1.3 Distance C: LAN Controller to Chipset

This section between chipset and LAN controller should be addressed separately for 82562EZ and 82540EM.

3.1.3.1 LAN Connect Interface (LCI) for 82562EZ

The LCI can be routed to support a 10/100 Mbps LOM solution with 82562EZ. Distance C, the LCI, should be less than 12 inches on ICH4 platform. The LAN_CLK traces should match the traces of other LCI signals.

3.1.3.2 PCI Interface for 82540EM

The PCI bus on 82540EM meets PCI 2.2 specification. The trace routing on the bus should follow PCI 2.2 specification.

3.1.4 Distance D: The Overall Length of Differential Traces from LAN to RJ45

The overall length of differential pairs should be less than 4 inches measured from the LAN controller to RJ45 through the magnetic module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25mm) and as symmetrical as possible.

3.1.5 Distance E: LAN Controller to PCB Edge

The LAN controller should be placed at least 2 inches from the printed circuit board edge.

3.2 Critical Dimensions for Integrated Mag-Jack

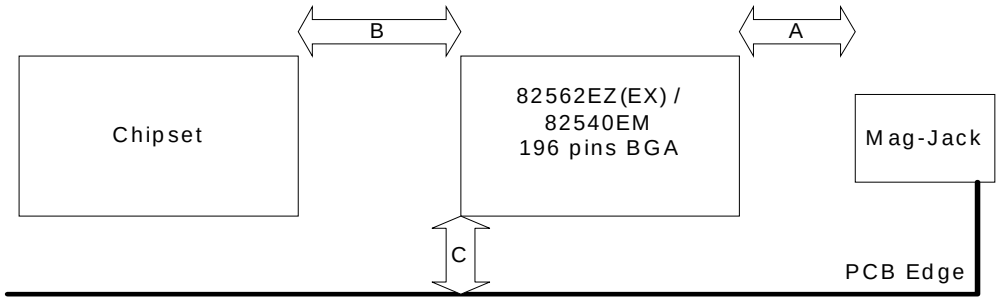


Figure 2. Critical Dimensions for 82562EZ and 82540EM Component Placement with Integrated Mag-Jack

3.2.1 Distance A: The Overall Length of Differential Traces

The overall length of differential pairs should be less than 4 inches measured from the LAN controller across the magnetic module to the RJ45 connector.

3.2.2 Distance B: LAN Controller to Chipset

For LCI on 82562EZ, the maximum length should be less than 12 inches on ICH4 platform. For PCI bus on 82540EM, the bus routing should meet PCI 2.2 specifications.

3.2.3 Distance C: LAN Controller to PCB Edge

The LAN controller should be placed at least 2 inches from the printed circuit board edge.

3.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.3 mil stackup.):

Maintain constant symmetry and spacing between the traces within a differential pair.

Keep the signal trace lengths of a differential pair equal to each other.

Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).

Keep maximum separation between differential pairs to 7 mils.

For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead.

Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

3.3.1 Trace Routing and Geometry

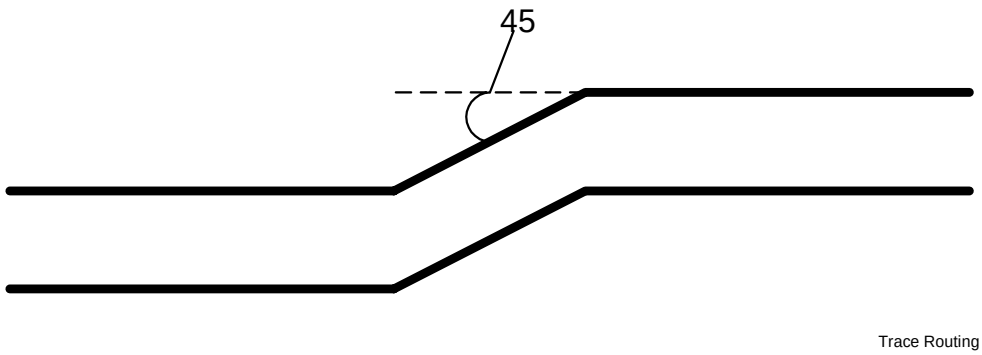


Figure 3. Trace Routing

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 O. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 O, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/ magnetics/edge of the board.

3.3.1.1 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

3.3.1.2 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

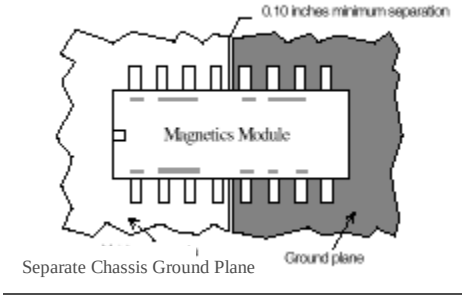


Figure 4. Ground Plane

3.3.1.3 Separation

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

3.4 Schematic for EEPROM Footprints and LCI Connection

There are 2 options for EEPROM footprints. OEMs can choose either a common EEPROM footprint for both 82540EM and ICHx or independent EEPROM footprint for each LAN silicon.

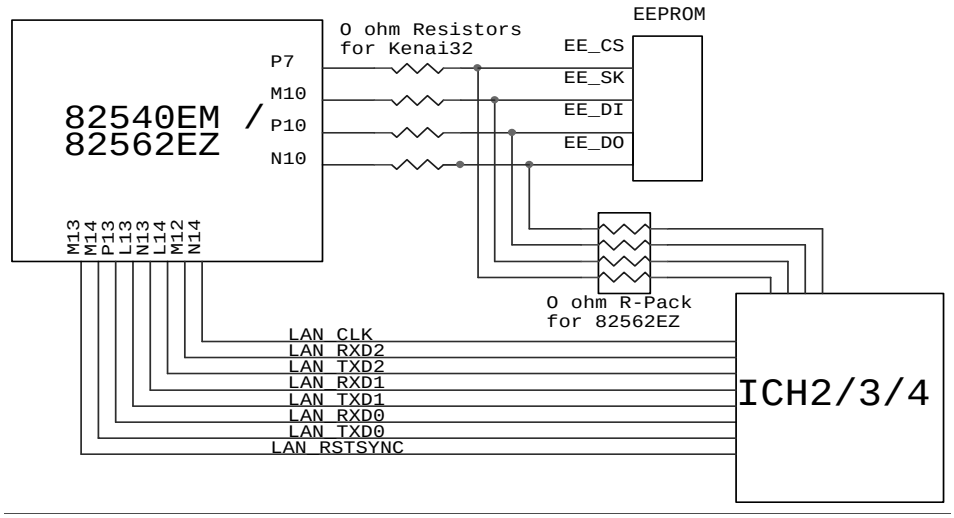


Figure 5. Common EEPROM Footprint for both 540EM and 562EZ

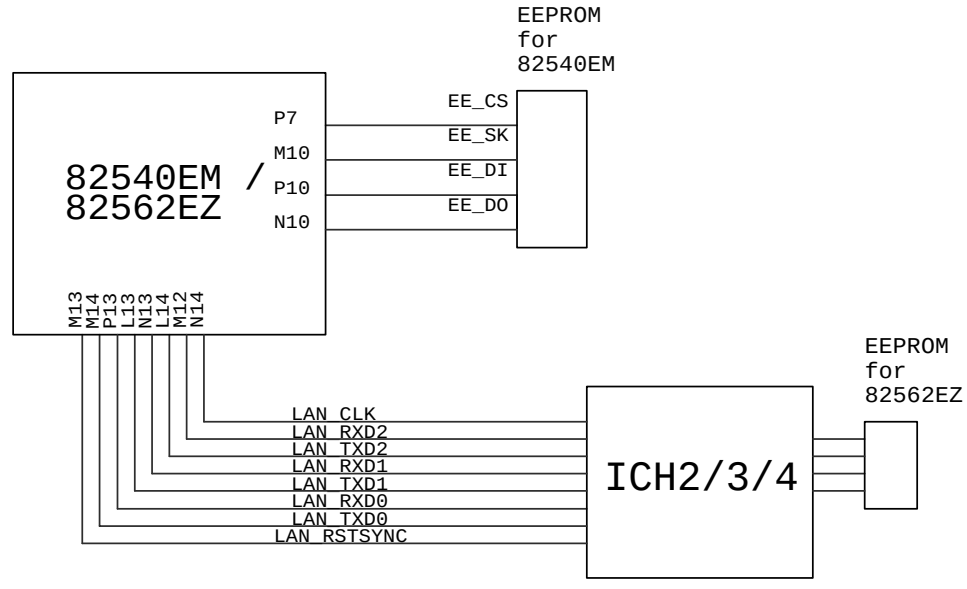


Figure 6. Independent EEPROM footprints for individual LAN silicon

3.5 Termination of Unused Differential Signals on Gb Magnetic for 10/100 LOM Design

Since the number of differential signals are different between a 10/100 LAN silicon and a gigabit LAN silicon, the 2 major problems confronted in designing the dual footprint LOM design are (1) choosing the pin compatible magnetic modules for both 10/100 and gigabit silicon, and (2) terminating unused differential signals for gigabit between the selected magnetic module and RJ45 connector when a 10/100 LAN design is implemented. Intel provides three options to remedy this issue:

3.5.1 Option 1: Board Level Stuffing

1. Layout resistor footprints on the pairs 3 and 4 of the differential traces for 82540EM LOM design. Refer to Figure 7
2. Possibly rework the magnetic module for 10/100 to be footprint compatible with the magnetic for gigabit
3. Replace the magnetic for 82540EM with the one for 82562EZ, and populate R1/R2 and R3/R4 for 82562EZ LOM design. Refer to Figure 8

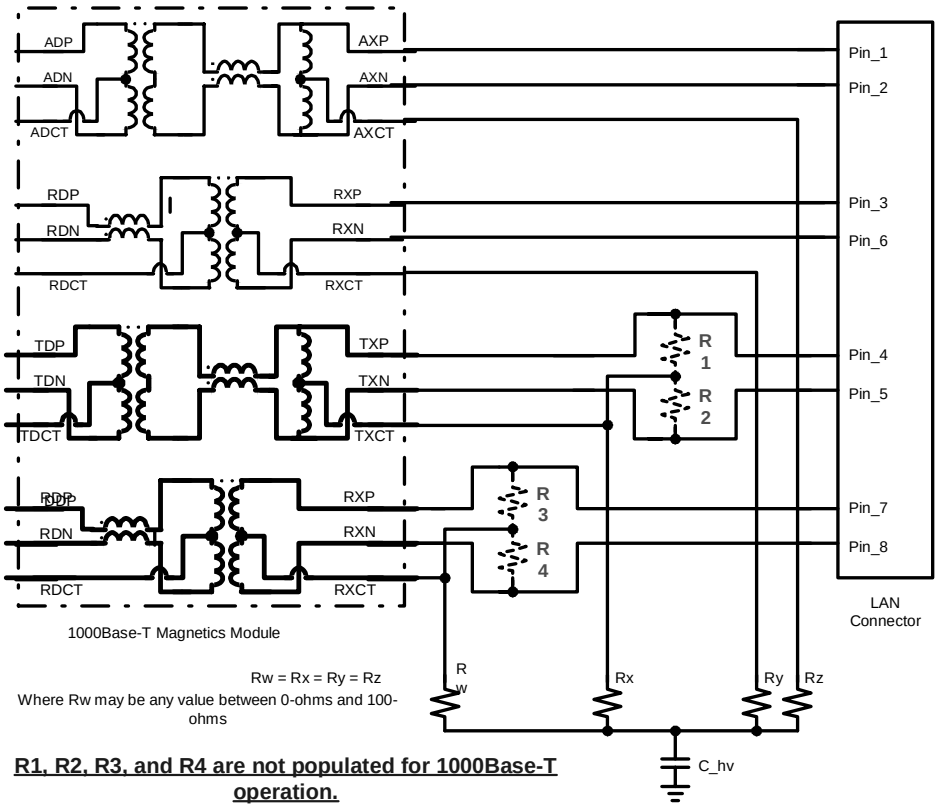


Figure 7. Typical magnetic for Gb LAN Controller with Optional Resistors Footprint

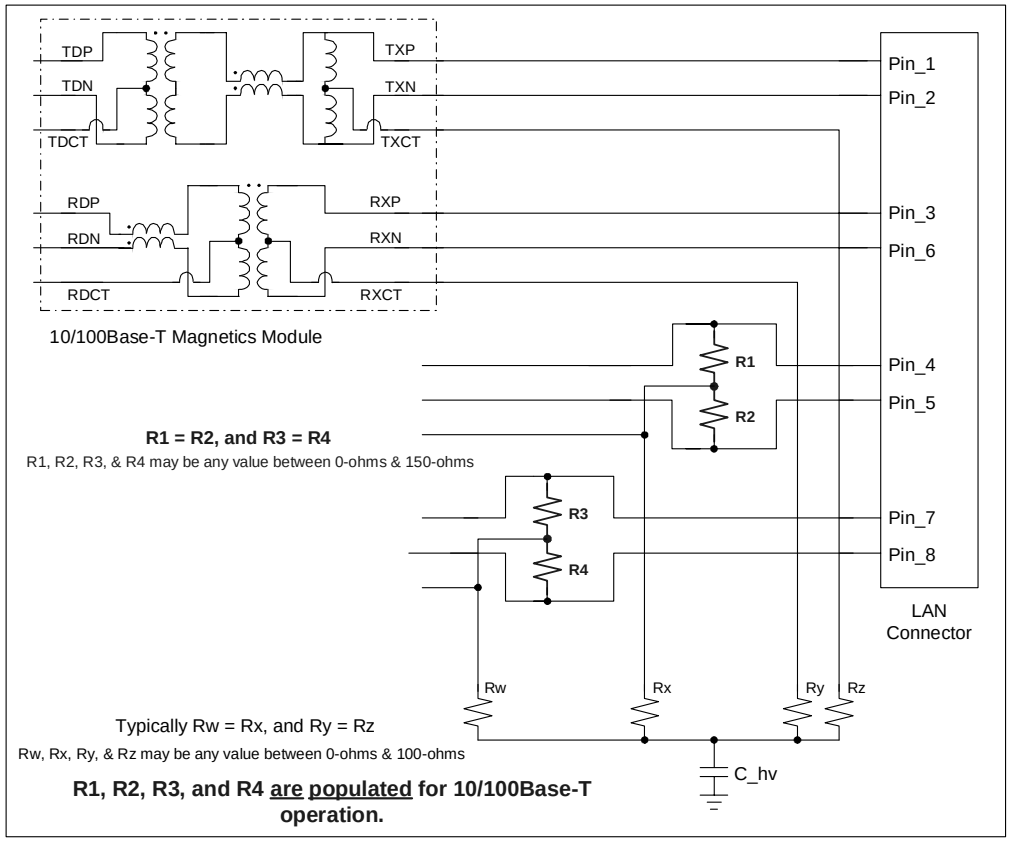


Figure 8. Replacement of magnetic for 10/100 LAN Controller with optional resistors populated.

3.5.2 Option 2: Rework of Gb Magnetic with an Internal Jumper for 10/100 Design[1]

In order to make a common footprint on differential pairs between the magnetic and RJ45 connector for both 10/100 and Gigabit LOM design, one of approaches is to rework the magnetic module for gigabit controller with internal jumpers to short pair 3 and 4 of differential signals. OEMs need to work with their magnetic vendors for the option.

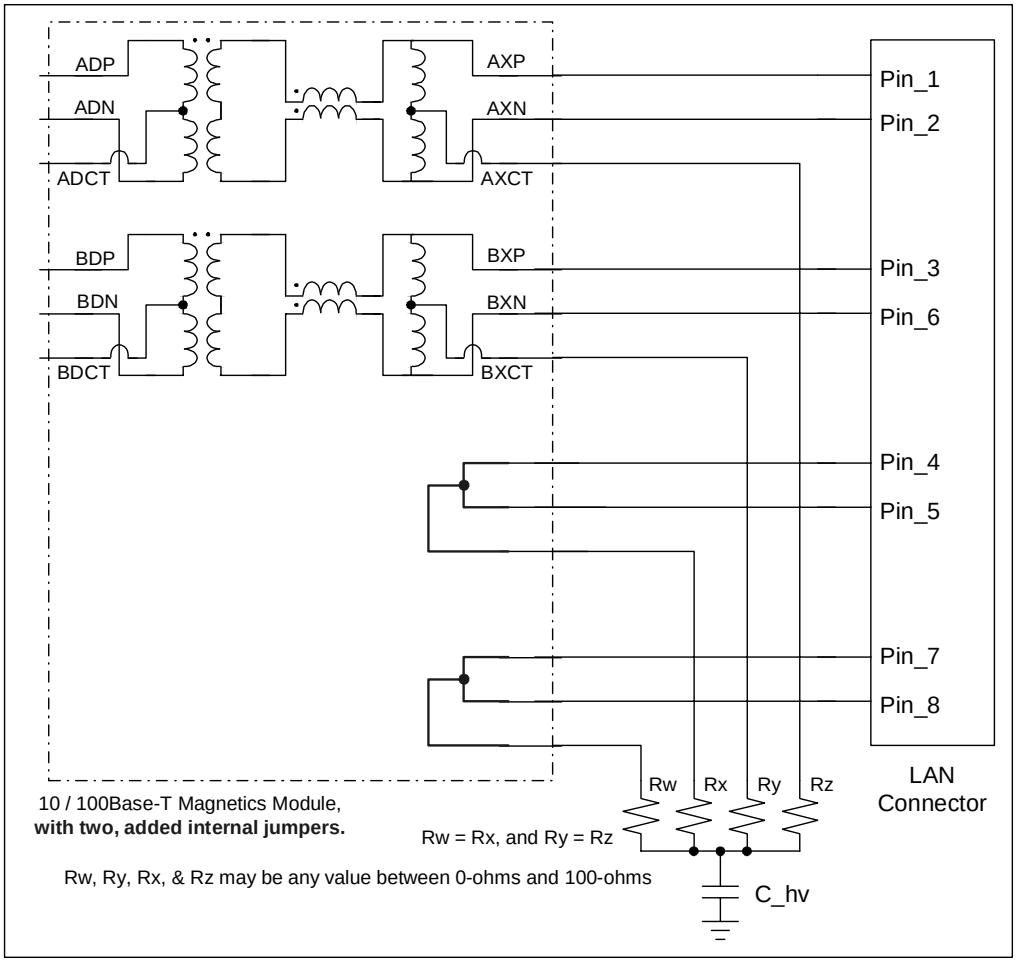


Figure 9. Rework of Gb magnetic with shorted pair 3 and 4 on differential traces for 10/100 LOM design.

3.5.3 Option 3: Integrated Mag-Jack for 10/100 and Gigabit

Refer to Table 3

1. Intel is working with some magnetic vendors to standardize the pinout assignments on the Mag-Jack.

Note: This page is intentionally left blank.

4.0 Selection of A Magnetic Module for 10/100/1000 LOM Design

4.1 Qualifying Magnetic for 10/100/1000 LOM Design

One of the most important component choices in a 10/100 and 1000 Mbps Ethernet LOM design is the magnetic module. The module has a critical effect on overall IEEE and emission compliance. The device selected should meet the required design performance. Occasionally, components that meet basic specifications may cause the system (LOM, NIC, Repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series of parallel capacitance values or expected series inductance values within the magnetic module. This may cause the design to fail certain IEEE specifications.

In order to help OEMs qualify a magnetic module, Intel provides the electrical specifications for magnetic modules used with Intel's LOM or NIC designs as a reference.

Table 3. Magnetics meeting Intel specifications (See Table 4 & 5)

	10/100	1000
Discrete Magnetic	H1012T / S558-5999-46	H5007
Footprint Compatible[1]	TBD	TBD

1. Intel is working with some magnetic vendors to standardize the pinout assignments on the Mag-Jack.

Table 4. Electrical Specifications at 25°C for 10/100 Magnetic

INSERTION LOSS (TX / RX)	
0.1 THRU 0.999MHz	1.0dB MAX
1.0 THRU 15MHz	0.35dB MAX
15.1 THRU 60MHz	0.7dB MAX
60.1 THRU 100MHz	1.2dB MAX
RETURN LOSS (TX / RX)	
1.0 THRU 30MHz	18dB MIN
30.1 THRU 60MHZ	19 - [20Log(f/30MHz)] dB MIN
60.1 THRU 80MHz	12dB MIN
TRANSMIT COMMON-MODE TO COMMON MODE REJECT	
1.0 THRU 60MHz	48dB MIN
60.1 THRU 100MHz	43dB MIN
100.1 THRU 150MHz	42dB MIN
EFFECTIVE COMMON-MODE TO COMMON-MODE REJECTION	
1.0 THRU 60MHz	38dB MIN
60.1 THRU 100MHz	34dB MIN
100.1 THRU 150MHz	32dB MIN
TRANSMIT DIFFERENTIAL TO COMMON MODE REJECT	
1.0 THRU 60MHz	38dB MIN
60.1 THRU 100MHz	35dB MIN
100.1 THRU 150MHz	32dB MIN
RECEIVE DIFFERENTIAL TO COMMON MODE REJECT	
1.0 THRU 60MHz	30dB MIN
60.1 THRU 100MHz	25dB MIN
100.1 THRU 150MHz	20dB MIN
CROSSTALK ISOLATION (TX / RX)	
1.0 THRU 60MHz	48dB MIN
60.1 THRU 100MHz	43dB MIN
100.1 THRU 150MHz	38dB MIN
HIGH VOLTAGE ISOLATION	
IEEE 14.3.1.1	2250V DC FOR 60 Sec.
OCL WITH 8mA Bias 100KHz	400uH

Table 5. Electrical Specifications at 25° C for 1000 Gb Silicon

INSERTION LOSS (TX / RX)	
0.1 THRU 999kHz	1.0dB MAX
1.0 THRU 60.0MHz	0.6dB MAX
60.1 THRU 80.0MHz	0.8dB MAX
80.1 THRU 100.0MHz	1.0dB MAX
100 THRU 125.0MHz	2.4dB MAX
RETURN LOSS (TX / RX)	
1.0 THRU 40.0MHz	18dB MIN
40.1 THRU 100MHZ	12 - [20Log(f/80MHz)] dB MIN
COMMON-MODE TO COMMON MODE REJECTION	
1.0 THRU 60MHz	48dB MIN
60.1 THRU 100MHz	42dB MIN
100.1 THRU 150MHz	37dB MIN
DIFFERENTIAL TO COMMON MODE REJECTION	
1.0 THRU 60MHz	35dB MIN
60.1 THRU 100MHz	29dB MIN
100.1 THRU 150MHz	22dB MIN
CROSSTALK ISOLATION (TX / RX)	
1.0 THRU 80MHz	36dB MIN
80.1 THRU 150MHz	27dB MIN
HIGH VOLTAGE ISOLATION	
1500 Vrms minimum, at 50 to 60 Hz, for 60 S.	2250V DC FOR 60 Sec.
OCL WITH 8mA Bias	400uH MIN

Note: This page is intentionally left blank.

5.0 EEPROM Information

Note: For complete EEPROM programming information, please refer to the EEPROM Map and Programming Guide corresponding to the LAN silicon.

5.1 EEPROM Map for the 82540EM

Table 6. EEPROM Map for the 82540EM (Sheet 1 of 2)

Word Address (hex)	HW Access	Description (Hi Byte)	Description (Low Byte)	Default Image Value (hex)	LAN# or Shared
0	Yes	IA Byte 2	IA Byte 1	IA(2,1)	Shared Value[1]
1	Yes	IA Byte 4	IA Byte 3	IA(4,3)	Shared Value[1]
2	Yes	IA Byte 6	IA Byte 5	IA(6,5)	Shared Value[1]
3	No	Compatibility high	Compatibility low	0000	Shared
4-7	No	Reserved	Reserved	0000	Shared
8	No	PBA, byte 1	PBA, byte 2	TBD	Shared
9	No	PBA, byte 3	PBA, byte 4	TBD	Shared
A	Yes	Init Control 1, high byte	Init Control 1, low byte	See Text	Shared
B	Yes	Subsystem_ID, high byte	Subsystem_ID, low byte	tbd	Shared
C	Yes	Subsystem_Vendor, high byte	Subsystem_Vendor, low byte	8086	Shared
D	Yes	Device ID, high	Device ID, low	tbd	LAN 0
E	Yes	Vendor ID, high	Vendor ID, low	8086	Shared
F	Yes	Init Control 2, high byte	Init Control 2, low byte	See Text	Shared
10-1F	No	*Note change from previous generation of silicon: range is no longer OEM Rsvd*	Note change from previous generation of silicon: range is no longer OEM Rsvd		
10	Yes	Software Definable Pin Control		xxxxh	LAN1
11		Device ID			LAN1
12			Common Power		Shared
13	Yes	Management Control			LAN1
14	Yes	Init Control 3	SMBus Address	xxxxx	LAN1
15	Yes	IPv4 Address Byte 2	IPv4 Address Byte 1	IP(2,1)	LAN1
16	Yes	IPv4 Address Byte 4	IPv4 Address Byte 3	IP(4,3)	LAN1
17	Yes	IPv6 Address Byte 2	IPv6 Address Byte 1	IP(2,1)	LAN1
18	Yes	IPv6 Address Byte 4	IPv6 Address Byte 3	IP(4,3)	LAN1

Table 6. EEPROM Map for the 82540EM (Sheet 2 of 2) (Continued)

Word Address (hex)	HW Access	Description (Hi Byte)	Description (Low Byte)	Default Image Value (hex)	LAN# or Shared
19	Yes	IPv6 Address Byte 6	IPv6 Address Byte 5	IP(6,5)	LAN1
1A	Yes	IPv6 Address Byte 8	IPv6 Address Byte 7	IP(8,7)	LAN1
1B	Yes	IPv6 Address Byte 10	IPv6 Address Byte 9	IP(10,9)	LAN1
1C	Yes	IPv6 Address Byte 12	IPv6 Address Byte 11	IP(12,11)	LAN1
1D	Yes	IPv6 Address Byte 14	IPv6 Address Byte 13	IP(14,13)	LAN1
1E	Yes	IPv6 Address Byte 16	IPv6 Address Byte 15	IP(16,15)	LAN1
1F	Yes	Reserved			
20	Yes	Software Defined Pins Control, high byte	Software Defined Pins Control, low byte	See Text	LAN0
21	Yes	Circuit Control, high	Circuit Control, low	0011	Shared
22	Yes	D0 Power	D3 Power	See Text	Shared
23	Yes	Management Control, high byte	Management Control, low byte	XxC8h	LAN0
24	Yes	Init Control 3	SMBus Addresss	xxxxx	LAN0
25	Yes	IPv4 Address Byte 2	IPv4 Address Byte 1	IP(2,1)	LAN0
26	Yes	IPv4 Address Byte 4	IPv4 Address Byte 3	IP(4,3)	LAN0
27	Yes	IPv6 Address Byte 2	IPv6 Address Byte 1	IP(2,1)	LAN0
28	Yes	IPv6 Address Byte 4	IPv6 Address Byte 3	IP(4,3)	LAN0
29	Yes	IPv6 Address Byte 6	IPv6 Address Byte 5	IP(6,5)	LAN0
2A	Yes	IPv6 Address Byte 8	IPv6 Address Byte 7	IP(8,7)	LAN0
2B	Yes	IPv6 Address Byte 10	IPv6 Address Byte 9	IP(10,9)	LAN0
2C	Yes	IPv6 Address Byte 12	IPv6 Address Byte 11	IP(12,11)	LAN0
2D	Yes	IPv6 Address Byte 14	IPv6 Address Byte 13	IP(14,13)	LAN0
2E	Yes	IPv6 Address Byte 16	IPv6 Address Byte 15	IP(16,15)	LAN0
2F					
30-35	No	PXE Configuration	PXE Configuration		Shared
33-3E	Fixed	Reserved	Reserved	0000	
3F	No	Checksum, high byte	Checksum, low byte	Checksum of words 0-3E	

1. Ethernet address will internally increment to even for LAN0 and odd for LAN1.

Table 7. Example EEPROM Image Files for 82540EM[1]

0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0200	00B3	0040	0000	0000	0000	0000	0000
A515	8007	660A	1107	8086	1008	8086	F26C
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	0011	3711	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	XXXX

1. See Document #10441 for an explanation of the EEPROM contents.

5.2 EEPROM Image for 82562EZ

Table 8. EPROM Image for 82562EZ

Word	HIgh Byte (Bits 15:8)		Low Byte (Bits 7:0)	Used by
00h	Ethernet Individual Address Byte 2		Ethernet Individual Address Byte 1	Hardware
01h	Ethernet Individual Address Byte 4		Ethernet Individual Address Byte 3	Hardware
02h	Ethernet Individual Address Byte 6		Ethernet Individual Address Byte 5	Hardware
03h	Compatibility Byte 1		Compatibility Byte 0	Intel® driver
04h	Reserved			
05h	Controller Type (02h for ICH2, ICH3 and ICH4)		Connector Type	Intel® driver
06h	PHY Device Record			
07h	Reserved			
08h	PWA Number Byte 4		PWA Number Byte 3	Factory
09h	PWA Number Byte 2		PWA Number Byte 1	Factory
0Ah	EEPROM ID			Hardware
0Bh	Subsystem ID			Hardware
0Ch	Subsystem Vendor ID			Hardware
0Dh	0000b	Heartbeat Packet Pointer	SMB Address Field	Alert on LAN* driver or hardware
0Eh to 22h	Reserved			
23h	ICH2 = Reserved ICH3 = Device ID ICH4 = Device ID			

Table 8. EPROM Image for 82562EZ

Word	HIgh Byte (Bits 15:8)	Low Byte (Bits 7:0)	Used by
24h to 2Fh	Reserved		
30h	Reserved for Intel Network Interface Division (NID) Boot Agent ROM Configuration (PXE and RPL version)		Firmware
31h	Reserved for Intel NID Boot Agent ROM Configuration (PXE and RPL version)		Firmware
32h	Reserved for Intel NID Boot Agent ROM Configuration (PXE and RPL version)		Firmware
33h to 3Ah	Reserved		
3Bh	Reserved for Intel® Architecture Labs (IAL) Boot ROM Configuration (PXE only)		Firmware
3Ch to 3Fh	Reserved		
40h to FAh	Alert on LAN alert packet structure		Alert on LAN driver
FFh	Checksum		Driver

Table 9. Example EEPROM Image Files for 82540EM

0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0200	00B3	0040	0000	0000	0000	0000	0000
A515	8007	49A2	ZZZZ	8086	1008	8086	F26C
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	1039	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	XXXX

6.0 Package Information

Although both the 82562EZ(EX) and 82540EM are 196 Ball Grid Array (BGA) package and footprint compatible, the package dimensions in height are slightly different. More information on Intel device packaging is available in the Intel Packaging Handbook (available from the Intel Literature Center or your local sales office).

6.1 82562EZ & 82562EX Package Information

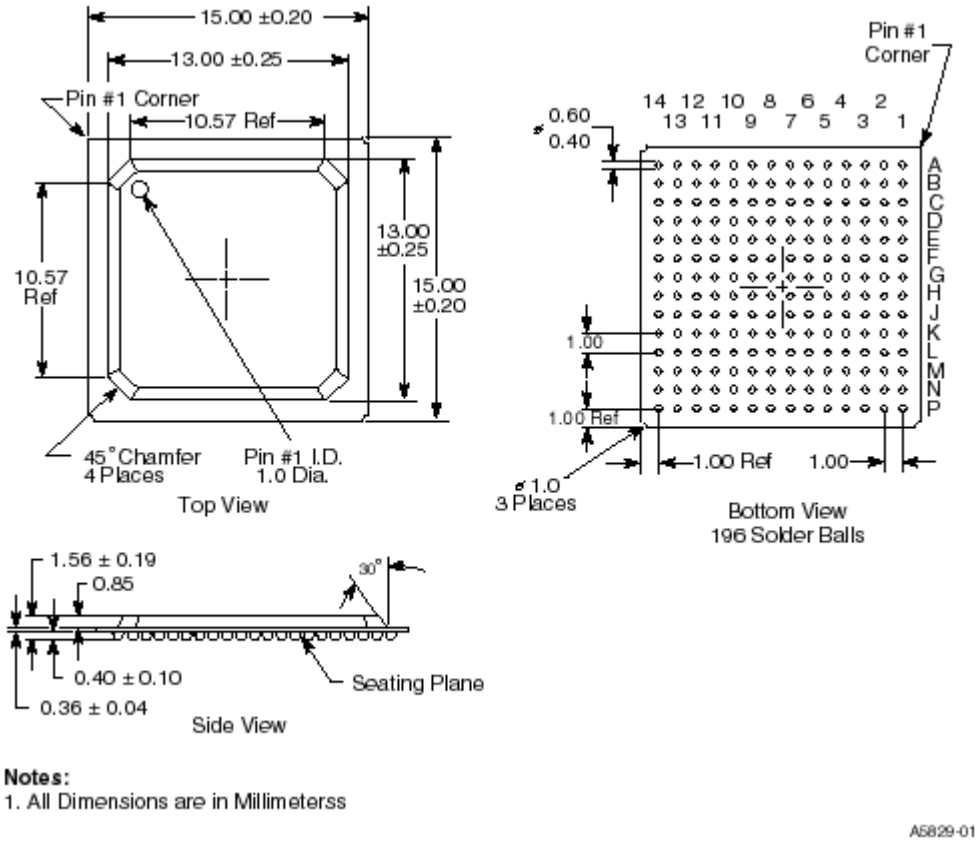
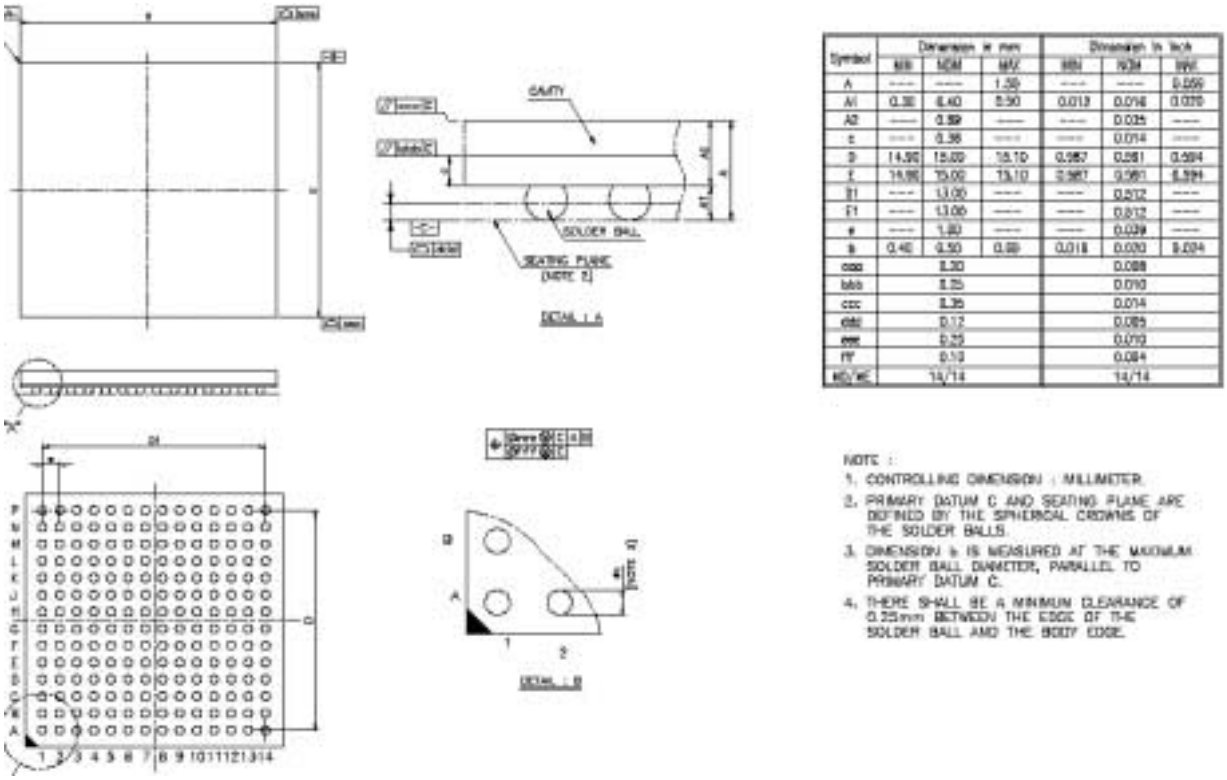


Figure 10. 82562EZ(EX) Package Information

6.2 82540EM Package Information



Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	1.55	-----	-----	0.059
A1	0.30	0.40	0.50	0.013	0.016	0.020
A2	-----	0.89	-----	-----	0.035	-----
c	-----	0.36	-----	-----	0.014	-----
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	-----	13.00	-----	-----	0.512	-----
E1	-----	13.00	-----	-----	0.512	-----
e	-----	1.00	-----	-----	0.039	-----
b	0.40	0.50	0.60	0.016	0.020	0.024
aaa	0.20			0.008		
bbb	0.25			0.010		
ccc	0.35			0.014		
ddd	0.12			0.005		
eee	0.25			0.010		
fff	0.10			0.004		
MD/ME	14/14			14/14		

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUN CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

Figure 11. 82540EM Package Information

7.0 Self-Review Checklist for 82540EM and 82562EZ Dual Footprint LOM Design

Table 10. 82562EZ LOM / Layout Checklist (Sheet 1 of 2)

Parts	Check Items	Recommendation/ Trace Length in Mil otherwise as indicated	Remark
Critical Dimension	Figure (1) Discrete Magnetic and RJ45	A <= 2”; B <= 2”; C <= 10”; E >= 1.5”	Refer to Figure (1), Priority Order A / E > B > C
	Figure (2) Integrated Magnetic and RJ45 (USB)	C <= 10”; E >= 1.5”; D <= 4”	Refer to Figure (2)., Priority Order B /E > C
Differential Signals	100/120 OHM termination resistors should be laid close to 562ET	<= 300	EMI alleviation (current passing through terminators will emit radiation)
	Trace-to-trace spacing within a pair (i.e., TX+/- spacing)	<= 12	CMN: Common Mode Noise should be coupled equally as the traces are routed close together; a common mode choke will give better performance
	Diff trace impedance 4-layer PCB: 6 width / 7 spacing / 5 height 6-layer PCB: 5 width / 7 spacing / 5 height	ZTXdiff = 100 ZRXdiff = 100	The differential impedance of wire should be 100 OHMS to match Cat5 cable impedance
	Trace length variation within a pair (i.e., Trace length variation in TX+/-)	<50	Skew. CMN minimization (balanced) & RX long cable BER improvement
	Trace symmetry		Traces should be symmetrical and of equal length to keep impedance uniformly distributed across traces.
	TX/RX pairs spacing	> 300 mil optimal; 100 mil minimum	1. Crosstalk minimization 2. If guard/ground traces are used (NOT recommended), spacing between the guard trace and the TX or RX pair, as coupling will induce impedance variations. 3. Guard trace/pair should be laid symmetrically (one for TX; the other for RX) and be equally spaced along the diff trace it guards; vias on the guard traces should also be populated symmetrically.
	Clearance to any traces (LED), ground, components (ESD cap)	> 25 mil for 1.5kV DC > 44 mil for 2.25V DC	This requirement is targeted for safety compliance
	Via budget per diff pair	<= 2	Impedance continuity

Table 10. 82562EZ LOM / Layout Checklist (Sheet 2 of 2) (Continued)

Parts	Check Items	Recommendation/ Trace Length in Mil otherwise as indicated	Remark
	Spacing between diff trace and ground shielding trace/ plane (if implemented)	> 30	Impedance matching
	Spacing between adjacent and parallel digital traces	> 100 mil minimum	1. Impedance spots, overshoot, undershoot and ringing minimization 2. If a ground isolation trace is required, care must be taken with spacing between ground isolation trace and TX or RX pair, as coupling will induce impedance variation
Bob Smith Termination Plane (if implemented)	Clearance to any traces	> 50	Prevents arcing during high-pot test
PLC I/F	Trace length	< = 10 inches	The trace spacing and loading can affect the signal integrity on PLC
	LAN_TXD and LAN_RXD trace length variation to LAN_CLK	< = 500	LAN_CLK should always be the longest trace
	Option: If RPACKsare populated, place RPACKs along LAN_RXD close to 562EZ	<= 300 mil from source to RPACK	Return lost minimization on Jordan signals. 22 or 33 OHM is recommended for the resistors.
Power and Ground Traces	Trace width to 562EZ and decoupling caps, length should be as shorter as possible (via to power plane is recommended)	> 20	Trace inductance alleviation

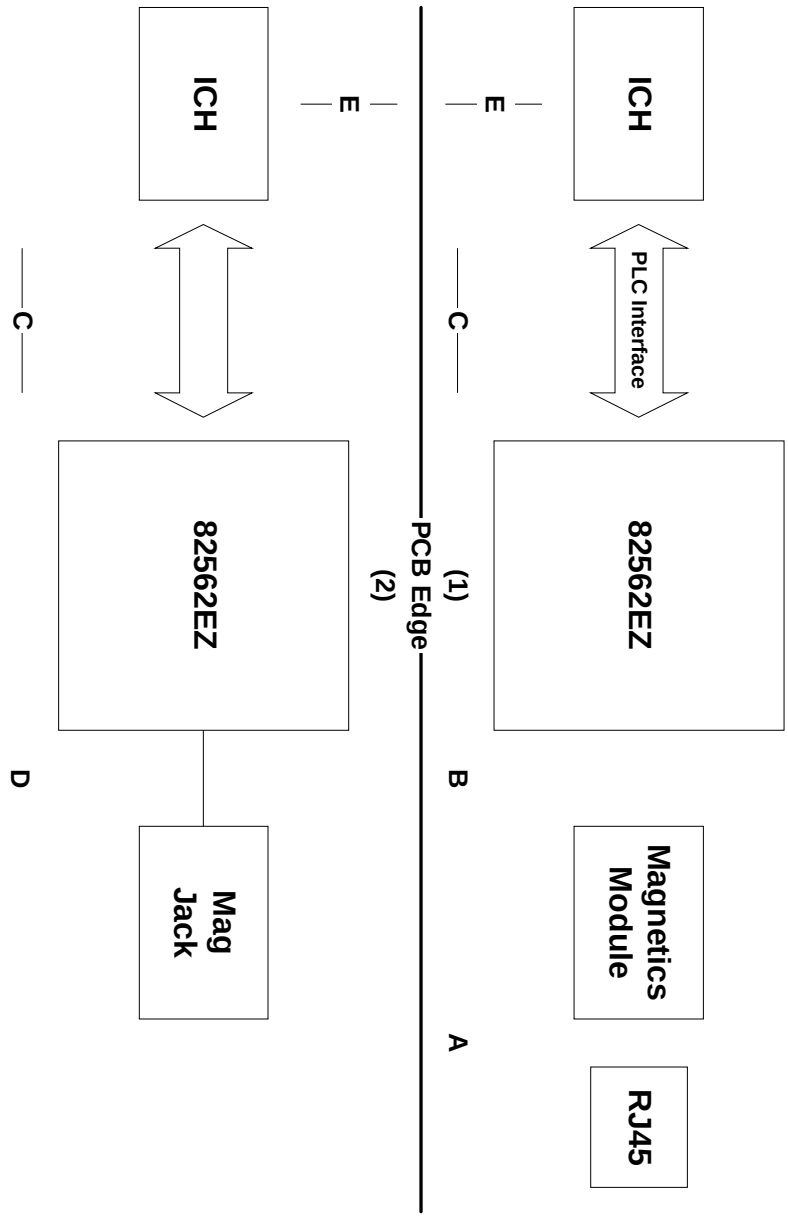


Figure 12. 82562EZ LOM / Layout Diagram

Table 11. 82562EZ LOM Schematic Checklist (Sheet 1 of 2)

Parts	Check Items	Remark
EEPROM	Model 93C46/CAT93C46/M93C46	93C46 for non-alerting / 93C66 for alterting
	Pin connections	
	VCC tiles to 3.3VSTB	
	ORG ties to 3.3VSTB for 64x16 access	
	0.1uF decoupling cap for VCC	
82562EZ	Analog Power Pins	FB Could be populated between digital and analog VCC pins
	Ground Pins	Connects to main digital GND planes
	Decoupling caps for analog power pin #G13, H11 and J11	These a re analog front end signals. Place 1 X 0.1uF caps + 1 X 4.7uF (+ 1 X 10uF or 1 X 1000pF) caps for optimal performance
	Decoupling caps for digital power pins	PLace 4 ~ 6 X 0.1uF caps + 4 X 4.7uF (4 X 10uF) caps for optimal performance Digital Power Pins connect to main digital power planes; a plane is recommended
	RBIAS10 = 549_1%; RBIAS100 = 619_1%	The resistance might be tuned to change diff output voltage. RBIAS is for 10/100Mbs. Reducing RBIAS increases output voltage
	100 _1% RESISITOR CROSS TX+/-	
	120_1% resistor cross RX+/-	120 OHMS is employed to magnify RX voltage for RXBER improvement./ 130 OHM is maximum
	ADV10/pin #41 ties to ground	
	Option 212 or 33 OHM resistor packs along PLC traces	The resistors should be placed close to the driving signals
LED Circuit	Pin connections	
	SPEEDLED is powered by 3.3VSTB	
	330 OHM resistor of LINK/ACT LED (implementation dependent)	Tune the resistance for flicker rate
	470pF cap tied to ACT LED pin at RJ45 conn	EMI filtering nearby RJ45 conn
LAN Disable Circuit	INverter is powered by 3.3VSTB	SINV will be a good implementation
	10K pull-down resistor	May be tuned to drive the inverter
	ICHx RSM_PWROK/LAN_RST# is tied to LAN_disable GPIO, but not tied to RSMRST# (or tie together via a 0 OHM resistor)	
	Option: Flexible design w/ a dummy 61K resistor (do not populate) ties to pin #21, 3x dummy resistors (do not populate) t9e to pin #28, 29, 30	

Table 11. 82562EZ LOM Schematic Checklist (Sheet 2 of 2) (Continued)

Parts	Check Items	Remark
Clock	25Mhz clock source (crystal or oscillator)	Crystal changes can result in EMI differences of +/0- 2 dB. Accuracy should be within +/- 50 ppm
	2 X 22pF cap w/ short leads (implementation dependent per vender's comment)	The capacitance will affect the accuracy that should be within +/- 50 ppm
X'mer / RJ45 Jack	Model H1012 - Strongly recommend 5 core magnetic with additional auto-transformer on the transmit path. For the magnetic specification, refer to the magnetic section in this application note	X'mer w/ better CMR characteristic could reduce common mode noise results to EMI failure. Changing magnetics modules can alter the EMI profile by as much as 2 dB.
	0.1uF lower ESR cap of RX primary side center tap	The resistor is mainly for the improvement of IEEE Bit Error Rate
	Bob Smith Termination: 4 X 75 Ohm resistors for RJ45 unused pins and wire side center taps	75 OHMS forCommon Mode Noise impedance matching on CAT5 cable
	Bob Smith Termination: 1 X EFT cap: 1500pF/2KV	The capacitor built in between termination plane and chassis ground is mainly for EMI and EFT protection.
	Option: an empty 10 - 22pF cap of TX canter tap	22pF cap might be populated if overshoot/undershoot
	0.1uF and 4.7uF sticking caps or pads cross signal and chassis ground (if implemented)	Buck cap (4.7uF, 10uF...) for providing the AC return path of low frequency signals. Decoupling cap for high frequency signals.