YAMAHA LSI

YMF278B

FM + Wave table Synthesizer LSI (OPL4)

■ OVERVIEW

The YMF278B (OPL4) is an advanced synthesizer LSI which integrates Wave Table synthesis and FM synthesis into one chip. It can generate twenty-four voices of Wave Table synthesis at a time. With wave data memory connected externally, it complies with GM System Level 1. The FM synthesis portion is register-compatible with the YMF262 (OPL3), which is a popular synthesizer LSI for IBM-PC.
With these features, this LSI (YMF278B) maintains software compatibility with applications currently in use and provides enhanced functions and higher performance when it is used in a multi-media personal computer or sound board.

■ FEATURES

- FM Synthesis (same as YMF262)
  1. Sound generation mode
     - Two-operator mode
       Generates eighteen voices or fifteen voices plus five rhythm sounds simultaneously.
     - Four-operator mode
       Generates six voices in four operator mode plus six voices in two-operator mode simultaneously, or generates six voices in four-operator mode plus three voices in two-operator mode plus five rhythm sounds simultaneously.
  2. Eight selectable waveforms.
  3. Stereo output.

- Wave Table Synthesis
  1. Generates twenty-four voices simultaneously.
  2. 44.1 kHz sampling rate for output sound data.
  3. Selectable from 8-bit, 12-bit, and 16-bit word lengths for wave data
  4. Stereo output. (16-stage panpot for each voice)

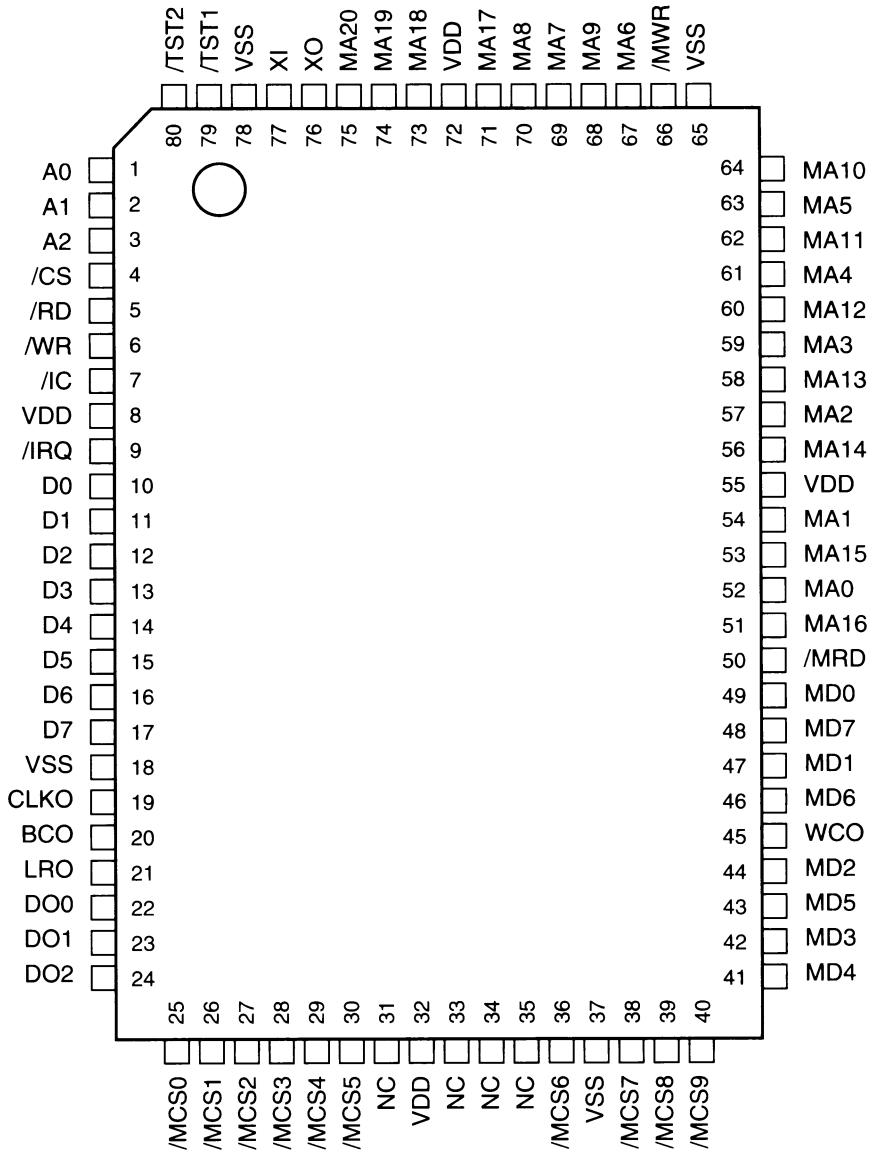
- Wave Data
  1. Accepts 32M bit external memory at maximum.
  2. Up to 512 wave tables.
  3. External ROM or SRAM can be connected. With SRAM connected, the CPU can download wave data.
  4. Outputs chip select signals for 1Mbit, 4Mbit, 8Mbit, or 16Mbit memory.
  5. Can be directly connected to the YRW801 (Wave data ROM).

- Others
  1. Has six sound output channels and can be directly connected to the YAC513 (external DAC).
  2. Can be directly connected to the YSS225 (EP), which adds various sound effects.
  3. 80-pin plastic QFP.

YAMAHA CORPORATION

YMF278 CATALOG
CATALOG No.: LSI-4MF2782
1993. 12

■ PIN OUT DIAGRAM



<80PIN QFP TopView>

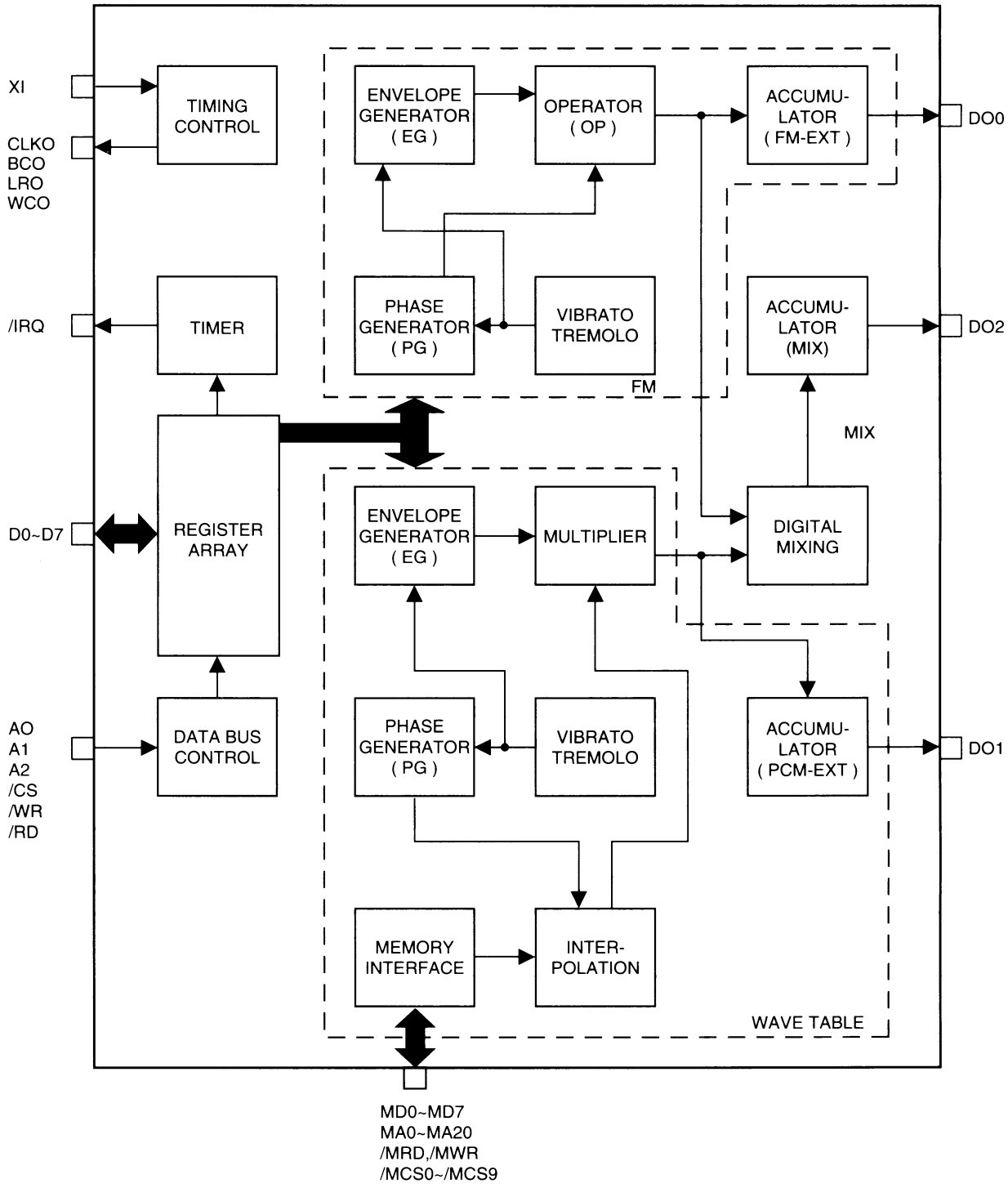
■ PIN DESCRIPTION

No.	Name	I/O	Function	
1	A0	I	CPU Interface	Address bus
2	A1	I		Address bus
3	A2	I		Address bus
4	/CS	I+		Chip select
5	/RD	I		Read enable
6	/WR	I		Write enable
7	/IC	I+	Initial clear	
8	VDD	–	+5V Power supply	
9	/IRQ	OD	CPU Interface	Interrupt
10	D0	I/O		Data bus
11	D1	I/O		Data bus
12	D2	I/O		Data bus
13	D3	I/O		Data bus
14	D4	I/O		Data bus
15	D5	I/O		Data bus
16	D6	I/O		Data bus
17	D7	I/O		Data bus
18	VSS	–	Ground	
19	CLKO	O	Clock (16.9344MHz)	
20	BCO	O	Dac Interface	Bit clock
21	LRO	O		L/R clock
22	DO0	O		FM-EXT
23	DO1	O		PCM-EXT
24	DO2	O		MIX (FM + PCM)
25	/MCS0	O	Memory Interface	Chip select
26	/MCS1	O		Chip select
27	/MCS2	O		Chip select
28	/MCS3	O		Chip select
29	/MCS4	O		Chip select
30	/MCS5	O		Chip select
31	(NC)	–		
32	VDD	–	+5V Power supply	
33	(NC)	–		
34	(NC)	–		
35	(NC)	–		
36	/MCS6	O	Memory Interface	Chip select
37	VSS	–	Ground	
38	/MCS7	O	Memory Interface	Chip select
39	/MCS8	O		Chip select
40	/MCS9	O		Chip select

No.	Name	I/O	Function	
41	MD4	I/O	Memory Interface	Data bus
42	MD3	I/O		Data bus
43	MD5	I/O		Data bus
44	MD2	I/O		Data bus
45	WCO	O	DAC Interface	Word clock
46	MD6	I/O	Memory Interface	Data bus
47	MD1	I/O		Data bus
48	MD7	I/O		Data bus
49	MD0	I/O		Data bus
50	/MRD	O		Read enable
51	MA16	O		Address Bus
52	MA0	O		Address Bus
53	MA15	O		Address Bus
54	MA1	O		Address Bus
55	VDD	–	+5V Power supply	
56	MA14	O	Memory Interface	Address Bus
57	MA2	O		Address Bus
58	MA13	O		Address Bus
59	MA3	O		Address Bus
60	MA12	O		Address Bus
61	MA4	O		Address Bus
62	MA11	O		Address Bus
63	MA5	O		Address Bus
64	MA10	O		Address Bus
65	VSS	–	Ground	
66	/MWR	O	Memory Interface	Write enable
67	MA6	O		Address Bus
68	MA9	O		Address Bus
69	MA7	O		Address Bus
70	MA8	O		Address Bus
71	MA17	O		Address Bus
72	VDD	–	+5V Power supply	
73	MA18	O	Memory Interface	Address Bus
74	MA19	O		Address Bus
75	MA20	O		Address Bus
76	XO	O	Crystal oscillator connection pin	
77	XI	I	Crystal oscillator connection pin or master clock input pin (33.8688MHz)	
78	VSS	–	Ground	
79	/TST1	I+	LSI test pin (Not connected normally)	
80	/TST2	I+	LSI test pin (Not connected normally)	

Notes) (NC), /TST1, /TST2 : These pins should normally be open.
I+ : Pin with a built-in pull-up resistor
OP : Open drain output pin

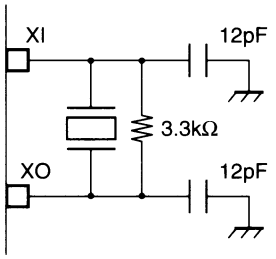
■ BLOCK DIAGRAM



■ FUNCTION OVERVIEW

1. CLOCK OSCILLATION XI, XO

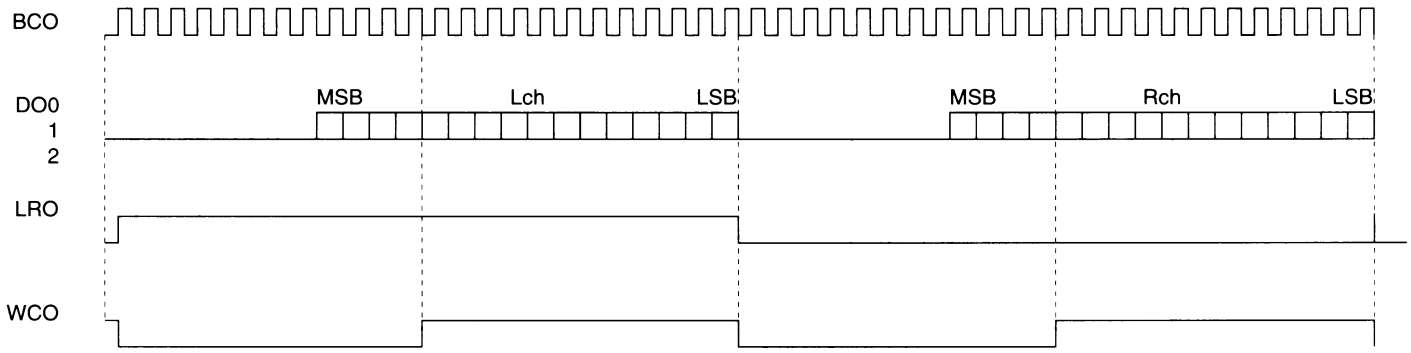
Use the XI and XO pins to construct the clock oscillation circuit.
Oscillating frequency is 33.8688MHz.
It is also possible to input an external clock to the XI pin.



2. AUDIO INTERFACE BCO, LRO, WCO, CLKO, DO0~DO2

The YMF278B output data is 16-bit 2's complement digital data.
The data is MSB first output. The sampling frequency is 44.1kHz.
The data output from each pin is shown below.

- DO0 pin: FM sound only (Sound of channel set by CHC and CHD of FM registers $C0 to C8H is output.)
- DO1 pin: Wave table sound only. (Sound of channel set at CH="1" of wave table registers $68 to 7FH is output.)
- DO2 pin: FM and wave table mixed data. (Sound of channel set by CHA and CHB of FM registers $C0 to C8H and sound of channel set at CH="0" of wave table registers $68 to 7FH are mixed and output.)



Name	Frequency	Duty
BCO	48fs	50%
LRO	fs	50%
WCO	2fs	50%

* fs=44.1kHz

3. CPU INTERFACE /CS, /RD, /WR, A0~A2, /IRQ

The OPL4 (YMF278B) is controlled by writing data to the registers. An eight-bit parallel CPU interface is provided for this purpose. D0 to D7 comprise the bi-directional data bus. /CS, /RD, /WR, A0, A1 and A2 are data bus control signal inputs.
This LSI has the modes shown below which depend on data bus control signals.

	/CS	/RD	/WR	A0	A1	A2	MODE
	H	×	×	×	×	×	Inactive mode
	L	L	H	L	L	L	Status read mode
FM	L	H	L	L	L/H	L	Address write mode
	L	H	L	H	×	L	Data write mode
PCM MIX	L	H	L	L	L	H	Address write mode
	L	H	L	H	L	H	Data write mode
	L	L	H	H	L	H	Data read mode

Note) ×: don't care

(a) Inactive mode

The data bus (D0 to D7) becomes high-impedance when /CS is high.

(b) Address write mode

In this mode, a write address (the register address in which data will be written) is specified. 56 master clock cycles (for FM) or 88 cycles (for PCM) are needed before the next write cycle or read cycle.
When register array 0 of FM is to be specified, A1 must be 'L'. When register array 1 is to be specified, A1 must be 'H'.

(c) Data write mode

In this mode, data is written in the register of the address most recently specified in the address write mode described above.
56 master clock cycles (for FM) or 88 cycles (for PCM) are needed before the next write cycle or read cycle.

(d) Data read mode

In this mode, data is read from the address most recently specified in the address write mode.

(e) Status read mode

In this mode, the contents of the Status Register are returned to the data bus.

When the interrupt signals are generated in status register, the /IRQ pin becomes 'L' and report to the CPU.

4. MEMORY INTERFACE MA0~MA20, MD0~MD7, /MWR, /MRD, /MCS0~/MCS9

External ROM or SRAM can be connected (× 8 bit, under150ns)

5. INITIAL CLEAR /IC

The YMF278B is needed initial clear.

■ REGISTERS

1-1 REGISTER TABLE FOR FM SYNTHESIS

The FM synthesis portion is register-compatible with the YMF262 (OPL3).
All register are set to '0' after a initial clear.

ADDRESS	REGISTER ARRAY 0 (A1='L')								REGISTER ARRAY 1 (A1='H')							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
00H~01H	LSI TEST								LSI TEST							
02H	TIMER 1															
03H	TIMER 2															
04H	RST	MT1	MT2				ST2	ST1			CONNECTION SEL					
05H															NEW2	NEW
08H		NTS														
20H~35H	AM	VIB	EGT	KSR	MULT				AM	VIB	EGT	KSR	MULT			
40H~55H	KSL		TL						KSL		TL					
60H~75H	AR				DR				AR				DR			
80H~95H	SL				RR				SL				RR			
A0H~A8H	F-NUMBER (L)								F-NUMBER (L)							
B0H~B8H			KON	BLOCK			F-NUM (H)				KON	BLOCK			F-NUM (H)	
BDH	DAM	DVB	RYT	BD	SD	TOM	TC	HH								
C0H~C8H	CHD	CHC	CHB	CHA	FB			CNT	CHD	CHC	CHB	CHA	FB			CNT
E0H~F5H						WS							WS			

Notes) 1. The register array 1, 05H NEW2bit is expanded from the YMF262 (OPL3) to the YMF278B (OPL4). For a detailed description of the NEW2bit, see the description of the registers.

2. Register LSI TEST and "▒▒▒" are should be written '0'.

1-2 REGISTER DESCRIPTION (FM SYNTHESIS)

Address	Name	Function
00H~01H	LSI TEST (REGISTER ARRAY0, 1)	LSI TEST is only for LSI testing.
02H	TIMER 1 (REGISTER ARRAY0)	TIMER 1 is an 8-bit programmable counter which has an 80.8μs resolution.
03H	TIMER 2 (REGISTER ARRAY0)	TIMER 2 is an 8-bit programmable counter which has a 323.1μs resolution.
04H	RST (REGISTER ARRAY0)	When set to '1' resets the /IRQ line to 'H',and clears FT1 and FT2 timer flags to '0'.
04H	MT1, MT2 (REGISTER ARRAY0)	When set to '1' masks the flag of TIMER 1 and TIMER 2.
04H	ST1, ST2 (REGISTER ARRAY0)	When set to '1' loads the value from counter of TIMER 1 and TIMER 2, and starts counting.
04H	CONNECTION SEL (REGISTER ARRAY1)	Selects four-operator mode.
05H	NEW (REGISTER ARRAY1)	When set to '1' becomes OPL3 mode.
05H	NEW2 (REGISTER ARRAY1)	When set to '1' access to PCM register and status (BUSY, LD) become possible.
08H	NTS (REGISTER ARRAY0)	Selects the keyboard split method to determine the key scale number.
20H~35H	AM (REGISTER ARRAY0, 1)	When set to '1' ampritude modulation will be applied to this operator.
20H~35H	VIB (REGISTER ARRAY0, 1)	When set to '1' turns vibrate on for the corresponding slot.
20H~35H	EGT (REGISTER ARRAY0, 1)	Selects envelope type (sustain or decay).
20H~35H	KSR (REGISTER ARRAY0, 1)	Sets the key scale rate.
20H~35H	MULT (REGISTER ARRAY0, 1)	Set the multiplier for the frequency data specified by BLOCK and F-NUMBER.
40H~55H	KSL (REGISTER ARRAY0, 1)	In acoustic musical instruments, the overall envelope volume decreases as you play higher notes. KSL are used to simulate this effect.
40H~55H	TL (REGISTER ARRAY0, 1)	Attenuation is performed according to the envelope generator output. The modulation or volume is controlled.
60H~75H	AR (REGISTER ARRAY0, 1)	This register specifies the attack rate.
60H~75H	DR (REGISTER ARRAY0, 1)	This register specifies the decay rate.
80H~95H	RR (REGISTER ARRAY0, 1)	This register specifies the release rate.

Address	Name	Function
A0H~A8H B0H~B8H	F-NUMBER (L) F-NUMBER (H) (REGISTER ARRAY0, 1)	Gives pitch data along with BLOCK data.
B0H~B8H	KON (REGISTER ARRAY0, 1)	Control the sound generation ON/OFF.
B0H~B8H	BLOCK (REGISTER ARRAY0, 1)	Generates octave data with F-NUMBER data.
BDH	DAM (REGISTER ARRAY0)	Selects amplitude modulation depth.
BDH	DVB (REGISTER ARRAY0)	Selects vibrate depth.
BDH	RYT (REGISTER ARRAY0)	Selects rhythm sound mode.
BDH	BD, SD, TOM, TC, HH (REGISTER ARRAY0)	Sound output ON/OFF switch for each sound.
C0H~C8H	CHD, CHC, CHB, CHA (REGISTER ARRAY0, 1)	Selects output channels among A, B, C and D.
C0H~C8H	FB (REGISTER ARRAY0, 1)	In every algorithm one of the operators can modulate itself.
C0H~C8H	CNT (REGISTER ARRAY0, 1)	Selects the algorithms which arrangements of operators.
E0H~F5H	WS (REGISTER ARRAY0, 1)	Selects the waveform used for carrier and modulation.

2-1 REGISTER TABLE FOR WAVE TABLE SYNTHESIS

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00H~01H	TEST							
02H	Device ID			Wave table header			Memory type	Memory access register
				2	1	0		
03H	[illegible]		Memory address register					
			A21	A20	A19	A18	A17	A16
04H	A15	A14	A13	A12	A11	A10	A9	A8
05H	A7	A6	A5	A4	A3	A2	A1	A0
06H	Memory data register							
07H	[illegible]							
08H~1FH	Wave table number							
	7	6	5	4	3	2	1	0
20H~37H	F-NUM							Wave table number
	f6	f5	f4	f3	f2	f1	f0	8
38H~4FH	Octave				REV	F-NUM		
	03	02	01	00		f9	f8	f7
50H~67H	Total level							Level direct
	6	5	4	3	2	1	0	
68H~7FH	KEY ON	DAMP	LFO RES	CH	Panpot			
					3	2	1	0
80H~97H	[illegible]			LFO		VIB		
				S2	S1	S0	V2	V1	V0
98H~AFH	AR				D1R			
	3	2	1	0	3	2	1	0
B0H~C7H	DL				D2R			
	3	2	1	0	3	2	1	0
C8H~DFH	Rate correction				RR			
	3	2	1	0	3	2	1	0
E0H~F7H	[illegible]						AM	
							2	1	0
F8H	[illegible]			Mixing control (FM-R)			Mixing control (FM-L)		
				2	1	0	2	1	0
F9H	[illegible]			Mixing control (PCM-R)			Mixing control (PCM-L)		
				2	1	0	2	1	0

Notes) 1. Be sure to set "[illegible]" and TEST register to '0'.

2. Mix control register (FM-R, FM-L) of F8H are set to 3 (–9 dB), other registers are set to '0' by intial clear.

2-2 REGISTER DESCRIPTION FOR WAVE TABLE SYNTHESIS

A voices referred to as a channel. OPL4 has 24 channels for Wave Table Synthesis in total. Register 08H-f7H (240 register) are divided into 10 groups by 24 bytes. And 24-Bytes data correspond to channel 1-24 in each group.

Address	Name	Function
00H~01H	TEST	These two registers are used for LSI testing.
02H	Memory access register	Selects sound generation mode or memory access mode.
02H	Memory type	This register represents what external memory can be connected.
02H	Wave table header	This register allows the used to specify the memory areas for the headers.
02H	Device ID	This is used for ID register.
03H-05H	Memory address register	These registers are used to specify the addresses of external memory to be written to or read from.
06H	Memory data register	Data is written to the external memory by writing to this register. Data from the external memory is read by reading this register.
08H-37H	Wave table number	The OPL4 supports a maximum of 512 Wave Tables. The header of the Wave Table is automatically loaded internally by setting the number of the Wave Table in the number register.
20H-4FH	F-NUM, Octave	These registers are used to control pitch.
38H-4FH	PSEUDO-REV	Selects Pseudo-Reverb effect ON/OFF.
50H-67H	Total level	Total level setting.
50H-67H	Level direct	This register is used to describe how the envelope level changes when total level is modified.
68H-7FH	KEY ON	Selects key on or key off.
68H-7FH	DAMP	A forced damp is enabled when this register is set to '1' in the decay state.
68H-7FH	LFO RES	This register is used to contro! LFO operation.
68H-7FH	CH	This register is used to control the output channel.
68H-7FH	Panpot	This register is used to control the panpot (so und position).
80H-97H	LFO	This register specifies the LFO speed.
80H-97H	VIB	This register specifies the vibrate depth.
98H-AFH	AR	This register specifies the attack rate.
98H-AFH	D1R	This register specifies the decay 1 rate.
B0H-C7H	DL	This register specifies the decay level.
B0H-C7H	D2R	This register specifies the decay 2 rate.
C8H-DFH	Rate correction	In this register a rate correction value is set.
C8H-DFH	RR	This register specifies the release rate.
E0H-F7H	AM	This register specifies the tremolo depth.
F8H-F9H	Mix control	These registers specifies the balance of the Mixed FM and the Mixed PCM stereo output signals.

■ STATUS REGISTER

1. SUTATUS ASSIGN

Bit assign	D7	D6	D5	D4	D3	D2	D1	D0
Status	IRQ	FT1	FT2				LD	BUSY

2. STATUS DESCRIPTION

Name	Function
BUSY	The BUSY flag is valid while NEW2='1'. This flag becomes '1' while writing address and data. BUSY flag automatically return to '0' when writing are completed.
LD (LOAD)	The LD flag is valid while NEW2='1'. When read Status Register this flag becomes '1' and output 02H after set NEW2='1'. LD flag automatically return to '0' when reading are completed. After that the LD flag becomes '1' while loading a Wave Table header. LD flag automatically return to '0' when loading are completed.
FT2 (FLAG TIMER2)	When TIMER 2 overflows, the FT2 flag becomes '1'. FT2 flag return to '0' when RST in register is set to '1'.
FT1 (FLAG TIMER1)	When TIMER 1 overflows, the FT1 flag becomes '1'. FT1 flag return to '0' when RST in register is set to '1'.
IRQ (INTERRUPT REQUEST)	When FT1 flag or FT2 flag becomes '1', the IRQ flag becomes '1'. IRQ flag return to '0' when RST in register is set to '1'.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	–0.3~7.0	V
Input voltage	V_{IN}	–0.3~V_{DD}+0.5	V
Operation temperature	T_{OP}	0~70	°C
Storage temperature	T_{STG}	–50~125	°C

2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

3. DC Characteristics (Conditions: T_a=0~70°C, V_{DD}=5.0±0.25V)

Item	Symbol	Condition	Min.	Max.	Unit
Power consumption	P_D	V_{DD}=5.0V f_M=33.8688MHz		250	mW
Input highlevel voltage (1)	V_{IH1}	*1	2.0		V
Input lowlevel voltage (1)	V_{IL1}			0.8	V
Input highlevel voltage (2)	V_{IH2}	*2	3.5		V
Input lowlevel voltage (2)	V_{IL2}			1.0	V
Input leakage current	I_{LI}	$0 \leqq V_{IN} \leqq V_{DD}$ *3	–10	10	µA
Input capacity	C_I			10	pF
Output highlevel voltage (1)	V_{OH1}	I_{OH}=–80µA *4	V_{DD}–1.0		V
Output lowlevel voltage (1)	V_{OL1}	I_{OL}=2mA		V_{SS}+0.4	V
Output highlevel voltage (2)	V_{OH2}	I_{OH}=–160µA *5	V_{DD}–1.0		V
Output lowlevel voltage (2)	V_{OL2}	I_{OL}=4mA		V_{SS}+0.4	V
Output capacity	C_O			10	pF
Output leakage current	I_{LO}	/CS=V_{IH} *6	–10	10	µA
Pull-up resistance	R_U	*7	50	400	kΩ

Notes) *1: Applied to /WR, /RD, /CS, A0~A2, D0~D7, MD0~MD7
*2: Applied to /TST1, /TST2, XI
*3: Applied to /WR, /RD, /CS, A0~A2, D0~D7, MD0~MD7
*4: Applied to D0~D7, CLKO, BCO, LRO, WCO, DO0~DO2, /MWR, /MRD, MD0~MD7 (when used as output pin)
*5: Applied to MA0~MA20, /MCS0~/MCS13
*6: When D0~D7 are in high impedance
*7: Applied to /CS, /IC, /TST1, /TST2

4. AC Characteristics (Conditions : T_a=0~70°C, V_{DD}=5.0±0.25V)

(1) Clock and reset

Item	Symbol	Figure	Min.	Typ.	Max.	Unit
Master clock frequency	f_{M1}	Fig1-1		33.8688		MHz
Master clock duty	D		40		60	%
Output clock frequency	f_{M2}	Fig1-2		16.9344		MHz
Output clock duty	D			50		%
Reset pulse width	N_{ICW}	Fig1-3	3000			cycle*1

Note) *1: Master clock cycle

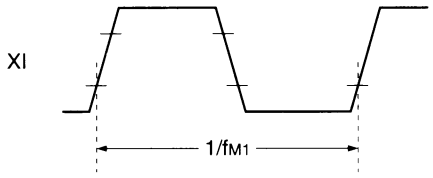


Fig1-1 Input clock timing

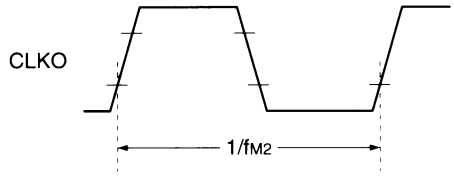


Fig1-2 Output clock timing

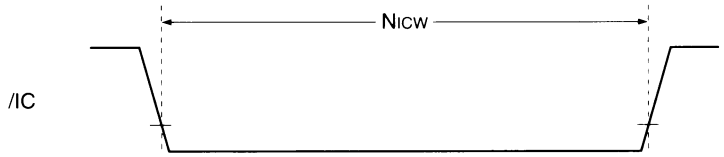
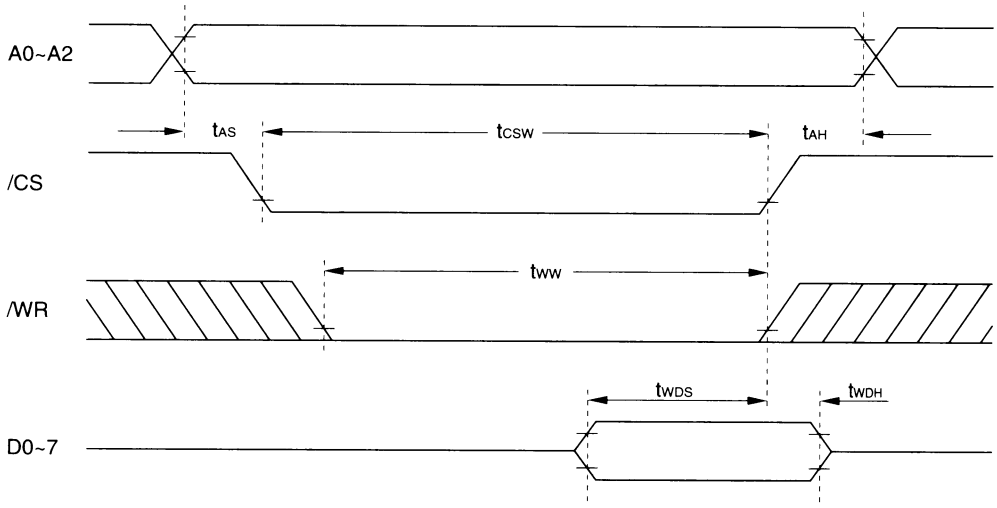


Fig1-3 Reset timing

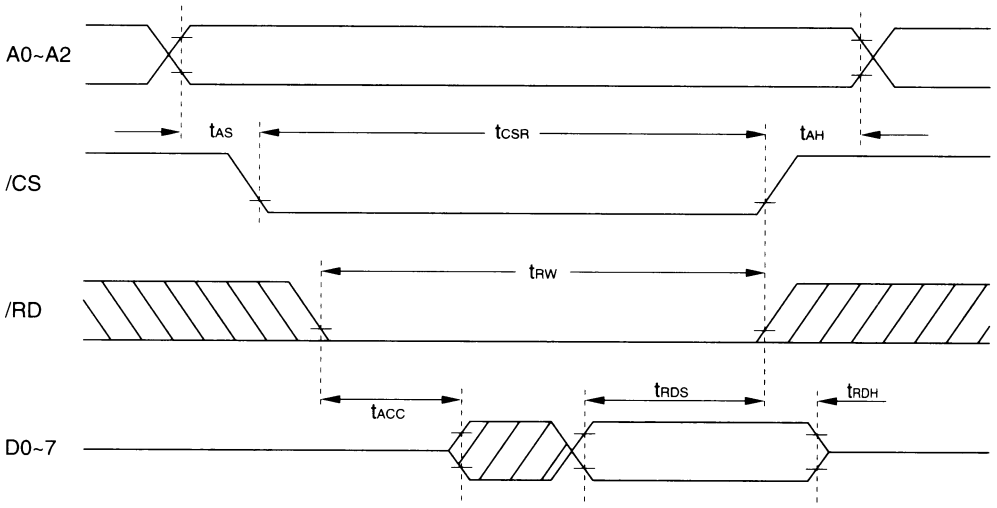
(2) CPU interface

Item	Symbol	Figure	Min.	Typ.	Max.	Unit
Address setup time	t_{AS}	Fig1-4, 5	5			ns
Address hold time	t_{AH}	Fig1-4, 5	5			ns
Chip select write width	t_{CSW}	Fig1-4	50			ns
Chip select read width	t_{CSR}	Fig1-5	80			ns
Write pulse width	t_{WW}	Fig1-4	50			ns
Write data setup time	t_{WDS}	Fig1-4	10			ns
Write data hold time	t_{WDH}	Fig1-4	10			ns
Read pulse width	t_{RW}	Fig1-5	80			ns
Read data access time	t_{ACC}	Fig1-5			60	ns
Read data hold time	t_{RDH}	Fig1-5	10			ns



Note)
tCSW, tWW, and tWDH are based on either $\overline{CS}$ or $\overline{WR}$ being driven to high level.

Fig1-4 CPU write timing



Note)
tACC is based on whichever of $\overline{CS}$ or $\overline{RD}$ goes to the low level last.

tCSW, tWW, and tWDH are based on either $\overline{CS}$ or $\overline{WR}$ being driven to high level.

Fig1-5 CPU read timing

(3) Audio interface

Item	Symbol	Min.	Typ.	Max.	Unit
Bit clock frequency	f_{BC}		48f_S		MHz
Bit clock H level time	t_{CH}	110			ns
Data output setup time	t_{DOS}	100			ns
Data output hold time	t_{DOH}	300			ns
LR clock setup time	t_{LRS}	100			ns
LR clock hold time	t_{LRH}	300			ns
Wold clock hold time	t_{WCH}	300			ns

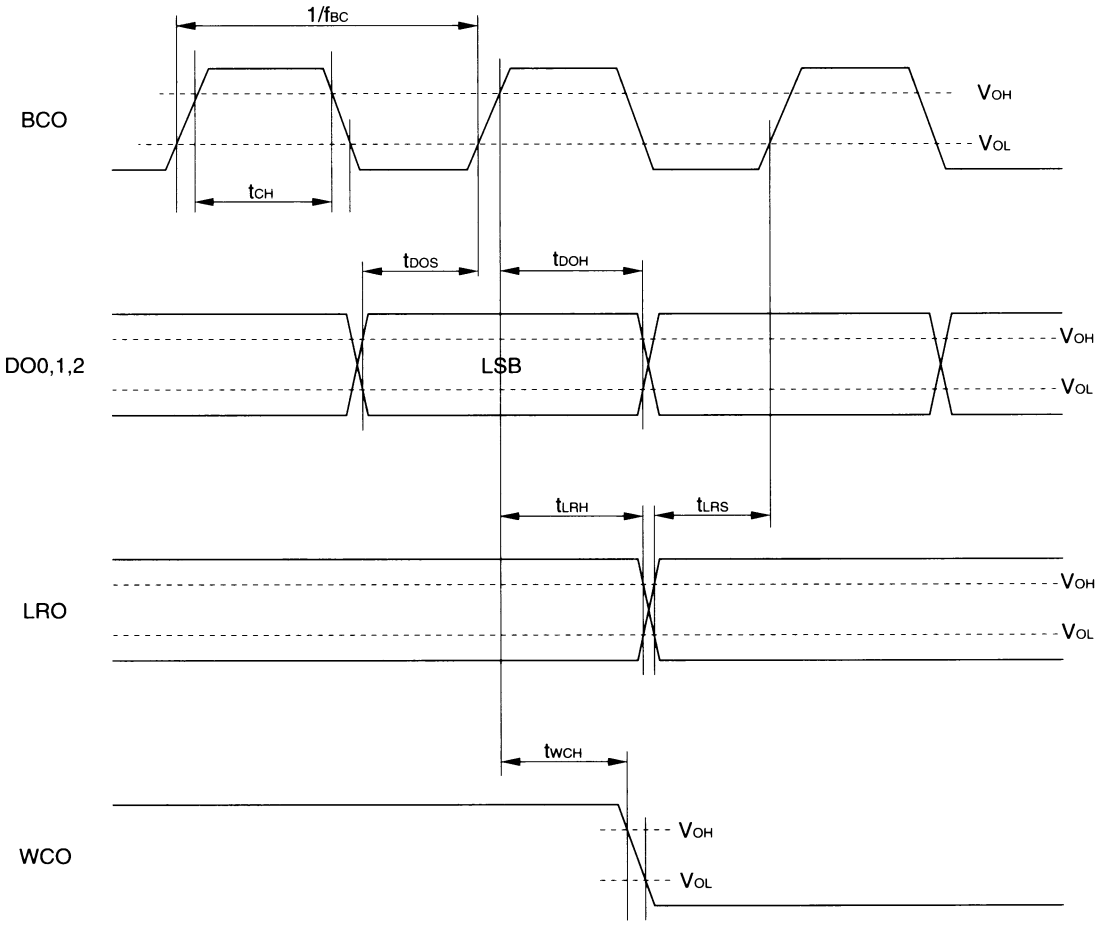


Fig1-6 Audio output timing

(4) Memory interface

Item	Symbol	Fig.	Min.	Typ.	Max.	Unit
Write cycle time	t_{WC}	Fig 1-7	600			ns
Address confirmation time for /MWR	t_{AW}	Fig 1-7	500			ns
/MCS confirmation time for /MWR	t_{CW}	Fig 1-7	450			ns
Write address set-up time	t_{WAS}	Fig 1-7	250			ns
Write recovery time	t_{WR}		50			
Write pulse width	t_{WW}	Fig 1-7	150			ns
Write data set-up time	t_{WDS}	Fig 1-7	150			ns
Write data hold time	t_{WDH}	Fig 1-7	5			ns
Address access time	t_{RC}	Fig 1-8			150	ns
Chip enable access time	t_{CE}	Fig 1-8			150	ns
Output disable time	t_{DF}	Fig 1-8			90	ns
Read data hold time	t_{RDH}	Fig 1-8	0			ns

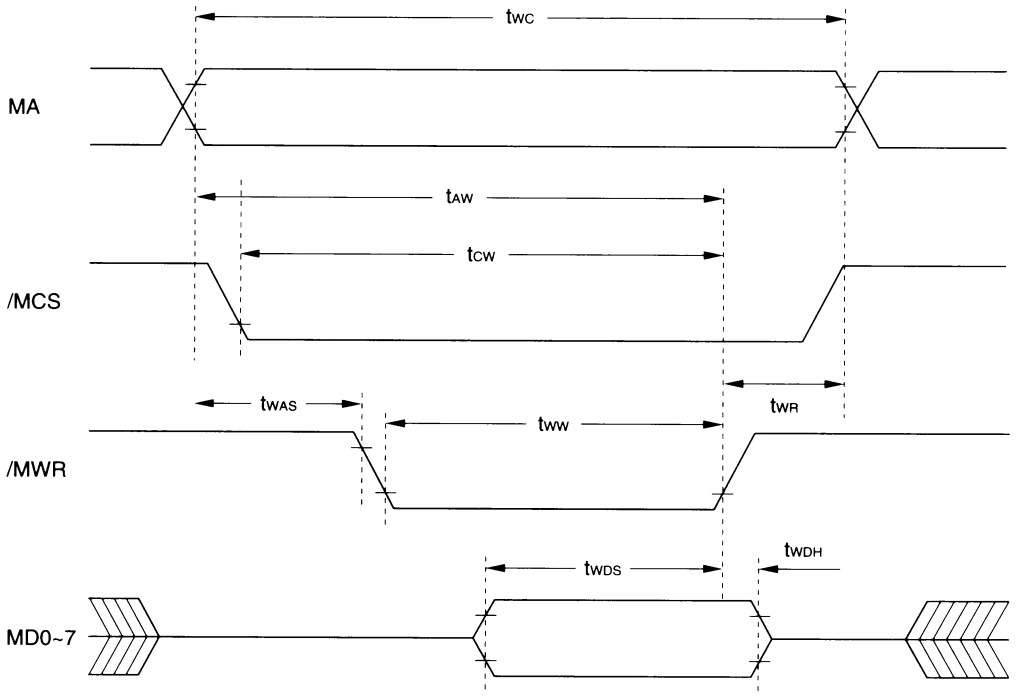


Fig1-7 Memory write timing

Note) The values above are the values when the write wait cycle time was secured.

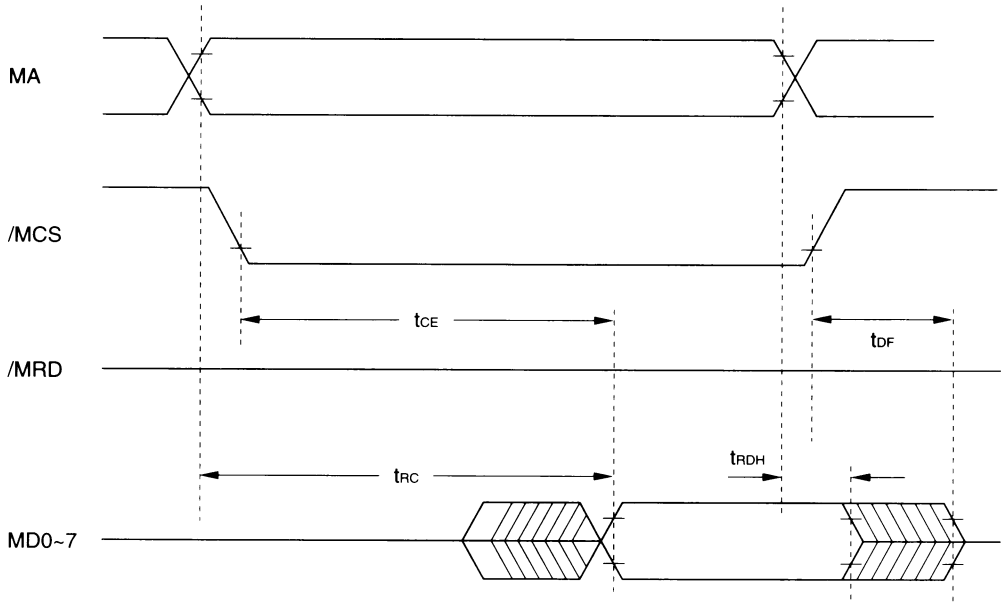


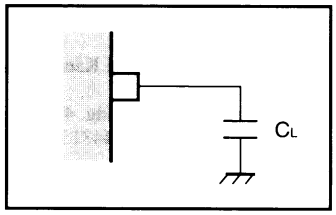
Fig1-8 Memory read timing

Note) *1: The read timing above is the memory read timing at sound generation.
*2: The /MRD signal is always "L".

(5) AC characteristics test conditions

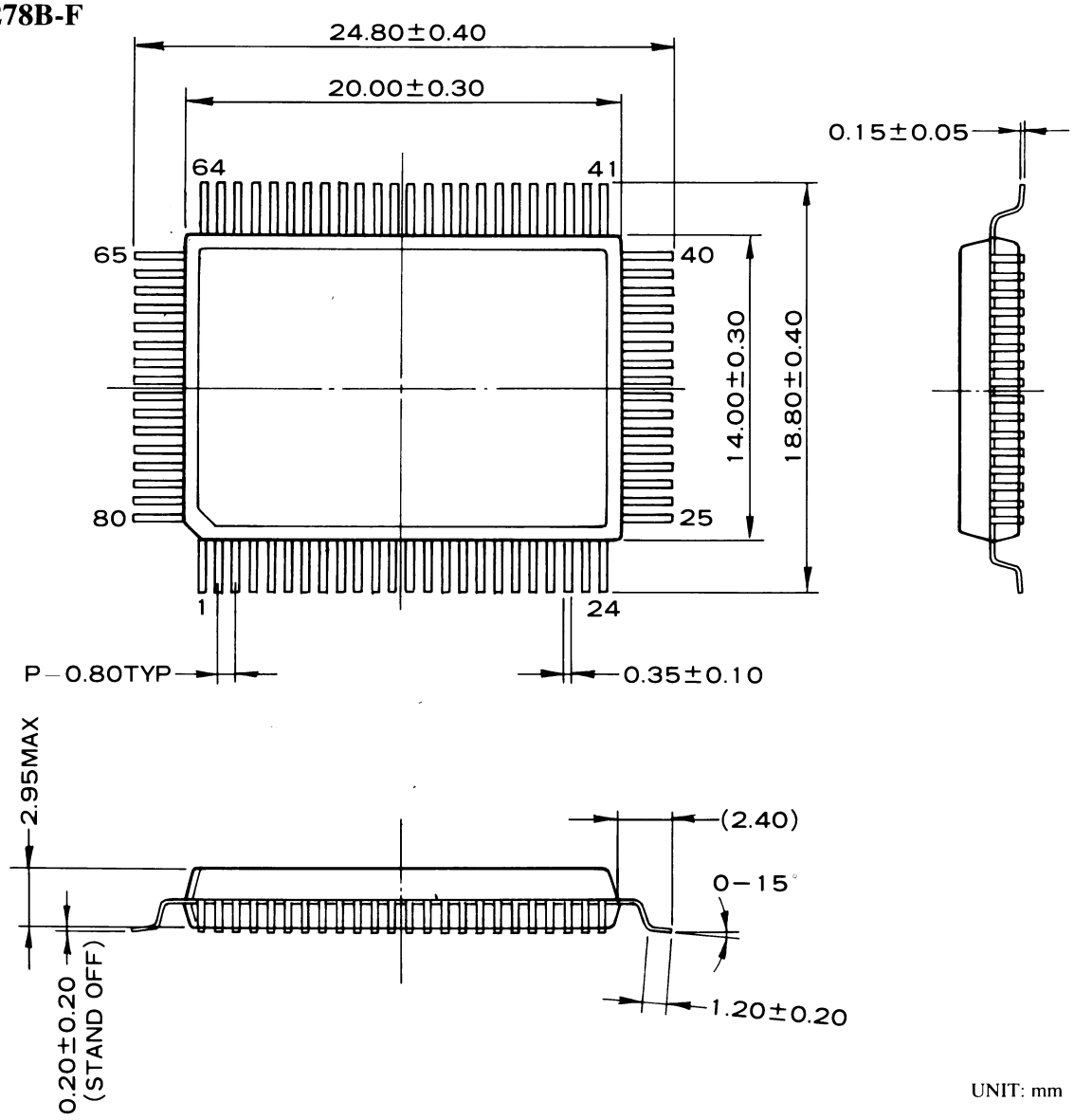
Item	
Input pulse voltage	V_{IH} = 2.4V V_{IL} = 0.4V (except XI, /TST1, /TST2) V_{IH} = 3.9V V_{IL} = 0.6V (XI, /TST1, /TST2)
Input pulse rise and fall times	t_{RF} = 5 ns
Timing measurement reference voltage	V_{OH} = 0.7✱V_{DD} V_{OL} = 0.2✱V_{DD} (CLKO, BCO, LRO, WCO, DO0~2)
	V_{OH} = 2.2V V_{OL} = 0.8V (D0~D7, MA0~20, /MCS0~9, MD0~7, /MWR, /MRD)
Output load	C_L = 100pF

- Output load circuit



■ EXTERNAL DIMENSIONS

YMF278B-F



UNIT: mm

The specifications of this product are subject to improvement changes without prior notice.

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