YAMAHA® LSI

OPL4
YMF278B

APPLICATION MANUAL

FM+WAVE TABLE SYSTHESIZER

YAMAHA

YMF278B APPLICATION MANUAL
CATALOG No. : -LSI 6MF2782
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OVERVIEW

The YMF278B (OPL4) is a synthesizer LSI which integrates Wave Table synthesis and FM synthesis into one chip. It can generate 24 voices of Wave Table synthesis at one time. With wave data memory connected externally, it complies with GM System Level 1.
The FM synthesizer portion is register-compatible with the YMF262 (OPL3), which is a popular synthesizer LSI for IBM-PC.
With these features, this LSI (YMF278B) maintains software compatibility with applications currently in use and provides enhanced functions and higher performance when it is used in a multi-media personal computer (MPC) or sound board.
The YRW801 is also available as a Wave Table synthesis waveform data ROM.

FEATURES

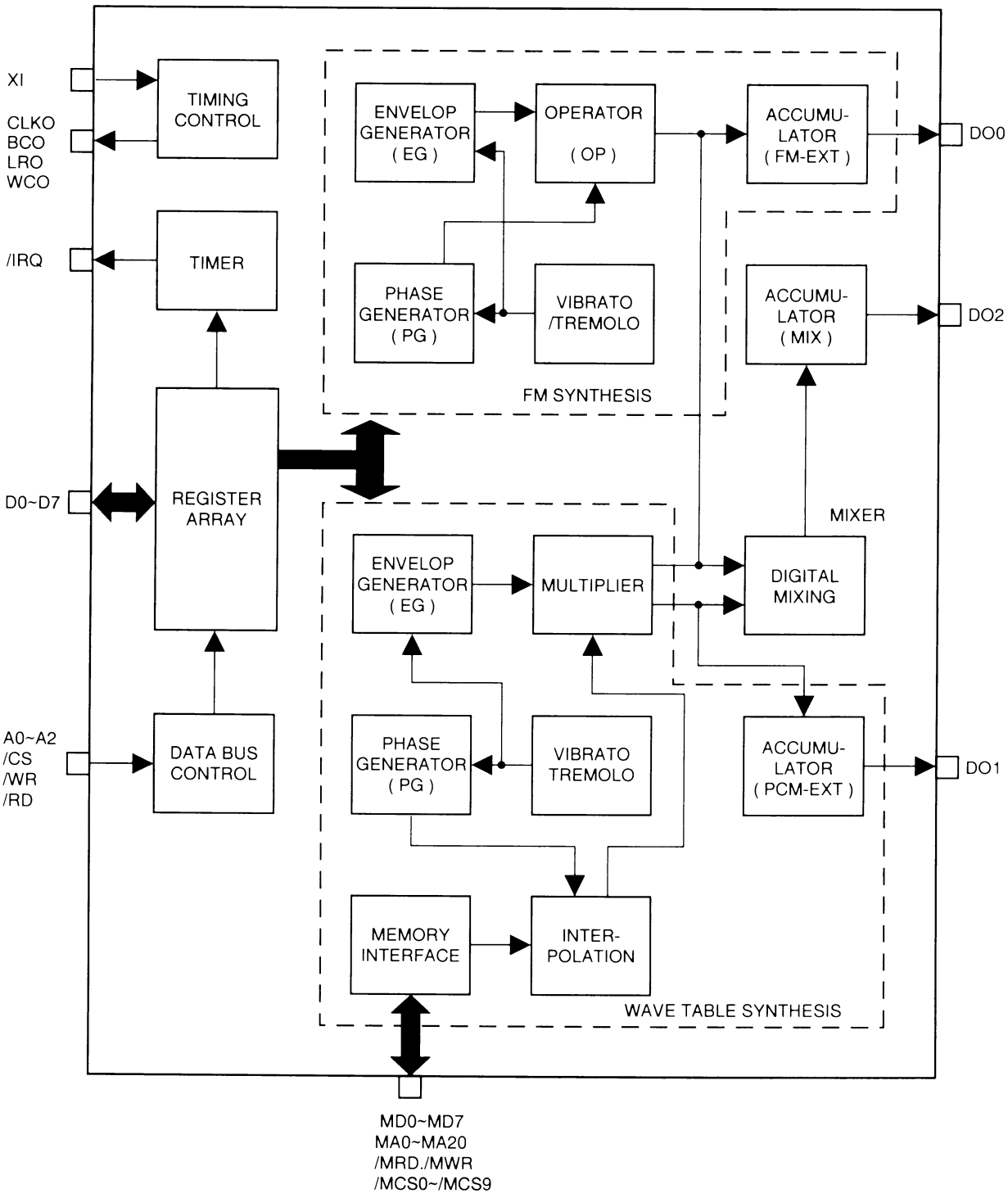
■ FM synthesis (same as YMF262)
1. Sound generation mode
   - Two-operator mode
     Generates eighteen voices in two operator modes or fifteen voices plus five rhythm sounds in two operator modes simultaneously.
   - Four-operator mode
     Generates six voices in four operator modes plus six voices in two operator modes or six voices in four operator modes plus three voices plus five rhythm sounds in two operator modes simultaneously.
2. Eight selectable waveforms.
3. Stereo output.

■ Wave Table Synthesis
1. Generates twenty-four voices simultaneously.
2. 44.1kHz sampling rate for output sound data.
3. Selectable from 8-bit , 12-bit, and 16-bit word lengths for wave data.
4. Stereo output. (16-stage panpot for each voice)

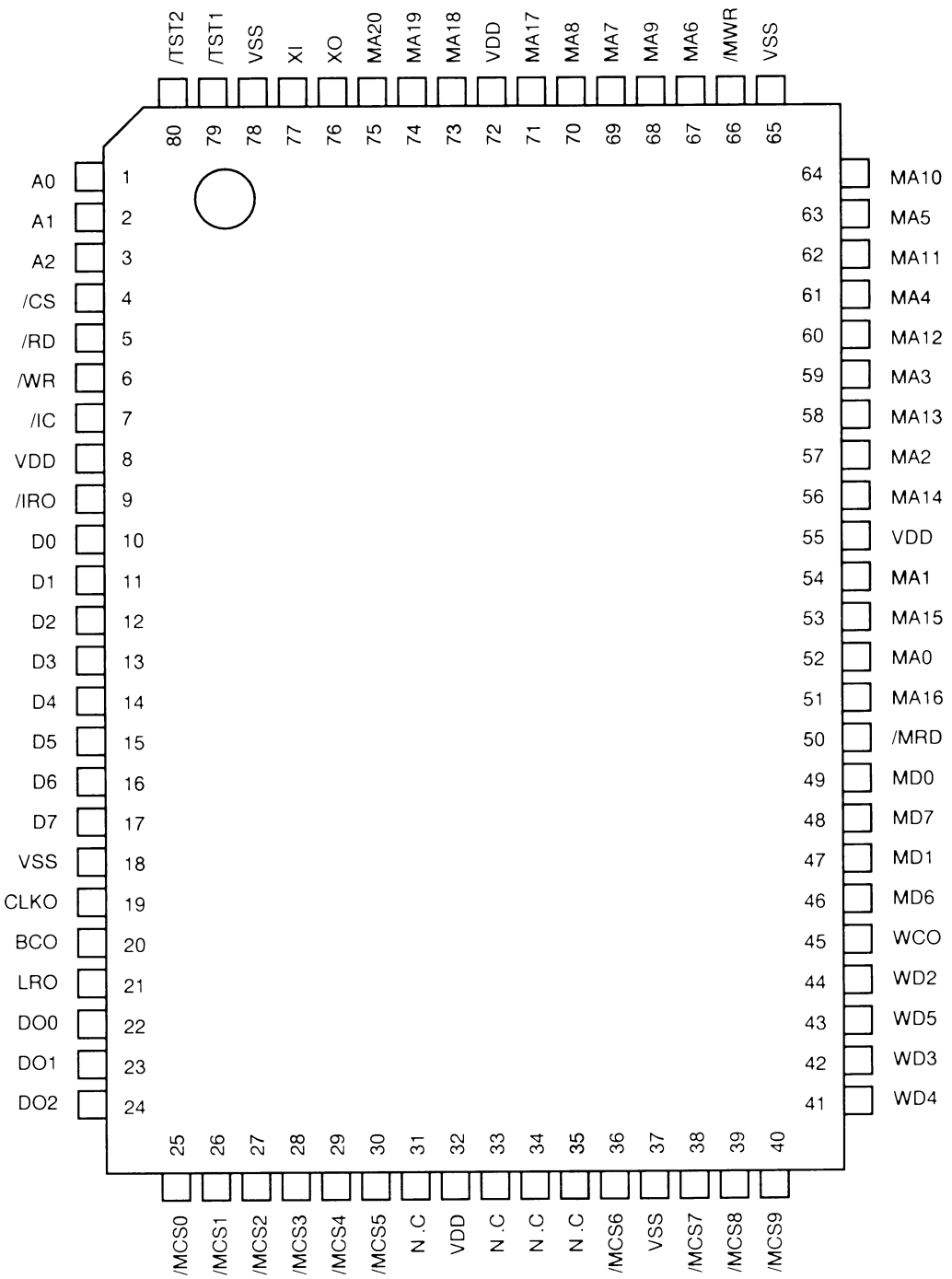
■ Wave Data
1. Accepts 32M bits external memory at maximum.
2. Up to 512 wave tables.
3. External ROM or SRAM can be connected. With SRAM connected, the CPU can download wave data.
4. Outputs chip select signals for 1Mbit, 4Mbit, 8Mbit, or 16Mbit memory.

■ Others
1. Has six sound output channels and can be directly connected to the YAC513 (external DAC).
2. Can be connected directly to the YSS225 (EP), which adds various sound effects.
3. 80-pin QFP package.

BLOCK DIAGRAM



PIN LAYOUT



< 80pin QFP Top View >

DESCRIPTION OF PIN FUNCTIONS

No	I/O	Pin Name	Function
1	I	A0	CPU interface address 0
2	I	A1	CPU interface address 1
3	I	A2	CPU interface address 2
4	I+	/CS	CPU interface chip select
5	I	/RD	CPU interface read enable
6	I	/WR	CPU interface write enable
7	I+	/IC	Initial clear
8	–	VDD	+5V power supply
9	OD	/IRQ	CPU interface interrupt
10	I/O	D0	CPU interface data bus
11	I/O	D1	CPU interface data bus
12	I/O	D2	CPU interface data bus
13	I/O	D3	CPU interface data bus
14	I/O	D4	CPU interface data bus
15	I/O	D5	CPU interface data bus
16	I/O	D6	CPU interface data bus
17	I/O	D7	CPU interface data bus
18	–	VSS	Ground
19	O	CLKO	Clock output (16.9344MHz)
20	O	BCO	Audio interface bit clock output
21	O	LRO	Audio interface L/R clock output
22	O	DO0	Audio interface FM-EXT output
23	O	DO1	Audio interface PCM-EXT output
24	O	DO2	Audio interface MIX (FM+PCM) output
25	O	/MCS0	Chip select for external memory 0
26	O	/MCS1	Chip select for external memory 1
27	O	/MCS2	Chip select for external memory 2
28	O	/MCS3	Chip select for external memory 3
29	O	/MCS4	Chip select for external memory 4
30	O	/MCS5	Chip select for external memory 5

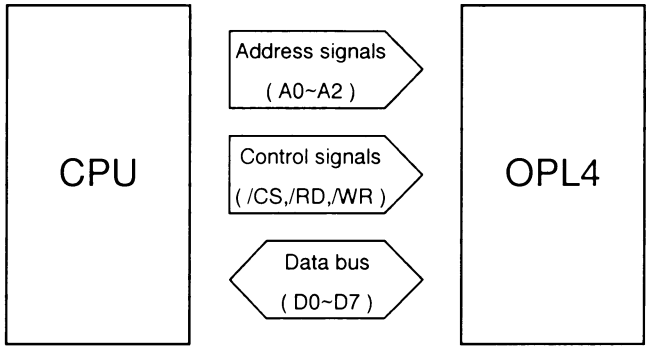
No	I/O	Pin Name	Function
31	–	N.C	No connection
32	–	VDD	+5V power supply
33	–	N.C	No connection
34	–	N.C	No connection
35	–	N.C	No connection
36	O	/MCS6	Chip select for external memory 6
37	–	VSS	Ground
38	O	/MCS7	Chip select for external memory 7
39	O	/MCS8	Chip select for external memory 8
40	O	/MCS9	Chip select for external memory 9
41	I/O	MD4	External memory data bus
42	I/O	MD3	External memory data bus
43	I/O	MD5	External memory data bus
44	I/O	MD2	External memory data bus
45	O	WCO	Audio interface word clock output
46	I/O	MD6	External memory data bus
47	I/O	MD1	External memory data bus
48	I/O	MD7	External memory data bus
49	I/O	MD0	External memory data bus
50	O	/MRD	External memory read enable
51	O	MA16	External memory address bus
52	O	MA0	External memory address bus
53	O	MA15	External memory address bus
54	O	MA1	External memory address bus
55	–	VDD	+5V power supply
56	O	MA14	External memory address bus
57	O	MA2	External memory address bus
58	O	MA13	External memory address bus
59	O	MA3	External memory address bus
60	O	MA12	External memory address bus

No	I/O	Pin Name	Function
61	O	MA4	External memory address bus
62	O	MA11	External memory address bus
63	O	MA5	External memory address bus
64	O	MA10	External memory address bus
65	–	VSS	Ground
66	O	/MWR	External memory write enable
67	O	MA6	External memory address bus
68	O	MA9	External memory address bus
69	O	MA7	External memory address bus
70	O	MA8	External memory address bus
71	O	MA17	External memory address bus
72	–	VDD	+5V power supply
73	O	MA18	External memory address bus
74	O	MA19	External memory address bus
75	O	MA20	External memory address bus
76	O	XO	Crystal oscillator connection pin
77	I	XI	Crystal oscillator connection pin or master clock input pin (33.8688MHz)
78	–	VSS	Ground
79	I+	/TST1	LSI test pin (Not connected normally)
80	I+	/TST2	LSI test pin (Not connected normally)

Notes: N.C., /TST1, /TST2: These pins should normally be open.
I+: Pin with built-in pull-up resistor
OD: Open drain output pin

CPU INTERFACE

A sketch of the CPU interface is shown below.



Sound generation is controlled by writing data to the registers.
An 8-bit parallel CPU interface is provided for this purpose.
A0 to A2 are address signals and D0 to D7 comprise the bi-directional data bus. /CS, /RD/ and /WR are control input signals.
This LSI has the modes shown below which depend on these input signals.

	/CS	/RD	/WR	A0	A1	A2	MODE
	H	×	×	×	×	×	Inactive mode
	L	L	H	L	L	L	Status read mode
FM	L	H	L	L	L/H	L	Address write mode
	L	H	L	H	×	L	Data write mode
PCM MIX	L	H	L	L	L	H	Address write mode
	L	H	L	H	L	H	Data write mode
	L	L	H	H	L	H	Data read mode

× : Don't Care

- Inactive mode
  The data bus (D0 to D7) becomes high-impedance when /CS is high.

- Address write mode
  In this mode, a write address is specified.
  Set the register address onto this data bus.
  To write or read data after the address is written, a master clock wait of
    FM register .....56 cycles
    PCM, MIX register ....88 cycles *
  is necessary.
  When register array 0 of FM is to be specified, A1 must be L. When register array 1 is to be specified, A1 must be H.

- Data write mode
  In this mode, data is written to the address set in the address write mode.
  Set the set data onto the data bus.
  56 master clock cycles (for FM) or 88 cycles (for PCM) are needed before the next address or data write cycle. *

- Data read mode
  In this mode, data is read from the address set in the address write mode.
  PCM and MIX register can be read. (FM register can't be read.)

- Status read mode
  In this mode, the status of this LSI is output. The status information is output on the data bus.

* Address setting (PCM registers $03H to 05H) to external memory and external memory data write/read wait time is different from these values.
See the description of each register for more information.

STATUS REGISTER

The structure of the status register is shown at the right.

D7	D6	D5	D4	D3	D2	D1	D0
IRQ	**FT1**	**FT2**				**LD**	**BUSY**

■ FT1, FT2, IRQ

The flags for the two timers built into the YMF278B are set in accordance with the set cycle. The CPU can read these flags by status information and interrupt signal. These timers can be used as the tempo counter, etc.

- FT1 (Flag Timer1): Timer 1 flag
  This bit becomes "1" when the time set at timer 1 is counted.
  It is reset when the RST bit of FM register $04H is set to "1".

- FT2 (Flag Timer2): Timer 2 flag
  This bit becomes "1" when the time set at timer 2 is counted.
  Similar to FT1, it is reset when the RST bit is set to "1".

- IRQ (Interrupt ReQuest): Interrupt request flag
  This bit becomes "1" when FT1 or FT2 becomes "1".
  It is reset when the RST bit is set to "1".

■ BUSY

- This flag becomes valid after the 05H_NEW2 bit of FM register array 1 is set to "1". (When NEW2 is "0", the BUSY flag is always "0".)

- This LSI requires a wait time at register access.
  The BUSY bit is provided as the flag that inhibits register access.
  When the BUSY flag is "1", do not execute a write or read operation, otherwise a malfunction may occur.

- The BUSY flag remains "1" while addresses and data are being written. It is automatically reset to "0" when writing is complete.
  Confirm that the BUSY flag is "0" before accessing a register.

■ LD (LOAD)

- This flag becomes valid after the 05H_NEW2 bit of FM register array 1 is set to "1". (When NEW2 is "0", this flag is always "0".)

- At the wave table synthesizer, the wave table header data from external memory is loaded into OPL4 by writing the wave table number to the register. During this time, access to some of the registers of that channel is inhibited.
  (Please see the section "PCM registers $08H to 2FH wave table number" for more information.)
  LD remains "1" while the header data is being loaded (approximately 300μs).

■ The first value of the status regester. (Device ID)

- When the status is read after initialization at OPL2, 06H (D1 and D2 bit="1") is output. For OPL3, 00H is read.
  For the YMF278B, when the status is read after NEW2 was set to "1", 02H is output. After reading, this bit is reset.
  However, 02H is read only once after initialization.
  The device ID register can be used as LSI identifier.

OVERVIEW OF WAVE TABLE SYNTHESIS

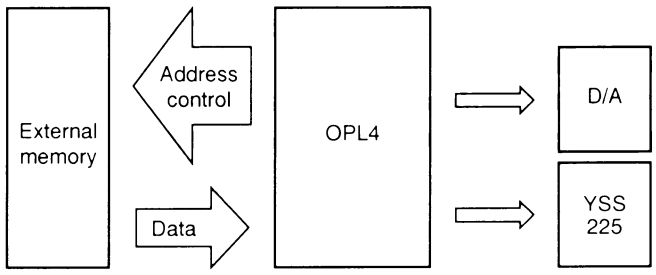
■ Features

FM synthesis can generate a wide range of sounds, from the sounds of natural musical instruments to electronic sound, depending on the setting of the operators and the algorithm form. However, it is limited near the sound of natural musical instruments.

In simple terms, wave table synthesis plays back external memory sampled data and can therefore faithfully reproduce the sounds of natural musical instruments.
Of course, it is not limited to the sounds of natural musical instruments, but can also faithfully reproduce any sound as long as sampling data is available.

■ Wave table synthesis block diagram

The wave table synthesis block diagram is shown below.



□ External memory

This block stores the sampled data and the information (start and end addresses, envelop data, etc.) needed to generate sounds.

□ OPL4

This block outputs the external memory address and control signals and reads the memory data and generates sounds from the sampled data.
Of course, envelop and pitch, level control, and various sound effects (vibrato and tremolo, panpot, etc.) can be added in OPL4.

OPL4 handles 8, 12, and 16 bit sampling data. The sampling frequency is 44.1kHz. Therefore, playback at CD quality is possible.

□ D/A converter and effect processor (YSS225)

The D/A converter converts the 16-bit, 44.1kHz digital data output from the OPL4 to analog data. An effect processor (YSS225), which can add reverberation, echo, flange, and other sound effects, is also available.
Higher quality playback is possible by connecting this LSI to it.

Since the OPL4 can digitally mix FM and wave table sounds, sounds over a wide wave table range, from sounds unique to FM to the sound of natural musical instruments, can be generated. Up to 44 sounds can be generated simultaneously as well. More advanced functions and higher quality than the OPL3 multi-media sound synthesizer are possible.

WAVE TABLE FOR WAVE TABLE SYNTHESIS AND MIXING

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
00~01H	LSI TEST							
02H	Device ID			Wave table header			Memory type	Memory access mode
03H			Memory address register					
04H	Memory address register							
05H	Memory address register							
06H	Memory data register							
07H								
08H~ 1FH	Wave table number							
	N7	N6	N5	N4	N3	N2	N1	N0
20H~ 37H	F_NUMBER							Wave table number
	f6	f5	f4	f3	f2	f1	f0	8
38H~ 4FH	Octave				Pseudo -reverb	F-NUMBER		
	O3	O2	O1	O0		f9	f8	f7
50H~ 67H	Total level							Level direct
	L6	L5	L4	L3	L2	L1	L0	
68H~ 7FH	KEY ON	DAMP	LFO RST	CH	Panpot			
					3	2	1	0
80H~ 97H			LFO			VIB		
			S2	S1	S0	V2	V1	V0
98H~ AFH	AR				D1R			
	3	2	1	0	3	2	1	0
B0H~ C7H	DL				D2R			
	3	2	1	0	3	2	1	0
C8H~ DFH	Rate correction				RR			
	3	2	1	0	3	2	1	0
E0H~ F7H						AM		
						2	1	0
F8H			Mixing control (FM_R)			Mixing control (FM_L)		
F9H			Mixing control (PCM_R)			Mixing control (PCM_L)		

Notes:

1. These registers cannot be accessed unless the NEW2 bit of the FM register is set to "1".
2. LSI TEST are used for factory testing. Always set them to "0" for normal operation.
3. After initialization, the F8H FM_MIX register is made -9dB as the default value. The other registers are cleared.
4. [ ] not used by the YMF278B may be used to expand the functions. Therefore, always set them to "0".

CHANNEL

- Channel number
  The wave table synthesizer can generate up to 24 sounds simultaneously.
  Each sound is referred to as a "channel". The channels are numbered from 1 to 24. These numbers are called "channel numbers".

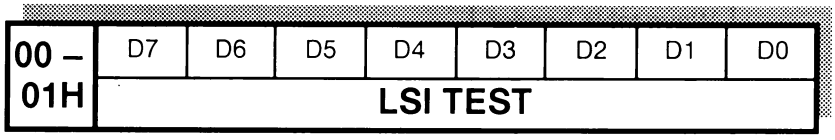
- Relation between channel and register
  As can be seen from the register table, registers 08 to 1FH and 20 to 37H have 24 addresses. These addresses correspond to channels 1 to 24.

  Set the register corresponding to each channel.

REGISTERS (WAVE TABLE SYNTHESIZER)

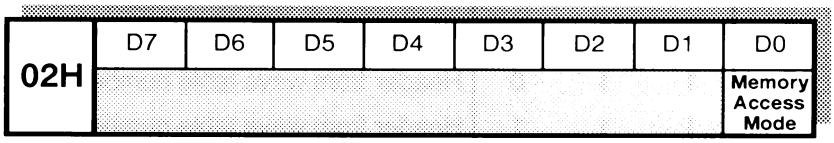
■ 00-01H LSI TEST

These registers are used for LSI testing.
All the bits should be set left at "0" for normal operation.



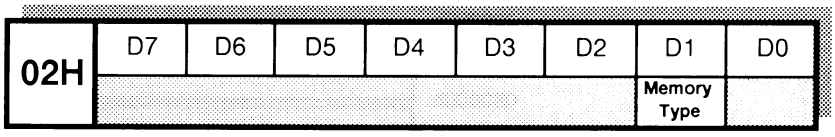
■ 02H MEMORY ACCESS MODE

When set to "0", this is the normal sound generation mode.
When set to "1", the CPU can read and write data to and from the external memory.
All the channels can not generate the sound in this mode.



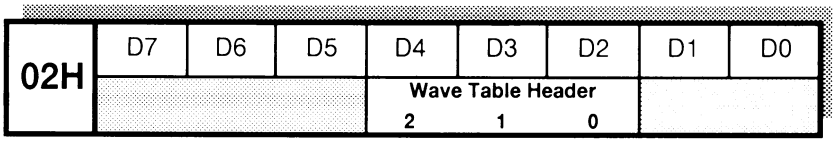
■ 02H MEMORY TYPE

This register represents what external memory can be connected.
When set to "0", ROM only.
When set to "1", SRAM plus ROM.
For a description of the external memory connection method, see the section "Connection to External Memory".



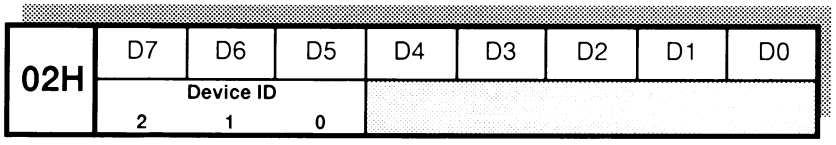
■ 02H WAVE TABLE HEADER

The wave table header must be set from external memory address 0 for wave table numbers 0 to 383 of wave tables 0 to 511.
(For a description of the header structure, see the section "external Memory Data Format".)
When bits D2, D3, and D4 are all "0", specify all 512 headers from external memory address 0.



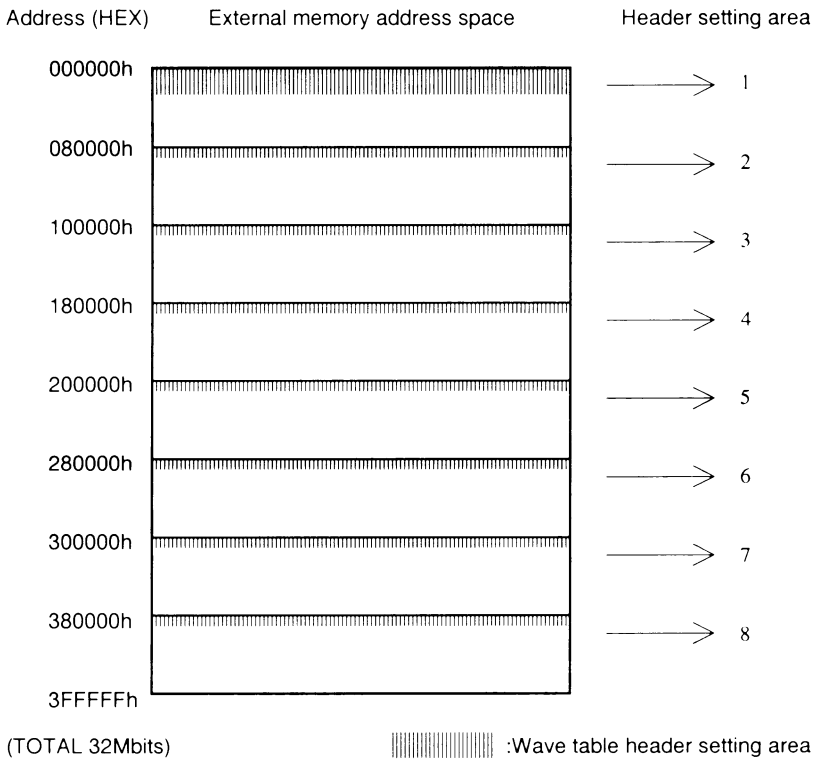
■ 02H DEVICE ID

When this register is read, 20H (D5="1", D6="0", D7="0") is output.
This register can be used as ID register of OPL4.



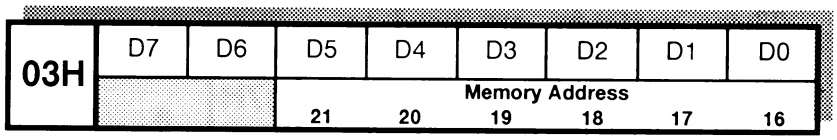
The external memory setting area for the wave table headers from wave table numbers 384 to 511 can be changed in 4Mbit segments.
The header setting areas corresponding to wave header bits 0 to 2 are shown in the table below.

Wave table header D4	D3	D2	Header set external memory area	Fig.
0	0	0	Header from wave table number 0 to 511 set from address 0	1
0	0	1	Header from wave table number 384 to 511 set from 4Mbit area	2
0	1	0	Header from wave table number 384 to 511 set from 8Mbit area	3
0	1	1	Header from wave table number 384 to 511 set from 12Mbit area	4
1	0	0	Header from wave table number 384 to 511 set from 16Mbit area	5
1	0	1	Header from wave table number 384 to 511 set from 20Mbit area	6
1	1	0	Header from wave table number 384 to 511 set from 24Mbit area	7
1	1	1	Header from wave table number 384 to 511 set from 28Mbit area	8

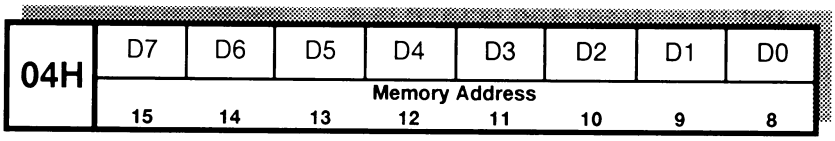


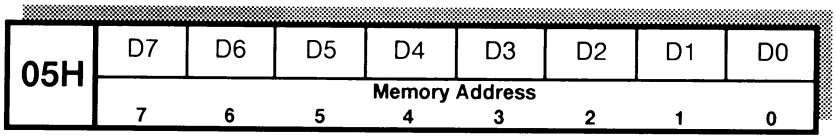
■ 03-05H MEMORY ADDRESS REGISTERS

These registers are used to specify the addresses of external memory to be written to or read from.



Address setting is completed when 05H is set. Always set the addresses sequentially from the highest-order address.

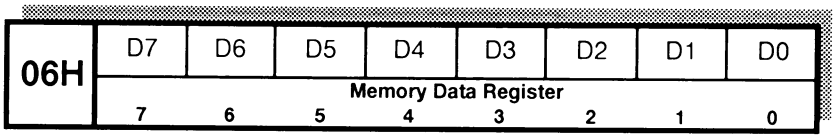




This address is incremented automatically every time data is written to or read from external memory.

■ 06H MEMORY DATA REGISTER

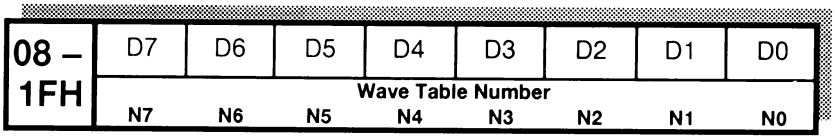
Data is written to the currently set external memory address by writing to this register. Data from the currently set external memory address is read by reading this register.



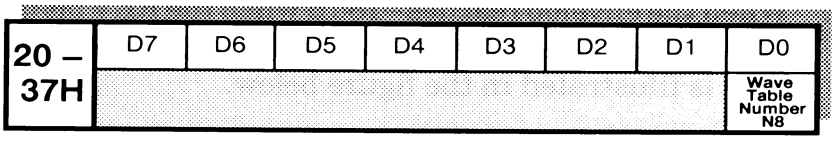
28 master clock cycles are necessary before the next data write cycle.
38 master clock cycles are necessary before the next data read cycle.

■ 08-37H WAVE TABLE NUMBER

The OPL4 supports up to 512 Wave Tables.



The wave table number that is to generate sound is selected from among 0 to 511 and the wave table header data set in the external memory is automatically loaded into the LSI by setting this register.



Setting of the Wave Table Number is completed when the Wave Table Number (N0-N7) is set. Therefore, always set the Wave Table Number (N0-N7) after Wave Table Number (N8).

Do not access the wave table number, LFO, VIB, AR, D1R, DL, D2R, rate correction, RR, or AM register of that channel while a Wave Table header is being loaded, otherwise a malfunction may occur.
The registers of other channels can be accessed.

It takes approximately 300μs for the header to be loaded.
Bit D1 of the status register is the flag indicating that a header is being loaded.

■ 20-4FH F-NUMBER, OCTAVE

These registers are used to control the pitch.

	D7	D6	D5	D4	D3	D2	D1	D0
20 – 37H	F_NUMBER f6	f5	f4	f3	f2	f1	f0	

	D7	D6	D5	D4	D3	D2	D1	D0
38 – 4FH						F_NUMBER f9	f8	f7

	D7	D6	D5	D4	D3	D2	D1	D0
38 – 4FH	Octave 03	02	01	00				

F_NUMBER is a positive number (0 ~ 1023) and octave is a 2's complement number(–7 to +7).
Do not set –8 at octave.

When F_NUMBER is "0" and octave is "1", the wave data in the external memory is played back at 44.1kHz. This is referred to as normal pitch F (¢)=0.
(¢: Cent)

The offset from normal pitch is calculated from the following equation:

$$F\ (¢) = 1200 \times (\text{Octave} - 1) + 1200 \times \log_2 \frac{1024 + \text{F\_NUMBER}}{1024}$$

however, 1 octave = 1200¢

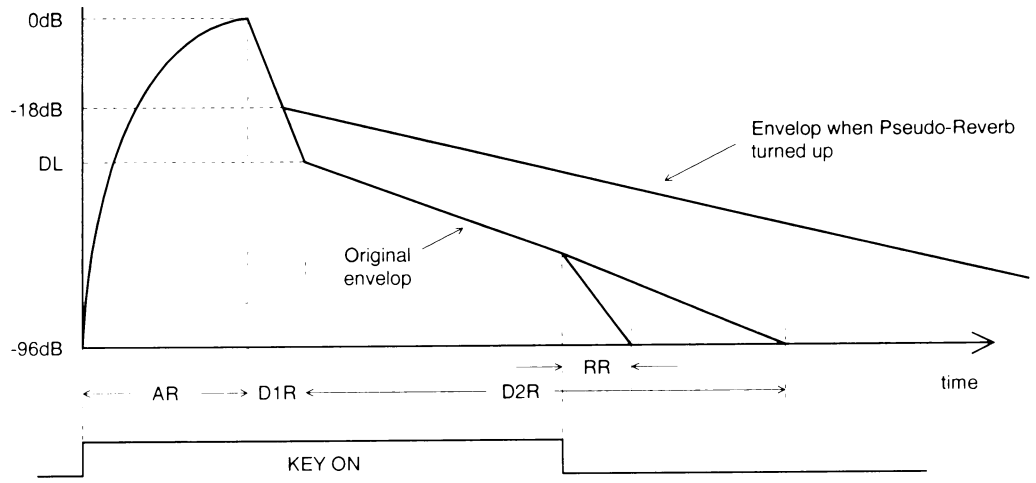
■ 38-4FH PSEUDO-REVERB

A reverberation effect can be applied to the generated sound.

	D7	D6	D5	D4	D3	D2	D1	D0
38 – 4FH					Pseudo -reverb			

"0": Pseudo-Reverb effect OFF
"1": Pseudo-Reverb effect ON

When the envelop reaches –18dB when the REV bit is set to "1", the value of the D1R, D2R, and RR registers is ignored and the reverb rate (RATE=5) is set automatically.
This is illustrated in the figure below.



■ 50-67H TOTAL LEVEL

The total level is set in this register.
Attenuation is given by the following equation:

	D7	D6	D5	D4	D3	D2	D1	D0
50 – 67H	Total level							
	L6	L5	L4	L3	L2	L1	L0	

Total level [dB] =
$(-24 \times L6) + (-12 \times L5) + (-6 \times L4) + (-3 \times L3) + (-1.5 \times L2) + (-0.75 \times L1) + (-0.375 \times L0)$

■ 50-67H LEVEL DIRECT

This register is used to select how the envelop level changes when the total level was changed during sound generation.

	D7	D6	D5	D4	D3	D2	D1	D0
50 – 67H								Level direct

"0".....Total level is changed while being interpolated.
"1".....Total level immediately becomes the set value.

When the level was interpolated, the time from minimum volume to maximum volume is 78.2msec and the time from maximum volume to minimum volume is 156.4msec.

■ 68-7FH KEY ON

This register controls sound generation.

	D7	D6	D5	D4	D3	D2	D1	D0
68 – 7FH	KEY ON							

"0": Key off
"1": Key on

■ 68-7FH DAMP

Forced damping can be enabled by making this register "1" in the decay state.

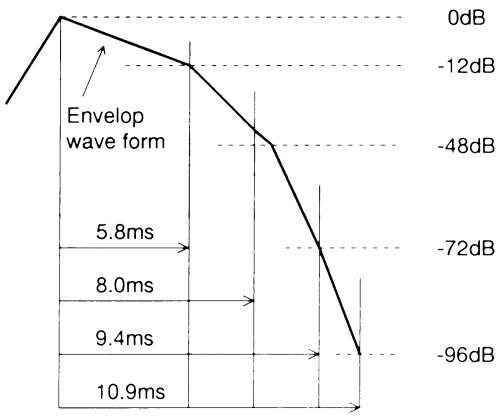
	D7	D6	D5	D4	D3	D2	D1	D0
68 – 7FH		DAMP						

The damping effect muffles the sound by making the decay and release rate times shorter.
"0" ...Enable set rate
"1" ...Disable set rate and automatically change to damp rate internally

Damping is applied as shown in the table below depending on the elapsed time.

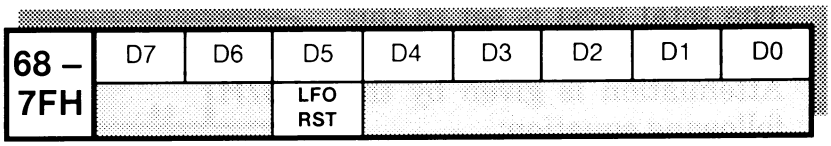
Time (msec.)	5.8	8.0	9.4	10.9
ATT. (dB)	–12	–48	–72	–96

Pseudo-reverb is disabled during damping.



■ 68-7FH LFO RESET

An LFO (Low Frequency Oscillator) is built into this LSI for the vibrato and tremolo functions.

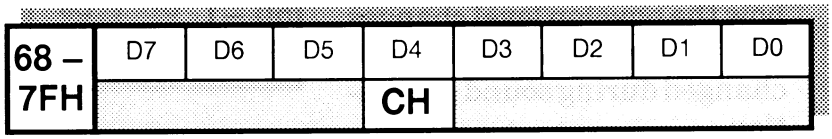


68 – 7FH	D7	D6	D5	D4	D3	D2	D1	D0
			LFO RST					

LFORST controls the operation of this LFO.
"0": Activate
"1": Deactivate and reset LFO

■ 68-7FH OUTPUT CHANNEL SELECTION

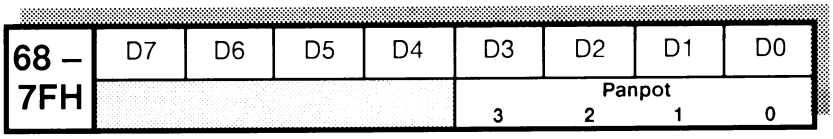
This register select output channel.
The sound of a selected channel is mixed with the FM sound and is output from the DO2 pin by setting its bit to "0".
The sound of a selected channel is output from the DO1 pin by setting its bit to "1".



68 – 7FH	D7	D6	D5	D4	D3	D2	D1	D0
				CH				

■ 68-7FH PANPOT

This register controls panpot (sound position).



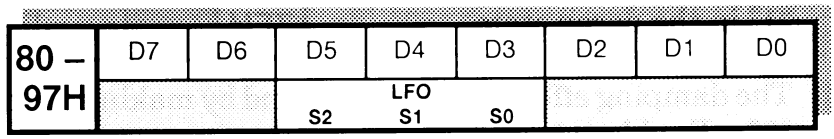
68 – 7FH	D7	D6	D5	D4	D3	D2	D1	D0
					Panpot 3	2	1	0

The set values and L and R output levels are shown in the table below.

Panpot		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Output level (dB)	L	0	–3	–6	–9	–12	–15	–18	–∞	–∞	0	0	0	0	0	0	0
	R	0	0	0	0	0	0	0	0	–∞	–∞	–18	–15	–12	–9	–6	–3

■ 80-97H LFO

This register specifies the LFO speed.



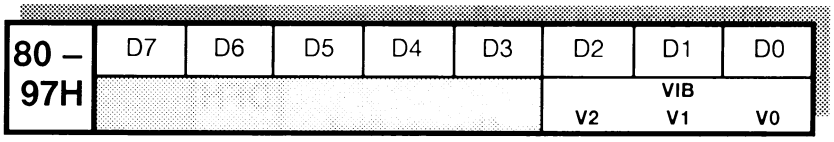
80 – 97H	D7	D6	D5	D4	D3	D2	D1	D0
			LFO S2	S1	S0			

The vibrato and tremolo oscillation frequency is determined by the specified LFO oscillation frequency as shown in the table below.

LFO value	0	1	2	3	4	5	6	7
LFO freq. (Hz)	0.168	2.019	3.196	4.206	5.215	5.888	6.224	7.066

■ 80-97H VIB

This register specifies the vibrato depth.



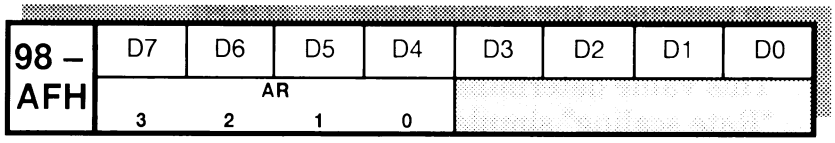
80 – 97H	D7	D6	D5	D4	D3	D2	D1	D0
							VIB	
						V2	V1	V0

The vibrato depth is determined by the written value as shown in the table below.

Value	0	1	2	3	4	5	6	7
Vibrato depth (¢)	off	3.378	5.065	6.750	10.114	20.170	40.108	79.307

■ 98-AFH AR

This register specifies the attack rate.

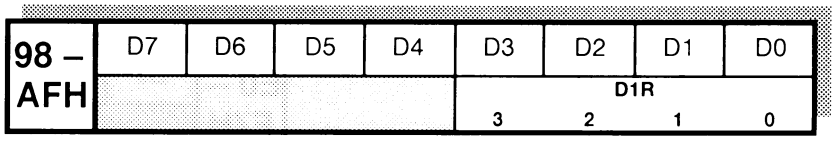


98 – AFH	D7	D6	D5	D4	D3	D2	D1	D0
			AR					
	3	2	1	0				

For a description of how to find the envelop waveform and rate value, see the sections "Envelop", "How to Calculate the Actual Rate" and "Relation Between Rate Value and Actual Time".

■ 98-AFH D1R

This register specifies the decay 1 rate.

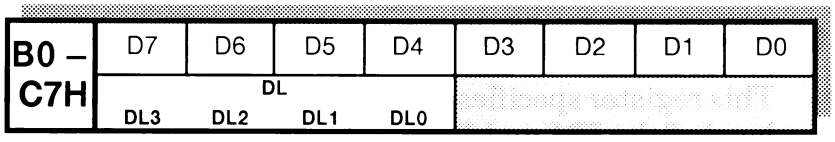


98 – AFH	D7	D6	D5	D4	D3	D2	D1	D0
							D1R	
					3	2	1	0

For a description of how to find the envelop waveform and rate value, see the sections "Envelop", "How to Calculate the Actual Rate", and "Relation Between Rate Value and Actual Time".

■ B0-C7H DL

This registers specifies the decay level.
The decay level is given by the following equation:

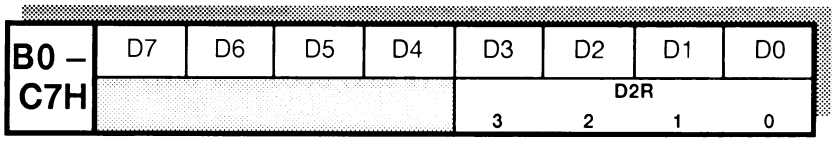


B0 – C7H	D7	D6	D5	D4	D3	D2	D1	D0
			DL					
	DL3	DL2	DL1	DL0				

Decay level [dB]= (–24 × DL3) + (–12 × DL2) + (–6 × DL1) + (–3 × DL0)
When all the bits are set to "1", the decay level becomes -93dB.

■ B0-C7H D2R

This register specifies the decay 2 rate.



B0 – C7H	D7	D6	D5	D4	D3	D2	D1	D0
							D2R	
					3	2	1	0

For a description of how to find the envelop waveform and rate value, see the sections "Envelop", "How to Calculate the Actual Rate", and "Relation Between Rate Value and Actual Time".

■ C8-DFH RR

This register specifies the release rate.

C8 – DFH	D7	D6	D5	D4	D3	D2	D1	D0
					RR 3	RR 2	RR 1	RR 0

For a description of how to find the envelop waveform and the rate value, see the sections "Envelop", "How to Calculate the Actual Rate" and "Rate Value and Actual Time Table".

■ C8-DFH RATE CORRECTION

This is the rate correction value at (Eq. 1) of the section "How to Calculate the Actual Rate".

C8 – DFH	D7	D6	D5	D4	D3	D2	D1	D0
	Rate Correction 3	Rate Correction 2	Rate Correction 1	Rate Correction 0				

This value determines the degree of rate scaling.
"Rate scaling" simulates speeding up of the rate as the interval becomes higher.

When all the bits are set to "1", scaling is turned off, otherwise scaling is carried out in accordance with the "How to Calculate the Actual Rate" correction value.

■ E0-F7H AM

This register specifies the tremolo depth.

E0 – F7H	D7	D6	D5	D4	D3	D2	D1	D0
						AM 2	AM 1	AM 0

The tremolo depth is determined by the written value as shown in the table below.

Value	0	1	2	3	4	5	6	7
Tremolo depth (dB)	off	1.781	2.906	3.656	4.406	5.906	7.406	11.91

■ F8-F9H MIX CONTROL

This register specifies the MIX level of the FM and PCM output from the DO2 pin.
The MIX level is determined by the written value as shown in the table below.
After the YMF278B is reset, FM_MIX control (F8H) becomes -9dB as the default value and PCM_MIX control (F9H) becomes 0dB to balance the FM sound and PCM volume.

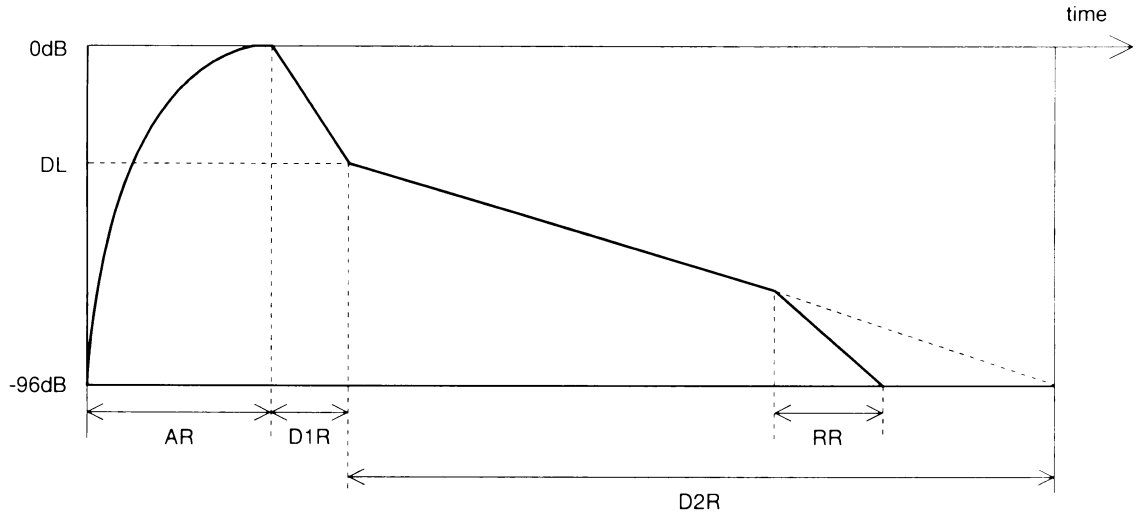
F8H	D7	D6	D5	D4	D3	D2	D1	D0
			MIX Control (FM_R) 2	MIX Control (FM_R) 1	MIX Control (FM_R) 0	MIX Control (FM_L) 2	MIX Control (FM_L) 1	MIX Control (FM_L) 0

F9H	D7	D6	D5	D4	D3	D2	D1	D0
			MIX Control (PCM_R) 2	MIX Control (PCM_R) 1	MIX Control (PCM_R) 0	MIX Control (PCM_L) 2	MIX Control (PCM_L) 1	MIX Control (PCM_L) 0

Value	0	1	2	3	4	5	6	7
MIX Level (dB)	0	–3	–6	–9	–12	–15	–18	–∞

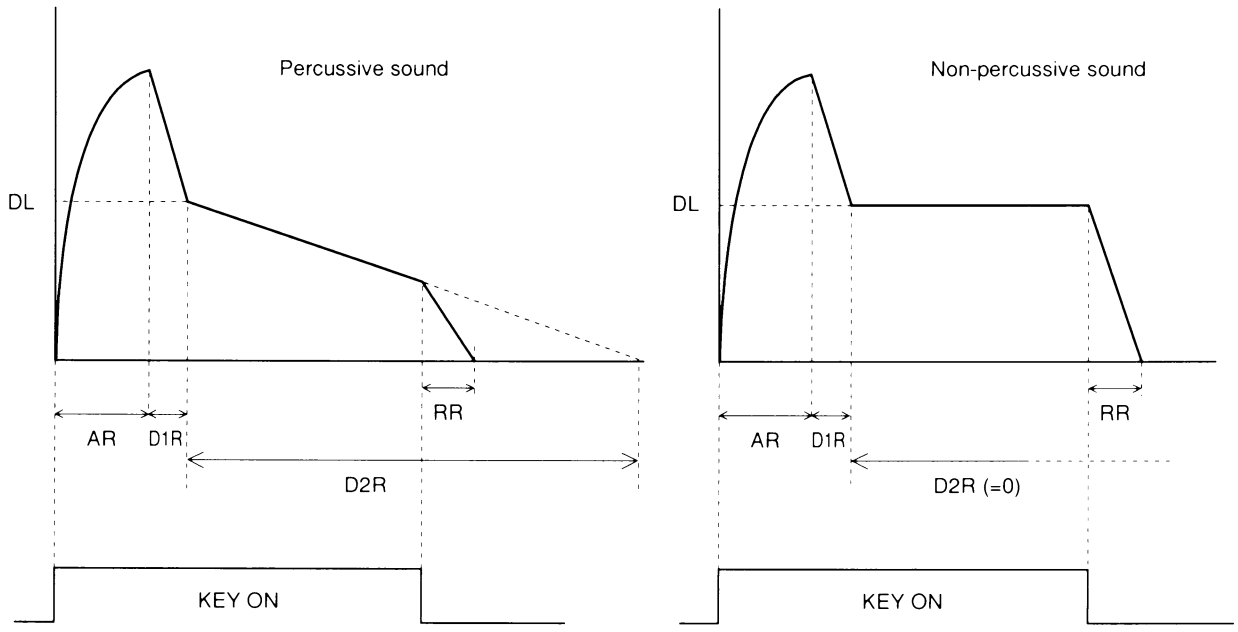
■ ENVELOP GRAPH

The envelop is shown in the figure below.



■ KEY ON AND ENVELOP

The relationship between key on, key off, and the envelop is shown below.
For non-percussive sounds, set D2R=0 (RATE=0, real time=∞).



HOW TO CALCULATE THE ACTUAL RATE

The actual rate time can be calculated finding the RATE of (Eq. 1) below and referring to the section "Relation Between Rate Value and Actual Time" on the next page.

RATE is calculated from the following equation:

$$RATE = (OCT + \text{rate correction}) \times 2 + f9 + RD \quad \text{..... (Eq. 1)}$$

OCT : Octave value (–7 to +7) set in registers 38H to 4FH
f9 : F_NUMBER f9 value (0 or 1)set in registers 38H to 4FH
Rate Correction: Rate correction value (0 to 14) of registers C8H to DFH

RD in Eq. (1) above is determined by the value set in AR, D1R, D2R, and RR.
The relation of the AR, D1R, D2R, and RR set value and RD is shown in the table below.

AR, D1R, D2R, RR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
(Eq. 1) RD value	4	8	12	16	20	24	28	32	36	40	44	48	52	56	63

However, when is more than 63 at Eq. 1, it is always set to 63.
When AR=D1R=D2R=RR="0", RATE is set to "0".
When AR=D1R=D2R=RR="15", RATE is set to "63".

RELATION BETWEEN RATE VALUE AND ACTUAL TIME

■ Attack rate

(Unit: ms)

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
0	∞	∞
1	∞	∞
2	∞	∞
3	∞	∞
4	6222.95	3715.19
5	4978.37	2972.20
6	4148.66	2476.83
7	3556.01	2122.99
8	3111.47	1857.60
9	2489.21	1486.12
10	2074.33	1238.41
11	1778.00	1061.50
12	1555.74	928.80
13	1244.63	743.08
14	1037.19	619.23
15	889.02	530.75
16	777.87	464.40
17	622.31	371.56
18	518.59	309.61
19	444.54	265.40
20	388.93	232.20
21	311.16	185.80
22	259.32	154.83
23	222.27	132.70
24	194.47	116.10
25	155.60	92.93
26	129.66	77.41
27	111.16	66.35
28	97.23	58.05
29	77.82	46.49
30	64.85	38.73
31	55.60	33.20

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
32	48.62	29.02
33	38.91	23.27
34	32.43	19.37
35	27.80	16.60
36	24.31	14.51
37	19.46	11.66
38	16.24	9.70
39	13.92	8.30
40	12.15	7.26
41	9.75	5.85
42	8.12	4.85
43	6.98	4.17
44	6.08	3.63
45	4.90	2.95
46	4.08	2.45
47	3.49	2.09
48	3.04	1.81
49	2.49	1.45
50	2.13	1.22
51	1.90	1.09
52	1.72	0.95
53	1.41	0.77
54	1.18	0.63
55	1.04	0.54
56	0.91	0.50
57	0.73	0.36
58	0.59	0.27
59	0.50	0.27
60	0.45	0.23
61	0.45	0.23
62	0.45	0.23
63	0.00	0.00

■ Decay rate and release rate

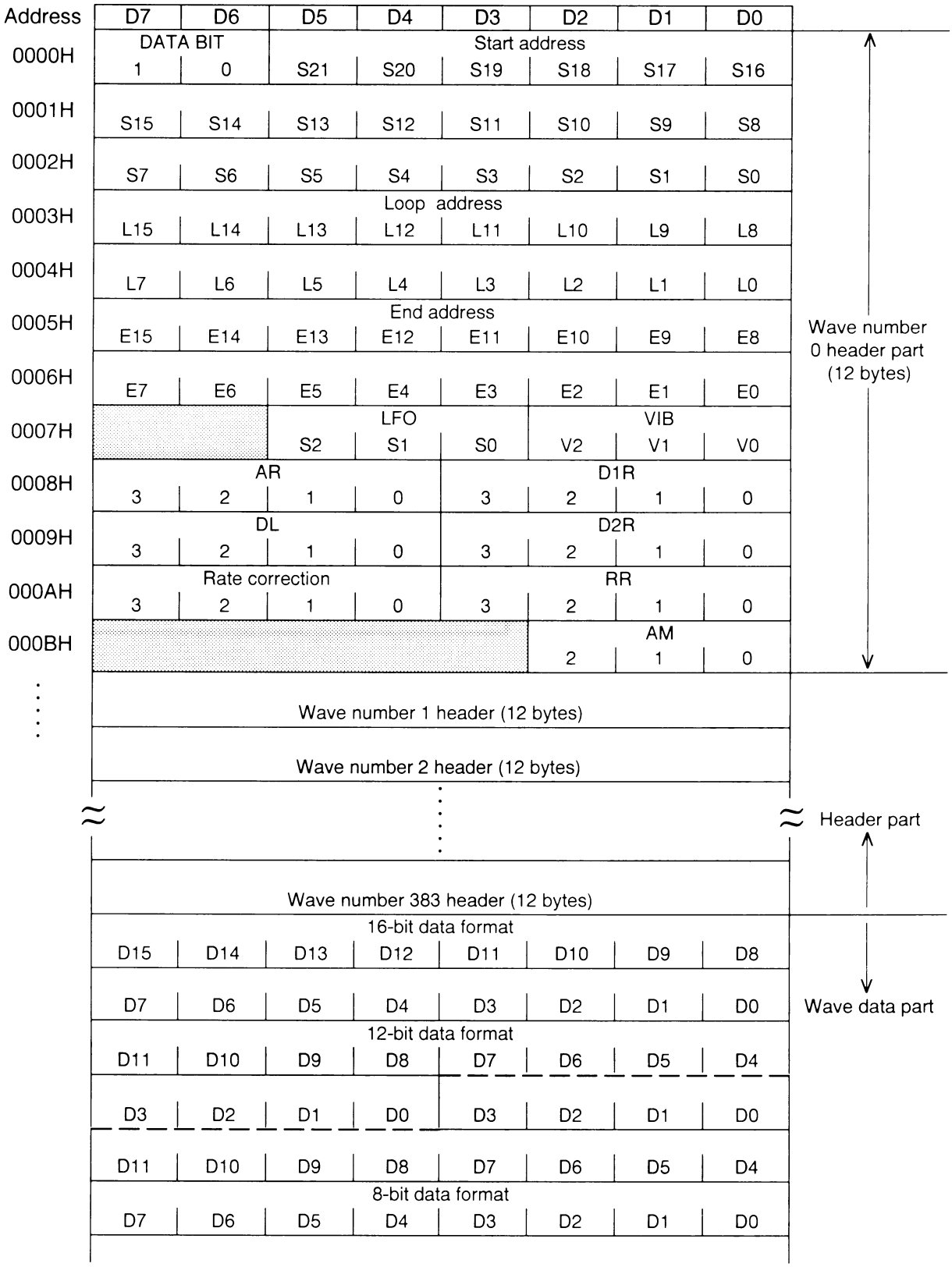
(Unit: ms)

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
0	∞	∞
1	∞	∞
2	∞	∞
3	∞	∞
4	89164.63	19040.36
5	71331.75	15278.73
6	59443.13	12724.54
7	50951.25	10890.16
8	44582.31	9520.18
9	35665.90	7639.37
10	29721.59	6362.27
11	25475.65	5445.08
12	22291.16	4760.09
13	17832.97	3819.68
14	14860.82	3181.13
15	12737.82	2722.54
16	11145.58	2380.05
17	8916.51	1909.84
18	7430.43	1590.57
19	6368.93	1361.27
20	5572.79	1190.02
21	4458.28	954.92
22	3715.24	795.28
23	3184.49	680.63
24	2786.39	595.01
25	2229.16	477.46
26	1857.64	397.64
27	1592.24	340.32
28	1393.20	297.51
29	1114.60	238.73
30	928.84	198.82
31	796.15	170.16

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
32	696.60	148.75
33	557.32	119.37
34	464.44	99.41
35	398.10	85.08
36	348.30	74.38
37	278.68	59.68
38	232.24	49.71
39	199.05	42.54
40	174.15	37.19
41	139.37	29.84
42	116.15	24.85
43	99.55	21.32
44	87.07	18.59
45	69.71	14.92
46	58.10	12.43
47	49.80	10.66
48	43.54	9.23
49	34.83	7.44
50	29.02	6.08
51	24.90	5.31
52	21.77	4.67
53	17.41	3.72
54	14.51	3.13
55	12.43	2.68
56	10.08	2.36
57	8.71	1.95
58	7.23	1.59
59	6.21	1.36
60	5.44	1.18
61	5.44	1.18
62	5.44	1.18
63	5.44	1.18

EXTERNAL MEMORY DATA FORMAT

The external memory header structure and data format are shown below.



■ DATA BIT

These specify the waveform data bit length.
The data bit length for each set value is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
DATA BIT							
1	0						

D7	D6	Data bit Length
0	0	8 bits
0	1	12 bits
1	0	16 bits
1	1	Prohibited

■ START ADDRESS

The wave data read start address is shown by external memory absolute address.

For 12-bit data, always specify the start address beginning from bit 8 of the higher-order byte.

D7	D6	D5	D4	D3	D2	D1	D0
		A21	A20	A19	A18	A17	A16
A15	A14	A13	A12	A11	A10	A9	A8
A7	A6	A5	A4	A3	A2	A1	A0

■ LOOP ADDRESS

When the wave data read address reaches the end address, the wave data is re-read from the address specified by the loop address.

D7	D6	D5	D4	D3	D2	D1	D0
L15	L14	L13	L12	L11	L10	L9	L8
L7	L6	L5	L4	L3	L2	L1	L0

Always specify the difference of one address subtracted from the number of data from the start address.

■ END ADDRESS

Shows the wave data read end address.

Specify the end address by subtracting one from the number of data from the start address and inverting all the bits.

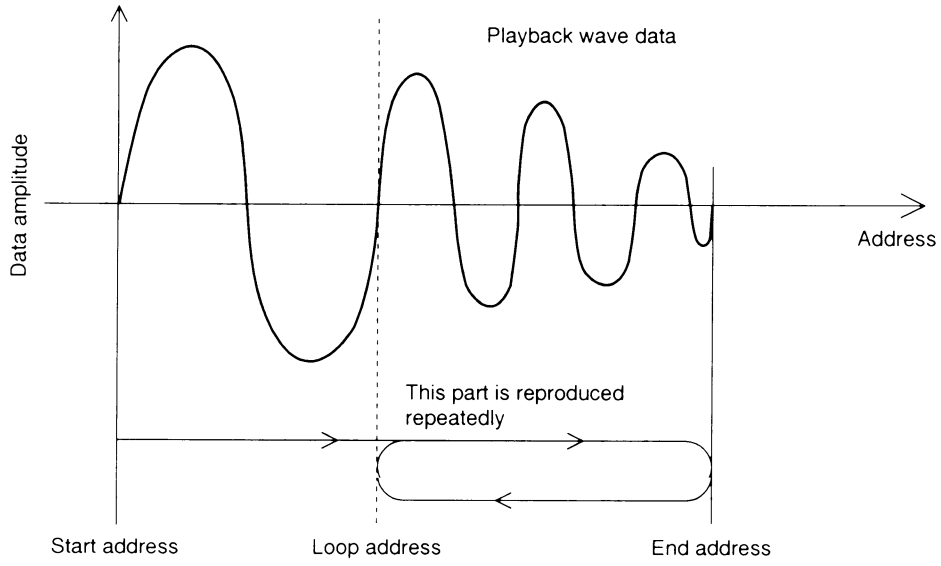
D7	D6	D5	D4	D3	D2	D1	D0
E15	E14	E13	E12	E11	E10	E9	E8
E7	E6	E5	E4	E3	E2	E1	E0

■ START, END, AND LOOP ADDRESSES

This section explains how the wave data is played back.

The wave data is read from the start address and when the wave data read address exceeds the end address, the read address returns to the loop address and the address is counted up again from the loop address to the end address.
The waveform is reproduced by repeating this process.

This is illustrated below.



Note: A loop address and end address must be specified for all the sounds.

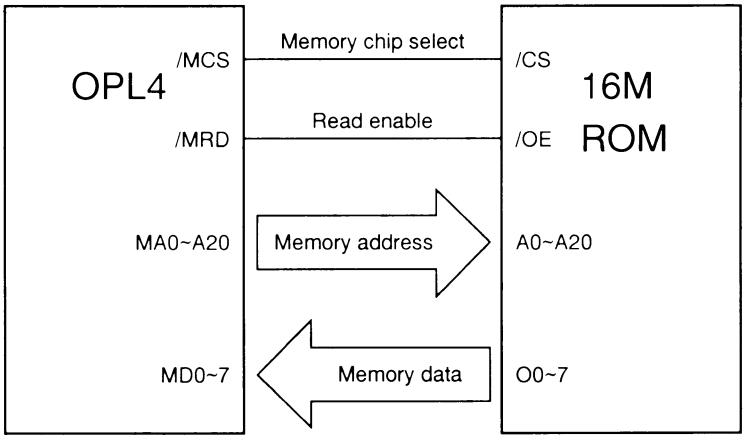
CONNECTION TO EXTERNAL MEMORY

This section describes how the the memory interface signal output from the YMF278B is connected to external memory.

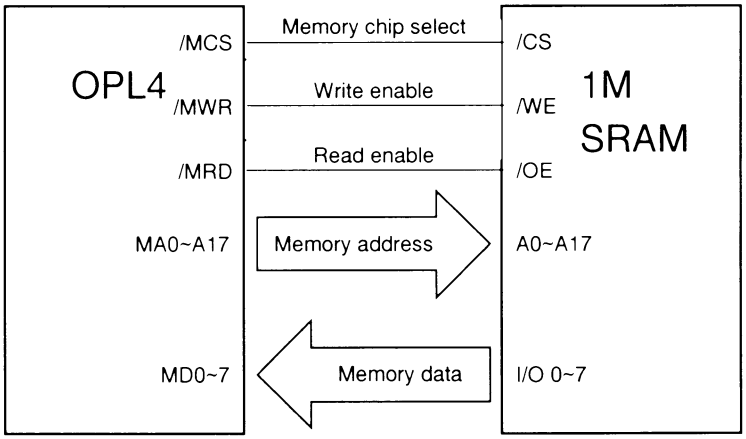
/MCS0 to /MCS9 are available as external memory chip select signals. For the chip select signal connections, see the section "External Memory Chip Select Signals".

The method of connecting a 16Mbit ROM and a 1Mbit SRAM is shown below as an example.

■ 16Mbit connection method (ROM)



■ 1Mbit connection method (SRAM)

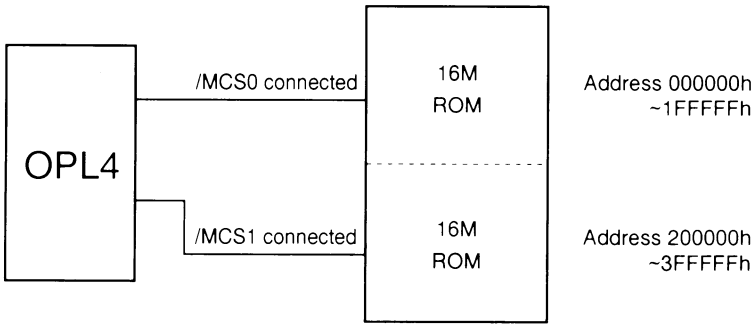


EXTERNAL MEMORY CHIP SELECT SIGNALS

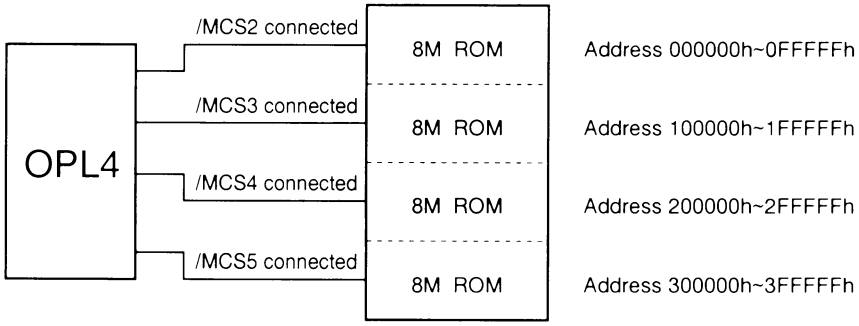
The YMF278B can be used with 1M, 4M, 8M, and 16Mbit memories. Up to 32M bits can be connected.
/MCS0 to /MCS9 are output as the external memory (ROM, SRAM) chip select signals.
Chip select signals /MCS0 to MCS9 determine the memory capacity that is connected to address space.
This section describes 16M, 8M, and 4M bits as ROM and 1M bit as SRAM.

■ ROM only configuration (02H-memory type "0")

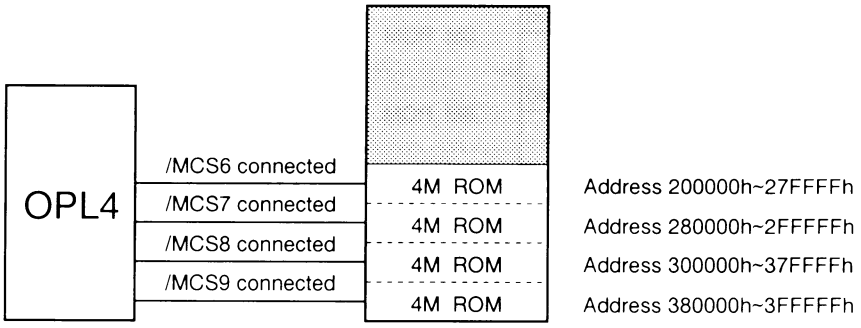
□ 16Mbit chip select signals



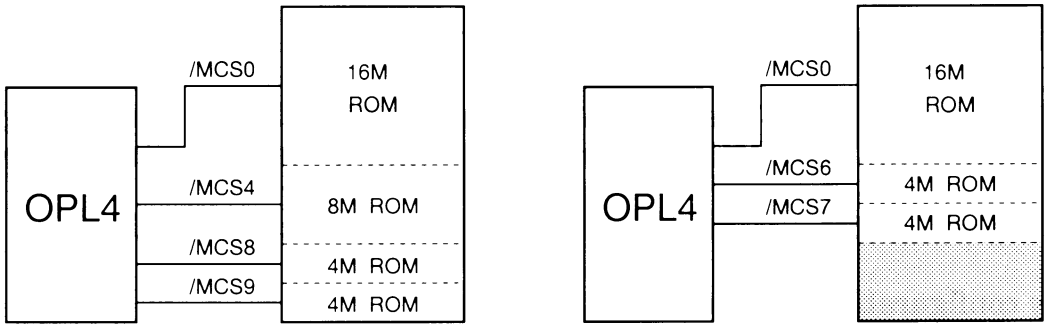
□ 8Mbit chip select signals



□ 4Mbit chip select signals

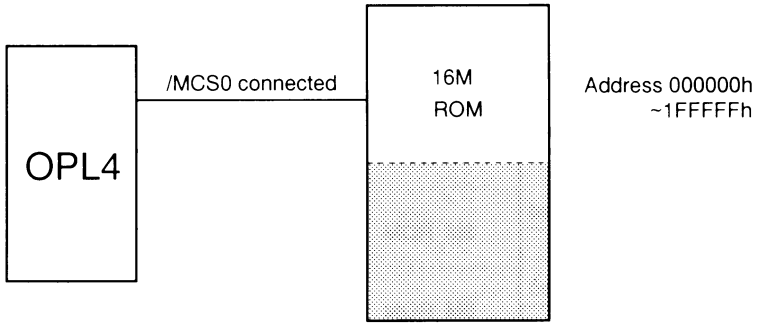


○ Two connection examples are shown below.

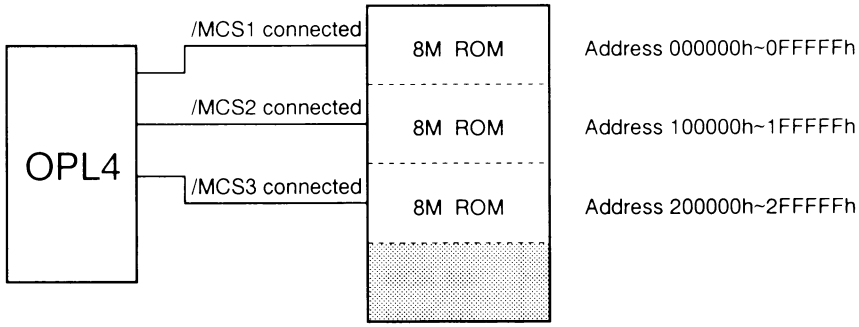


■ ROM+SRAM structure (02H-memory type "1")

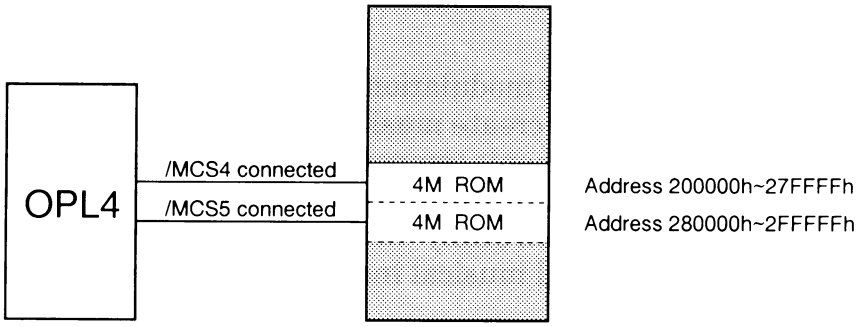
□ 16Mbit chip select signal



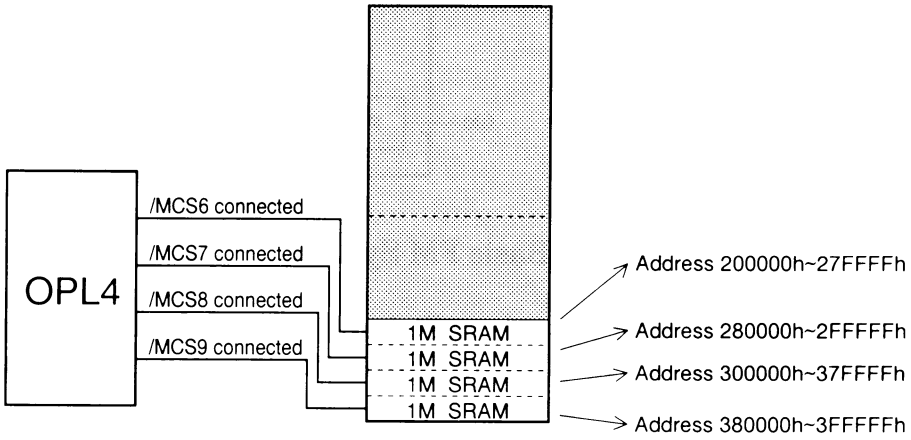
□ 8Mbit chip select signals



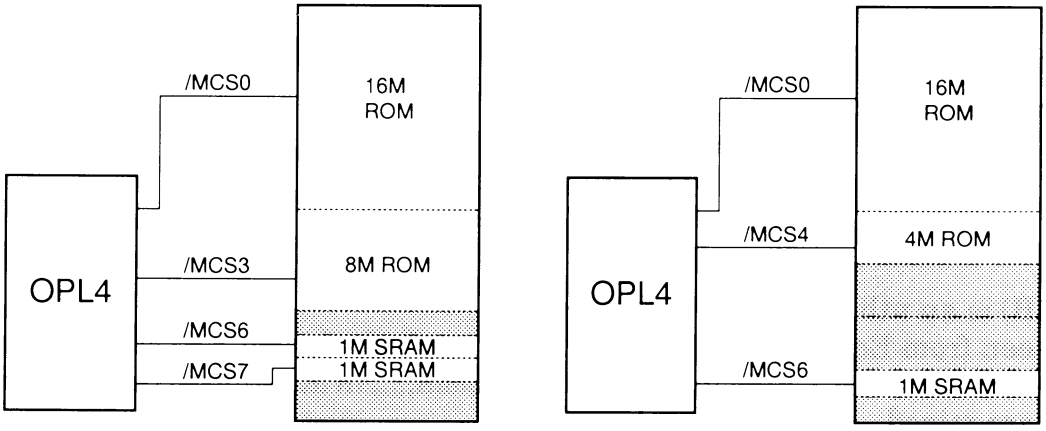
□ 4Mbit chip select signals



□ 1Mbit chip select signals



○ Two ROM+SRAM connection examples are shown below.



OVERVIEW OF FM SYNTHESIZER

☐ What is FM?

"FM" is the abbreviation for "frequency modulation". The FM synthesizer uses harmonics generated by frequency modulation to create music.

The FM system can generate high harmonic components containing non-harmonic sounds with a comparatively simple circuit. Since the correspondence of the modulation index and harmonics spectral distribution is extremely natural, a wide range of sounds, from synthesization of the sounds of natural musical instruments to electronic sounds, can be produced.

☐ FM system structure

The block diagram of the basic FM system is shown in Fig. 1-1.

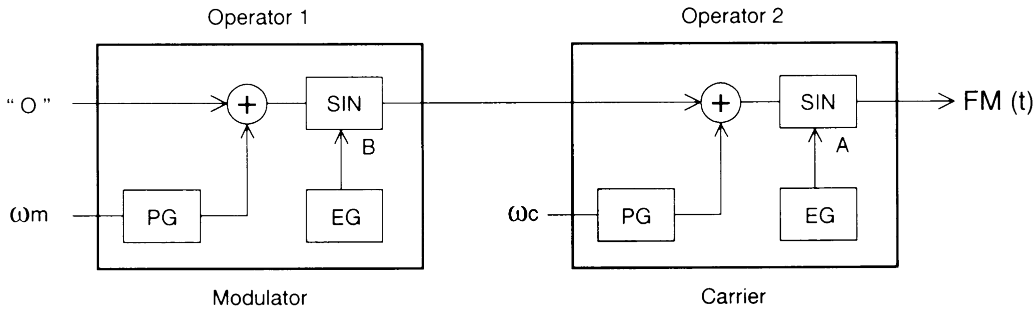


Fig. 1-1 Basic FM System

The part that generates one sine wave is called an "operator". A combination of these operators is called an "algorithm". The first stage operator is called the "modulator" and the second stage operator is called the "carrier".

The frequency and envelop can be set for each operator.

☐ FM system equation

The block diagram shown in Fig. 1-1 is represented by Eq. (1).

$$FM(t) = A\sin(\omega c t + B\sin\omega m t) \;\dots\dots\dots\dots\; (1)$$

Where, A is the amplitude of operator 2, B is the amplitude of operator 1, ωc is the angular frequency of operator 2, and ωm is the angular frequency of operator 1.

Eq. (1) can be rewritten by Fourier transformation as shown in Eq. (2).

$$\begin{aligned} FM(t) = A\,[&J_0(B)\sin\omega c t \\ &+J_1(B)\{\sin(\omega c + \omega m)t - \sin(\omega c + \omega m)t\} \\ &+J_2(B)\{\sin(\omega c + 2\omega m)t - \sin(\omega c + 2\omega m)t\} \\ &+J_3(B)\{\sin(\omega c + 2\omega m)t - \sin(\omega c + 2\omega m)t\} \\ &\dots\dots\dots\dots\dots\dots\dots\dots\quad] \qquad \dots\dots (2) \end{aligned}$$

Where, Jn(B) is an nth order Bessel function.

As can be seen from Eq. (2), when modulation is applied, elements having frequencies of $\omega c+\omega m$, $\omega c-\omega m$, $\omega c+2\omega m$, $\omega c-2\omega m$, $\omega c+3\omega m$, $\omega c-3\omega m$,..., in addition to the original carrier frequency, are mixed.

These elements are called "harmonics". The frequency of these harmonics is determined by the modulator frequency and the carrier frequency. Their amplitude is determined by the modulator amplitude B.

☐ Feedback FM

A system called "feedback FM" is available to generate a wider range of sounds. This system modulates itself as shown in Fig. 1-2. It is represented by Eq. (3).

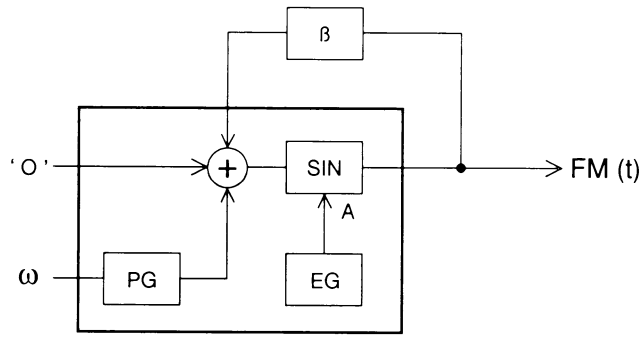


Fig. 1-2 Feedback FM System

$$FM(t) = A\sin\{\omega t + \beta FM(t)\} \quad \ldots\ldots\ldots (3)$$

Where, ß is the feedback rate. When feedback FM is used, the harmonic spectral becomes a sawtooth wave and the sound of string instruments can be easily created.

Since the YMF278B has four operators, the same as the YMF262 (OPL3), it can generate complex sounds.

REGISTER TABLE FOR FM SYNTHESIS

The registers are compatible with the YMF262 (OPL3).
When all the registers are initialized except COH~C8H CHA and CHB bit, they are cleared to (/IC="L").

Address (HEX)	REGISTER ARRAY 0 (A1='1')							
	D7	D6	D5	D4	D3	D2	D1	D0
00~01H	LSI TEST							
02H	TIMER 1							
03H	TIMER 2							
04H	RST	MT1	MT2				ST2	ST1
05H								
08H		NTS						
20H~35H	AM	VIB	EGT	KSR	MULT 3	MULT 2	MULT 1	MULT 0
40H~55H	KSL 1	KSL 0	TL L5	TL L4	TL L3	TL L2	TL L1	TL L0
60H~75H	AR 3	AR 2	AR 1	AR 0	DR 3	DR 2	DR 1	DR 0
80H~95H	SL 3	SL 2	SL 1	SL 0	RR 3	RR 2	RR 1	RR 0
A0H~A8H	F NUMBER (L) F7	F NUMBER (L) F6	F NUMBER (L) F5	F NUMBER (L) F4	F NUMBER (L) F3	F NUMBER (L) F2	F NUMBER (L) F1	F NUMBER (L) F0
B0H~B8H			KON	BLOCK B2	BLOCK B1	BLOCK B0	FNUM (H) F9	FNUM (H) F8
BDH	DAM	DVB	RYT	BD	SD	TOM	TC	HH
C0H~C8H	CHD	CHC	CHB	CHA	FB 2	FB 1	FB 0	CNT
E0H~F5H						WS W2	WS W1	WS W0

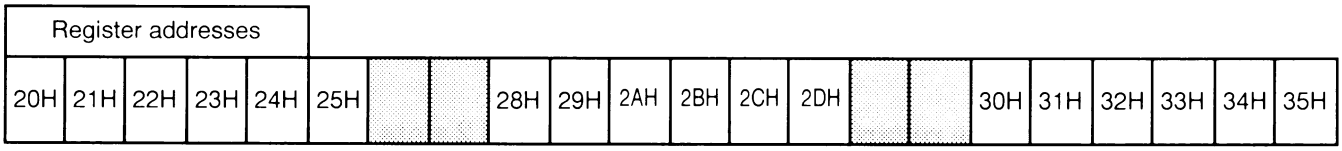
	REGISTER ARRAY 1 (A1='H')							
	D7	D6	D5	D4	D3	D2	D1	D0
	LSI TEST							
			CONNECTION SEL					
							NEW2	NEW
	AM	VIB	EGT	KSR	MULT 3	MULT 2	MULT 1	MULT 0
	KSL 1	KSL 0	TL L5	TL L4	TL L3	TL L2	TL L1	TL L0
	AR 3	AR 2	AR 1	AR 0	DR 3	DR 2	DR 1	DR 0
	SL 3	SL 2	SL 1	SL 0	RR 3	RR 2	RR 1	RR 0
	F NUMBER (L) F7	F NUMBER (L) F6	F NUMBER (L) F5	F NUMBER (L) F4	F NUMBER (L) F3	F NUMBER (L) F2	F NUMBER (L) F1	F NUMBER (L) F0
			KON	BLOCK B2	BLOCK B1	BLOCK B0	FNUM (H) F9	FNUM (H) F8
	CHD	CHC	CHB	CHA	FB 2	FB 1	FB 0	CNT
						WS W2	WS W1	WS W0

Notes:
1. The register array 1, 05H NEW2 bit is expanded from the YMF262 (OPL3) to the YMF278B (OPL4). For a detailed description of the NEW2 bit, see the description of the registers.
2. LSI TEST is used in factory testing. Always set it to "0" for normal operation.
3. ▨ not used with the YMF278B may be used to expand the functions. Therefore, always set them to "0".

REGISTER SETTING

The YMF278B has 36 circuits that generate a sine wave. Sounds are generated by performing FM operations with these circuits.
A circuit which generates a sine wave is called a "slot". One sound unit which is generated by combining two or four operators is called a "channel".

■ Setting of registers in slot units
There are two kinds of sound generation control registers: registers settable in slot units and registers set in channel units.
The registers that can be set in slot units are 20 to 35H, 40 to 55H, 60 to 75H, 80 to 95H, and E0 to F5H.
These registers do not have addresses ×6H, ×7H, ×EH, or ×FH. (Register addresses 20 to 35H are shown below as an example.)

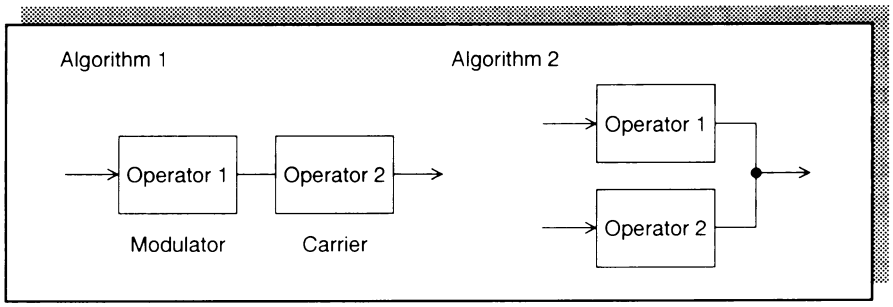


■ Slot No.
The 36 slots are numbers from 1 to 36. These numbers are called the "slot number". The relation between slot No. and register address set for each slot is shown in the table below.

Slot No.	Set register address (A1=0)					Slot No.	Set register address (A1=1)				
1	20H	40H	60H	80H	E0H	19	20H	40H	60H	80H	E0H
2	21H	41H	61H	81H	E1H	20	21H	41H	61H	81H	E1H
3	22H	42H	62H	82H	E2H	21	22H	42H	62H	82H	E2H
4	23H	43H	63H	83H	E3H	22	23H	43H	63H	83H	E3H
5	24H	44H	64H	84H	E4H	23	24H	44H	64H	84H	E4H
6	25H	45H	65H	85H	E5H	24	25H	45H	65H	84H	E5H
7	28H	48H	68H	88H	E8H	25	28H	48H	68H	88H	E8H
8	29H	49H	69H	89H	E9H	26	29H	49H	69H	89H	E9H
9	2AH	4AH	6AH	8AH	EAH	27	2AH	4AH	6AH	8AH	EAH
10	2BH	4BH	6BH	8BH	EBH	28	2BH	4BH	6BH	8BH	EBH
11	2CH	4CH	6CH	8CH	ECH	29	2CH	4CH	6CH	8CH	ECH
12	2DH	4DH	6DH	8DH	EDH	30	2DH	4DH	6DH	8DH	EDH
13	30H	50H	70H	90H	F0H	31	30H	50H	70H	90H	F0H
14	31H	51H	71H	91H	F1H	32	31H	51H	71H	91H	F1H
15	32H	52H	72H	92H	F2H	33	32H	52H	72H	92H	F2H
16	33H	53H	73H	93H	F3H	34	33H	53H	73H	93H	F3H
17	34H	54H	74H	94H	F4H	35	34H	54H	74H	94H	F4H
18	35H	55H	75H	95H	F5H	36	35H	55H	75H	95H	F5H

■ Two-operator mode and slot and channel

In the two-operator mode, two slots are used to generate one FM sound.
Consequently, since there are 36 slots, in the two-operator mode, 18 channels of sound can be generated.
Channels are also numbered, the same as slots. These numbers are called the "channel number".
For two operators, the following two algorithms are available:



Algorithm 2 is the same regardless of the operator 1 and 2 slots. However, for algorithm 1, since the wave table depends on which slot is the carrier and which slot is the modulator, care must be given to the slot No.

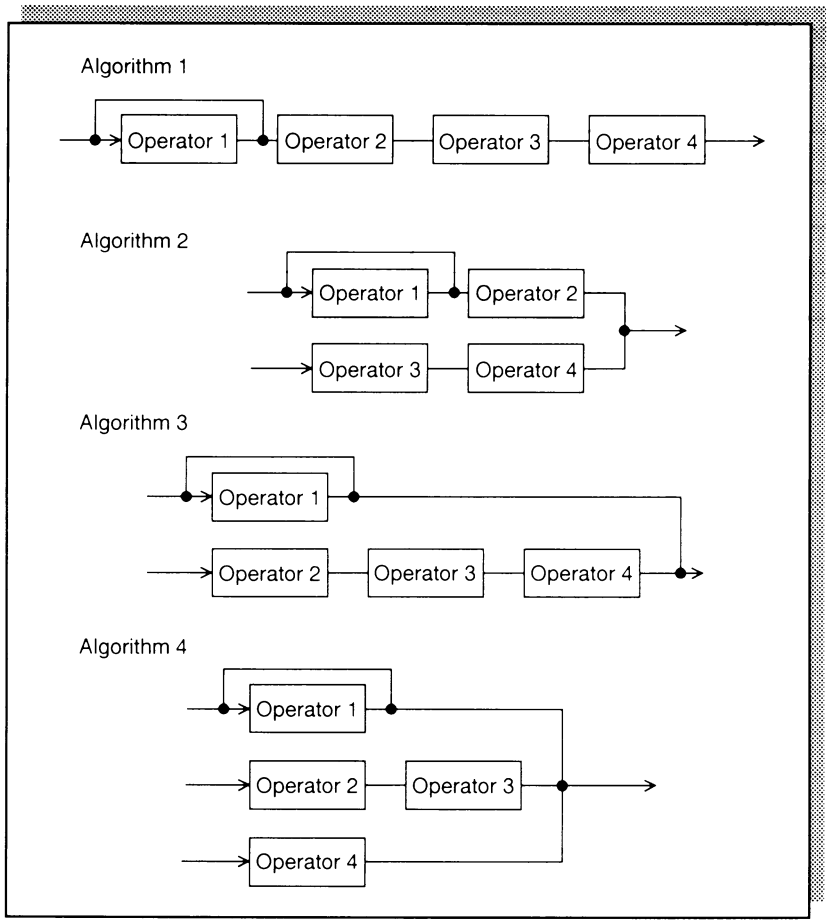
The slot No. corresponding to operators 1 and 2 is fixed. the channel number and slot numbers corresponding to operators 1 and 2 are shown in the table below.

A1	Slot No.		Channel No.
	Operator 1	Operator 2	
0	1	4	1
	2	5	2
	3	6	3
	7	10	4
	8	11	5
	9	12	6
	13	16	7
	14	17	8
	15	18	9
1	19	22	10
	20	23	11
	21	24	12
	25	28	13
	26	29	14
	27	30	15
	31	34	16
	32	35	17
	33	36	18

■ Registers set in channel units (two-operator mode)
The registers set in channel units are A0 to A8H, B0 to B8H, and C0 to C8H.
The relation between channel number and set register address is shown in the table below.
However, this relation is different in the four-operator mode. (The four-operator mode will be described later.)

Channel No.	Set register address (A1=0)			Channel No.	Set register address (A1=1)		
1	A0H	B0H	C0H	10	A0H	B0H	C0H
2	A1H	B1H	C1H	11	A1H	B1H	C1H
3	A2H	B2H	C2H	12	A2H	B2H	C2H
4	A3H	B3H	C3H	13	A3H	B3H	C3H
5	A4H	B4H	C4H	14	A4H	B4H	C4H
6	A5H	B5H	C5H	15	A5H	B5H	C5H
7	A6H	B6H	C6H	16	A6H	B6H	C6H
8	A7H	B7H	C7H	17	A7H	B7H	C7H
9	A8H	B8H	C8H	18	A8H	B8H	C8H

■ Four-operator mode and slot and channel
In the four-operator mode, four slots are used to generate one FM sound. Sounds can be generated simultaneously by six channels by using 24 slots.



In the four-operator mode, the slot numbers corresponding to operators 1, 2, 3, and 4 are fixed, the same as in the two-operator mode.
The channel No. and slot Nos. corresponding to operators 1, 2, 3, and 4 are shown in the table below.

A1	Slot No.				Channel No.
	Operator 1	Operator 2	Operator 3	Operator 4	
0	1	4	7	10	1
	2	5	8	11	2
	3	6	9	12	3
1	19	22	25	28	4
	20	23	26	29	5
	21	24	27	30	6

■ Registers set in channel units (four-operator mode)
The registers set in channel units are A0 to A2H, B0 to B2H, and C0 to C2H.
However, to select the four algorithms, only the CNT bit of C0 to C8 require register setting other than C0 to C2H.
For more information, see the CNT bit of the section "Registers".

Channel No.	Set register address (A1=0)			Channel No.	Set register address (A1=1)		
1	A0H	B0H	C0H	4	A0H	B0H	C0H
2	A1H	B1H	C1H	5	A1H	B1H	C1H
3	A2H	B2H	C2H	6	A2H	B2H	C2H

■ Rhythm slot No.
Rhythm uses six slots to generate the sounds of five musical instruments (bass drum, snare drum, tom-tom, top cymbal, high hat). Slot numbers 13 to 18 generate rhythm sounds. For the relation between slot No. and musical instrument, see the section "Registers".

■ All 36 slots
How all 36 slots are used is summarized below.

Slot Nos. 1 to 12 can be used as the two-operator mode or four-operator mode.
Slot Nos. 13 to 18 can be used as the two-operator mode or rhythm.
Slot Nos. 19 to 30 can be used as the two-operator mode or four-operator mode.
Slot Nos. 31 to 36 can be used as the two-operator mode.

■ 00-01H LSI TEST

These two registers are used for LSI testing.
All bits should be left at "0" for normal operation.

	D7	D6	D5	D4	D3	D2	D1	D0
00 – 01H	LIST TEST							

(REGISTER ARRAY 0, 1)

■ 02H TIMER 1

TIMER 1 is a 80.8μs resolution timer.
Set the timer count value in this register.
The count value that can be set is 0 to 255.

	D7	D6	D5	D4	D3	D2	D1	D0
02H	TIMER 1							

(REGISTER ARRAY 0)

The timer operation is described here.
Counting is started by setting the timer count value and starting the timer.
When the set time elapses, the flag becomes "1" and the /IRQ pin is made "L" and a timer interrupt is sent to the CPU. At the same time, the count value is reloaded into the timer and counting is continued.

Time t1 until the timer 1 flag is raised is given by the following equation:

t1 [ms] = (256 – N1) × 0.08 N1: Count value (0 ~ 255)

■ 03H TIMER2

Timer 2 is a 323.1μs resolution timer.
Set the timer count value into this register.

	D7	D6	D5	D4	D3	D2	D1	D0
03H	TIMER 2							

(REGISTER ARRAY 0)

Timer 2 operation is the same as timer 1.

Time t2 until the timer 2 flag is raised is given by the following equation:

t2 [ms] = (256 – N2) × 0.32 N2: Count value (0 ~ 255)

* Note:
The resolution of timers 1 and 2 is somewhat different from that of the YMF262 (OPL3).
- OPL3 Timer 1 ..... Resolution 80.5μs
  Timer 2 ..... Resolution 321.8μs
- OPL4 Timer 1 ..... Resolution 80.8μs
  Timer 2 ..... Resolution 323.1μs

■ 04H TIMER 1,2 CONTROL

This register controls starting and stopping of timers 1 and 2.
ST1 is the timer 1 control bit and ST2 is the timer 2 control bit.

	D7	D6	D5	D4	D3	D2	D1	D0
04H							ST2	ST1

(REGISTER ARRAY 0)

When the pertinent bit is set to "1", the timer operates and when it is set to "0", the timer stops.

■ 04H FLAG CONTROL

When MT1 is set to "1", the flag always becomes "0" regardless of timer 1 operation. (The /IRQ pin does not become "L" either.)

	D7	D6	D5	D4	D3	D2	D1	D0
04H	RST	MT1	MT2					

(REGISTER ARRAY 0)

MT2 controls timer 2 the same as MT1 controls timer 1.

When the RST bit is set to "1", the flags of status register bits D5, D6, and D7 are reset. The /IRQ pin becomes "H" level. (When pulled-up externally)
After the flags are reset, the RST bit automatically returns to "0".

■ 04H 4-OPERATOR MODE SETTING

When a bit is set to "1", the corresponding slot can be used as the four-operator mode.

	D7	D6	D5	D4	D3	D2	D1	D0
04H			CONNECTION SEL					

(REGISTER ARRAY 1)

The relationship between the CONNECTION SEL bits and four-operator mode channel No. is shown below.

CONNECTION SEL	D5	D4	D3	D2	D1	D0
Four-operator mode channel No.	6	5	4	3	2	1

For the relation between channel No. and slot No., see the section "Channel and Slot".

■ 05H EXPANSION REGISTER

When accessing the registers (REGISTER ARRAY 1) expanded to OPL3 from OPL2, the NEW bit must be set to "1".

	D7	D6	D5	D4	D3	D2	D1	D0
05H							NEW2	NEW

(REGISTER ARRAY 1)

When accessing the registers expanded to OPL4 from OPL3, the NEW2 bit must be set to "1".

Since these bits become "0" after reset, when used as OPL4, set both the NEW and NEW2 bits to "1" before accessing the registers.

■ 08H KEYBOARD SPLIT SELECTION

Eight octaves are split into a total of 16 and rate key scaling is performed by splitting one octave in half.

08H	D7	D6	D5	D4	D3	D2	D1	D0
		NTS						

(REGISTER ARRAY 0)

This octave splitting is called "keyboard split".

NTS determines the keyboard split separation point.
When NTS is set to "0", the separation point is determined by the higher two bits of the F number.
When NTS is set to "1", the separation point is determined by the MSB of the F number.
This is shown in the table below.

□ NTS="0"

BLOCK data	0		1		2		3		4		5		6		7		
F number MSB																	*
F number 2nd	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Key scale No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

□ NTS="1"

BLOCK data	0		1		2		3		4		5		6		7		
F number MSB	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
F number 2nd																	*
Key scale No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

* ▨: Don't care

■ 20-35H, BDH TREMOLO EFFECT

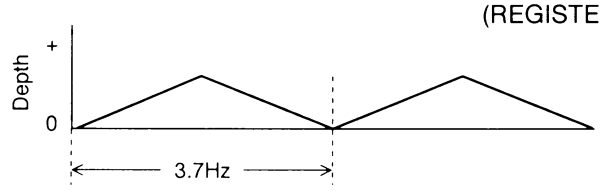
When AM is set to "1", a tremolo effect can be applied to the corresponding slot.
The tremolo frequency is 3.7Hz. Its depth is determined by DAM.
DAM="1": 4.8dB
DAM="0": 1dB

20 – 35H	D7	D6	D5	D4	D3	D2	D1	D0
	AM							

(REGISTER ARRAY 0, 1)

BDH	D7	D6	D5	D4	D3	D2	D1	D0
	DAM							

(REGISTER ARRAY 0)



■ 20-35H, BDH VIBRATO EFFECT

When VIB is set to "1", a vibrato effect can be applied to the corresponding slot.

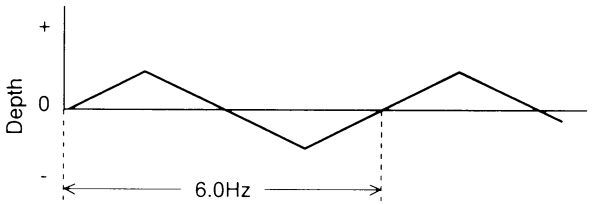
	D7	D6	D5	D4	D3	D2	D1	D0
20 – 35H		VIB						

(REGISTER ARRAY 0, 1)

The vibrator modulation frequency is 6.0Hz. Its depth is determined by DVB.
DVB="1": 14 cent
DVB="0": 7 cent
(One cent is a semi-tone divided by 100.)

	D7	D6	D5	D4	D3	D2	D1	D0
BDH		DVB						

(REGISTER ARRAY 0)



■ 20-35H PERCUSSIVE SOUND/NON-PERCUSSIVE SOUND

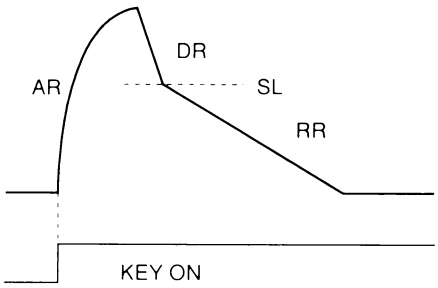
EGT="0": Non-percussive sound
EGT="1": Percussive sound

	D7	D6	D5	D4	D3	D2	D1	D0
20 – 35H			EGT					

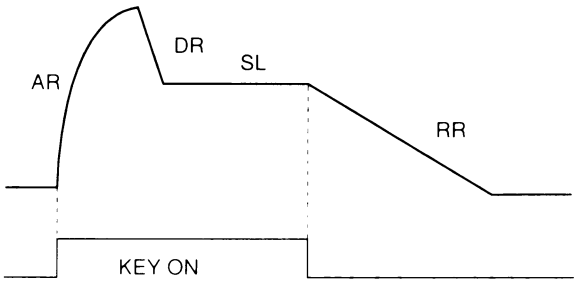
(REGISTER ARRAY 0, 1)

The envelop waveform of each mode is shown below.

□ Percussive sound



□ Non-percussive sound



■ 20-35H RATE KEY SCALE

Rate key scaling is carried out by setting KSR to "1". "Key scaling" simulates the phenomena that speeds up the rise and fall of the sound as the interval of natural musical instruments increases.

	D7	D6	D5	D4	D3	D2	D1	D0
20 – 35H				KSR				

(REGISTER ARRAY 0, 1)

□ Relation between rate value and actual time

The actual ATTACK, DECAY, and RELEASE times are the sum of the rate value and the offset by key scaling shown below.
The offset Rof by key scale (KSR) value is shown in the table below.

Key scale value		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Rof	KSR = 0	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
	KSR = 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

* For the key scale Nos., see the section "08H KEYBOARD SPLIT".

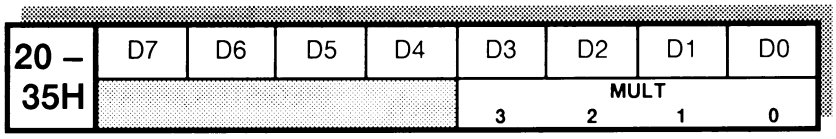
To find the actual rate time, calculate the following RATE value and refer to the "Rate Value and Actual Time Table".
The rate is found from the following equation:

RATE=(Rate value) × 4 + Rof
Where, (when (rate value) = 0, RATE = 0.

When the RATE value exceeds 63, RATE is set to 63.

■ 20-35H MULT

MULT specifies the multiplier for the frequency set by BLOCK and F-NUMBER.



(REGISTER ARRAY 0, 1)

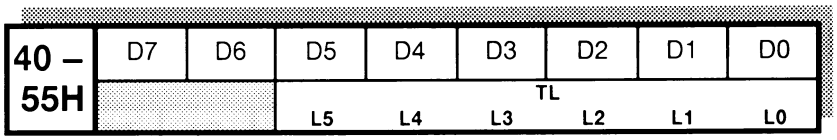
The actual frequency of each operator is the product of the specified frequency multiplied by the multiplier shown in the table below.

MULT determines the frequency ratio between operators.

MULT	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Multiplier	1/2	1	2	3	4	5	6	7	8	9	10	10	12	12	15	15

■ 40-55H TOTAL LEVEL

Total level sets the damping for the envelop.
It controls the volume and modulation rate.



(REGISTER ARRAY 0, 1)

Total level is given by the following equation:
TL [dB] = (–24 × L5) + (–12 × L4) + (–6 × L3) + (–3 × L2) + (–1.5 × L1) + (–0.75 × L0)

■ 40-55H LEVEL KEY SCALE

For natural musical instruments, the volume decreases as the interval increases. Level key scale simulates this phenomena.

40 – 55H	D7	D6	D5	D4	D3	D2	D1	D0
	KSL 1	0						

(REGISTER ARRAY 0, 1)

The damping for each octave is set by KSL set value.
The relation between set value and damping is shown below.

KSL	0	1	2	3
Damping	0	3 dB/oct	1.5 dB/oct	6 dB/oct

The actual level damping is determined by splitting one octave into 16 parts by the value of the higher four bits of F-NUMBER.

The damping rate shown below is the damping for 3dB/oct.

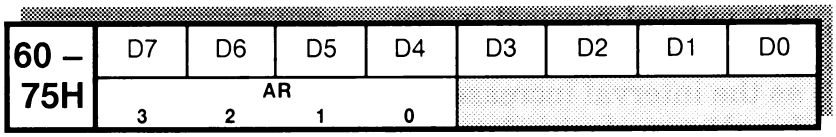
(Units: dB)

oct / F_NUM	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	3.000	6.000	9.000
2	0	0	0	0	3.000	6.000	9.000	12.000
3	0	0	0	1.875	4.875	7.875	10.875	13.875
4	0	0	0	3.000	6.000	9.000	12.000	15.000
5	0	0	1.125	4.125	7.125	10.125	13.125	16.125
6	0	0	1.875	4.875	7.875	10.875	13.875	16.875
7	0	0	2.625	5.625	8.625	11.625	14.625	17.625
8	0	0	3.000	6.000	9.000	12.000	15.000	18.000
9	0	0.750	3.750	6.750	9.750	12.750	15.750	18.750
10	0	1.125	4.125	7.125	10.125	13.125	16.125	19.125
11	0	1.500	4.500	7.500	10.500	13.500	16.500	19.500
12	0	1.875	4.875	7.875	10.875	13.875	16.875	19.875
13	0	2.250	5.250	8.250	11.250	14.250	17.250	20.250
14	0	2.625	5.625	8.625	11.625	14.625	17.625	20.625
15	0	3.000	6.000	9.000	12.000	15.000	18.000	21.000

For 1.5dB/oct, the damping is 1/2 the above and for 3.0dB/oct, the damping is double the above.

■ 60-75H AR

This register specifies the attack rate.

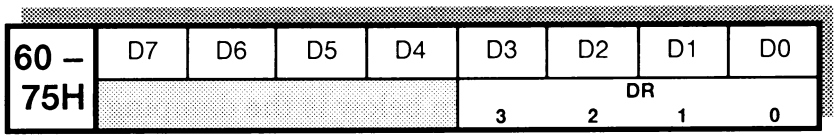


(REGISTER ARRAY 0, 1)

The set value is 0 to 15. The larger the value, the shorter the rise time of the sound.
To find the actual rate time, see the sections "$20-35H RATE KEY SCALE" and "Rate Value and Actual Time Table".
For the envelop flag, see the section "Envelop".

■ 60-75H DR

Specifies the decay rate.
The set value is 0 to 15. The larger the set value, the shorter the time.

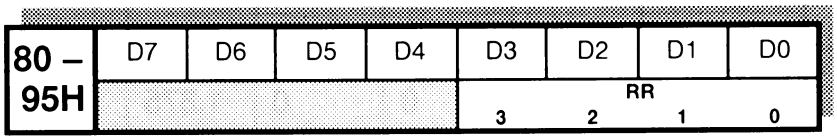


(REGISTER ARRAY 0, 1)

To find the actual rate time, see the sections "$20-35H RATE KEY SCALE" and "Rate Value and Actual Time Table".

■ 80-95H RR

Specifies the release rate.
The set value is 0 to 15. The larger the set value, the shorter the time.

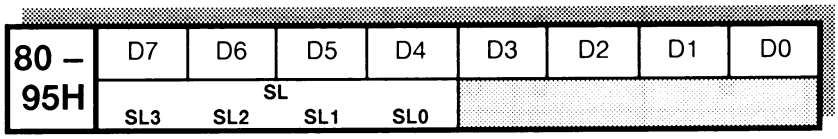


(REGISTER ARRAY 0, 1)

To find the actual rate time, see the sections "$20-35H RATE KEY SCALE" and "Rate Value and Actual Time Table".

■ 80-95H SL

Specifies the sustain level.
The sustain level is the transition point which holds the level after the decay reaches the set level when the envelop is a non-percussive sound.
During damping, it is the transition point from decay to release rate.



(REGISTER ARRAY 0, 1)

The sustain level (SL) is represented by damping amount as follows:
SL [dB] = (–24 × SL3) + (–12 × SL2) + (–6 × SL1) + (–3 × SL0)

When all bits are "1", SL is set to –93dB.

■ A0-A8H, B0-B8H F_NUMBER

This register determines the frequency information for one octave.
The set value is 0 to 1023.

	D7	D6	D5	D4	D3	D2	D1	D0
A0 – A8H	F_NUMBER							
	F7	F6	F5	F4	F3	F2	F1	F0

	D7	D6	D5	D4	D3	D2	D1	D0
B0 – B8H							F_NUMBER	
							F9	F8

(REGISTER ARRAY 0, 1)

■ B0-B8H BLOCK

"BLOCK" is the octave information.
The set value is 0 to 7 octaves.

	D7	D6	D5	D4	D3	D2	D1	D0
B0 – B8H				BLOCK				
				B2	B1	B0		

(REGISTER ARRAY 0, 1)

The F_NUMBER setting can be found from the desired frequency and set BLOCK value.

The relation of the desired frequency, F_NUMBER, and BLOCK is given by the following equation:

$$\text{F\_NUMBER} = \frac{(\text{Desired frequency}) \times 2^{19} \div (\text{Sampling frequency}/684)}{2^{\text{BLOCK}-1}}$$

Examples of F_NUMBER setting using the F_NUMBER equation are shown below. (BLOCK value is "4".)

Note	Frequency	F_NUMBER	Note	Frequency	F_NUMBER
C	261.6	346	G	392.0	519
C#	277.2	367	G#	415.3	550
D	293.7	389	A	440.0	582
D#	311.1	412	A#	466.2	617
E	329.6	436	B	493.9	654
F	349.2	462	C	523.3	693
F#	370.0	490			

F_NUMBER can also be set to other than the above.
However, when the F_NUMBER setting is small, the difference between the frequency generated by the YMF278B and the frequency of the note becomes large.

■ B0-B8H KEY ON

This register controls sound generation.
"1": Key on
"0": Key off

	D7	D6	D5	D4	D3	D2	D1	D0
B0 – B8H			KEY ON					

(REGISTER ARRAY 0, 1)

■ BDH RHY (RHYTHM)

When RHY is set to "1", slots 13 to 18 are set to the rhythm mode.

	D7	D6	D5	D4	D3	D2	D1	D0
BDH			RHY					

(REGISTER ARRAY 0)

■ BDH RHYTHM INSTRUMENT SELECTION

This register controls sound generation of each rhythm. When the bit corresponding to the each musical instrument is set to "1" after RHY is set to "1" (rhythm), sound is generated.

	D7	D6	D5	D4	D3	D2	D1	D0
BDH				BD	SD	TOM	TC	HH

(REGISTER ARRAY 0)

The slot No. used by each rhythm instrument is shown below.
Set the rate, etc. to match the special features of each musical instrument.

Rhythm instrument	Slot No.
Bass drum (BD)	13, 16
Snare drum (SD)	17
Tom-tom (TOM)	15
Top cymbal (TC)	18
High hat (HH)	14

When a slot is set to the rhythm mode, set KEY ON of slots 13 to 18 to "0".

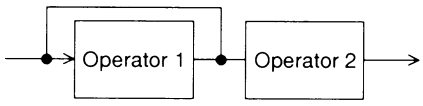
■ C0-C8H CNT

This register selects the algorithm.
"Algorithm" is a combination (connection form) of operators.

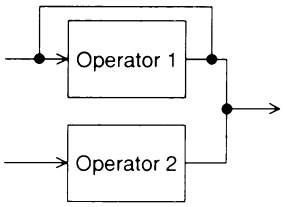
C0 – C8H	D7	D6	D5	D4	D3	D2	D1	D0
								CNT

(REGISTER ARRAY 0, 1)

□ Two-operator mode
When CNT is set to "0", algorithm 1 is selected. When CNT is set to "1", algorithm 2 is selected.



Algorithm 1



Algorithm 2

Registers C0 to C8H are set for each channel. Therefore, select algorithm 1 and 2 at each channel.

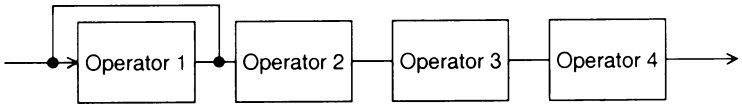
□ Four-operator mode
To select the four-operator mode, CONNECTION SEL of 05H (REGISTER ARRAY 1) is set and four algorithms are selected by setting two CNT bits.

The two CNT bits needed in algorithm selection at each channel are shown in the table below.

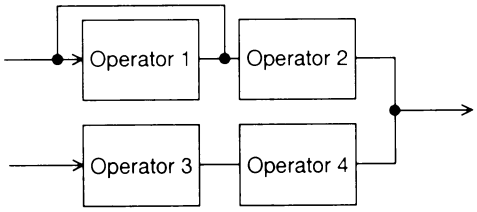
A1	Channel No.	Set CNT bit register	
		CNT_n	CNT_{n+3}
0	1	C0H	C3H
	2	C1H	C4H
	3	C2H	C5H
1	4	C0H	C3H
	5	C1H	C4H
	6	C2H	C5H

The algorithm form by CNT_n and CNT_{n+3} combination is shown on the next page.

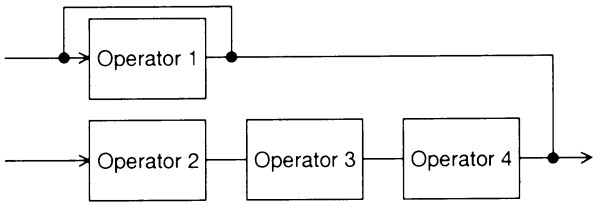
○ Algorithm 1 CNT_n = "0" CNT_{n+3} = "0"



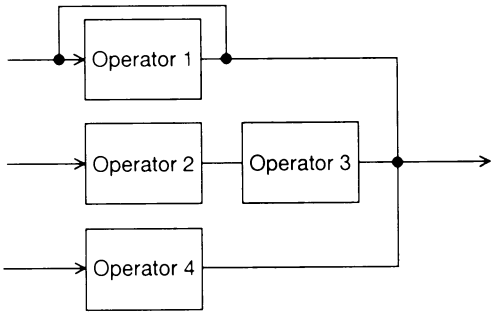
○ Algorithm 2 CNT_n = "0" CNT_{n+3} = "1"



○ Algorithm 3 CNT_n = "1" CNT_{n+3} = "0"



○ Algorithm 4 CNT_n = "1" CNT_{n+3} = "1"



■ C0-C8H FEEDBACK

Feedback modulation can be applied to slot 1 of each channel.

C0 – C8H	D7	D6	D5	D4	D3	D2	D1	D0
					FB 2	FB 1	FB 0	

(REGISTER ARRAY 0, 1)

When feedback modulation is used, string instrument sounds can be created.

The feedback modulation modulation rate can be selected by FB setting.
The relation between FB value and modulation rate is shown below.

FB	0	1	2	3	4	5	6	7
Modulation rate	0	π/16	π/8	π/4	π/2	π	2π	4π

■ C0-C8H OUTPUT CHANNEL SELECTION

A total of four channels are output from the FM synthesizer.

C0 – C8H	D7	D6	D5	D4	D3	D2	D1	D0
	CHD	CHC	CHB	CHA				

(REGISTER ARRAY 0, 1)

Each bit "1": Output
"0": Not output

☐ CHA, CHB

The FM synthesizer output is digitally mixed with the wave table synthesis of the channel at which the CH bit of the wave table synthesizer register $68 to 7FH is set to "0" and is output from the DO2 pin.
CHA is mixed with the wave table synthesis Lch and CHB is mixed with the wave table synthesis Rch.

☐ CHC, CHD

The output set by CHC and CHD is output from the DO0 pin.
Since FM is output from the DO0 pin and PCM is output from the DO1 pin, a sound effect can be applied to a certain sound by connecting an YSS225 to the DO0 and DO1 pins. Of course, a D/A converter can also be connected.

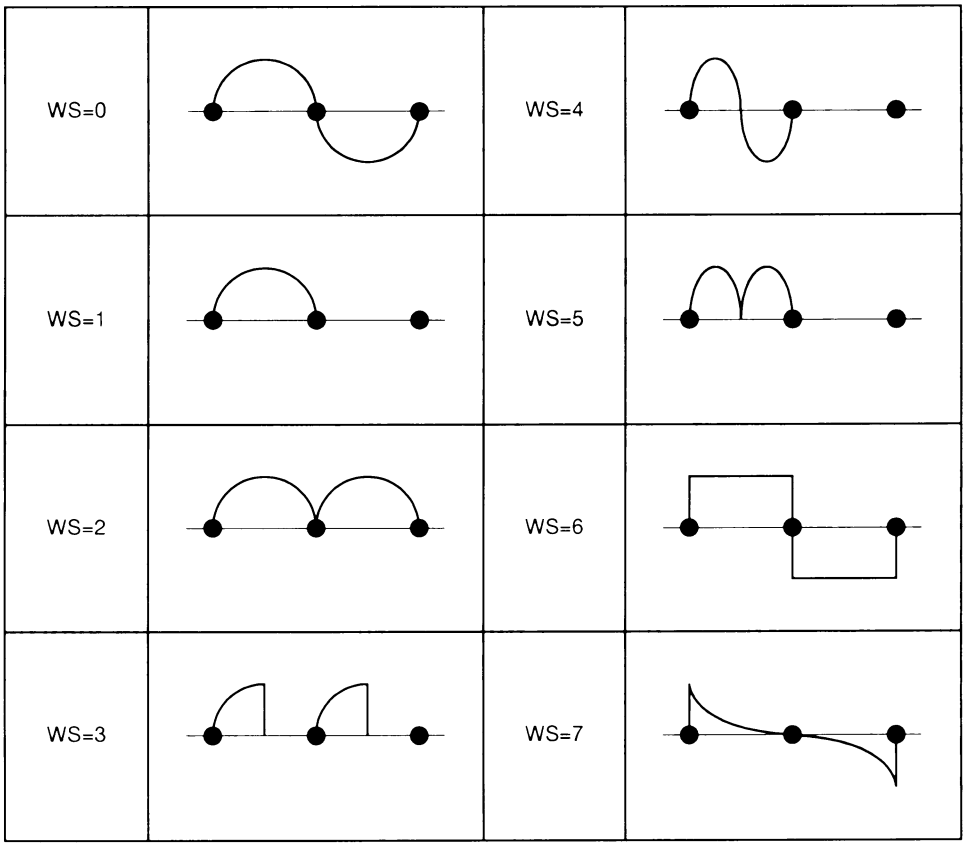
■ E0-F5H WAVE SELECT

The waveform used in FM operation can be set for each slot.
This allows the generation of complex sounds.

E0 – F5H	D7	D6	D5	D4	D3	D2	D1	D0
						WS 2	WS 1	WS 0

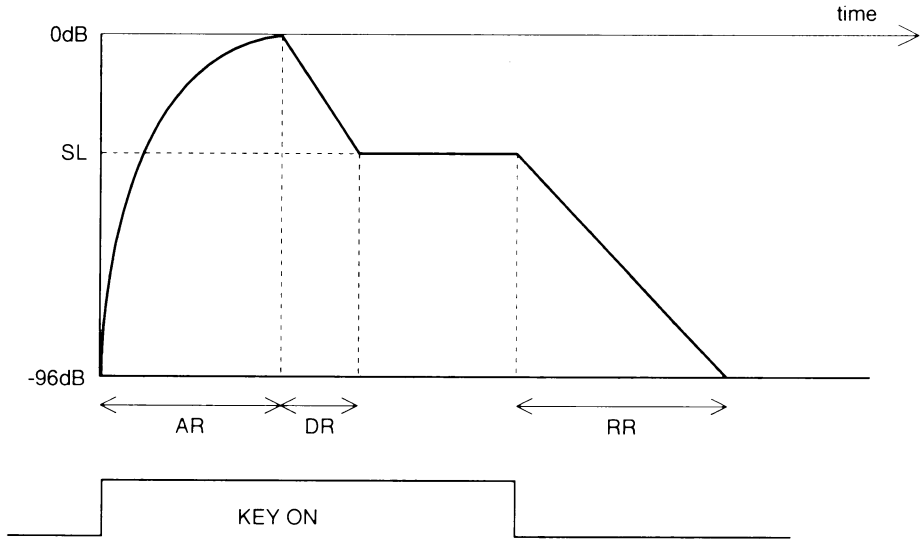
(REGISTER ARRAY 0, 1)

The relation between WS value and selectable waveform is shown below.
When this LSI is used in the OPL2 mode, only WS0 to WS3 can be selected.



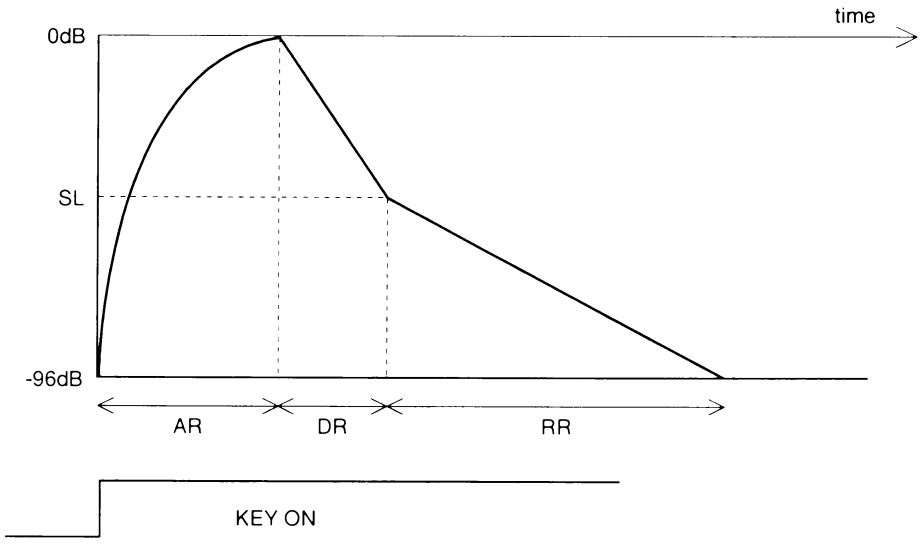
ENVELOP GRAPH (FM)

☐ Non-percussive sound envelop



This envelop has a dynamic range of 96dB (resolution: 0.1875dB) and is expressed by damping amount.
The attack rate changes exponentially by time from key on to 0dB.
When 0dB is reached, attack rate is switched to decay rate. Decay rate changes linearly by time up to the sustain level.
At key off, the rate switches to release rate. Release rate changes linearly with the time from the sustain level to –96dB.

☐ Damping sound envelop



The attach rate changes exponentially with the time from key on to 0dB.
When 0dB is reached, attach rate is switched to decay rate. Decay rate changes linearly with the time up to the sustain level. Release rate changes linearly with the time from the sustain level to –96dB.
Transition to release rate is unrelated to KEY ON.

RATE VALUE AND ACTUAL TIME TABLE

■ Attack rate

(Units: ms)

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
0	∞	∞
1	∞	∞
2	∞	∞
3	∞	∞
4	2826.24	1482.75
5	2252.80	1155.07
6	1884.16	991.23
7	1597.44	868.35
8	1413.12	741.38
9	1126.40	577.54
10	942.08	495.62
11	798.72	434.18
12	706.56	370.69
13	563.20	288.77
14	471.04	247.81
15	399.36	217.09
16	353.28	185.34
17	281.60	144.38
18	235.52	123.90
19	199.68	108.54
20	176.76	92.67
21	140.80	72.19
22	117.76	61.95
23	99.84	54.27
24	88.32	46.34
25	70.40	36.10
26	58.88	30.98
27	49.92	27.14
28	44.16	23.17
29	35.20	18.05
30	29.44	15.49
31	24.96	13.57

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
32	22.08	11.58
33	17.60	9.02
34	14.72	7.74
35	12.48	6.78
36	11.04	5.79
37	8.80	4.51
38	7.36	3.87
39	6.24	3.39
40	5.52	2.90
41	4.40	2.26
42	3.68	1.94
43	3.12	1.70
44	2.76	1.45
45	2.20	1.13
46	1.84	0.97
47	1.56	0.85
48	1.40	0.73
49	1.12	0.61
50	0.92	0.49
51	0.80	0.43
52	0.70	0.37
53	0.56	0.31
54	0.46	0.26
55	0.42	0.22
56	0.38	0.19
57	0.30	0.14
58	0.24	0.11
59	0.20	0.11
60	0.00	0.00
61	0.00	0.00
62	0.00	0.00
63	0.00	0.00

■ Decay and release rates

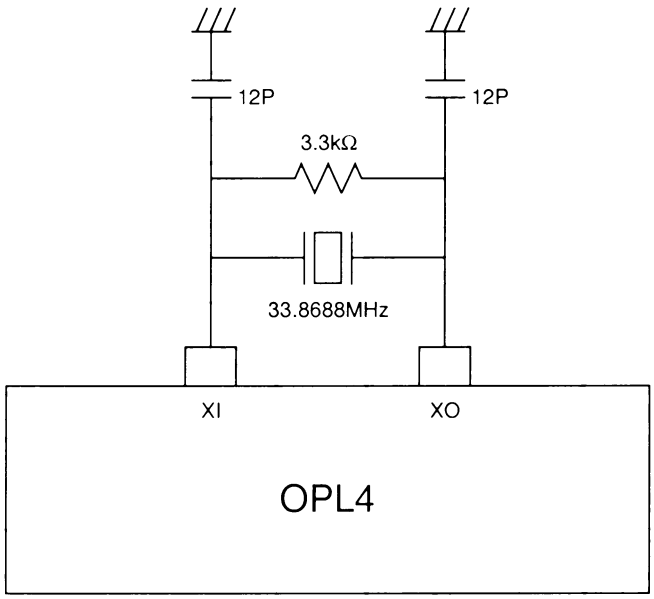
(Units: ms)

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
0	∞	∞
1	∞	∞
2	∞	∞
3	∞	∞
4	39280.64	8212.48
5	31416.32	6574.08
6	26173.44	5509.12
7	22446.08	4730.88
8	19640.32	4106.24
9	15708.16	3287.04
10	13086.72	2754.56
11	11223.04	2365.44
12	9820.16	2053.12
13	7854.08	1643.52
14	6543.36	1377.28
15	5611.52	1182.72
16	4910.08	1026.56
17	3927.04	821.76
18	3271.68	688.64
19	2805.76	591.36
20	2455.04	513.28
21	1936.52	410.88
22	1635.84	344.34
23	1402.88	295.68
24	1227.52	256.64
25	981.76	205.44
26	817.92	172.16
27	701.44	147.84
28	613.76	128.32
29	490.88	102.72
30	488.96	86.08
31	350.72	73.92

RATE	Time (0 ~ 100%)	Time (10 ~ 90%)
32	306.88	64.16
33	245.44	51.36
34	204.48	43.04
35	175.36	36.96
36	153.44	32.08
37	122.72	25.68
38	102.24	21.52
39	87.68	18.48
40	76.72	16.04
41	61.36	12.84
42	51.12	10.76
43	43.84	9.24
44	38.36	8.02
45	30.68	6.42
46	25.56	5.38
47	21.92	4.62
48	19.20	4.02
49	15.36	3.22
50	12.80	2.68
51	10.96	2.32
52	9.60	2.02
53	7.68	1.62
54	6.40	1.35
55	5.48	1.15
56	4.80	1.01
57	3.84	0.81
58	3.20	0.69
59	2.74	0.58
60	2.40	0.51
61	2.40	0.51
62	2.40	0.51
63	2.40	0.51

INPUT CLOCK

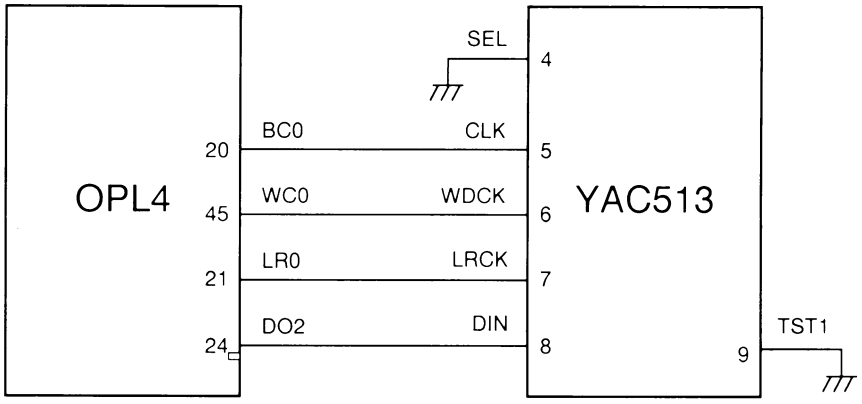
Connect a 33.8688MHz crystal oscillator to the XI and XO pins.
Rate, pitch, and everything else related to frequency are based on this clock.
An input clock circuit reference example is shown below.



CONNECTION TO D/A CONVERTER AND EFFECT PROCESSOR

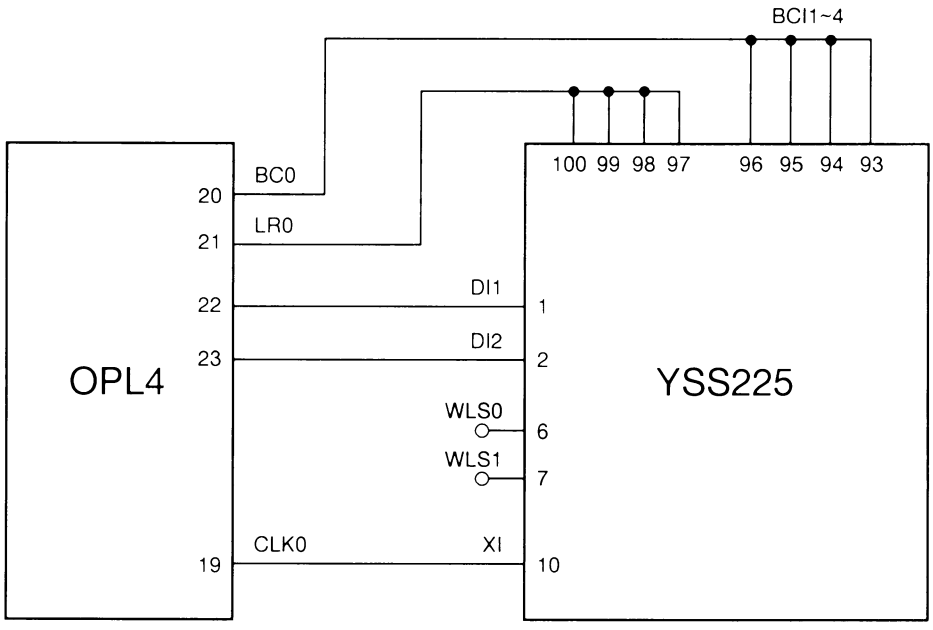
This section describes how OPL4 and YAC513 OPL4-dedicated DAC are connected. Connection examples are shown below.

OPL4 outputs three serial data (DO0-DO2).
Basically, DO0 to DO2 can connect to pin 8 (SD) of the YAC513.
However, a sound effect should be applied to a specified sound by connecting DO2 to the YAC513 and connecting DO0 and DO1 to the YSS225.



The method of connecting the YSS225 Effect Processor, which applies reverberation, echo, and other effects to the OPL4 wave table, is described below.

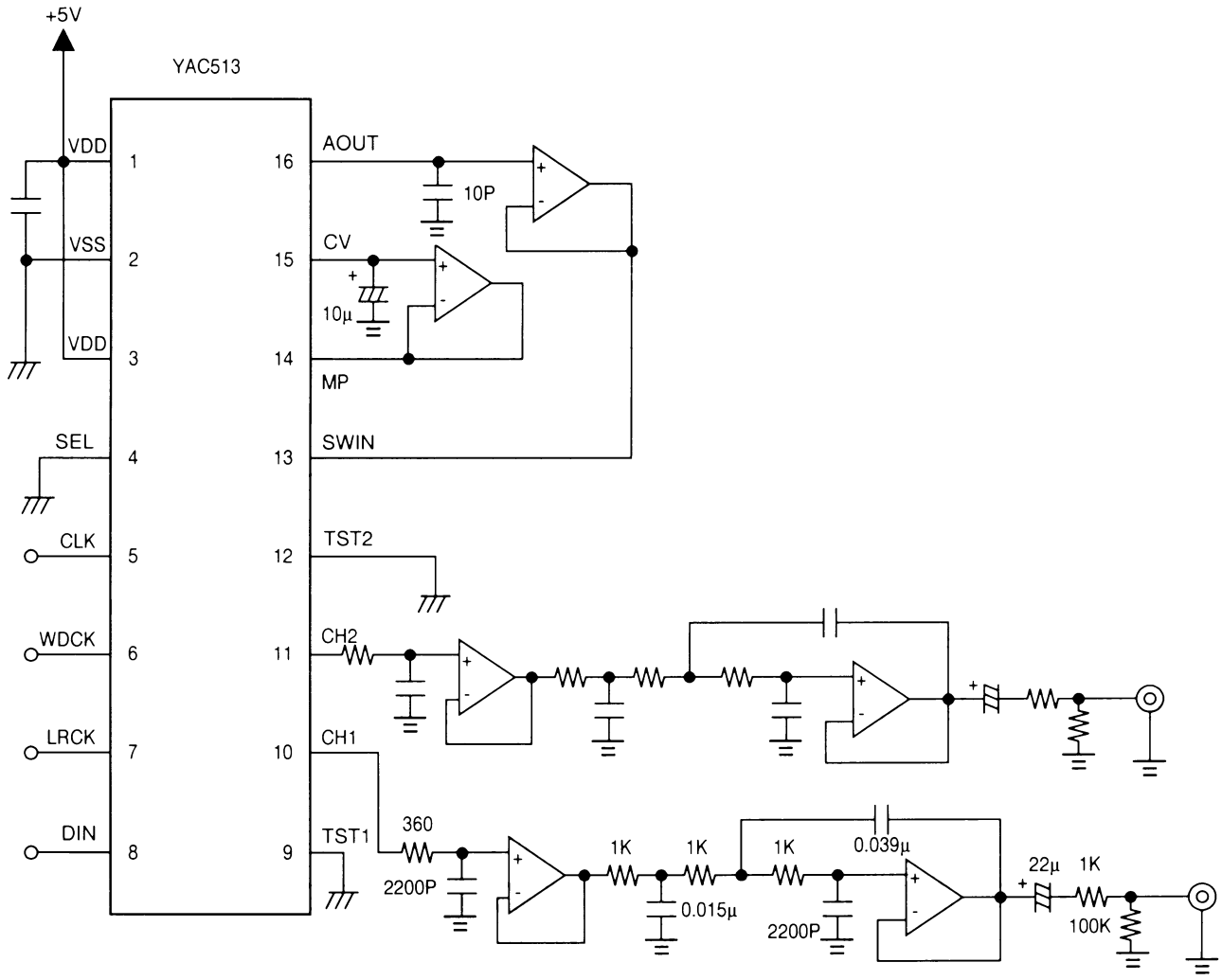
A connection example is shown below.



Note: Do not connect YSS225 pins 6 and 7.
(WLS0,1...input data length (16/18bit) switching.)

DAC OUTPUT CIRCUIT EXAMPLE

A DAC (YAC513) output circuit example is shown below.



The CH1 and CH2 low-pass filters are the same circuit.
The low-pass filter cutoff frequency should be about 15 to 20kHz.

AUDIO OUTPUT INTERFACE

The YMF278B output data is 16-bit 2's complement digital data.
The data is MSB first output. The sampling frequency is 44.1kHz.
The data output from each pin is shown below.

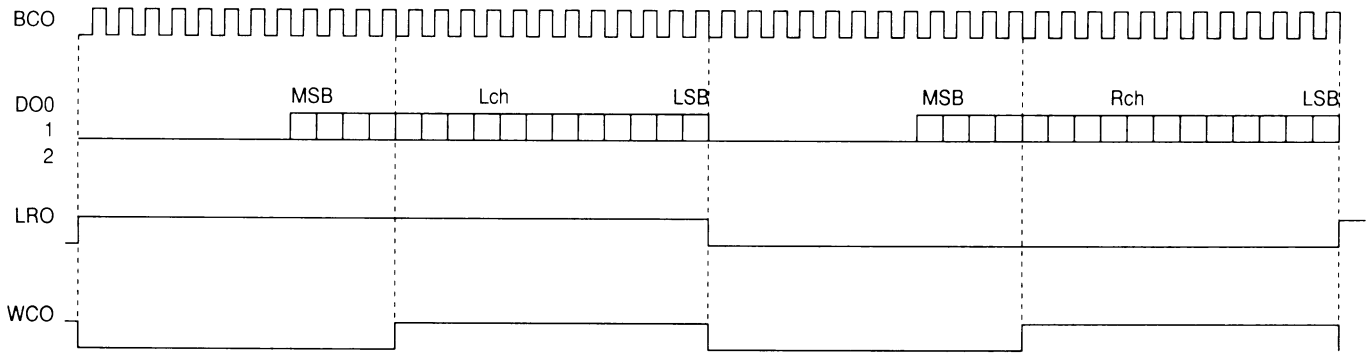
- DO0 pin: FM sound only (Sound of channel set by CHC and CHD of FM registers $C0 to C8H is output.)
  When CHC is set, sound is output to Lch.
  When CHD is set, sound is output to Rch.

- DO1 pin: Wave table sound only. (Sound of channel set at CH="1" of wave table registers $68 to 7FH is output.)

- DO2 pin: FM and wave table mixed data. (Sound of channel set by CHA and CHB of FM registers $C0 to C8H and sound of channel set at CH="0" of wave table registers $68 to 7FH are mixed and output.)
  When CHA is set, sound is output to Lch.
  When CHB is set, sound is output to Rch.

The YSS225 Effect Processor and YMF278B dedicated DAC are available from YAMAHA to apply effects (echo, reverberation, etc.) to the output sound.

OUTPUT TIMING



The BCO frequency is 48fs. Its duty is 50%. (fs=44.1kHz)
DO0, DO1, and DO2 fs is 44.1kHz.
The LRO frequency is fs. Its duty is 50%.
The WCO frequency is 2fs. Its duty is 50%.

ELECTRICAL CHARACTERISTICS

■ Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	–0.3 ~ 7.0	V
Input voltage	V_{IN}	–0.3 ~ V_{DD}+0.5	V
Operating ambient temperature	T_{OP}	0 ~ 70	°C
Storage temperature	T_{STG}	–50 ~ 125	°C

■ Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating ambient temperature	T_{OP}	0	25	70	°C

■ DC characteristics (conditions : Ta = 0~70°C, V_{DD} = 5.0±0.25V)

Item	Symbol	Condition	Min.	Max.	Unit
Power consumption	P_D	V_{DD} = 5.0V f_M = 33.8688MHz		250	mW
High level input voltage (1) Low level input voltage (1)	V_{IH1} V_{IL1}	Applicable to /WR, /RD, /CS, A0-A2, D0-D7, MD0-MD7.	2.0	 0.8	V V
High level input voltage (2) Low level input voltage (2)	V_{IH2} V_{IL2}	Applicable to /TST1, /TST2, X1.	3.5	 1.0	V V
Input leak current	I_{LI}	0V ≦ V_{IN} ≦ V_{DD} Applicable to /WR, /RD, /CS, A0-A2, D0-D7, MD0-MD7.	–10	10	µA
Input capacitance	C_I			10	pF
High level output voltage (1) Low level output voltage (1)	V_{CH1} V_{OL1}	I_{OH} = –80µA I_{OL} = 2mA *1	V_{DD} –1.0	 V_{SS} +0.4	V V
High level output voltage (2) Low level output voltage (2)	V_{OH2} V_{OL2}	I_{OH} = 160µA I_{OL} = 4mA *2	V_{DD} –1.0	 V_{SS} +0.4	V V
Output capacitance	C_O			10	pF
Output leak current	I_{OL}	/CS = V_{IH}	–10	10	µA
Pull-up resistor	R_U	/CS, /IC, /TST1, /TST2	50	400	kΩ

*1 Applicable to D0-D7 (at output), CLKO, BCO, LRO, WCO, DO0-DO2, /MWR, /MRD, MD0-MD7 (at output).
*2 Applicable to MA0-MA20, /MCS0-/MCS9.

■ AC characteristics 1 Clock, CPU interface (conditions : Ta = 0~70°C, V_{DD} = 5.0±0.25V)

Item	Symbol	Fig.	Min.	Typical	Max.	Unit
Master clock frequency	f_{M1}	Fig1-1		33.8688		MHz
Duty	D		40		60	%
Output clock frequency	f_{M2}	Fig1-2		16.9344		MHz
Duty	D			50		%
Reset pulse width	N_{ICW}	Fig1-3	3000 *3			Cycle
Address set-up time	t_{AS}	Fig1-4, 5	5			ns
Address hold time	t_{AH}	〃	5			ns
Chip select write width	t_{CSW}	Fig1-4	50			ns
Chip select read width	t_{CSR}	Fig1-5	80			ns
Write pulse width	t_{WW}	Fig1-4	50			ns
Data set-up time	t_{WDS}	〃	10			ns
Write data hold time	t_{WDH}	〃	10			ns
Read pulse width	t_{RW}	Fig1-5	80			ns
Read data access time	t_{ACC}	〃			60	ns
Read data hold time	t_{RDH}	〃	10			ns

*3 Number of master clock cycles

□ Input clock timing

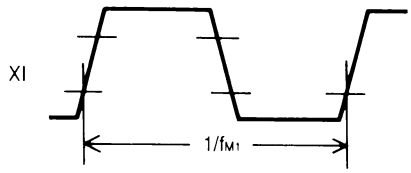


Fig. 1-1

□ Output clock timing

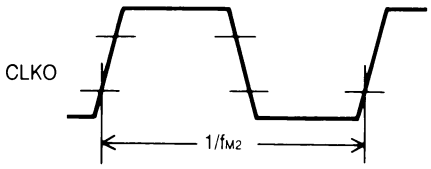


Fig. 1-2

□ Reset pulse width

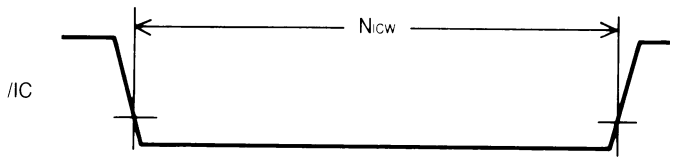
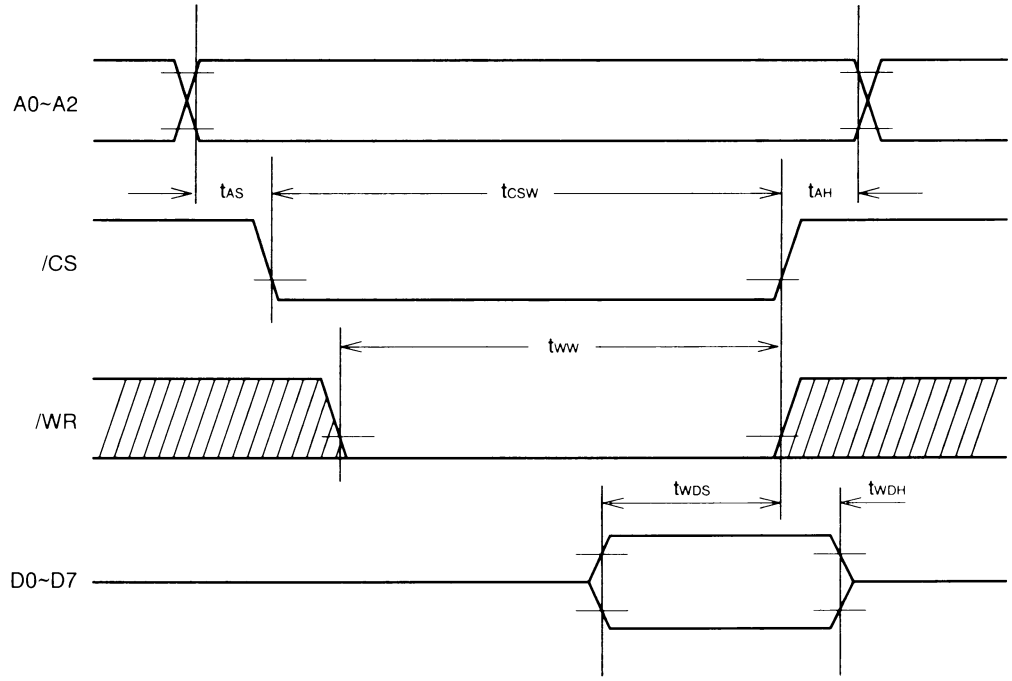


Fig. 1-3

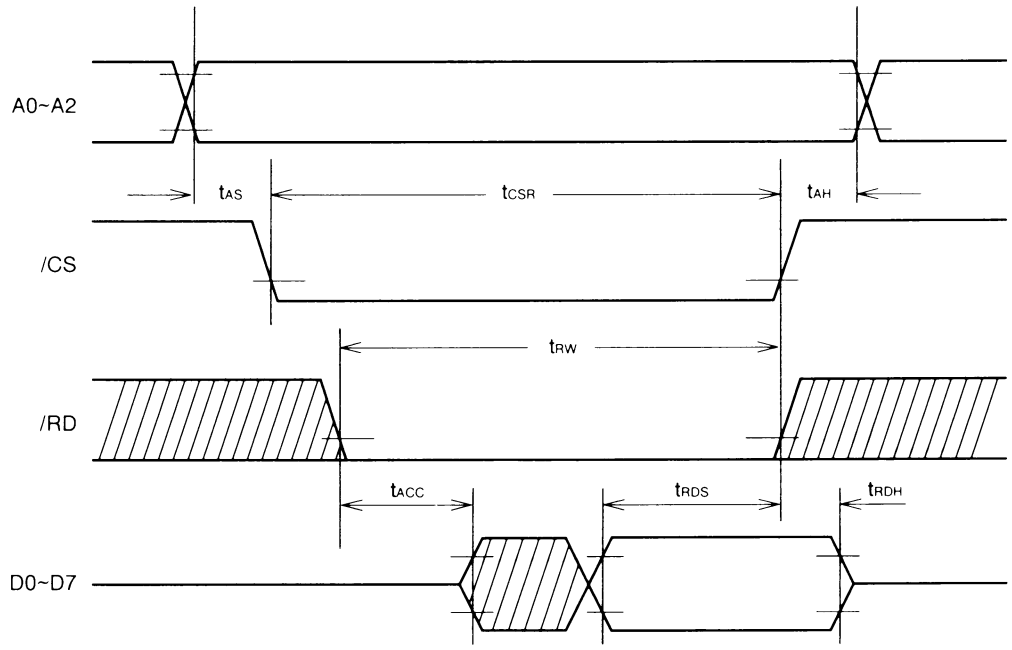
□ CPU write timing



Note: tCSW, tWW, and tWDH are based on either /CS or /WR being driven to High level.

Fig. 1-4

□ CPU read timing



Note: tACC is based on whichever of /CS or /RD goes to the Low level last.
tCSR, tRW, and tRDH are based on either /CS or /RD being driven to High level.

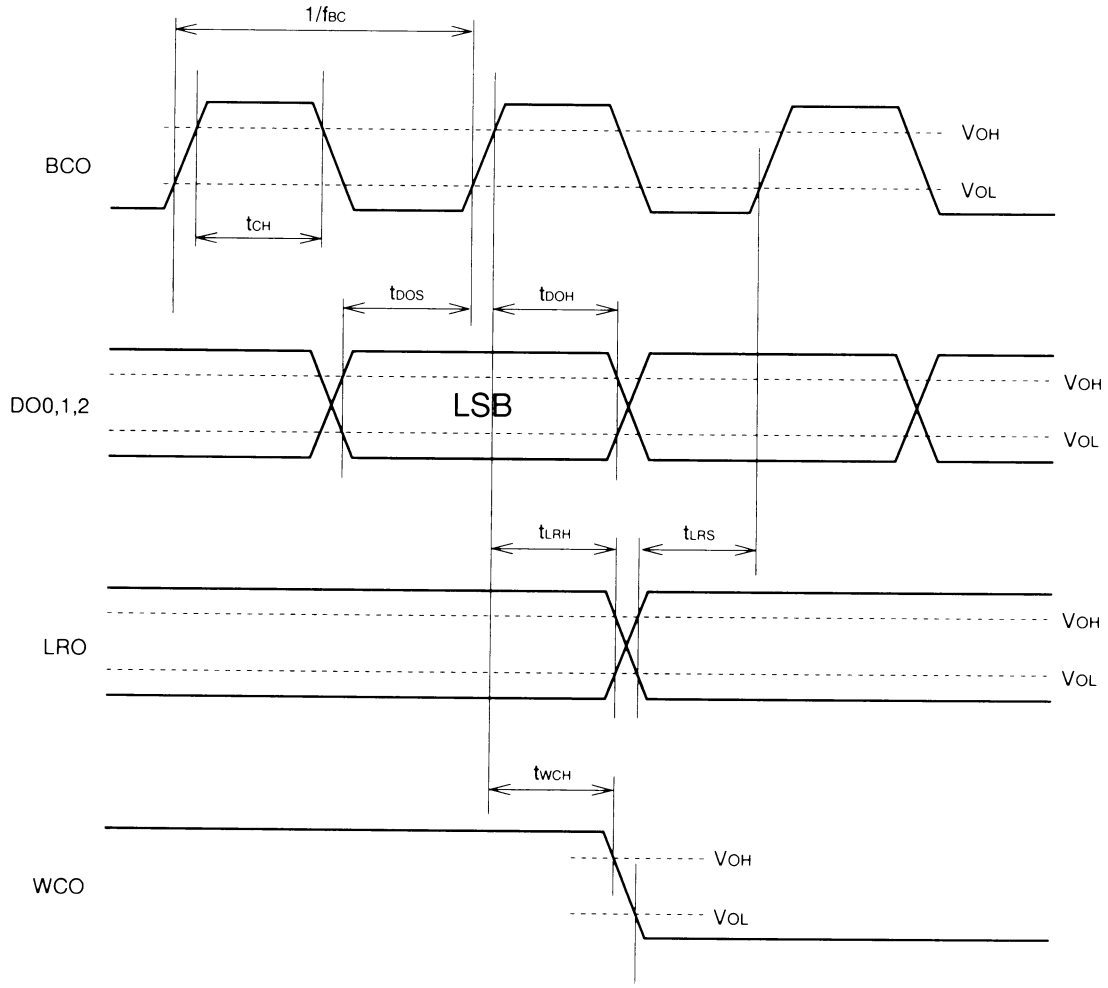
Fig. 1-5

■ AC characteristics 2 Audio interface (conditions : Ta = 0~70°C, V_{DD} = 5.0±0.25V)

Item	Symbol	Fig.	Min.	Typical	Max.	Unit
Bit clock frequency	f_{BC}	Fig1-6		48 f_S*		MHz
Bit clock high level cycle	t_{CH}	"	110			ns
Data out set-up time	t_{DOS}	"	100			ns
Data out hold time	t_{DOH}	"	280			ns
LR clock set-up time	t_{LRS}	"	100			ns
LR clock hold time	t_{LRH}	"	280			ns
Word clock hold time	t_{WCH}	"	280			ns

* f_S = 44.1 kHz

Fig. 1-6



■ AC characteristics 3 Memory interface (conditions : Ta = 0~70°C, V_{DD} = 5.0±0.25V)

Item	Symbol	Fig.	Min.	Typical	Max.	Unit
Write cycle time	t_{WC}	Fig1-7	600			ns
Address confirmation time for /MWR	t_{AW}	"	500			ns
/MCS confirmation time for /MWR	t_{CW}	"	450			ns
Write address set-up time	t_{WAS}	"	250			ns
Write recovery time	t_{WR}		50			
Write pulse width	t_{WW}	"	150			ns
Write data set-up time	t_{WDS}	"	150			ns
Write data hold time	t_{WDH}	"	5			ns
Address access time	t_{RC}	Fig1-8			150	ns
Chip enable access time	t_{CE}	"			150	ns
Output disable time	t_{DF}	"			90	ns
Read data hold time	t_{RDH}	"	0			ns

□ Memory write timing

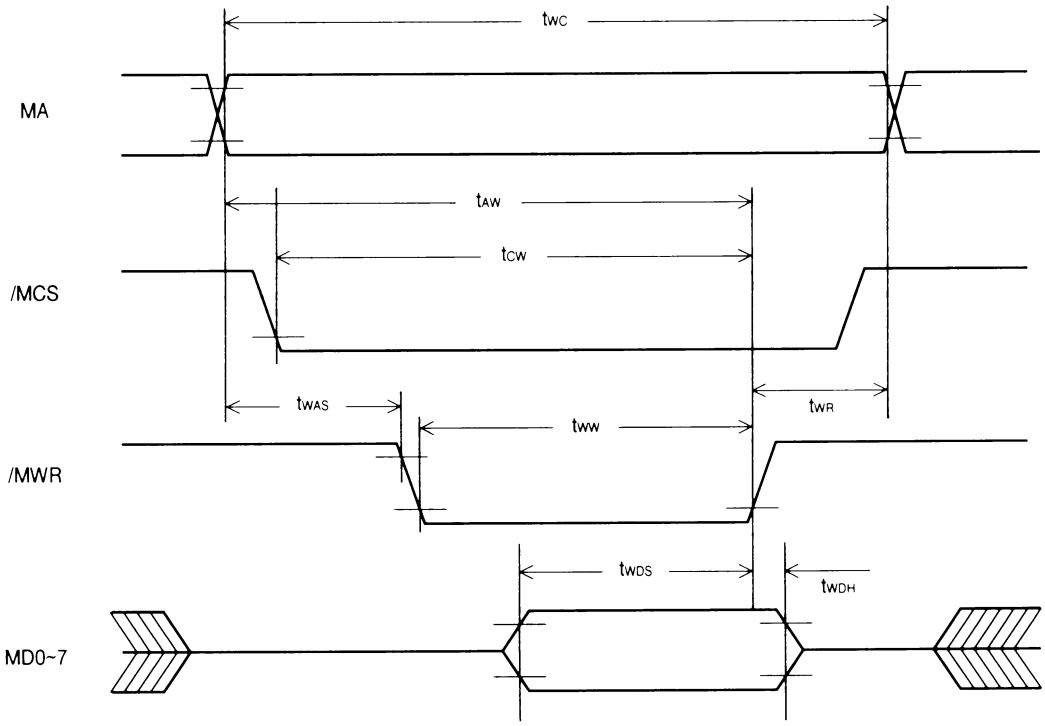


Fig. 1-7

Note: The values above are the values when the write wait cycle time was secured.

□ Memory read timing

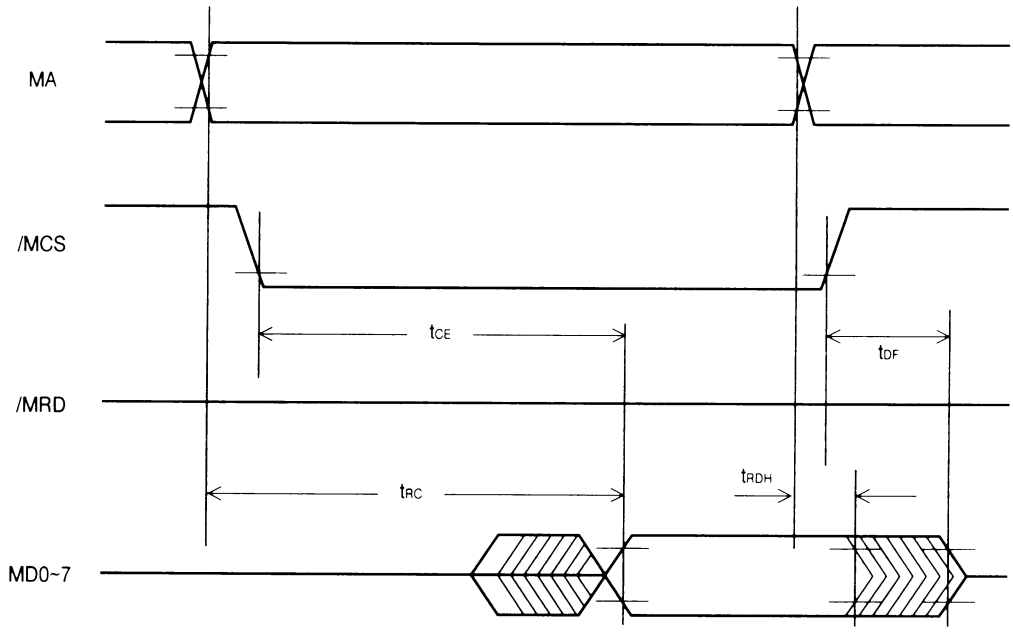


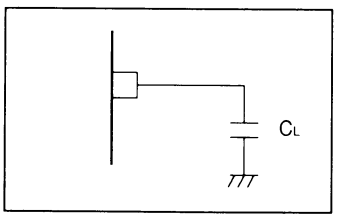
Fig. 1-8

Notes:
1. The read timing above is the memory read timing at sound generation.
2. The /MRD signal is always "L".

■ AC characteristics test conditions

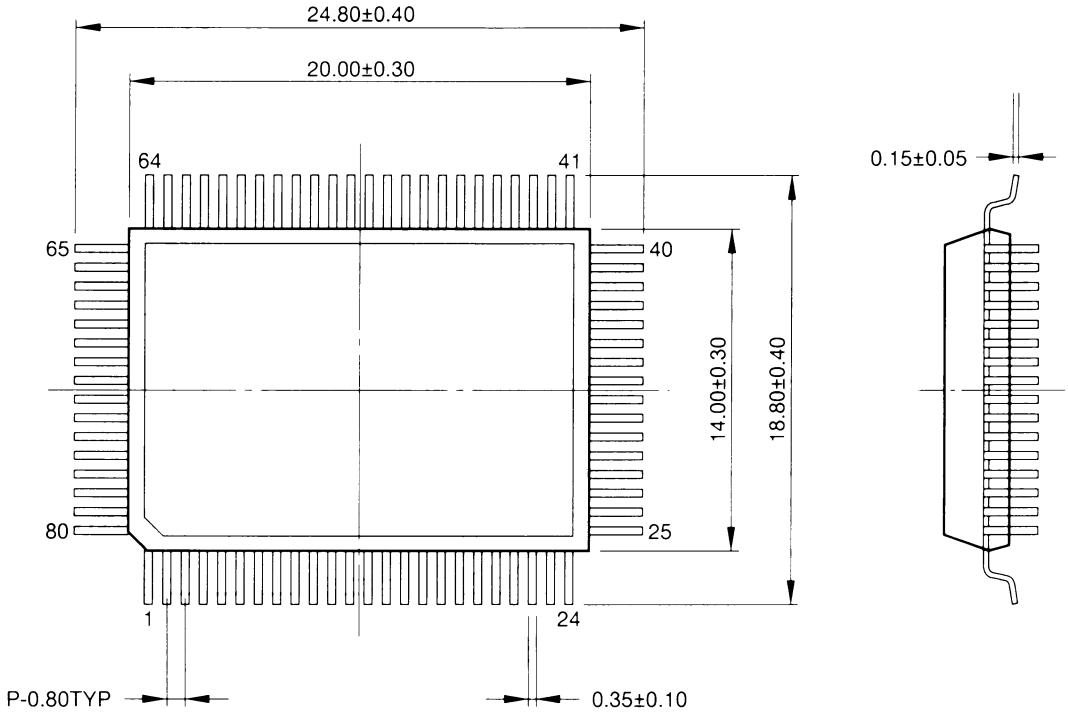
Item	
Input pulse voltage	V_{IH} = 2.4V V_{IL} = 0.4V (except XI, /TST1, /TST2) V_{IH} = 3.9V V_{IL} = 0.6V (XI, /TST1, /TST2)
Input pulse rise and fall times	t_{RF} = 5ns
Timing measurement reference voltage	V_{OH} = 0.7*VDD V_{OL} = 0.2*VDD (CLKO, BCO, LRO, WCO, DO0 ~ 2)
	V_{OH} = 2.2V V_{OL} = 0.8V (D0 ~ D7, MA0 ~ 20, /MCS0 ~ 9, MD0 ~ 7, /MWR, /MRD)
Output load	C_L = 100pF

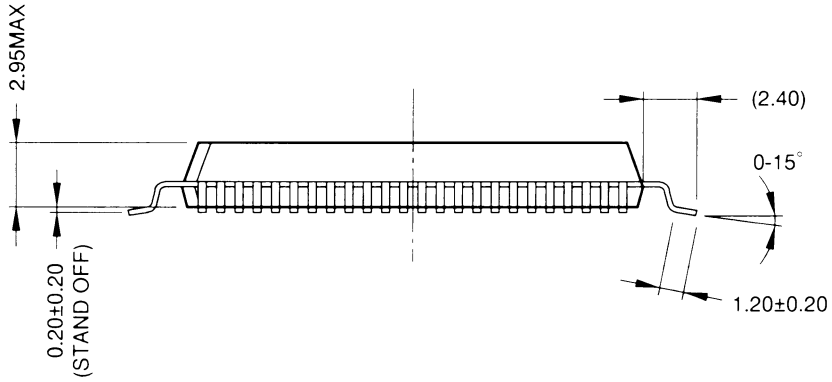
□ Output load circuit



■ EXTERNAL DIMENSIONS

• YMF278B-F





UNIT: mm

The specifications of this product are subject to improvement changes without prior notice.

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