YAMAHA LSI

Y8950

APPLICATION MANUAL

(MSX-AUDIO)

YAMAHA

Y8950アプリケーションマニュアル
CATALOG No. : LSI-2[illegible]8950X

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I. INTRODUCTION

I-1 Outline of MSX-AUDIO

The MSX-AUDIO is a sound generator LSI developed as optional sound source for the MSX2 personal computer. To create realistic, exciting sounds, the MSX-AUDIO incorporates an FM sound generator, similar to that previously used in Yamaha Electones and the DX-7 synthesizer. This product also has ADPCM voice analysis/synthesis functions in addition to the composite sinusoidal modeling function of conventional FM sound generators.

This new function allows simplified sound data processing.

Either of the AD/DA converters built in the analysis/synthesis circuit can be used independently to process even analog data.

The MSX-AUDIO is equipped with input/output ports for a keyboard interface, as well as general-purpose input/output ports.

Consequently, one MSX-AUDIO unit allows you to perform a variety of data processing for sound production.

I-2. Features

* Realistic sound due to FM sound generator. The FM sound generator is compatible with the YM3526.
* Selection of two sound-generation modes: simultaneous sounding of nine tones or six melodies and five rhythms (compatible with the Character and Pattern Telephone Access Information Network system and Teletex)
* The vibrato and AM oscillators are built in.
* 4-bit ADPCM voice analysis/synthesis circuits are built-in.
* AD/DA converters are built in.
* External 256-Kbytes memory (ROM or RAM) can be connected (as ADPCM data storage or auxiliary CPU storage)
* 8-bit input/output ports are built in for keyboard scanning.
* Built-in general-purpose 4-bit input/output ports
* Two built-in general-purpose timers
* TTL compatible input/output
* Si-gate CMOS LSI
* 5V single power supply

I-3. Outline of FM Sound Generator

The FM (frequency modulation) sound generation uses higher harmonics, produced during signal modulation, to compose sounds. This sound generation method only requires a relatively simple circuit, although can generate waveforms with higher harmonics, including non-harmonic components. And because the modulation indexes correspond much more naturally to the spectrum distribution of higher harmonics, the FM sound generator can be used to generate a variety of sounds -- from acoustic instrument sounds to electronic instrument sounds.

The frequency modulation can be expressed by using four parameters as follows:

$$F = A \sin(\omega ct + I \sin \omega mt) \quad (1)$$

Here, "A" indicates the output amplitude, "I" indicates the modulation index, and "wc" and "wm" indicate the circular frequencies of the carrier wave and modulator, respectively.

This expression (1) can be transformed to:

$$F = A\{Jo(I)\sin \omega ct + J_1(I)\{\sin(\omega c+\omega m)t - \sin(\omega c-\omega m)t\} + J_2(I)\{\sin(\omega c+2\omega m)t + \sin(\omega c-2\omega m)t + \cdots\cdots\} \quad (2)$$

In expression (2), "Jn (I)" indicates the first Bessel function of the nth degree. As shown by the expression, each harmonic amplitude is given by the Bessel function for corresponding amplitude index. Therefore, note that the frequency modulation with expression (1) is extremely useful to generate specific instrument sound and effect notes. However, this type of frequency modulation does not create a uniform distribution of higher harmonics, and is not suitable for generating string instrument sound. A new frequency modulation method "feedback FM" has been developed to overcome this drawback. This is indicated by the expression below.

$$F = A \sin(\omega ct + \beta F) \quad (3)$$

"ß" indicates the feedback rate. This feedback FM generates a saw-tooth wave for a higher harmonic spectrum so that it is also suited for string sounds.

The above-mentioned FM sound generation requires the following three functional blocks:

a. Phase generator (PG) to generate wt

b. IEnvelope generator (EG) to obtain amplitude A and modulation index I as time functions

c. Sine table (sin)

The FM sound generation can be diagramed as in Fig. I-1 by combining the above three-block components in one unit. When this unit (operator cell:OP) design is used, FM sound generation can be performed by specifying the frequency and EG parameters in each unit and creating data for the combined.

I-4. Outline of ADPCM Voice Analysis/Synthesis

The MSX-AUDIO has two different voice data processing functions:

adaptive differential pulse code modulation (ADPCM), which specifies voice analysis/synthesis and synthesizes realistic sound, and composite sinusoidal modeling, which requires complicated processing (using a computer) for data analysis, but less memory capacity for synthesis. ADPCM voice analysis/synthesis, which is the major feature of the MSX-AUDIO along with the FM sound generator, is outlined as follows:

ADPCM is a voice analysis/synthesis method in which the difference between actual data and expected data is encoded using a quantization width (adaptive quantization width) that changes according to waveform variation. This method prevents the synthesized voice from deterioration and reduces the number of required data bits. The encoding and decoding processes are described as follows:

(a) Voice analysis

The MSX-AUDIO converts 8-bit PCM data into 4-bit ADPCM data.

(1) Voice data of every sampling rate (1.8 KHz–16 KHz) is converted into 8-bit PCM data (X1,n).

(2) The resulting PCM data (X1,n) is multiplied by 256 for conversion into 16-bit data, (Xn), and is then compared with the expected data ($\hat{X}n$) to obtain a difference (dn).

(3) When the difference is a positive value, ADPCM data MSB(L4) is specified as "0"; when negative, as "1". At the same time, the absolute value (|dn|) of the difference is caluculated.

(4) Then, the remaining three bits are determined by the relationship between the absolute value (|dn|) and quantization width (Δ n) as shown in Table I-1.

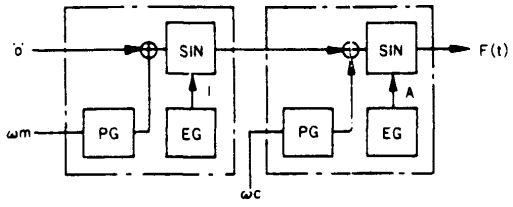
Table I-1 ADPCM codes

1. Condition

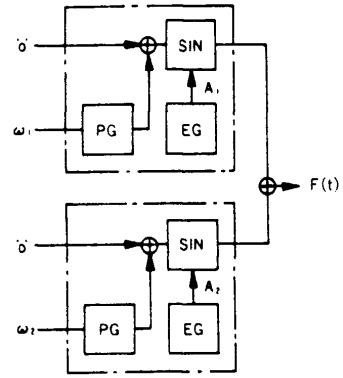
L_4		L_3	L_2	L_1	条	件
dn≧0	dn<0					
0	1	0	0	0		|dn| < △n/4
		0	0	1	△n/4 ≦	|dn| < △n/2
		0	1	0	△n/2 ≦	|dn| < △n*3/4
		0	1	1	△n*3/4 ≦	|dn| < △n
		1	0	0	△n ≦	|dn| < △n*5/4
		1	0	1	△n*5/4 ≦	|dn| < △n*3/2
		1	1	0	△n*3/2 ≦	|dn| < △n*7/4
		1	1	1	△n*7/4 ≦	|dn|

Conversion of voice data into ADPCM data is thus completed.

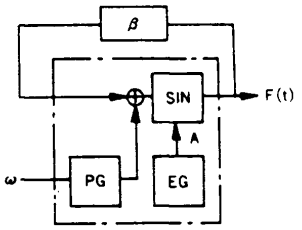
(5) After ADPCM data has been obtained, the new expected data ($\hat{X}n+1$) and quantization width (Δ n+1) are created.



a . $F(t) = A \sin(\omega ct + I \sin \omega mt)$



b . $F(t) = A_1 \sin \omega_1 t + A_2 \sin \omega_2 t$



c . $F(t) = A \sin(\omega t + \beta F(t))$

(FIG)

Fig. I-1 FM sound generation expressed by unit cell design

$\hat{X}_{n-1} = (1 - 2 * L_4) * (L_3 + L_2/2 + L_1/4 + 1/8) * \triangle n + \hat{X}n$

$\triangle_{n-1} = f(L_3, L_2, L_1) * \triangle n$

(Expressions)

Table I-2 Quantization width rate of change

L_3	L_2	L_1	f
0	0	0	0.9
0	0	1	0.9
0	1	0	0.9
0	1	1	0.9
1	0	0	1.2
1	0	1	1.6
1	1	0	2.0
1	1	1	2.4

Comprehensive ADPCM voice analysis is achieved by repeating steps (1) through (5) for each sampling time.

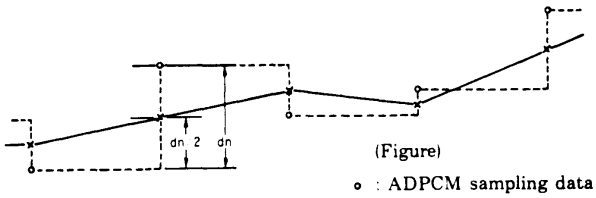
(b) Voice synthesis

(1) In the voice synthesis procedures, the expressions used to calculate the new expected data and quantization width obtained in step (5) are used to calculate the reproduced data. In other words, the expected data determines the actual voice reproduction. However, the reproduced voice obtained through this calculation has a staircase waveform (stepped at every sampling time) and may suffer from poor tone quality, including step noise. Consequently, the MSX-AUDIO incorporates the following procedure to smoothen the staircase waveform.

(2) First, reproduced voice signals are processed through a smoothing circuit. This is the same as inserting a low pass filter in the circuitry to eliminate high-frequency noise.

Next, as a linear interpolation, samplings are repeated at every 50 KHz for intervals between the original samplings.

The smoothing and re-sampling results are shown below.



(Figure)

o : ADPCM sampling data

× : data after smoothing

------ : reproduced voice without smoothing

—— : voice reproduced after smoothing and 50 KHz re-sampling

Fig. I-2 ADPCM voice synthesis waveform

2. OUTLINE OF MSX-AUDIO FEATURES

2-1. Major Features

The MSX-AUDIO has such major operating features as the FM sound generator, ADPCM voice analysis /synthesis, external memory control, AD/DA converters, and input/output ports for keyboard scanning.

(a) FM sound generator

The FM sound generator has three sounding modes: simultaneous generation of nine tones, generation of six melodies and five rhythms, and composite sinusoidal modeling. One of the three modes is selected by software according to the application. Because this FM sound generator is equivalent to that of the OPL (YM3526), the software for the OPL can be used with the MSX-AUDIO.

- Simultaneous nine-tone generation:

This mode simultaneously generates nine FM sounds of different tone colors. Both the rhythm selection bit (R) and composite sinusoidal modeling bit (CSM) should be specified with "0" for this mode.

- Six-melodies/five-rhythms sounding:

This mode is useful when the MSX-AUDIO is used with equipment in the CAPTAIN or teletex system. The five available rhythmic sounds are bass drum, snare drum, tom-tom, high-hat cymbals, and top cymbal.

- Composite sinusoidal modeling:

This is a speech synthesis mode to simulate sounds by using three to six sine waves.

(b) ADPCM voice analysis/synthesis

This function provides the voice analysis and synthesis using 4-bit ADPCM. The sampling rate for modulation can be arbitrarily programmed within 1.8 KHz--16 KHz (analysis) and 1.8 KHz--50 KHz (synthesis). Analysis results and synthesis data can be stored in either external memory (ROM or RAM) or the processor's storage.

(c) External-memory control

This function controls the external memory used to store the analysis/synthesis data processed through ADPCM. Available external memories are 256K-bytes DRAM, 64K-bytes DRAM, and the ROMs accessible in units of byte. The maximum storage capacity is 256 K-bytes (both RAM and ROM).

(d) AD/DA converters

The AD/DA converters in the ADPCM unit can be operated independently.

In this AD/DA conversion mode, FM sound generation and ADPCM voice analysis/synthesis are ineffective.

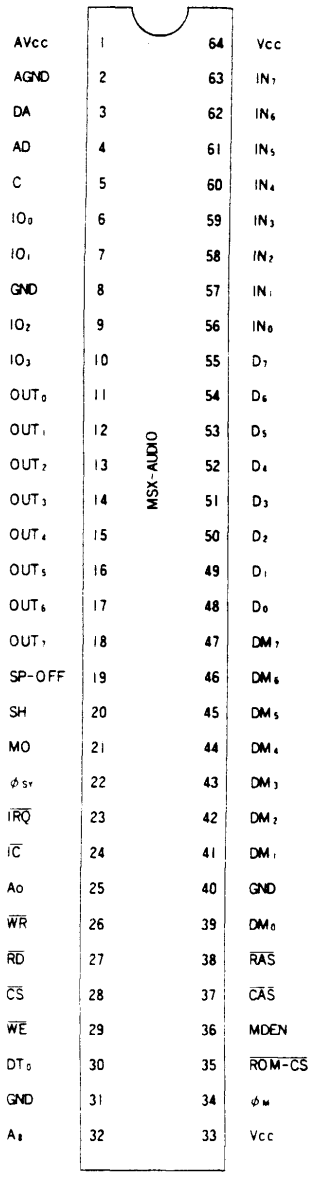
(e) Keyboard input/output ports

These are 8-bit input/output ports for external keyboard scanning.

In addition to the above-mentioned functions, the MSX-AUDIO is equipped with vibrato and amplitude-modulation oscillators for further natural sound generation, two general-purpose timers for various interface signals, and general-purpose 4-bit input/output ports.

2-2. Pin Layout

(Figure)



2-3. Description of Terminal Functions

(a) φM

This is the master clock of the MSX-AUDIO. The input frequency is 3.579545 MHz (typical).

(b) φSY, SH, MO

The MO is the sound output terminal of the MSX-AUDIO. Because the MO outputs serial 13-bit (virtual 10 bits and characteristic 3 bits) data, the data must be converted into analog values by using the synchronous clock (φSY), synchronizing signals (SH), and the DA converter (YM3014).

(c) D0--D7

This is an 8-bit bidirectional data bus used for data transfer between the MSX-AUDIO and the processor.

(d) $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0

These terminals are used to control data bus lines D0--D7.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	
0	1	0	0	1. The register address is written to the MSX-AUDIO.
0	1	0	1	2. The register contents are written to the MSX-AUDIO.
0	0	1	0	3. The MSX-AUDIO status contents are read.
0	0	1	1	4. The MSX-AUDIO register contents are read (specific registers only).
1	×	×	×	5. Bus lines D0--D7 have high impedance.

(e) $\overline{IRQ}$

This terminal outputs interrupt signals from the two timers, ADPCM, and memory control. The signals can be masked by a program.

(f) DA, AD, C

These terminals are used for AD conversion. DA is connected to DA converter output (reference data). The analog input (AD) allows AD conversion within Vcc/2 ± Vcc/4. Capacity terminal C is used for sample holding of analog data.

(g) DM0--DM7

These terminals are used to multiply signals from external storage addresses (A0--A7), for data input (DI0--DI7), and for data output (DO1--DO7). (DO0 uses another terminal.)

(h) A8, DT0

The A8 is the terminal used for external memory address (A8) and the DT0 is used for data output (DO0).

(i) $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

These terminals output control signals to external memory. When a DRAM is used as external storage, an RAM-compatible terminal should be used. When an external ROM is used, these terminals are used for address latch signals ($\overline{RAS}$, $\overline{CAS}$).

(j) MDEN, $\overline{ROM\text{-}CS}$

These terminals specify the timing of data input from external memory. When MDEN is set to "1", DRAM data is input to DM1-DM7. when $\overline{ROM\text{-}CS}$ is "0", ROM data is input to DM1-DM7. (Terminal DT0 is used for data output O.)

(k) IN0–IN7, OUT0–OUT7

These are the input (IN0–IN7) and output (OUT0–OUT7) ports for keyboard scanning. The input ports are pull-up types, and the output ports are open-drain types.

(l) $I\overline{O}0$–$I\overline{O}3$

These are general-purpose input/output ports.

(m) SP-OFF

This terminal is used to switch off amplifier-speaker connection when the DA converter is used as reference voltage generator during AD conversion.

(n) $\overline{IC}$

This terminal activates MSX-AUDIO operation.

(o) GND, AGND

Grounding terminals

(p) Vcc, AVcc

+5 V power terminals

II-4. Data Bus Control

In the MSX-AUDIO, the data bus control, including read/write of addresses and data, is performed by using the signals sent from $\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and AO. By combining these four signals, four different modes can be specified.

Table II-1 Mode selection

	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	
1	1	×	×	×	1. Inactive mode
2	0	1	0	0	2. Address write mode
3	0	1	0	1	3. Data write mode
4	0	0	1	0	4. Status read mode
5	0	0	1	1	5. Data read mode

(a) Inactive mode

When $\overline{CS}$ is set to "1", data bus lines D0–D7 have high impedance.

(b) Address write mode

To write addresses, set the control signals for the address write mode, and set the address data on the data bus. In this way, the specified register addresses become ready for data writing. Note that, after an address data has been written, a delay time of 12 cycles (master closk ϕM) must be allotted before writing sound data.

(c) Data write mode

By setting the control signals for the data write mode, the data on D0--D7 is written to the specified register addresses.

Similar to the address write mode, the data write mode requires a delay time of 84 cycles (φM) between the previous data write and subsequent data address writing. (The delay time is 12 cycles for register addresses $00--$1A.)

(d) Status read mode

When the control signals have been set for the status read mode, the status data stored in the MSX-AUDIO's status register is output.

(e) Data read mode

When the control signals have been set for the data read mode, the MSX-AUDIO register data that can be read out is output to the data bus.

Note the following for the address and data write mode.

The MSX-AUDIO requires a delay time after address/data has been written to its register. Different delay times (shown in Table 2-2) apply to the address write mode and data write mode. The processor does not perform subsequent operation for the MSX-AUDIO for the specified delay time. If the delay time is ignored, correct data processing cannot be assured.

Table 2-2 Delay times

Mode	Delay time
Address write mode	12 cycles
Data write mode	84 (12) cycles

(Note)

The "cycle" of the delay time is counted in units of master clock cycles.

The "(12) cycles" in the data write mode column is used for register addresses $00--$1A.

2-5. Channels and Slots

The MSX-AUDIO can generate nine different FM sounds (nine channels). It has a single operator cell but the operator cell is sequentially used 18 times to calculate and generate the nine different sounds. The sequence (slot No.) used to pass data through the operator cell corresponds to the register numbers consequently, the corresponding register must be controlled for the generator of each sound.

The specified channel data, such as the F-Number, controls two slots (classified as the 1st and 2nd slots) at a time. In the FM mode, the 1st slot is used for modulated waves and the 2nd slot is used for carrier waves. In addition, the 1st slot can be set for the feedback FM mode. See Section III-1-22 for details on setting the feedback FM mode.

Table II-3 shows the relationship between channels and slots.

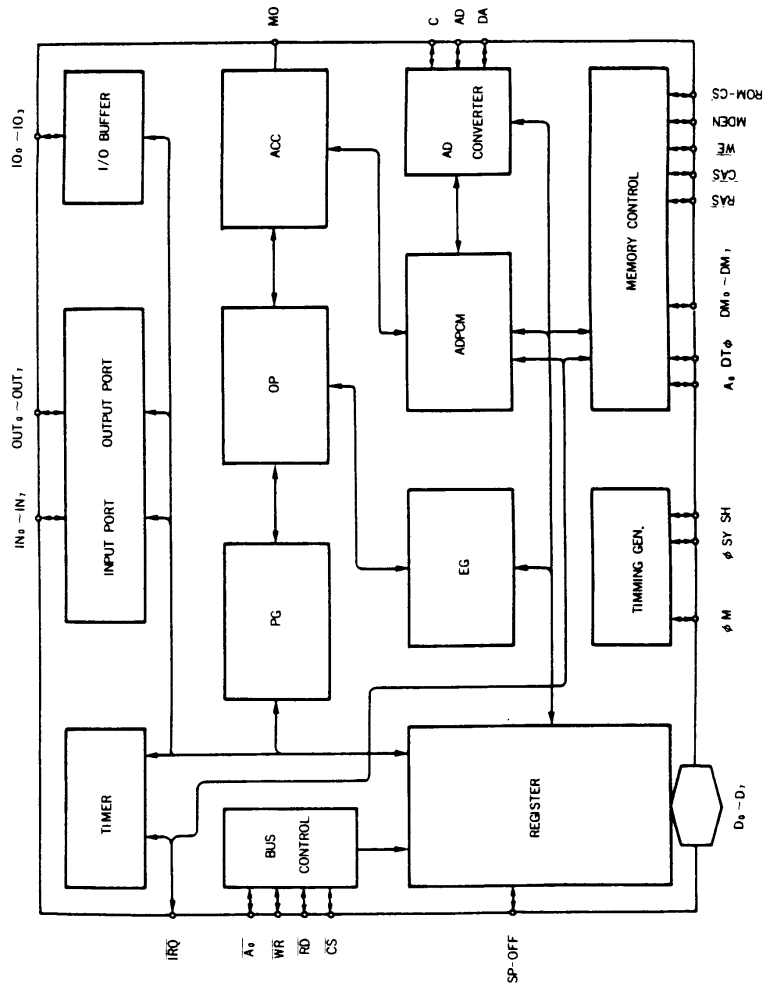
Table II-3 Channels and slots

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	2	3	1	2	3	4	5	6	4	5	6	7	8	9	7	8	9
1			2			1			2			1			2		
20	21	22	23	24	25	28	29	2A	2B	2C	2D	30	31	32	33	34	35
C0	C1	C2	C0	C1	C2	C3	C4	C5	C3	C4	C5	C6	C7	C8	C6	C7	C8

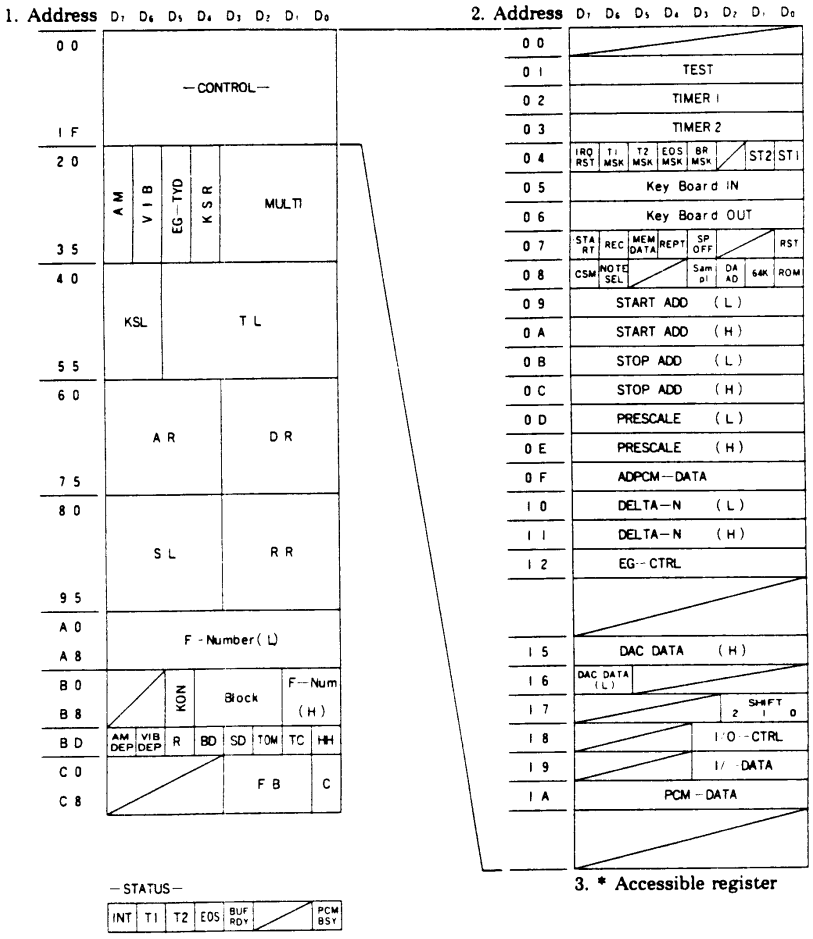
1. Slot No.
2. Channel No.
3. Slot No. according to each channel
4. Data/register relationship for each slot (Ex.: register $20–$35)
5. Data/register relationship for each channel (Ex.: register $C0–C8)

2-6. Block Diagram

(Fig)



2-7. Address Map



3. * Accessible register

3. DESCRIPTION OF FUNCTIONS

The MSX-AUDIO is controlled by the data written in the register array. In other words, the register array contents specify the MSX-AUDIO functions, including instrumental sound (e.g., piano and violin) generation, voice analysis/synthesis, and external-memory control. In this manual, the register functions are explained in detail using simple descriptions of other functional blocks. The FM sound generation, however, is described in Part 5, GENERATION OF INSTRUMENTAL SOUND.

3-1. Registers

As shown by the address map, registers have a capacity of about 1K bits. These 1k bits area are divided, according to function, into bytes to which addresses are assigned. When data is to be stored in the MSX-AUDIO, the address must be specified before the data is entered. If the same address is successively repeated, there will be no need to the repeat address setting for subsequent data entry. Note that the following register addresses marked with "*" indicate that the register is set to "0" at initialization (initial clear: IC = "0").

3-1-1 TEST: ADDRESS [$01]

This address is used only for factory LSI testing. It is normally set to "0".

3-1-2. TIMER

There are two timers: timer-1 with 80 μs resolution and timer-2 with 320 μs resolution. Both timers can perform start, stop, and flag operations. If a flag is set, terminal $\overline{IRQ}$ will become low and a timer interrupt will be posted to the processor.

(1) TIMER-1: ADDRESS [$02] *

Timer-1 is an 8-bit presettable counter. When the counter overflows, the timer-1 flag is set and preset values are loaded.

Timer-1 can also control composite sinusoidal modeling. When a counter overflow occurs, all slots are set to Key-ON (sounding) and, soon after that, are reset to Key-OFF. This operation simplifies composite sinusoidal modeling.

$02	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

$$Tov(ms) = (256 - N_1) * 0.08 \qquad @\phi M = 3.6MHz$$

$$N_1 = D_7 * 2^7 + D_6 * 2^6 + \cdots\cdots + D_1 * 2 + D_0$$

(2) TIMER-2: ADDRESS [$03] *

Similar to timer-1, timer-2 is an 8-bit presettable counter, but has a resolution of 320 μs (timer-1, 80 μs).

$03	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

$$Tov(ms) = (256 - N_2) * 0.32 \qquad @\phi M = 3.6MHz$$

$$N_2 = D_7 * 2^7 + D_6 * 2^6 + \cdots\cdots + D_1 * 2 + D_0$$

3-1-3. FLAG CONTROL: ADDRESS [$04]

This register is used to control start, stop, and flag operations for timers-1/2 and to set/reset flags for ADPCM and external memory control. At initialization, bits D3 and D4 are set to "1" and other bits are set to "0".

$04

D7	D6	D5	D4	D3	D2	D1	D0
IRQ RESET	MASK T1	MASK T2	MASK EOS	MASK BUF RDY		ST2	ST1

D0 (ST1): This bit controls the start/stop operations of timer-1.

When set to "1", timer-1 is loaded with the preset data and starts counting. When set to "0", timer-1 is ineffective.

D1 (ST2): This bit controls timer-2 as D0 (ST1) controls timer-1.

D3 (MASKBUF.RDY): When this bit is set to "1", data write/read requests are masked during data transfer between the processor and ADPCM or external storage.

D4(MASKEDS): This bit is used to mask the flag indicating the end of read/write of ADPCM or external storage, or the end of AD conversion.

D5 (MASKT2): When this bit is set to "1", timer-2 flag is set to "0" regardless of the timer-2 state.

D6 (MASKT1): This bit masks timer-1 flag.

D7 (IRQESET): Each flag in the MSX-AUDIO is set to "1" when a corresponding event occurrs, and $\overline{IRQ}$ then becomes "0".

This bit is used to reset the above flag/$\overline{IRQ}$ status. When this bit is set to "1", all flags are reset to "0". If only specified flags need to be reset, set the corresponding MASK bit to "1".

Note: A D7 bit setting of "1" is reset to "0" after all flags have been reset. When D7 is set to "1", the D0--D6 settings are ignored.

3-1-4. KEYBOARD IN: ADDRESS [$05]

This is the read-only address for input ports IN0--IN7. IN0--IN7 correspond to data bus lines D0--D7, respectively.

$05

D7	D6	D5	D4	D3	D2	D1	D0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

3-1-5. KEYBOARD OUT: ADDRESS [$06] *

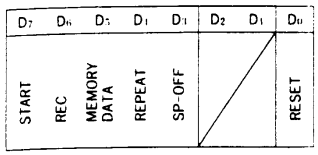
This is the address for output ports OUT0--OUT7. When set to "1", the output is low level. (@ sink current = 2mA, output level ≦ 0.4 V). the current (voltage 0.4 V or less). OUT0--OUT7 correspond to data bus lines D0--D7, respectively.

$06

D7	D6	D5	D4	D3	D2	D1	D0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

3-1-6. START/REC/MEM DATA/REPEAT/SP-OFF/RESET: ADDRESS [$07] *

This address is used to control the start of ADPCM voice analysis/synthesis and the setting for external memory access.



D0 (RESET): When this bit is set to "1" during ADPCM voice synthesis using external memory as a data source, the ADPCM synthesis circuit and externalmemory controller are reset to the initial status. In this case, the REPEAT bit must be set to "0". The RESET bit can be used when the ADPCM circuit or external-memory controller are no longer controlled.

D3 (SP-OFF): This bit is connected to terminal SP-OFF. When D3 is set to "1", SP-OFF is set to "1". This bit is used to protect the speaker during ADPCM analysis or AD conversion.

D4 (REPEAT): During ADPCM voice synthesis using external memory, this bitis set to "1" to enable repeated data synthesis in the same area (from start address to stop address).

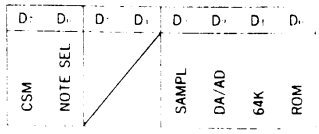
D5 (MEMORY DATA): This bit is set to "1" when external memory should be accessed.

D6 (REC): This bit is set to "1" for ADPCM voice analysis or data entry from the processor to external memory.

D7 (START): This bit is set to "1" for ADPCM voice analysis/synthesis. The start timing differs according to the data storage location (processor or external memory). If the data is stored in the processor, ADPCM processing will start with the reading/writing of address $0F. On the other hand, if the data is in external memory, the processing will start when the START bit is set to "1". Consequently, when the data is in external memory, it is necessary to arrange all other conditions before setting the START bit to "1". To reset START bit to "0", set SART bit to "0" first and reset all other bits.

3-1-7. CSM/KEYBOARD · SPLIT/SAMPLE/DA · AD/64K/ROM: ADDRESS [$08] *

This address is used to specify the composite sinusoidal modeling mode, AD/DA conversion, and type of external memory.



D0 (ROM): This bit is used to specify the type of external memory ("0" = RAM and "1" = ROM).

D1 (64K): This bit is used to specify the type of external memory ("0" = 256-Kbits DRAM and "1" = 64-Kbits DRAM). When this bit is set to "1", the output from address A8 is ignored. For ROM, this bit is set to "0".

D2 (DA/AD): This bit is used in combination with SAMPLE below.

When this bit is set to "1", MO output sends the data specified with $15--$17. This bit is set to "0" for AD conversion (with SAMPLE set to "1") or for MUSIC output (with SAMPLE set to "0").

D3 (SAMPLE): This bit is used to enable the timer for AD/DA conversion. AD conversion is started by setting this bit to "1".

D6 (NOTESEL): This bit is used to specify the separating points for keyboard splits in one octave. When this bit is set to "0", the separating points are specified by the second bits from F-Number MSB; when this bit is set to "0", the separating points are specified by the F-Number MSB. Tables below show the setting conditions. (Also refer to "F-Number/BLOCK".)

D_6 = "0"

0		1		2		3		4		5		6		7		Octave
0		1		2		3		4		5		6		7		Block data
1		1		1		1		1		1		1		1		F-Num·MSB
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	F-Num·2nd
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Keyboard split No.

D_6 = "1"

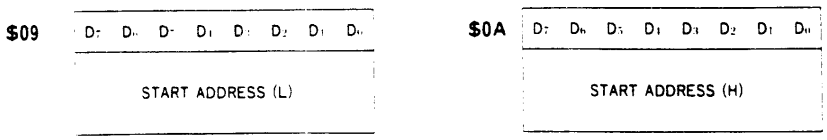
0		1		2		3		4		5		6		7		Octave
0		1		2		3		4		5		6		7		Blockdata
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	F-Num·MSB
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	F-Num·2nd
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Keyboard split No.

* DON'T CARE

D7 (CSM): This bit is set to "1" for the composite sinusoidal modeling mode. For the setting, all channels must be set to Key-OFF.

3-1-8 START ADDRESS L/H: ADDRESS [$09, $0A]

These addresses specify the start address of external memory to be accessed (by ADPCM or CPU) with 16-bit data: L ($09) and H ($0A). The specification differs a little according to memory type (ROM or RAM).



* For RAM

(a) 64 K DRAM

BANK			CAS ADDRESS								RAS ADDRESS									
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−$0A−								−$09−												
D_7	D_6	D_5	*	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	*	D_2	D_1	D_0	0	0	0	0	0

* D4 of $0A and D3 of $09 must be "0".

(b) 256 K DRAM

BANK			CAS ADDRESS								RAS ADDRESS									
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−$0A−								−$09−												
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	0	0	0	0	0

* For ROM

BANK			CAS ADDRESS								RAS ADDRESS									
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−$0A−								−$09−												
*	*	*	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	0	0	0	0	0

* D5--D7 of $0A must be equivalent to those of $0C.

3-1-9. STOP ADDRESS L/H: ADDRESS [$0B, $0C]

These addresses specify the stop address of external memory to be accessed (by ADPCM or CPU) with 16-bit data: L ($0B) and ($0C).

The specification differs a little according to memory type (ROM or RAM).

$0B	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	STOP ADDRESS (L)							

$0C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	STOP ADDRESS (H)							

* For RAM

(a) 64 K DRAM

BANK			CAS ADDRESS								RAS ADDRESS								
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−0C−								−$0B−												
D_7	D_6	D_5	*	D_4	D_2	D_1	D_0	D_7	D_6	D_5	D_4	*	D_2	D_1	D_0					

* D4 of $0C and D3 of $0B must be "0".

(b) 256 K DRAM

BANK			CAS ADDRESS								RAS ADDRESS								
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−$0C−								−$0B−												
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					

* For ROM

BANK			CAS ADDRESS								RAS ADDRESS								
2^2	2^1	2^0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
−$0C−								−$0B−												
*	*	*	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					

* D5–D7 of $0C must be equivalent to those of $0A.

3-1-10. PRESCALE L/H: ADDRESS [$0D, $0E]

These addresses are used to specify the sampling rate for AD conversion (including ADPCM analysis) and DA conversion. The sampling rate is given by the expression below. The maximum rate is 16 KHz; the minimum, 1.8 KHz.

fsample = 3.6 MHz/NPRE (@ ϕ_M = 3.6 MHz)

NPRE: prescale value

$0D

D_7	D_6	D_5	D_4	D_3	D_2	D	D_0
PRESCALE (L)							

$0E

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
					PRESCALE (H)		

3-1-11. ADPCM-DATA: ADDRESS [$0F]

This register is used to transmit data for ADPCM analysis/synthesis with the processor. It is also used as a buffer when external memory is accessed by the processor.

$0F

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
ADPCM-DATA							

(Note) Data structure for ADPCM analysis/synthesis

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
nth data				n+1th data			
L_4	L_3	L_2	L_1	L_4	L_3	L_2	L_1

As shown by the table to the left, one byte contains two ADPCM data items. If the four high-order bits are the nth data items, the four low-order bits will be the n+1th data item.

3-1-12. DELTA-N L/H: ADDRESS [$10, $11]

These addresses are used to specify the factor used for linear interpolation at 50 kHz of the sampling intervals during ADPCM voice synthesis. This factor is also used as the sampling rate for synthesis; therefore, no prescale data is used for synthesis.

$$\triangle N = k * 2^{16},\ k = \left(\frac{3.6MHz}{50KHz}\right) / \left(\frac{3.6MHz}{fsample}\right) \quad (@\ \phi_M = 3.6\ MHz)$$

$$VOICE_{n+1} = VOICE_n + (Noff_n + i_n * k) * (VOICE_{n+1} - VOICE_n)$$

$$\begin{cases} 0 \leqq Noff_n + i_n * k < 1 \\ Noff_n < k,\ \ Noff_n = Noff_{n-1} + i'_{n-1} * k + k - 1 \end{cases}$$

i'n-1 is the maximum value of n-1th sampling.

$10

D_7	D_6	D_5	D_4	D_3	D_2	D	D_0
DELTA-N (L)							

$11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DELTA-N (H)							

3-1-13. ENVELOPE CONTROL (at ADPCM): ADDRESS [$12]

This address is used to control the output level of ADPCM voice synthesis in up to 256 steps (from 0 to 256). This address data is not effective for MUSIC output and DA conversion, only for ADPCM output.

$$AUDIO\ OUT = VOICE_n * EG$$

$12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
EG-CONTROL							

3-1-14. DAC-DATA: ADDRESS [$15--$17]

These addresses are used to specify digital data for DA conversion. The three-bytes (13-bit) data is calculated through the expressions below and output (via DAC) as analog data. The data entry at address $15 triggers the output of register ($15--$17) contents. For the DA conversion, initial values must be written to registers $15-$17 before setting D2 (DA/AD) of register $08 to "1".

$$\begin{cases} V_{OUT} = \frac{Vcc}{2} + \frac{Vcc}{4} * (-1 + F_0 + F_1 * 2^{-1} + \cdots\cdots + F_7 * 2^{-8} + F_8 * 2^{-9} + 2^{-10}) * 2^E \\ E = \overline{S_2} * 2^2 + \overline{S_1} * 2^1 + \overline{S_0} * 2^0 \qquad (\sigma\ \ S_0 + S_1 + S_2 \geqq 1) \end{cases}$$

	D7	D6	D5	D4	D3	D2	D1	D0
$15	F0	F1	F2	F3	F4	F5	F6	F7
$16	F8	F9						
$17						S2	S1	S0

3-1-15. I/O-CONTROL AND I/O-DATA: ADDRESS [$18, $19] *

These registers are used to control the 4-bit general-purpose input/output ports of the MSX-AUDIO. $18 specifies input or output: initially set to "0", set to "1" for output, and set to "0" for input. $19 is used for data transfer through the input/output ports.

$18	D7	D6	D5	D4	D3	D2	D1	D0
					I/O-CTRL			

$19	D7	D6	D5	D4	D3	D2	D1	D0
					I/O-DATA			

3-1-16. PCM-DATA: ADDRESS [$1A]

This address is used to store data processed through AD conversion.

(Note) PCM code is expressed in two's Compliment.

$1A	D7	D6	D5	D4	D3	D2	D1	D0
	PCM-DATA							

3-1-17. AM/VIB/EG-TYP/KSR/MULTIPLE: ADDRESS [$20--$35] *

These addresses are used to specify envelope shapes and multipliers for converting frequency data obtained by using the F-Number, into the frequency of carrier/modulated waves that correspond to realistic instrumental sounds.

$20~$35	D7	D6	D5	D4	D3	D2	D1	D0
	AM	VIB	EG-TYP	KSR	MULTI			
					2^3	2^2	2^1	2^0

D0--D3 (MULTIPLE): These bits specify the multipliers (shown in Table 3-1) used to convert carrier and modulated waves.

(Example)

F-Number frequency: wf

Multiplier for carrier waves: 1

Multiplier for modulated waves: 7

$F(t) = E\sin(\omega ft + I\sin(7\omega ft))$

Table III-1 Multipliers

MUL	Multiplier	MUL	Multiplier	MUL	Multiplier	MUL	Multiplier
0	½	4	4	8	8	C	12
1	1	5	5	9	9	D	12
2	2	6	6	A	10	E	15
3	3	7	7	B	10	F	15

D4 (KSR): This bit specifies the key scales for the attack and decay rates. Acoustic instruments generally have quicker attack and decay in sound production as the pitch of the sound becomes higher. The key scales are used to simulate fast attack and decay, and a scale value (shown in Table 3-2) is added as an offset value to the note at the corresponding pitch. Consequently, the actual attack/decay rates are the ADSR preset data with the offset values added.

RATE = 4*R + Rks

- R: ADSR preset value
- Rks: key-scale offset value
- If R = 0, RATE = 0.

Table III-2 Key scales for RATE

D_4	N	RKS	N	RKS	N	RKS	N	RKS
0	0	0	4	1	8	2	12	3
	1	0	5	1	9	2	13	3
	2	0	6	1	10	2	14	3
	3	0	7	1	11	2	15	3
1	0	0	4	4	8	8	12	12
	1	1	5	5	9	9	13	13
	2	2	6	6	10	10	14	14
	3	3	7	7	11	11	15	15

* Column N indicates key scale No.

D5 (EG-TYP): This bit specifies the sounding of a non-percussive tone or a percussive tone. These two sounding modes are classified by the use of the release rates shown in Fig. 3-1.

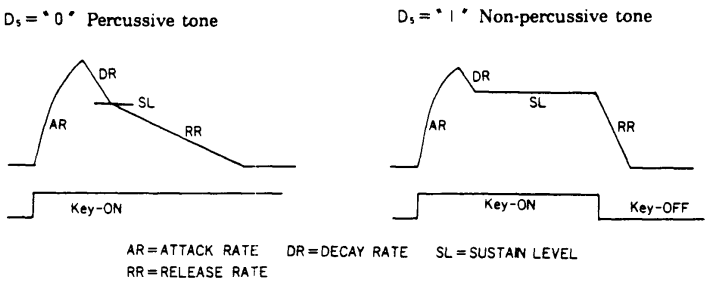


Fig. 3-1 Two sounding modes

D6 (VIB): This bit specifies vibrato ON/OFF. When set to "1", vibrato is generated for the corresponding slot at a frequency of 6.4 Hz (@φM = 3.6 MHz). The depth of vibrato is set by the VIB-DEPTH of register $BD.

D7 (AM): This bit specifies amplitude modulation ON/OFF. When set to "1", amplitude modulation is performed for the corresponding slot at a frequency of 3.7 Hz (@φM = 3.6 MHz). The depth of modulation is set by the AM-DEPTH of register $BD.

3-1-18. KSL/TOTAL LEVEL: ADDRESS [$40--$55]

The total level is used to increase the amount of decay for controlling the degree of modulation (tone color) and output level according to envelope generator output. The level key scale (KSL) is used to simulate the actual reduction in the instrument output level along with the increase in pitch.

$40~$55

D7	D6	D5	D4	D3	D2	D1	D0
KSL		Total Level					

D0--D5 (Total level): The maximum resolution of decay is 0.75 dB. The output level can be reduced by up to 47.25 dB.

Table 3-3 Total level

	D5	D4	D3	D2	D1	D0
Decay amount	24 dB	12 dB	6 dB	3 dB	1.5 dB	0.75dB

D6. D7 (KSL): These bits specify the key scales for the output level. In the key scale mode, the higher the pitch, the lower the output level. The four available decay amounts are 0 dB/octave, 1.5 dB/octave, 3 dB/octave, and 6 dB/octave.

Table 3-4

D6	D7	Decay amount
0	0	0
1	0	1.5dB/OCT
0	1	3 dB/OCT
1	1	6 dB/OCT

Table 3-5 3 dB/octave decay according to

F-Num / OCT	0 8	1 9	2 10	3 11	4 12	5 13	6 14	7 15
0	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000	0.000 0.000
1	0.000 0.000	0.000 0.750	0.000 1.125	0.000 1.500	0.000 1.875	0.000 2.250	0.000 2.625	0.000 3.000
2	0.000 3.000	0.000 3.750	0.000 4.125	0.000 4.500	0.000 4.875	1.125 5.250	1.875 5.625	2.625 6.000
3	0.000 6.000	0.000 6.750	0.000 7.125	1.875 7.500	3.000 7.875	4.125 8.250	4.875 8.625	5.625 9.000
4	0.000 9.000	0.000 9.750	3.000 10.125	4.875 10.500	6.000 10.875	7.125 11.250	7.875 11.625	8.625 12.000
5	0.000 12.000	3.000 12.750	6.000 13.125	7.875 13.500	9.000 13.875	10.125 14.250	10.875 14.625	11.625 15.000
6	0.000 15.000	6.000 15.750	9.000 16.125	10.875 16.500	12.000 16.875	13.125 17.250	13.875 17.625	14.625 18.000
7	0.000 18.000	9.000 18.750	12.000 19.125	13.875 19.500	15.000 19.875	16.125 20.250	16.875 20.625	17.625 21.000

Unit: dB

(Note)

- F-Number indicates 4 high-order bits
- Multiply each value by 1/2 for 1.5 dB/octave decay.
- Multiply each value by 2 for 6 dB/octave decay.

3-1-19. ATTACK/DECAY RATE: ADDRESS [$60--$75] *

The attack rate specifies the rise time of the sound, and the decay rate specifies the decay time after the attack. Table 3-6 shows the time settings for the two rates.

$60~$75

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
AR				DR			
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0

3-1-20. SUSTAIN LEVEL/RELEASE RATE: ADDRESS [$80--$95] *

The sustain level specifies the level at which sound is sustained after the decay. For a percussive tone, the sustain level specifies the turning point from the decay mode to the release mode.

The release rate, for a non-percussive tone, specifies the decay rate after Key-OFF; for a percussive tone, the release rate specifies the decay rate for the sound below the sustain level.

$80~$95

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SL				RR			
24 dB	12 dB	6 dB	3 dB	2^3	2^2	2^1	2^0

- When D4--D7 are all set to "1", the sustain level is 93 dB.
- Decay time setting of the release rate is same the decay time.

Table 3-6 Attack and decay time according to RATE

The RATE data in the table shows the RATE after key scale. The RATE data is divided into four high-order bits (RM) and two loworder bits (RL), and is expressed as "RM-RL". RATE = RM*4 + RL

*** EG ATTACK TIME *** RATE	ms (@ 10% - 90%)	*** EG DECAY TIME *** RATE	ms
15 3	0.00	15 3	0.51
15 2	0.00	15 2	0.51
15 1	0.00	15 1	0.51
15 0	0.00	15 0	0.51
14 3	0.11	14 3	0.58
14 2	0.11	14 2	0.69
14 1	0.14	14 1	0.81
14 0	0.19	14 0	1.01
13 3	0.22	13 3	1.15
13 2	0.26	13 2	1.35
13 1	0.31	13 1	1.62
13 0	0.37	13 0	2.02
12 3	0.43	12 3	2.32
12 2	0.49	12 2	2.68
12 1	0.61	12 1	3.22
12 0	0.73	12 0	4.02
11 3	0.85	11 3	4.62
11 2	0.97	11 2	5.38
11 1	1.13	11 1	6.42
11 0	1.45	11 0	8.02
10 3	1.70	10 3	9.24
10 2	1.94	10 2	10.76
10 1	2.26	10 1	12.84
10 0	2.90	10 0	16.04
9 3	3.39	9 3	18.48
9 2	3.87	9 2	21.52
9 1	4.51	9 1	25.68
9 0	5.79	9 0	32.08
8 3	6.78	8 3	36.96
8 2	7.74	8 2	43.04
8 1	9.02	8 1	51.36
8 0	11.58	8 0	64.16
7 3	13.57	7 3	73.92
7 2	15.49	7 2	86.08
7 1	18.05	7 1	102.72
7 0	23.17	7 0	128.32
6 3	27.14	6 3	147.84
6 2	30.98	6 2	172.16
6 1	36.10	6 1	205.44
6 0	46.34	6 0	256.64
5 3	54.27	5 3	295.68
5 2	61.95	5 2	344.32
5 1	72.19	5 1	410.88
5 0	92.67	5 0	513.28
4 3	108.54	4 3	591.36
4 2	123.90	4 2	688.64
4 1	144.38	4 1	821.76
4 0	185.34	4 0	1026.56
3 3	217.09	3 3	1182.72
3 2	247.81	3 2	1377.28
3 1	288.77	3 1	1643.52
3 0	370.69	3 0	2053.12
2 3	434.18	2 3	2365.44
2 2	495.62	2 2	2754.56
2 1	577.54	2 1	3287.04
2 0	741.38	2 0	4106.24
1 3	868.35	1 3	4730.88
1 2	991.23	1 2	5509.12
1 1	1155.07	1 1	6574.08
1 0	1482.75	1 0	8212.48

*** EG ATTACK TIME *** RATE	ms (@ 0dB - 96dB)	*** EG DECAY TIME *** RATE	ms
15 3	0.00	15 3	2.40
15 2	0.00	15 2	2.40
15 1	0.00	15 1	2.40
15 0	0.00	15 0	2.40
14 3	0.20	14 3	2.74
14 2	0.24	14 2	3.20
14 1	0.30	14 1	3.84
14 0	0.38	14 0	4.80
13 3	0.42	13 3	5.48
13 2	0.46	13 2	6.40
13 1	0.56	13 1	7.68
13 0	0.70	13 0	9.60
12 3	0.80	12 3	10.96
12 2	0.92	12 2	12.80
12 1	1.12	12 1	15.36
12 0	1.40	12 0	19.20
11 3	1.56	11 3	21.92
11 2	1.84	11 2	25.56
11 1	2.20	11 1	30.68
11 0	2.76	11 0	38.36
10 3	3.12	10 3	43.84
10 2	3.68	10 2	51.12
10 1	4.40	10 1	61.36
10 0	5.52	10 0	76.72
9 3	6.24	9 3	87.68
9 2	7.36	9 2	102.24
9 1	8.80	9 1	122.72
9 0	11.04	9 0	153.44
8 3	12.48	8 3	175.36
8 2	14.72	8 2	204.48
8 1	17.60	8 1	245.44
8 0	22.08	8 0	306.88
7 3	24.96	7 3	350.72
7 2	29.44	7 2	408.96
7 1	35.20	7 1	490.88
7 0	44.16	7 0	613.76
6 3	49.92	6 3	701.44
6 2	58.88	6 2	817.92
6 1	70.40	6 1	981.76
6 0	88.32	6 0	1227.52
5 3	99.84	5 3	1402.88
5 2	117.76	5 2	1635.84
5 1	140.80	5 1	1963.52
5 0	176.64	5 0	2455.04
4 3	199.68	4 3	2805.76
4 2	235.52	4 2	3271.68
4 1	281.60	4 1	3927.04
4 0	353.28	4 0	4910.08
3 3	399.36	3 3	5611.52
3 2	471.04	3 2	6543.36
3 1	563.20	3 1	7854.08
3 0	706.56	3 0	9820.16
2 3	798.72	2 3	11223.04
2 2	942.08	2 2	13086.72
2 1	1126.40	2 1	15708.16
2 0	1413.12	2 0	19640.32
1 3	1597.44	1 3	22446.08
1 2	1884.16	1 2	26173.44
1 1	2252.80	1 1	31416.32
1 0	2826.24	1 0	39280.64

(Note) There is no change in the envelope when the RATE is "0".

3-1-21. BLOCK/F-NUMBER: ADDRESS [$A0-$B8] *

These addresses are used to specify pitch and scale. An F-Number is specified by both $A* and $B*.

$A0~$A8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F-Number							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$B0~$B8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
		KEY-ON	BLOCK			F-Num	
			2^2	2^1	2^0	2^9	2^8

D0-D7 [$A*], D0--D1 [$B*] (F-Number): An F-Number is specified by 10-bit data: Eight bits of address $A* and two low order bits of address $B*.

The F-Number sets a scale in a procedure that is described later.

D2--D4(BLOCK): These bits are used to specify octave data.

D5(Key-ON): This bit corresponds to keyboard ON/OFF. When set to "1", the channel is turned on for sounding; when set to "0", Key-OFF.

*F-NUMBER/BLOCK

In the MSX-AUDIO, the desired frequency can be obtained by specifying a phase increment corresponding to the frequency. The phase increment is determined by the F-Number, Block, and Multiple data. First, the phase increment for the desired frequency is given by the following expression.

(Expression) ...(1)

$\triangle P = fmus * 2^{19} / fsam$ $\qquad fsam = fM / 72$

fmus : Desired frequency

fsam : Sampling frequency (50 kHz)

fM : Input clock frequency (3.6 MHz)

The phase increment is thus calculated. However, it is difficult to manage the increment data for multiple octaves because of the large number of resulting data bits. In the MSX-AUDIO, only the increment data for one octave is specified, and , for other octave sounds, the original data will be shifted (multipled by 2, 4, etc.). Consequently, the phase increment is given as:

(Expression)...(2)

$\triangle P = 2^B * F' * MUL$

B : Octave data

F' : Increment for one octave

MUL : Multiplier

Similar to expressions (1) and (2), the increment (F) is specified by using 10-bit data. The F-Number and Block are expressed as follows:

$$F = (fmus * 2^{19} / fsam) / 2^{b-1} \qquad @MUL = 1$$

F : F-Number data

b : Block data

Table 3-7-1 F-Number (1)

Scale	Frequency (4oct)	F-Number	$B*		$A*							
			D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
C#	277.2	363	0	1	0	1	1	0	1	0	1	1
D	293.7	385	0	1	1	0	0	0	0	0	0	1
D#	311.1	408	0	1	1	0	0	1	1	0	0	0
E	329.6	432	0	1	1	0	1	1	0	0	0	0
F	349.2	458	0	1	1	1	0	0	1	0	1	0
F#	370.0	485	0	1	1	1	1	0	0	1	0	1
G	392.0	514	1	0	0	0	0	0	0	0	1	0
G#	415.3	544	1	0	0	0	1	0	0	0	0	0
A	440.0	577	1	0	0	1	0	0	0	0	0	1
A#	466.2	611	1	0	0	1	1	0	0	0	1	1
B	493.9	647	1	0	1	0	0	0	0	1	1	1
C	523.3	686	1	0	1	0	1	0	1	1	1	0

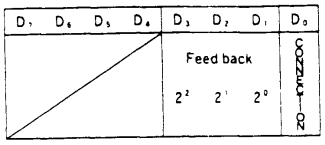
Table 3-7-2 F-Number (2)

Scale	Frequency (4~5oct)	F-Number	$B*		$A*							
			D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
G	392.0	514	1	0	0	0	0	0	0	0	1	0
G#	415.3	544	1	0	0	0	1	0	0	0	0	0
A	440.0	577	1	0	0	1	0	0	0	0	0	1
A#	466.2	611	1	0	0	1	1	0	0	0	1	1
B	493.9	647	1	0	1	0	0	0	0	1	1	1
C	523.3	686	1	0	1	0	1	0	1	1	1	0
C#	554.4	727	1	0	1	1	0	1	0	1	1	1
D	587.3	770	1	1	0	0	0	0	0	0	1	0
D#	622.2	816	1	1	0	0	1	1	0	0	0	0
E	659.3	864	1	1	0	1	1	0	0	0	0	0
F	698.5	916	1	1	1	0	0	1	0	1	0	0
F#	740.0	970	1	1	1	1	0	0	1	0	1	0

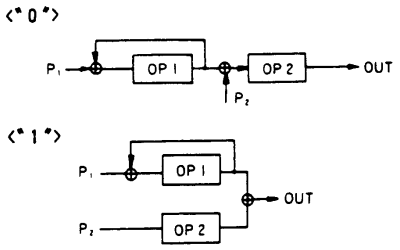
3-1-22. FEEDBACK/CONNECTION: ADDRESS [$C0--$C8] *

These addresses are used to specify the degree of self-feedback frequency modulation.

$C0~$C8



D0 (CONNECTION): This bit is used to specify the connection of the two slots. This bit is set to "0" for the FM mode, but set to "1" to connect the slots in parallel for composite sinusoidal modeling.



D1–D3 (FEEDBACK): These bits are used to specify the degree of Feedback frequency modulation.

Table III-8 Degree of modulation

	0	1	2	3	4	5	6	7
Modulation degree	0	π/16	π/8	π/4	π/2	π	2π	4π

3-1-23 AM.VIB-DEPTH/RHYTHM:ADDRESS [$BD] *

This address is used to specify the depth of amplitude modulation (AM) and vibrato (VIB), rhythm, and ON/OFF of rhythmic sounds.

$BD

D7	D6	D5	D4	D3	D2	D1	D0
AM-DEPTH	VIB-DEPTH	RHYTHM	BD	SD	TOM	TOP-CY	HH

D0–D5 (RHYTHM): When D5 = "1", the MSX-AUDIO is set for the rhythmic sound mode by using channels 7–9 (see page 9) for rhythmic sounds. Consequently, the sounding of melodies is limited to six tones. Bits D0–D4 are used to specify rhythmic sound ON/OFF. As a result, Key-ON registers $B6–$B8 must be set to "0". The slots 13–18 correspond to the rhythmic sounds (shown in Table 3-9). It is necessary to input other data items, including RATE data, to correspond to each rhythmic sound.

Table III-9 Rhythm slots

Instrument	Slot
BD	13.16
SD	17
TOM	15
TOP•CYM	18
HH	14

D6 (VIB-DEPTH): This bit is used to select one of the two vibrato depths: 14 cents (D6 = "1") and 7 cents (D6 = "0").

D7 (AM-DEPTH): This bit is used to select one of the two amplitude-modulation depths: 4.8 dB (D7 = "1") and 1 dB (D7 = "0").

3-2. Phase Generator (PG)

The phase generator (PG) provides phase data by accumulating the increment for the desired frequency in units of time. The increment is calculated using the frequency data (F-Number, Block, and Multiplier) sent from the corresponding registers. The PG also includes a vibrato oscillator to produce a vibrato effect by using the oscillation and frequency data.

3-3. Envelope Generator (EG)

The envelope generator (EG) is controlled by attack, decay, and release rates, and the sustain and total levels, to set the shifting of tone color and sound volume. It provides a dynamic range of 96 dB (at a resolution of 0.1875 dB). EG data is expressed by logarithmic values for the amount of decay. Figure 3-2 shows a typical waveform characterized by the exponential shifting at attack time and the linear shifting of other portions. The waveform shows the shifting from attack to decay when the level reaches ` dB, and the shifting from decay to sustain when the level decays to the sustain level. The release starts at Key-OFF. Sound effects are produced by adding the specified data for total level, level key scale, and amplitude modulation to EG data, which can be used to change the envelope waveform.

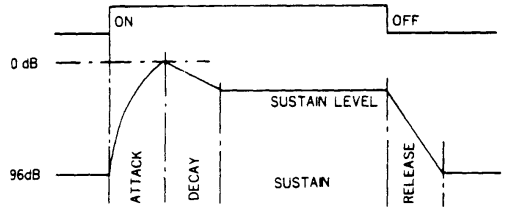


Fig. 3-2 Envelope waveform

3-4. Operator (OP) and Accumulator (ACC)

The operator circuit performs FM operations. It calculates sine values from phase data sent from the phase generator, and multiplies the calculation result by using envelope generator output. The operation result is returned to the operator input (when the data is a modulated wave) or the operation result is sent to the accumulator (when the data is for instrumental sounds). This data transfer is controlled by feedback/connection data. The accumulator collects operator output for each channel
and converts the accumulated result into offset binary data with a 10-bit virtual part (including sine bits) and a 3-bit exponent part. Finally, the accumulator outputs the data from the LSB as shown in

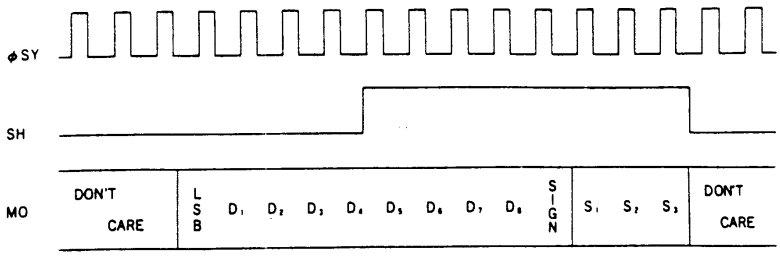


Fig. 3-3 Output timing

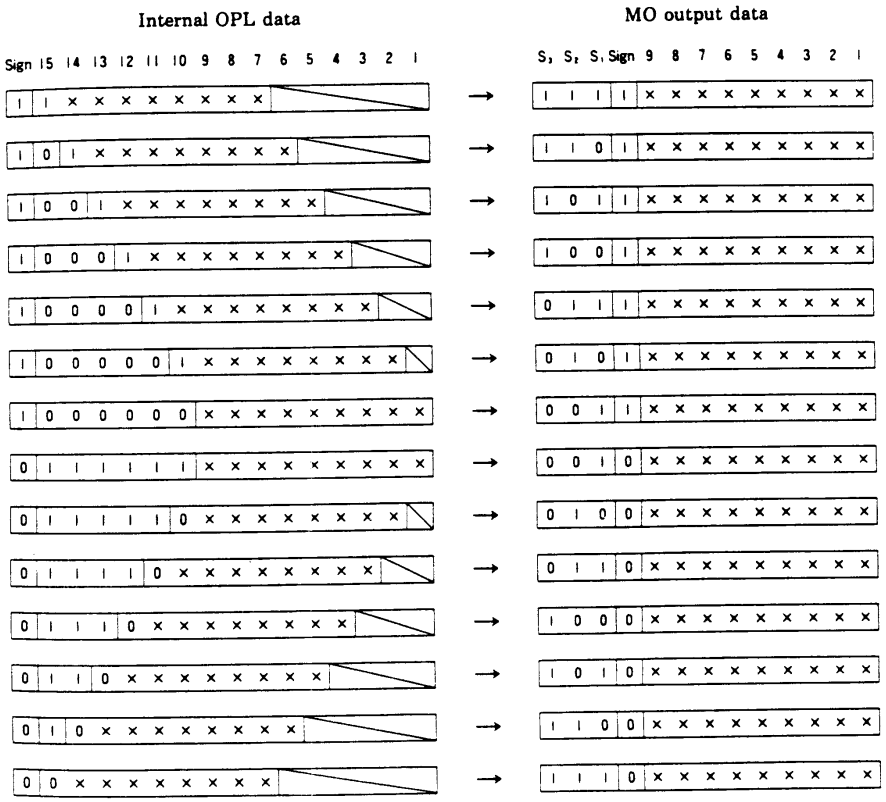


Fig. 3-4 Internal and output data

3-5. ADPCM Voice Analysis/Synthesis

The protocols used in ADPCM voice analysis/synthesis between the register is as follows.

(1) Voice analysis (AUDIO→CPU)

Address	Data	R/W	Comment
			Initialization
$04	$00	W	Each flag is enabled.
$04	$80	W	Each flag is reset.
$07	$C8	W	ADPCM analysis is enabled and the speaker is OFF.
$08	$00	W	
$0D	$C2	W	Sampling rate is set to 8 kHz (NPRE = 450).
$0E	$01	W	
			Analysis starts.
$0F		R	Start with dummy read
			Analysis
$0F		R	When BUF.RDY flag is "1", $0F is read, the analysis data is
($04	$80	W)	stored, and the flag is reset. When BUFD.RDY flag is "0", wait.
			Analysis ends.
$07	$48	W	ADPCM analysis is completed.
$07	$00	W	Address $ 07 is reset.

(2) Voice synthesis (CPU→AUDIO)

Address	Data	R/W	Comment
			Initialization
$04	$00	W	Each flag is enabled.
$04	$80	W	Each flag is reset.
$07	$80	W	ADPCM synthesis is enabled.
$08	$00	W	
$10	$F6	W	Sampling rate is set to 8 kHz (Δ N = 10486).
$11	$28	W	
$12	$□□	W	Output level is specified.
			Synthesis starts.
$0F	$××	W	Start by writing ADPCM data to $0F
			Synthesis
$0F	$△△	W	When BUF.RDY flag is "1", synthesis data is written to $0F
($04	$80	W)	and the flag is reset. When flag is "0", wait.
			Synthesis ends.
$07	$00	W	ADPCM synthesis is completed.

(3) Voice analysis (AUDIO→EXT.MEMORY)

Address	Data	R/W	Comment
			○Initialization
$04	$08	W	Only BUF.RDY flag is masked.
$04	$80	W	Each flag is reset.
$07	$68	W	ADPCM analysis is enabled.
$08	$02/$00	W	RAM type is specified.
$09	$××	W	Start address in memory
$0A	$××	W	
$0B	$^^	W	Stop address in memory
$0C	$^^	W	
$0D	$E1	W	Sampling rate is set to 16 kHz (NPRE = 225).
$0E	$00	W	
			○Analysis starts.
$07	$E8	W	Start when D7 ($07) becomes "1".
			○Analysis
			$07 waits till end of synthesis is posted (i.e. till EOS flag becomes "1").
			○Analysis ends.
$07	$68	W	ADPCM analysis is completed.
$07	$00	W	Address $07 is reset.

(4) Voice synthesis (EXT.MEMORY→AUDIO)

Address	Data	R/W	Comment
			○Initialization
$04	$08	W	Only BUF.RDY flag is masked.
$04	$80	W	Each flag is reset.
$07	$20/$30	W	ADPCM synthesis is enabled.
$08	$00,$01,$02	W	Memory type is specified.
$09	$××	W	Start address in memory
$0A	$××	W	
$0B	$^^	W	Stop address in memory
$0C	$^^	W	
$10	$EC	W	Sampling rate is set to 16 kHz (Δ N = 20972).
$11	$51	W	
$12	$	W	Output level is set.
			○Synthesis starts.
$07	$A0/$B0	W	Start when D7 ($07) becomes "1".
			Synthesis
			$07 waits till end of synthesis is posted (i.e. till EOS flag becomes "1").
$07	$A0	W	Repeat mode is released.
$07	$A1	W	Synthesis is forcibly interrupted.
			Synthesis ends.
$07	$20	W	ADPCM synthesis is completed.
$07	$00	W	Address $07 is reset.

3-6. AD/DA Conversion

The built-in AD/DA converter can be used for FM sounding and ADPCM voice analysis/synthesis, as well as for AD or DA conversion. Conversion rates range from a maximum sampling rate of 16kHz to a minimum sampling rate of 1.8 kHz.

(1) AD conversion

The MSX-AUDIO uses the DA converter in the sound generator for AD conversion. The DA converter performs conversion in a voltage range within Vcc/2 ± Vcc/4. The maximum voltage is 3 Vcc/4 (127), the mid point is Vcc/2 (0), and the minimum voltage is Vcc/4 (-128). Converted data is expressed as 8-bit two's complement data. (Successive approximation type conversion)

Auxilliary equipment, including the music output equipment, must be disconnected from the DA converter during AD conversion. If not, problems may result – e.g., excessively loud sound output.

(2) DA conversion

The same DA converter is used for DA conversion (output voltage within Vcc/2 ± Vcc/4). Converted data is expressed as 13-bit data with a 3-bit exponent part and a 10-bit virtual part. However, if necassary to process the data expressed in 8 bits (in relation to AD conversion), only vary the data of address $15 and fix $16 and $17 data to enable processing in units of bytes.

3-7. External-Memory Control

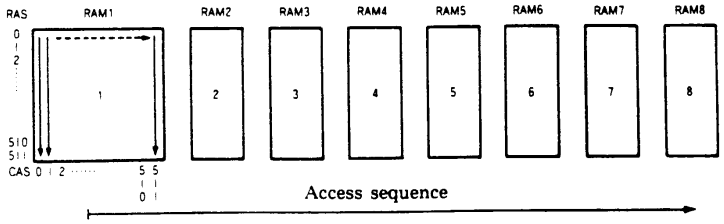
Up to 256K-bytes (RAM or ROM) of external memory can be accessed as a data file for ADPCM voice analysis/synthesis. The MSX-AUDIO's external-memory controller controls the external memories and provides an interface.

(1) RAM

Up to eight DRAMs (either 64K DRAM or 256K DRAM) can be connected.

The MSX-AUDIO sequentially accesses the memories from the 1st to the 8th DRAM. Each RAM is sequentially read/written (as shown in the figure below) – from address (0,0) through address (511,0), and from (0,1) through (511,511). Consequently, RAM data processing is performed in units of single bits, while address-specification is performed in units of 32 bits (4 bytes).

The contents of RAMs are refreshed by the MSX-AUDIO's counter, and addresses are automatically generated.



Unlike the addresses in RAMs which are connected with MSX-AUDIO's DM output, the addresses are input in ROMs via latches. ROMs are accessed in byte unit and addresses are specified for every 32 bytes.

(3) Memory access

During ADPCM, the memories are automatically accessed by the MSX-AUDIO. For data transfer between the processor and the memories, the following programming is required.

(a) RAM-WRITE

Address	Data	R/W	Comment
			Initialization
$04	$00	W	Each flag is enabled.
$04	$80	W	Each flag is reset.
$07	$60	W	Memory write mode is set.
$08	$00 $02	W	Memory type is specified.
$09	$××	W	Start address is specified.
$0A	$××	W	
$0B	$△△	W	Stop address is specified.
$0C	$△△	W	
			Memory write
$0F	$□□	W	Data is written.
$04	$80	W	When BUF.RDY flag is "1", data write; when "0", wait. When EOS flag is "1", data write ends.
			Reset
$07	$00	W	Address $07 is reset.

(b) RAM/ROM-READ

Address	Data	R/W	Comment
			Initialization
$04	$00	W	Each flag is enabled.
$04	$80	W	Each flag is reset.
$07	$20	W	Memory read mode is set.
$08	$00, $01, $02	W	Memory type is specified.
$09	$××	W	Start address is specified.
$0A	$××	W	
$0B	$△△	W	Stop address is specified.
$0C	$△△	W	
			Memory read
$0F		R	Start after dummy reading two times
$0F		R	(Necessary to check flag)
$0F	$□□	R	Data is read.
$04	$80	W	When BUF.RDY flag is "1", data is read; when "0", wait. When EOS is set to "1", data read ends.
			Reset
$07	$00	W	Address $07 is reset.

3-8. Keyboard IN/OUT

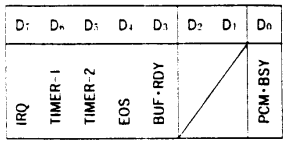
For easy keyboard connection, the keyboard input/output ports have an input terminal with pull-up resistors and an open-drain type output terminal. The 8-bits input/output ports enable the connection of the keyboard with up to 49 keys. The drive capacity affords a load of up to 500 pF with a scanning rate of 20 μs. General-purpose input/output ports can also be connected.

3-9. Status Data and Interrupt Requests

The MSX-AUDIO's status data includes the flags set by two timers and two flags (BUF.RDY, EOS) used during ADPCM voice analysis/synthesis and access to external memories. Each flag is set to "1" when the corresponding event occurs. Unnecessary flags can be masked.

An interrupt request (IRQ) is output (set to low level) when any one of the flags is set to "1". Because the IRQ is output from the open-drain type ports, it can be transmitted to other equipment through the wired logic.

Status



D0 (PCM.BSY): During ADPCM voice analysis/synthesis, this bit is set to "1" when bit D7 (SDTART) of address $07 becomes "1". No IRQ is generated by this setting.

D3(BUF.RDY): This bit is set to "1" in the following cases:

- ADPCM voice analysis: at the end of analysis (@ADD. $07, D5 = 0)
- ADPCM voice synthesis: at the end of synthesis (@ADD. $07, D5 = 0)
- External memory write: at the end of writing
- External memory read: at the end of reading

D4(EOS): This bit is set to "1" when analysis and synthesis are completed during ADPCM voice analysis/synthesis, or when the sampling time elapses during AD/DA conversion.

D5(TIMER-2): This bit specifies the flag signal sent from timer-2 and is set to "1" when the time set for timer-2 elapses.

D6(TIMER-1): This bit is used by the timer-1 as D5 is for timer-2.

D7(IRQ): This bit is set to "1" when any of D3--D6 is "1".

4 INTERFACE

The MSX-AUDIO is controlled by a microcomputer, and audio signals are converted into analog signals through the DA converter of the MSX-AUDIO. The MSX-AUDIO can controls external memories (ROM/RAM), keyboards, and other external devices. The interface between the MSX-AUDIO and peripheral equipment is described as follows.

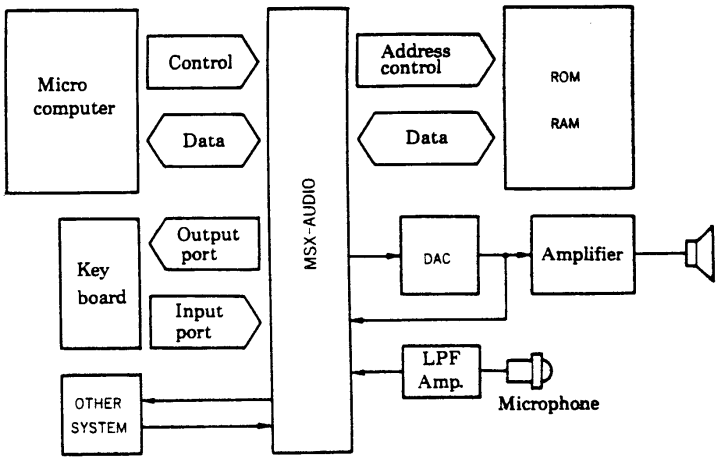


Fig. IV-1 System block diagram

4-1. Audio Output Interface

The MSX-AUDIO outputs digital sound signals, and it requires an external DA converter, such as the Yamaha YM3014. The YM3014 is a floating DA converter that uses thin-film resistors with a resolution of 16 bits, and can be used with the MSX-AUDIO to drive the audio amplifier. Because the output line transmits different types of signals, including FM sound generator output, ADPCM voice synthesis data, and PCM sounding data, a low pass filter that matches the sampling frequency of the signals must be inserted between the DA converter and amplifier. The filter is controlled by the input/output ports. Also required are a speaker-protection circuit (for AD conversion) and a circuit to eliminate click noises.

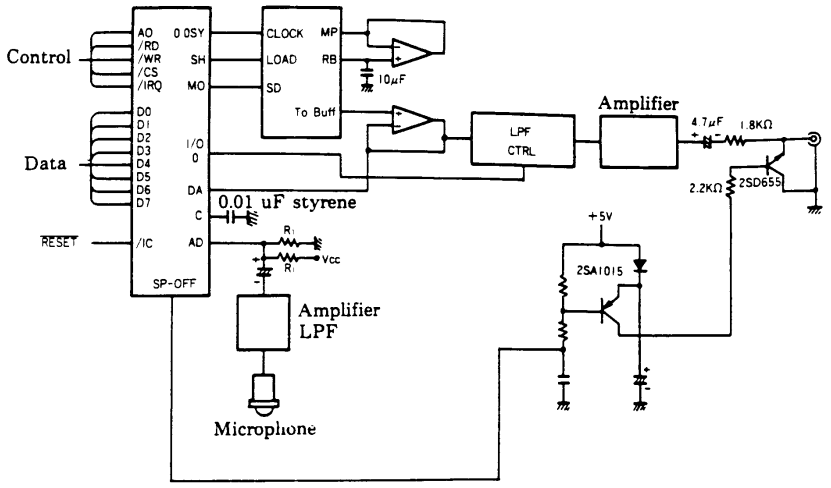


Fig. 4-2 Audio output interface

4-2. External-Memory Interfaces

Up to 256K-bytes of ROM and DRAM capacity can be connected externally to the MSX-AUDIO. Because all signals used to control the memories are provided by the MSX-AUDIO, the DRAM interface requires a tri-state buffer, and the ROM interface requires the circuits to latch addresses with $\overline{RAS}$ / $\overline{CAS}$ clock signals.

No external circuits are required for connecting one DRAM.

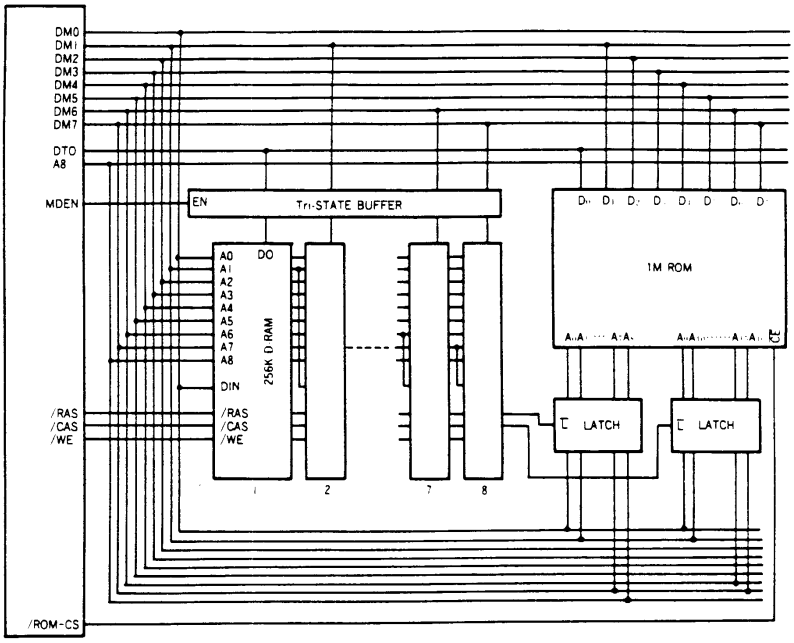


Fig. 4-3 Memory interface

4-3. Keyboard Interface

The MSX-AUDIO has the input/output ports (8 bits each) for connecting a keyboard equipped with up to 49 keys. Fig. 4-4 shows the keyboard interface.

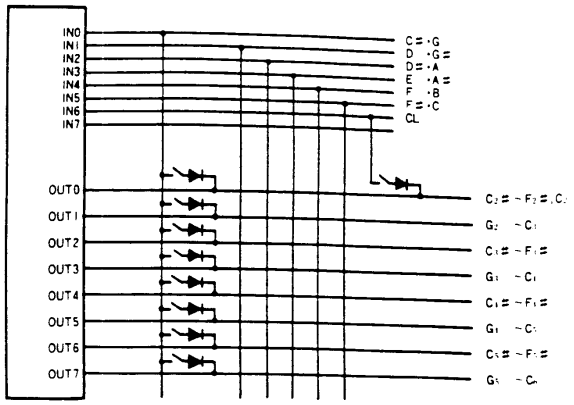


Fig. IV-4 Keyboard interface

4-4 Microcomputer Interface

The MSX-AUDIO is connected with a microcomputer via data bus lines (D0–D7) and a control-signal (A0, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, $\overline{IRQ}$) line. The data bus is used to write addresses and data to the MSX-AUDIO, and the control signals are used to specify the direction of data transfer on the data bus and type of data (address, data, or status) to be sent.

V-1 Bases for sound Generation

Item	Related parameters	MIN←tone change→MAX
Carrier output level	TOTAL LEVEL Each A, D, S, R data key scale data	Low output level ⟷ high output level
Modulator output level		"Round" tone ⟷ bright tone
Modulator feedback level	F B	Normal tone ⟷ sharp tone (Noise)
Carrier frequency	MULTI (BLOCK/F-Number)	Low pitch ⟷ high pitch
Modulator frequency		Neighboring harmonics ⟷ distant harmonics

5-3. Example of Sound Generation

(1) Electric piano

(a) Connection

Set the Connection to "0". Almost all kinds of sound can be generated with Connection = "0". In this example, operator 1 is used to generate an accent in attack and rich harmonics.

(b) Operator frequency

Set the multiplier of the two operators to "1" to generate all harmonics of the integrally multiplied frequencies.

(c) Operator output level

Vary the modulation output to control the tone color. Set the operator 1 level for low tones with rich harmonics. Then, adjust operator 1 by level scaling for tone shifting toward higher tones. High tones require enough level scaling to nearly generate sine waves.

(d) EG setting

Specify the output level and tone-color envelope. Set operator 2 for sharp attack and a fairly sustained envelope. Operator 1 (modulator) must be set for rich harmonics at attack time and stable harmonics after the attack time. Key scaling is done for operator 2 to adjust the output level. It is recommended to scale the RATE for sharp high tones.

(e) Readjustment of data

The tone colors become slightly different from the original tone because of the EG settings. Consequently, readjustment must be done for operator output and feedback levels. For instance, if an excessive metallic tone exists, decrease the level of operator 1.

(f) Addition of effects

Use the LFO to add a tremolo effect, which is a characteristic of electric piano sound. The tremolo effect can also be added by using the built-in amplitude modulator or by setting the software to shift total level value at 2--6 Hz cycle by using traiangular waves.

(2) Trumpet

(a) Connection

Set the Connection to "0" also for brass sounds. By controlling the feedback level of operator 1, bright, loud brass sounds can be generated.

(b) Operator output

The total level of "modulation" operator 1 must be set low at around $10--$28, but the feedback level must be set to the maximum "7" for brighter tone color.

(c) Operator frequency

Normally, set the multiplier to "1" for both operators.

(d) EG setting

Set both operators for slow attack. For brass sounds, modulator attack must be set slower than the carrier waves to generate the typical attack ("Bwan") of brass sounds.

(e) Key scaling

Because the attack has been set slow, high tones have less clarity. To maintain natural brass tone colors even during fast melodies, scale the RATE to some extent as necessary.

(f) LFO

Even a talented brass player cannot precisely maintain a pitch of a long tone. To add such slight pitch shifting to the sound generated, set the vibrato effect.

V-4. Generation of Rhythmic Sounds

The MSX-AUDIO uses three channels (7, 8, and 9) with six slots to generate a total of five rhythmic sounds. Only the bass drum sound is generated by two slots with the FM sounding. Therefore, the procedures (v-1)~(v-3) can be basically used to generate bass drum sounds. Here, the setting procedure for the remainning four rhythmic sounds (high-hat cymbals, top cymbal, tom-tom, and snare drum) are described.

The OPL has a noise oscillator to provide white noise and several kinds of frequencies for generating rhythmic sounds. The oscillator combines the frequency data (BLOCK/F-Number/Multi) of channels 8 and 9 with white noise to generate phase output corresponding to rhythmic instruments and sends the outut to the operator. In other words, four different phase data items for four instruments are generated from two frequency data items. It is empirically known that an optimum ratio of two set frequencies should be 3:1 (f7CH = 3*f8CH). Consequently, add the envelope information to the obtained phase data. For the envelope setting, one slot is used per instrument. Set the required parameters for generating specific features of each instrument in the registers. (See 3-1-23.) Rhythmic sounds are generated according to the above procedure.

6. ELECTRIC CHARACTERISTICS

6-1. Absolute Maximum Rating

Item	Rated value	Unit
Terminal voltage	−0.3 ~ 7.0	V
Operating ambient temperature	0 ~ 70	℃
Storage temperature	−50 ~ 125	℃

6-2. Recommended Operating Conditions

Item	Symbol	Minimum	Standard	Maximum	Unit
Power voltage	Vcc	4.75	5.0	5.25	V
	Vss	0	0	0	V

6-3. DC Characteristics

Item		Symbol	Condition	Minimum	Standard	Maximum	Unit
Inut high-level voltage	Input except for	V_{IH1}		2.0			V
	IN0--7	V_{IH2}		3.5			V
Input low-level voltage	Input except for	V_{IL1}				0.8	V
	IN0--7	V_{IL2}				1.5	V
Input leak current	A_0, WR, RD, DTO	I_{IL}	V_{IN} = 0 ~ 5V	−10		10	μA
Three-state (offset-state) input current	D_0 ~ D_7, DM_0 ~ DM_7	I_{TSL}	V_{IN} = 0 5V	−10		10	μA
	IO_0 IO_7						
Output high-level voltage	Output except for $\overline{IRQ}$, OUT0--7	V_{OH1}	I_{OH1} = 0.4mA	2.4			V
		V_{OH2}	I_{OH2} = 40μA	3.3			V
Output low-level voltage	All output	V_{OL}	I_{OL} = 2mA			0.4	V
Output leak current (offset state)	$\overline{IRQ}$, OUT_{0-7}	I_{OL}	V_O = 0 5V	−10		10	μA
Analog input voltage	AD, DA	V_A		Vcc-1		Vcc+1	V
Pull-up resistor	$\overline{IC}$, $\overline{IRQ}$	R_{P1}		60		600	KΩ
	IN_{0-7}	R_{P2}		5		10	KΩ
Input capacity	All input	C_{IN}	f = 1MHz			10	pF
Output capacity	All output	C_{OUT}	f = 1MHz			10	pF
Power supply current		I_{CC}				70	mA

6-4. AC Characteristics

Item	Symbol		Condition	Minimum	Standard	Maximum	
Input clock frequency	φM	fc	A-1	3	3.58	4	MHz
Input clock duty	φM			40	50	60	%
Input clock rise time	φM	T_{cr}	A-1			50	ns
Input clock fall time	φM	T_{cf}	A-1			50	ns
Address setup time	A_0	T_{AS}	A-2, A-3	10			ns
Address hold time	A_0	T_{AH}	A-2, A-3	10			ns
Chip select write width	$\overline{CS}$	T_{CSW}	A-2	380			ns
Chip select read width	$\overline{CS}$	T_{CSR}	A-3	380			ns
Write pulse write width	$\overline{WR}$	T_{WW}	A-2	380			ns
Write data setup time	D_0 D_7	T_{WDS}	A-2	10			ns
Write data hold time	D_0 D_7	T_{WDH}	A-2	30			ns
Read pulse width	$\overline{RD}$	T_{RW}	A-3	380			ns
Read data access time	D_0 D_7	T_{AC}	A-3			380	ns
Read data hold time	D_0 D_7	T_{RDH}	A-3	10			ns
Output port fall time	OUT_0 ~	T_{OPF}	C_L = 500pF (Note)	20			μs
Memory data set time	DM_{1-7}, DT_0	T_{MDS}	A-6	70			ns
Memory data hold time	DM_{1-7}, DT_0	T_{MDH}	A-6	10			ns
Output rise time	DM_{0-7}, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A_8, MDEN, $\overline{ROM-CS}$, ϕ_{SY}	T_{OR}	A-4			100	ns
	SH, MO	T_{OR}	A-4			150	ns
Output fall time	DM_{0-7}, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A_8, MDEN, $\overline{ROM-CS}$, ϕ_{SY}	T_{OF}	A-4			100	ns
	SH, MO	T_{OF}	A-4			150	ns
Reset pulse width	$\overline{IC}$	N_{IC}	A-5	80			cycle

(Note)

A time period from when the output request was issued through the output ports until the output port voltage becomes 1.0 V.

7. TIMING CHART (Timing setting using reference values VH = 2.0V and VL = 0.8V)

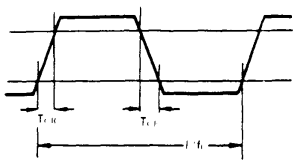


Fig. A-1 Clock timing

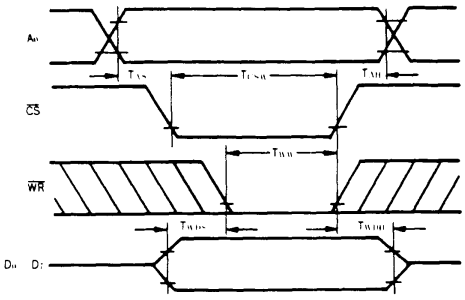


Fig. A-2 Write timing

(Note)

TWDS is based on whether $\overline{CS}$ or $\overline{WR}$ is subsequently set to a low level.

TCSW, TWW, and TWDH are based on whether $\overline{CS}$ or $\overline{WR}$ is set to a high level.

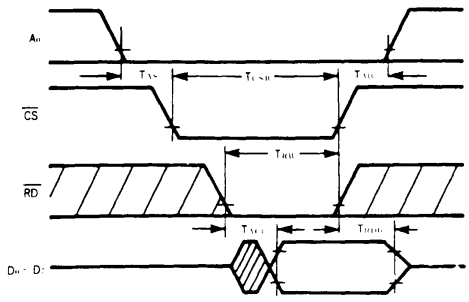


Fig. A-3 Read timing

(Note)

TACC is based on whether $\overline{CS}$ or $\overline{RD}$ is subsequently set to a low level.

TCSR, TRW, and TRDH are based on whether $\overline{CS}$ or $\overline{RD}$ is set to a high level.

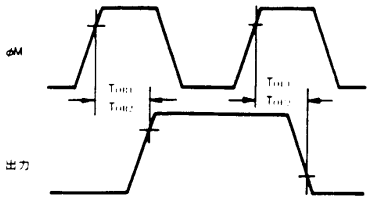


Fig. A-4 Output timing

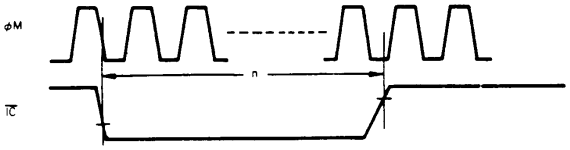


Fig. A-5 Reset pulse width

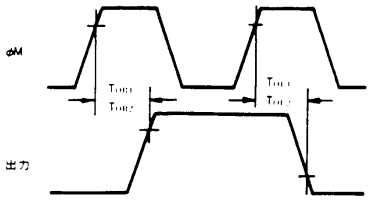


Fig. A-4 Output timing

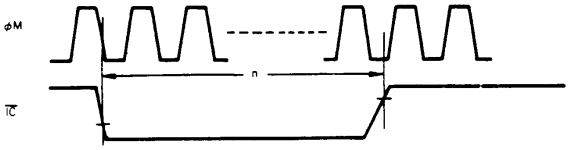
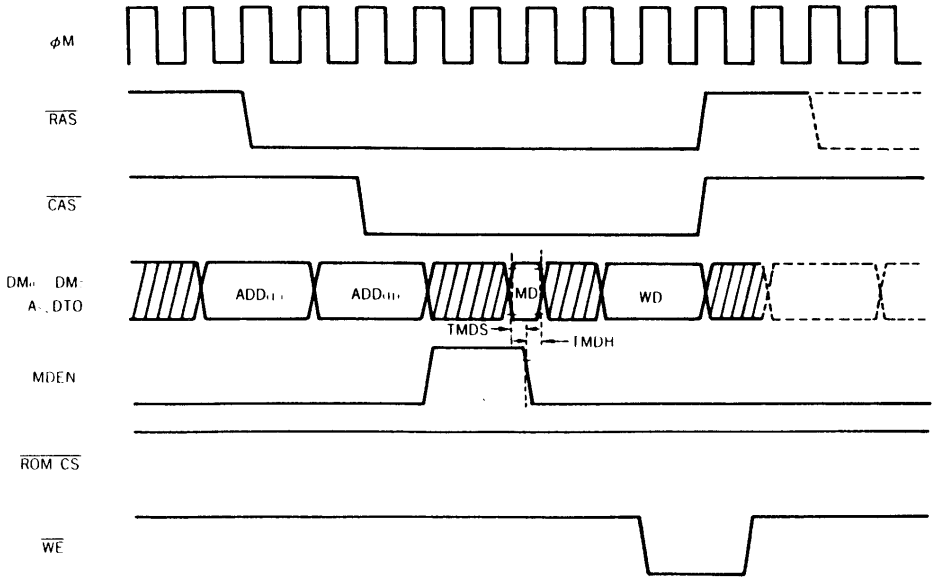


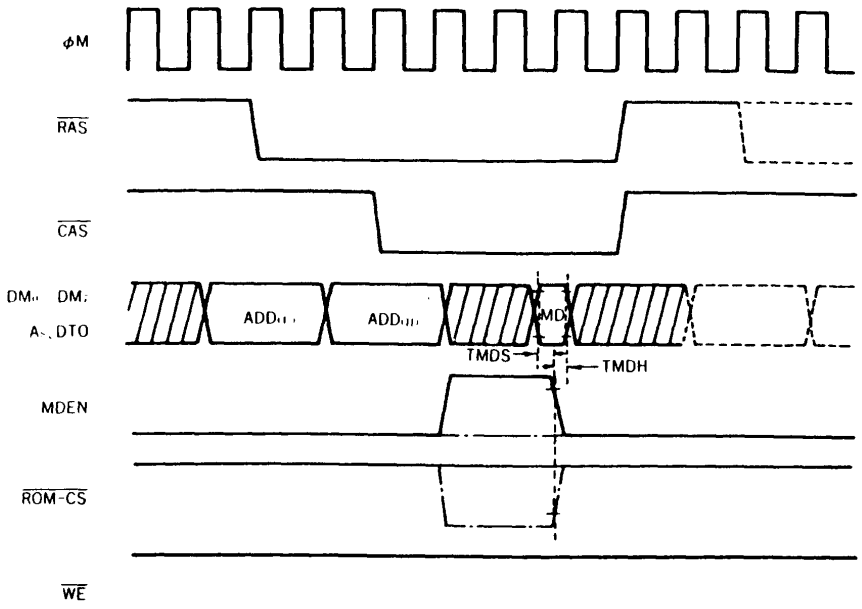
Fig. A-5 Reset pulse width



(Note)

Only ADD(L) and ADD(H) are specified for A8, only MD is specified for DT0, only ADD(L), ADD(H), and WD are specified for DM0.

Fig. A-6-a External-memory write cycle



(Note)

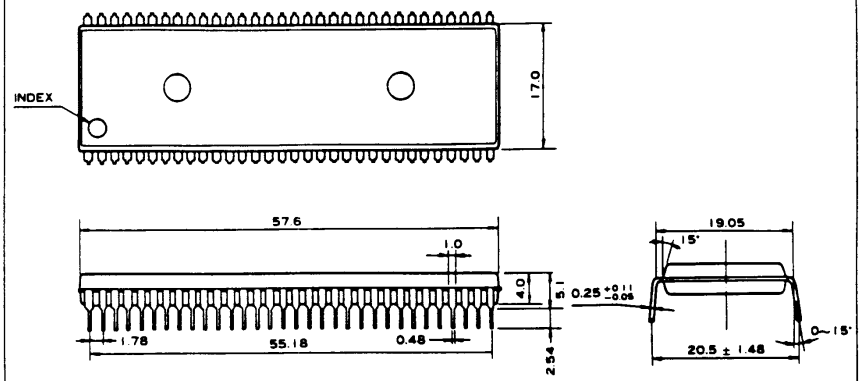
Only ADD(L) and ADD(H) are specified for A8, only MD is specified for DT0, and only ADD (L) and ADD(H) are specified for DM0. For MDEN and $\overline{\text{ROM-CS}}$, the solid line indicates the RAM read cycle. The dotted line (with points and short lines) indicates the ROM read cycle.

Fig. A-6-b External-memory read cycle

8. PACKAGE DIMENSIONS

Y8950

1. 64-pin shrink DIL



(Note) Specifications of this product are subject to change for purpose of improvement without prior notice.