Universal Serial Bus Implementers Forum Hub High-speed Electrical Test Procedure

Revision 1.0

Dec 23, 2001

Revision History

Rev	Date	Filename	Comments
0.8	June-29-2001	Hub HS Test.DOC	Initial draft revision
0.81	12-Jul-01	Hub HS Test.DOC	Changed el_17 on page 58 to reference section 7.1.6.2
0.9 (Beta)	Aug-31-2001	Hub HS Test.DOC	Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification
1.0	Dec-23-2001	Hub HS Test.DOC	Edit for final release. Delete TDR section.

Please send comments via electronic mail to techsupp@usb.org

USB-IF High-speed Electrical Test Procedure

Table of Contents

1 Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Hub High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Host High-speed Electrical Test Procedure and Device High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Equipment Required

The commercial test equipment listed here are base on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

- Digital Sampling Oscilloscope:
  - Tektronix TDS694C digital sampling oscilloscope
    - Tektronix P6247 or P6248 or equivalent differential probe, qty = 2
    - Tektronix P6245 FET probes, qty = 2

- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent
  - Mini-clip DMM lead – one each of black and red color
- Digital Signal Generator
  - Tektronix DG2040 Digital Signal Generator
    - 5x attenuator – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2
    - 50-ohm coaxial cable with female SMA connectors at both ends, qty = 4
- High-speed USB Electrical Test Fixtures
    - Host high-speed signal quality test fixture, qty = 1
    - Device high-speed signal quality test fixture, qty = 1
    - Disconnect test fixture, qty = 1
    - 5V test fixture power supply, qty = 1
    - Female Serial B to female Serial A adaptor, qty = 1
- Miscellaneous Cables
    - 1M USB cable, qty = 1
    - 1.5M USB cable, qty = 1
    - 4-inch USB cable, qty = 1
    - Modular AC power cord, qty = 2
- High-speed Signal Quality Analysis Computer

This is a computer with Windows 2000 Profession OS, and have the GPIB-DAQ and Mathworks, Inc's Matlab installed. It retrieves the captured data from the oscilloscope through a GPIB interface. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

- High-speed USB Test Bed Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. This OS on this computer is Windows 2000 Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

Note: One can consolidate the High-speed Signal Quality Analysis Computer and the High-speed USB Test Bed Computer into one single PC.

3.1 Equipment Setup

3.1.1 TDS694C Digital Sampling Oscilloscope

Before turning on the oscilloscope. Attach a P6247 or P6248 differential probes to Channel-1 and Channel-4. Attach two P6245 FET probes, one to Channel-2 and one to Channel-3. The probe assignment will be used through out the entire test procedure. Turn on the oscilloscope to allow for 10 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the TDS694C (in the Utility menu) if the ambient temperature has changed more than 5

degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes will be cancelled later as a part of the test procedure process. The offset of the differential probe will be adjusted by the step identified in the test procedure.

For P6247/P6248 differential probes, the following setting will be used through out the entire test procedure:

- DC Reject <OFF> (P6247 only)
- BW <Full> (P6247 only)
- Attenuation <÷1>

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.1.2 DG2040 Digital Signal Generator

The DSG is needed to perform the receiver sensitivity test that is structured toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the DSG about 15 minutes prior to performing the measurement.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operation Systems

Microsoft Windows 2000 Professional is required on the High-speed Electrical Test Bed Computer. Microsoft Windows 2000 Professional is required on the High-speed Signal Quality Analysis Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.

- Proprietary EHCI Driver Stack - The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result much more robust test bed environment. Since the proprietary EHCI driver stack is designed

for debug and test validation purposes, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.

- Matlab 6 – Data analysis programming software
- USB Electrical Test Analysis Scripts for Matlab 6 – For performing electrical signal quality test on USB devices.
- GPIB DAQ – This is developed by USB-IF for importing the digitized signal in TSV (Tab Separated Value) file format from the DSO into the Matlab analysis script for signal analysis.

3.3.1 Test Equipment Setup Files

These are 3 ½ inch floppy diskettes that contain the setup files for the test equipment. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these setup disks.

DSO Setup Disk – Contain setup files for Tektronix TDS694C DSO (Digital Storage Oscilloscope).

DPG Setup Disk – Contain setup files for Tektronix DG2040 DPG (Digital Pattern Generator).

4 Test Procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, power delivery (inrush, drop and droop), and TDR shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date

2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the hub under test must also pass the following legacy compliance tests applicable to the high-speed hub:

- Low speed signal quality – Downstream facing ports only
- Full speed signal quality – Upstream and downstream facing ports
- Inrush current – Upstream facing port only
- Drop / Droop – Downstream facing ports
- Interoperability

Perform all these tests and record the measurements and summarized Pass / Fail status in Appendix A.

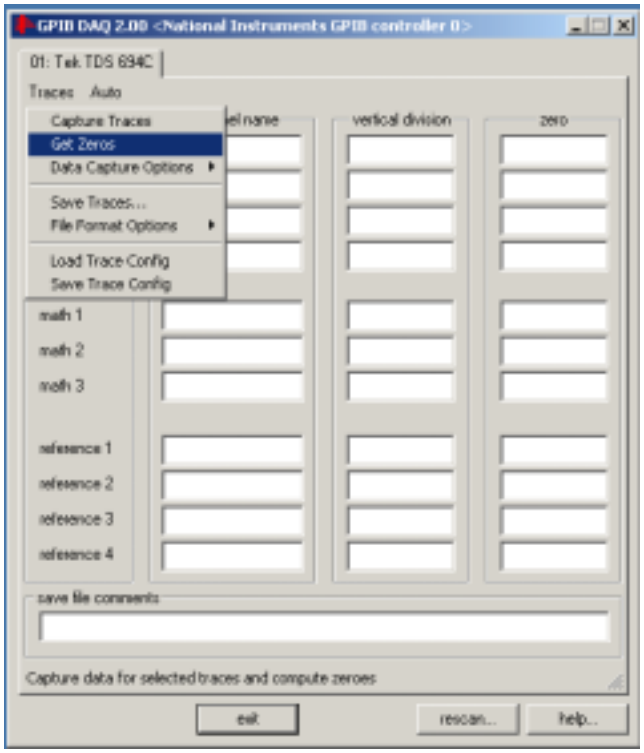
4.4 Hub High-speed Signal Quality – Upstream Facing Port (EL_2, EL_46, EL_6, EL_7)

This test is applicable only for the upstream facing port of the hub.

1. Turn on the oscilloscope if not already have done so. Allow about 10 minutes for warm up.

2. Boot the High-speed Signal Quality Analysis Computer to Windows 2000 OS. Invoke the GPIB-DAQ program. Invoke also Mathworks' Matlab program.

3. Recall HS_SQ_1.SET oscilloscope setup. Ensure the differential probe is not connected to anything. Force-trigger the oscilloscope to capture a near-zero differential measurement.



Get Zeros on GPIB-DAQ

4. On the GPIB-DAQ, click Get Zeros from the Traces drop down menu. This should generally be less than a few millivolts. The near-zero differential measurement will be used by the Matlab script to null out the residual offset on the probe / oscilloscope combination.

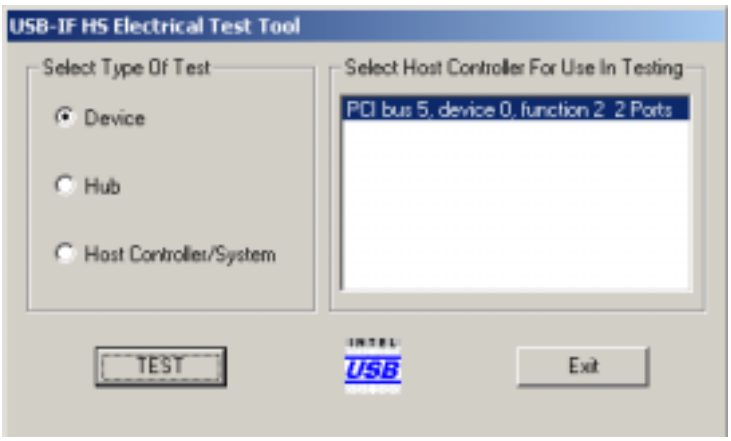
5. Attach the 5V power supply to J8 of the Device High-speed Signal Quality test fixture.

6. Verify green Power LED (D1) is lit, and the yellow Test LED (D2) is off.

7. Connect the Test port of the Device High-speed Signal Quality test fixture into the upstream facing port of the hub under test. Connect the Init port of the test fixture to a port of the Test Bed Computer. Apply power to the hub.

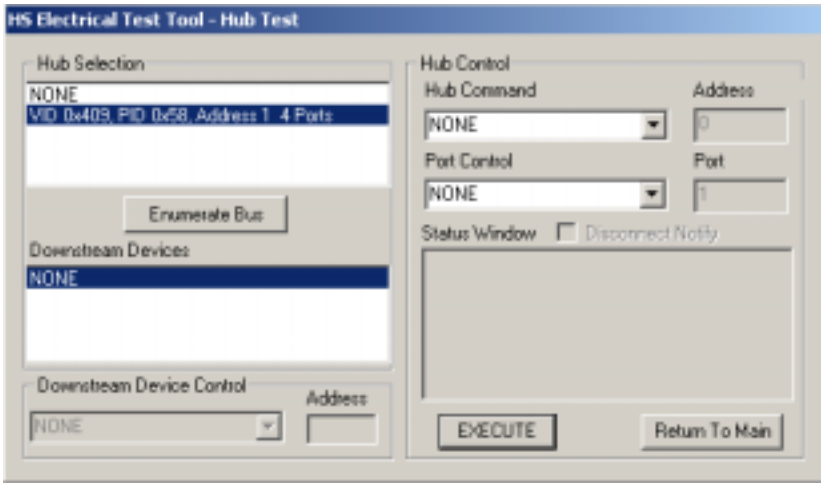
8. Attach the differential probe to J7 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

9. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



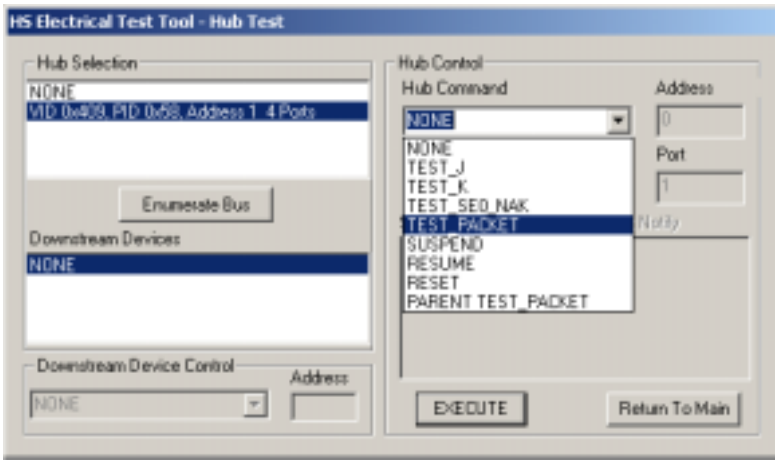
High-speed Electrical Test Tool – Main Menu

10. Select Hub and click the TEST button to enter the HS Electrical Test Tool – Hub Test menu. The hub under test should be enumerated with the hub's VID shown together with the USB address.



High-speed Electrical Test Tool – Hub Test Menu

11. Select TEST_PACKET from the Hub Command drop down menu and click EXECUTE. This forces the hub under test to continuously transmit test packets.



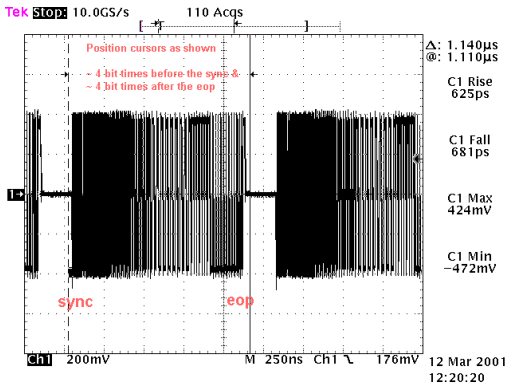
Hub Upstream TEST_PACKET

12. Place the Test Switch (S1) in the TEST position and verify the yellow TEST LED is lit.

13. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change to the trigger holdoff.

14. Pause the oscilloscope acquisitions using the Run / Stop button.

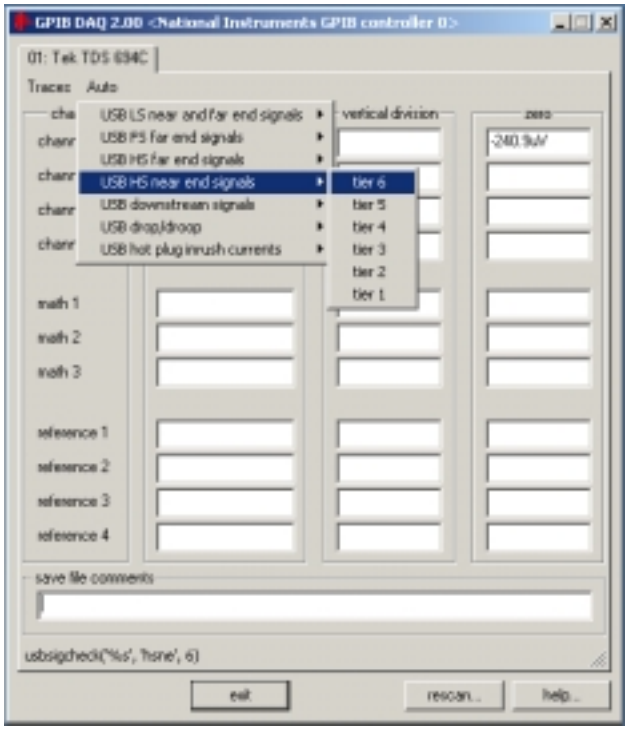
15. On the oscilloscope place the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure for reference.



Test Packet – Upstream Facing Port

16. On the GPIB DAQ graphical user interface select:

    Auto -> USB HS near end signals -> tier 6.

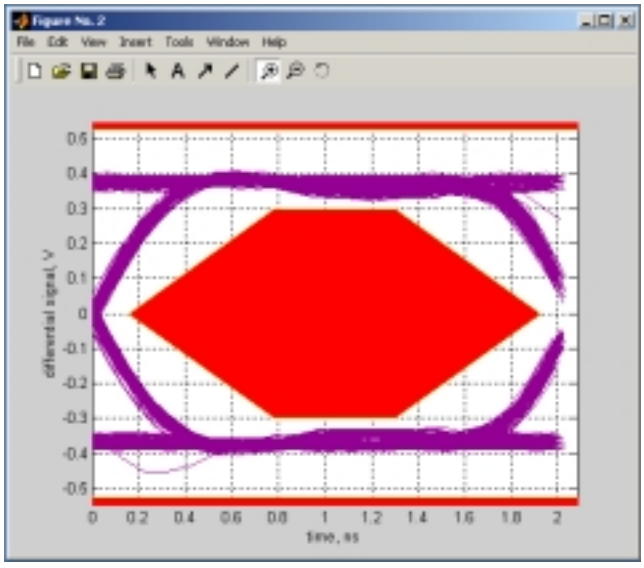


GPIB-DAQ

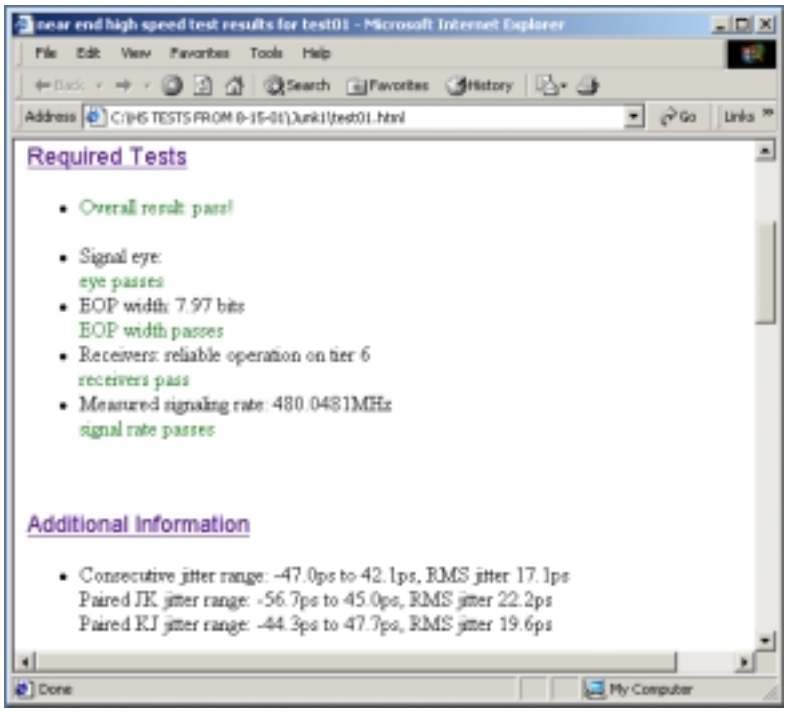
17. The GPIB may prompt you if you want to save the Get Zeros value at this point. Respond with No. Enter a descriptive file name (e.g. TIDxxxxxxx USNE.tsv) and save the *.tsv file to the desired directory.

18. Switch to the Matlab command window. Verify that the directory path, file name and test selected are correct. Press the Enter key to initiate analysis.

19. Verify the Signal Eye, EOP Width, and Signaling Rate all pass. The results displayed in the Matlab command window are also recorded to an HTML report located in the same directory as the *.tsv file.



High-speed SQ Eye Diagram



High-speed SQ HTML Report

20. Save all files created during the tests. Record the test result in EL_2, EL_46, EL_6, and EL_7.

21. Return the Test switch (S1) of the test fixture back to the Normal position and verify the yellow TEST LED is not lit. Cycle power on the hub in preparation for subsequent tests.

Note: If you desire to save a file to the same name as a previous test run, be sure you delete the old file first since the GPIB DAQ software will append the new data to the old file. This will cause the Matlab analysis script to fail..

4.5 Hub High-speed Signal Quality – Downstream Facing Ports (EL_2, EL_3, EL_6, EL_7)

This section applies only to the downstream facing ports of the hub under test.

1. Attach the 5V power supply to J8 of the Host High-speed Signal Quality test fixture.

2. Set the Test switch to the TEST position. Verify green POWER LED (D1) and the yellow TEST LED (D2) are both lit.

3. Attach the differential probe to J7 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

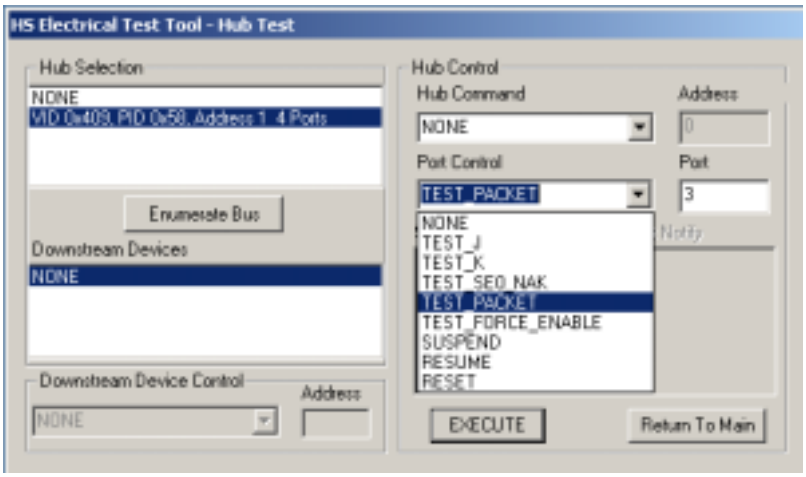
4. Recall the HS_SQ_1.SET oscilloscope setup.

5. Connect the upstream port of the hub to a high-speed root port of the test bed computer.

6. Connect the Test port of the Host High-speed Signal Quality test fixture into the down stream facing port under test of the hub. Apply power to the hub.

7. Click the Enumerate Bus button once. The hub under test should be enumerated with the hub's VID shown together with the USB address.

8. Select TEST_PACKET from the Port Control drop down menu. Enter the port number of the hub port being tested and click EXECUTE. This forces the hub port under test to continuously transmit test packets.

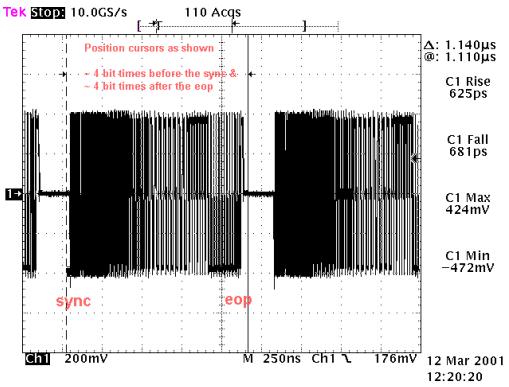


Hub Downstream TEST_PACKET

9. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change on the trigger holdoff.

10. Pause the oscilloscope acquisitions using the Run / Stop button.

11. On the oscilloscope place the two vertical cursors around one test packet, one just before the sync field and the other just after the EOP. Refer to the following figure.



Test Packet – Downstream Facing Ports

12. Using the GPIB DAQ graphical user interface select:

Auto -> USB HS near end signals -> tier 6

13. Enter a descriptive file name (e.g. TIDxxxxxxx DSNE port 1.tsv) and save the *.tsv to the desired directory.

14. Switch to the Matlab command window. Verify that the directory path, file name and test selected are correct. Hit the Enter key.

15. Verify the Signal eye, EOP Width, and Signaling Rate all pass. The results displayed in the Matlab command window are also recorded to an HTML report located in the same directory as the *.tsv file. Record the test result in EL_2, EL_3, EL_6, and EL_7.

16. Disconnect the test fixture from downstream facing port just tested. Reconnect it to the next downstream facing port to be tested.

17. Repeat steps 7 through 16 for all remaining ports.

18. Save all files created during the tests. Cycle power on the hub under in preparation for subsequent tests.

Note: A specific port fails to enter TEST_PACKET mode after TEST_PACKET command has been issued to the hub a number of times. Cycle power on the hub and click Enumerate Bus will alleviate this problem.

4.6 Hub Jitter – Downstream Facing Ports (EL_47)

This section applies only to the downstream facing ports of the hub under test.

1. Attach the 5V power supply to J8 of the Host High-speed Signal Quality test fixture. Set the Test switch of the test fixture to the TEST position. Verify green POWER LED (D1) and the yellow TEST LED (D2) are both lit.

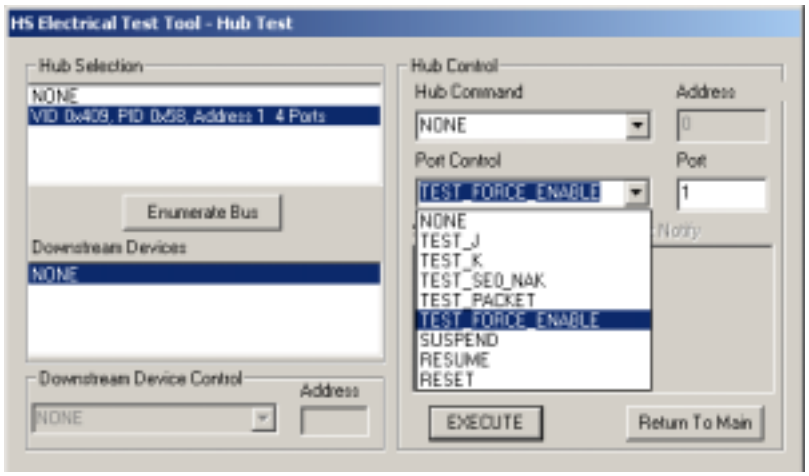
2. Attach the differential probe to J7 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture. Recall the HS_SQ_1.SET oscilloscope setup.

3. Connect the upstream port to a known good high-speed root port of the test bed computer using a 4-inch USB cable. Click the Enumerate Bus button once. The hub under test should be enumerated with the hub's VID shown together with the USB address.

4. Connect the Test port of the Host High-speed Signal Quality test fixture into the down stream facing port under test of the hub.

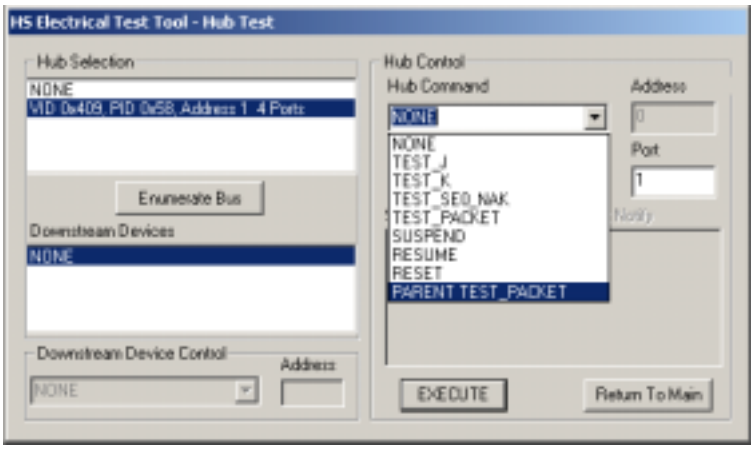
Note: The known good high-speed root port should have excellent signal quality eye and minimum clock jitter. A host controller with poor eye quality or clock jitter will tend to negatively affect the result of the hub under test.

5. Select TEST_FORCE_ENABLE from the Port Control drop down menu. Enter the port number of the hub port being tested and click EXECUTE once to force-enable the hub port under test.



Force-Enable Hub Downstream Port

6. Select PARENT PORT TEST_PACKET from the Hub Command drop down menu and click EXECUTE. This forces the parent port in which the hub is connected to continuously put out test packets. The hub port under test repeats these test packets and is ready for signal quality and jitter tests.

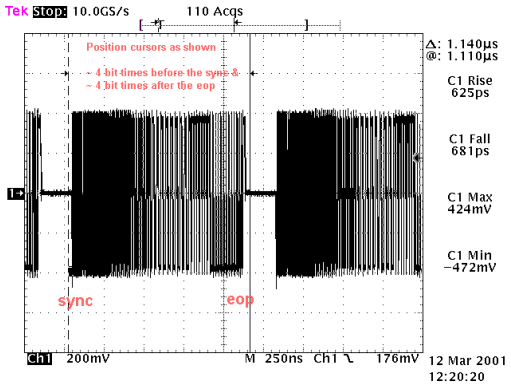


Placing Parent Port in TEST_PACKET

7. Using the oscilloscope, verify test packets are being transmitted from the hub port under test. Adjust the trigger level as necessary.

8. Pause the oscilloscope acquisitions using the Run / Stop button.

9. On the oscilloscope place the two vertical cursors around one test packet, one just before the sync field and the other just after the EOP. Refer to the following figure for reference.



Test Packet – Downstream Facing Repeater Jitter

10. Using the GPIB DAQ graphical user interface select: Auto -> USB HS near end signal -> tier 6.

11. Enter a descriptive file name (e.g. TIDxxxxxxxxDSNE hub jitter.tsv) and save the *.tsv to the desired directory.

12. Switch to the Matlab command window. Verify that the directory path, file name and test selected are correct. Press the Enter key to initiate the analysis.

13. Verify the Signal eye, EOP Width, and Signaling Rate all pass. The EOP width result should be ignored. The results displayed in the Matlab command window are also recorded to an HTML report located in the same directory as the *.tsv file. Record the test result in EL_47.

14. Repeat step 4 through step 13 for all remaining ports.

15. Save all files created during the tests. Cycle power on the hub under test in preparation for the subsequent test.

4.7 Hub Disconnect Detect (EL_36, EL_37)

Please note that the Disconnect Detect tests in this section apply only to downstream facing ports of the hub.

This section uses the Disconnect test fixture to verify the disconnect thresholds of the port under test by simulating the disconnect condition.

When the TEST switch on the test fixture is in the Test position, the port under test is subjected to a threshold <525mV. The port should not detect a disconnection.

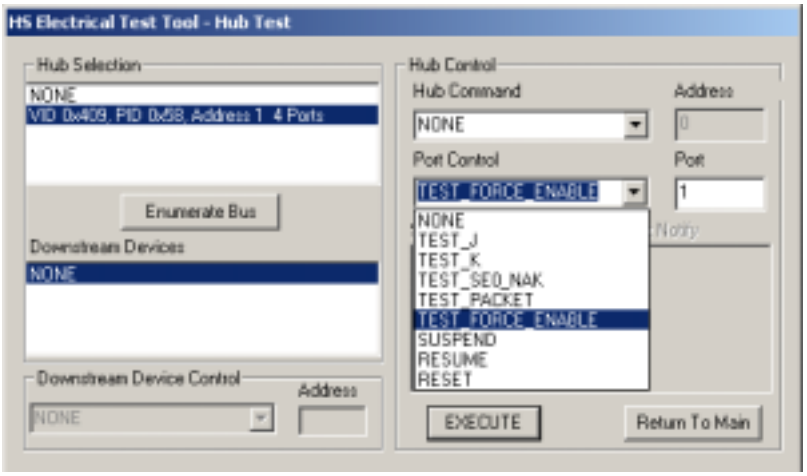
When the TEST switch is in the Normal position, the port under test is subjected to a threshold >625mV. The port should detect a disconnection.

1. Attach the 5V power supply to Disconnect test fixture (J8).

2. Attach the differential probe to J7 of the test fixture. Ensure the + tip on probe lines up with D+ on the fixture. Recall the DISCDETE.SET oscilloscope setup.

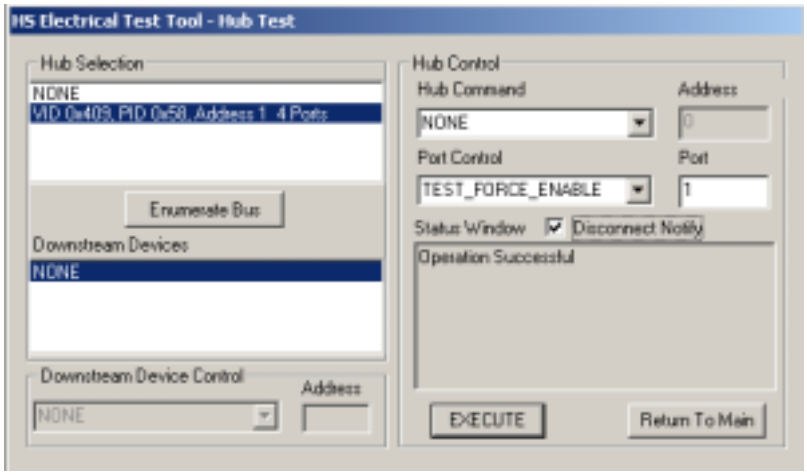
3. Set the TEST switch to the Test position. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is also lit. This sets the test fixture to emulate a must-not-disconnect threshold.

4. Cycle power on the hub under test. Click Enumerate Bus once and verify the hub successfully enumerates. Attach the Test port of the test fixture to the port under test. In the HS Electrical Test Tool – Hub Test menu select TEST_FORCE_ENABLE from the Port Control window. Enter the port number and click Execute once and ensure the operation is successful in the Status Window.



Force-Enable Hub Downstream Port

5. Click the Disconnect Notify check box to monitor the disconnect status in the Status Window.

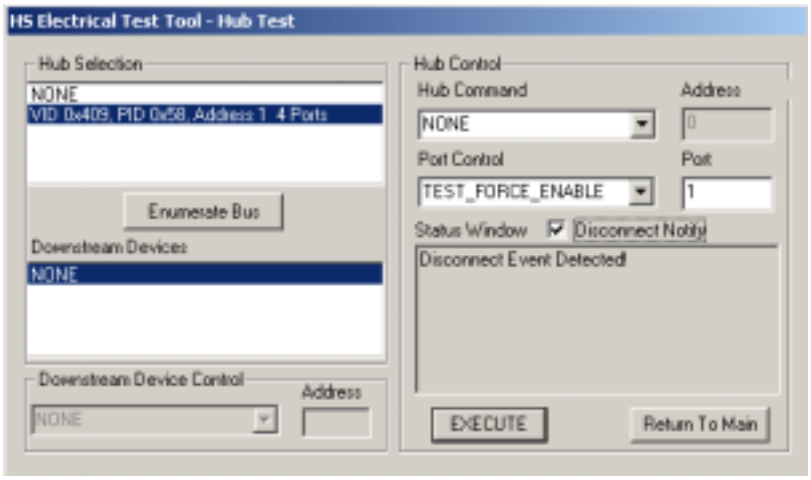


Enable Disconnect Notify

6. Using the oscilloscope, verify the SOF packets are being transmitted from the port under test. The differential amplitude should be less than +/- 525mV. Verify that the Status Window does not display Disconnect Event Detected. Record the pass/fail result in EL_37.

7. Set the TEST switch of the Disconnect test fixture to the Normal position and verify the yellow TEST LED (D2) is not lit.

8. Using the oscilloscope monitor the differential amplitude of the SOF. It should be greater than +/- 625mV. Verify that the Status Window now displays the Disconnect Event Detected. Record the pass/fail result in EL_36.



Disconnect Event Detected

9. Return the TEST switch on the fixture back to the TEST position and verify the yellow TEST LED (D2) is lit.

10. Repeat step 4 through 9 for all the remaining ports.

11. Remove the Disconnect test fixture from the port under test before proceeding.

4.8 Hub Packet Parameters – Upstream Facing Port (EL_21, EL_22, EL_25)

1. Connect the Init port of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.

2. Connect the Device Signal Quality test fixture (Test Port) into B receptacle of the upstream facing port under test of the hub. Apply power to the hub.

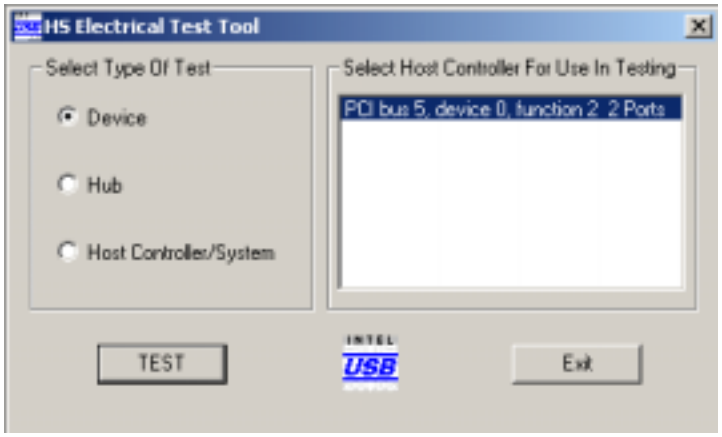
Note: The use of the Device High-speed Signal Quality test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the channel 1 differential probe to J7 on the fixture near the device connector. Ensure the + polarity on the probe lines up with D+ on the fixture.

4. Recall the PACKPARA.SET oscilloscope setup.

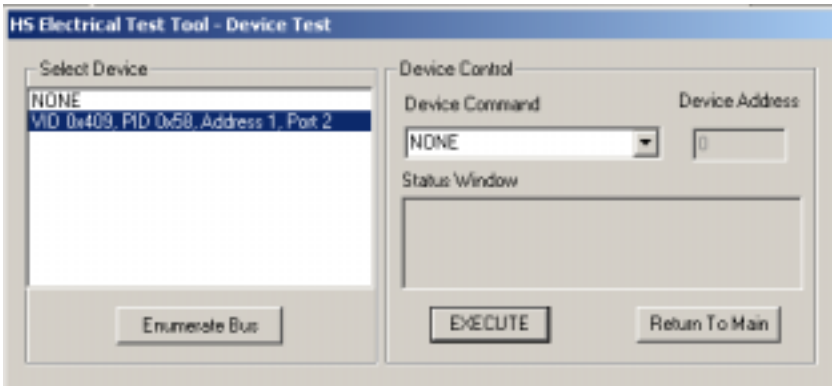
5. Exit the HS Electrical Test Tool – Hub Test menu by clicking the Return to Main button.

6. From the HS Electrical Test Tool main menu select Device and click TEST to enter the Device Test menu.



HS Electrical Test Tool Main Menu

7. The HS Electrical Test Tool – Device Test menu should appear as in the figure:

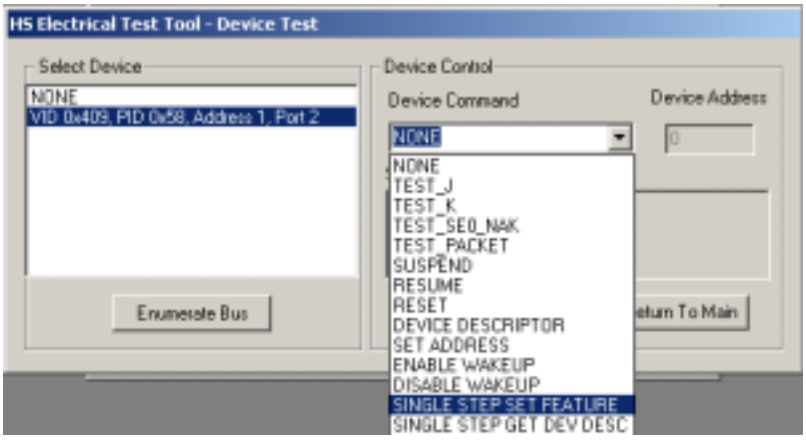


HS Electrical Test Tool – Device Test Menu

8. Using the oscilloscope, verify SOFs (Start Of Frame) packets are being transmitted on the port under test. You may need to lower the trigger level to somewhat below 400mV.

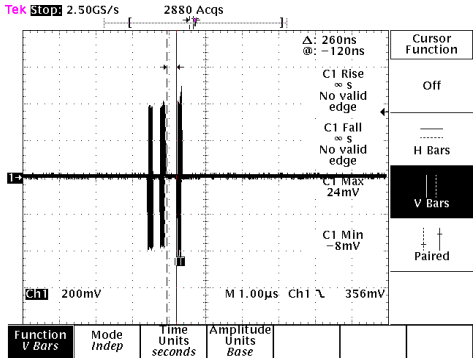
9. Now raise the oscilloscope's trigger level slowly until it doesn't trigger on SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the hub and the length of cable used on the fixture.

10. In the HS Electrical Test Tool – Device Test ensure the hub under test is selected (highlighted). Select SINGLE STEP SET FEATURE from the Device Command window.



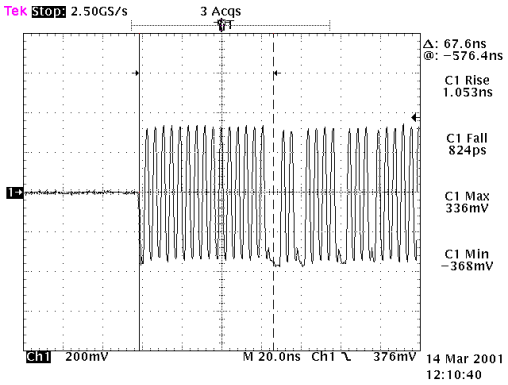
Single Step Set Feature on the Device Downstream of the Hub

11. Click EXECUTE once. The oscilloscope capture should appear as follows. Press STOP on the oscilloscope to pause it from further trigger. If the oscilloscope doesn't trigger on the device traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 8.



Host and Hub Packets

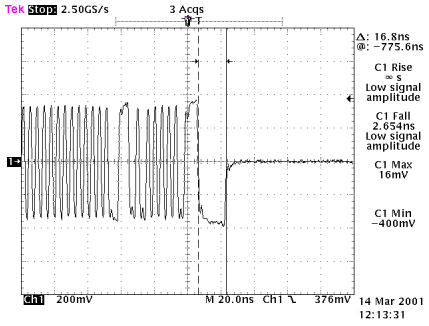
12. Use the Zoom function of the oscilloscope to expand the time division. Measure the sync field length (number of bits) of the third (from the hub) packet on the oscilloscope and verify that it is 32 bits per EL_21. Refer to the figure below for reference. Note that sync field starts from the high-speed idle transitions to a falling edge (due to the first zero). Count both rising and falling edges until the first two consecutive 1's and include the first 1. There should be 32 bits. Record the number in EL_21.



Sync Field Width – Upstream Packet

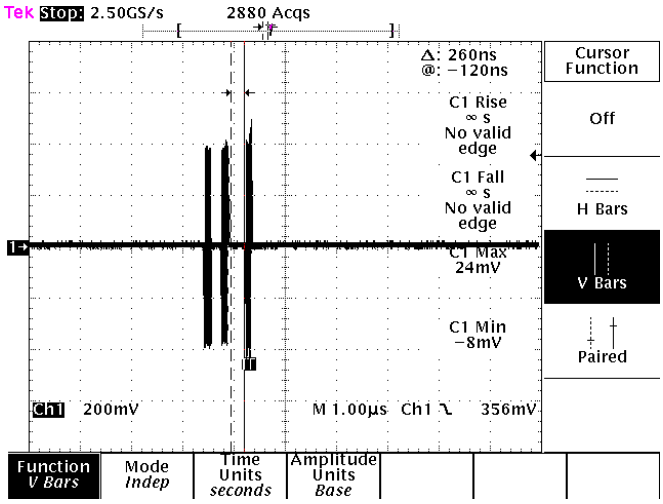
13. Measure the EOP length (number of bits) of the third packet on the oscilloscope and verify that it is 8 bits per EL_25. It is advisable to use the cursors to measure the EOP pulse width to determine the number of bits, based on 2.08nS / bit (480Mbps). Record the result in EL_25.

Note: EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The figure below illustrates the negative going pulse.



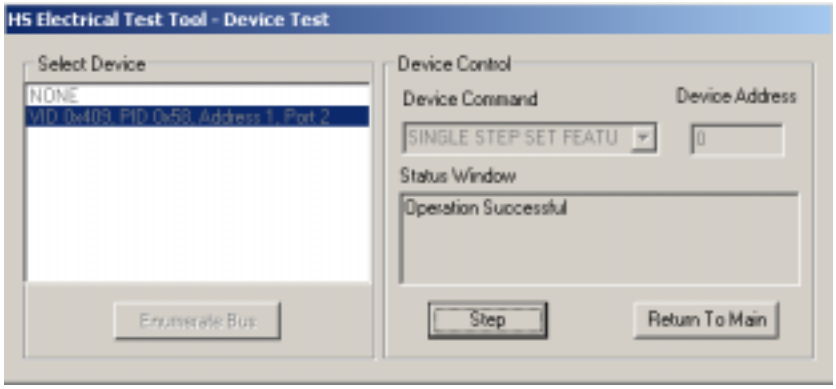
EOP Width – Upstream Packet

14. Measure the inter-packet gap between the second (from host) and the third (from the hub in respond to the host's) packets shown on the oscilloscope. The second is a host packet and the third (of higher amplitude) is the hub's response. Compute the number of bits by dividing the time measure by 2.08S. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22. One more sample of the inter-packet gap will be measured in the next few steps.



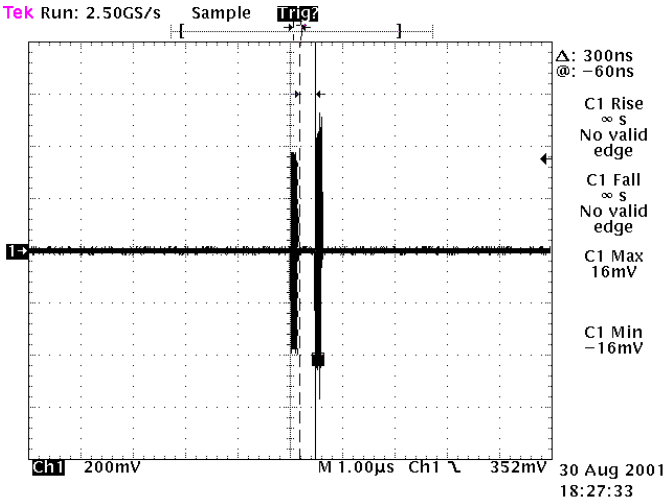
Inter-Packet Gap – Transmit after Receive

15. Ensure the oscilloscope is armed. In the HS Electrical Test Tool - Device Test menu, Click the Step button once. This is the second step of the two-step Single Step Set Feature command.



Step Button of the SINGLE STEP SET FEATURE

16. The captured oscilloscope acquisition should appear as follows. Press STOP on the oscilloscope to pause it from further trigger.



Hub Packet Following Host Packet

17. Measure the inter-packet gap between the first (from host) and the second (from the hub in respond to the host's) packets shown on the oscilloscope. The first (of lower amplitude) is from the host and the second (of higher amplitude) is a hub's response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.

18. Exit the HS Electrical Test Tool – Device Test menu by clicking the Return to Main button.

19. From the HS Electrical Test Tool main menu select Hub and click TEST to enter the Hub Test menu.

4.9 Hub Receiver Sensitivity – Upstream Facing Port (EL_16, EL_17, EL_18)

This section tests the sensitivity of the receivers on the upstream facing port of the hub under test. A Tektronix DG2040 Data Generator emulates the IN command from the hub port to device address 1.

1. Attach the 5V power supply to the Device Receiver test fixture (J8) and verify green power LED (D1) is lit. Leave the TEST switch at the Normal position. The yellow LED (D2) should be off.

2. Connect the Init port of the fixture to a port on the Test Bed Computer. Connect the Test Port of the fixture to the upstream facing port of the hub under test. Apply power to the hub. Click Enumerate Bus and verify that the hub enumerates properly.

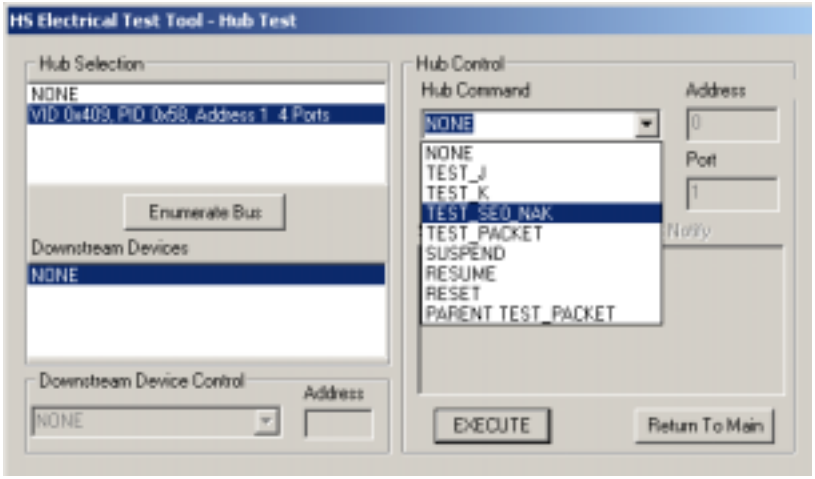
3. Connect the Tektronix DG2040 Data Generator to the Device Receiver Sensitivity test fixture using the SMA cables. Two sets of SMA cables are required, each with a 5x attenuators inserted. Connect CH 1 to SMA1, and CH 0 to SMA2.

4. Connect the Oscilloscope Channel 1 differential probe to J7 of the test fixture, with the + probe tip to D+ and – probe tip to D-. Recall the RCVRSENS.SET oscilloscope setup.

5. On the DG2040, select the Edit menu. Then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the MIN-ADD1.PDA setup file. Press OK to load it. This generates IN packets (of compliant amplitude) with a 12-bit SYNC field.

6. Start the data generator output with the START / STOP button.

7. On the HS Electrical Test Tool – Hub Test menu, select TEST_SE0_NAK from the Hub Command drop down menu. Click EXECUTE once to place the hub into TEST_SE0_NAK test mode.



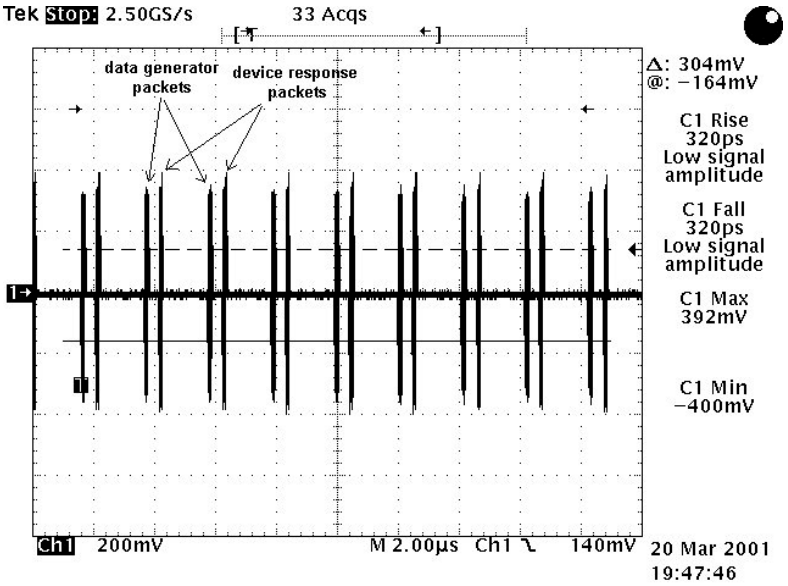
TEST_SE0_NAK – Hub Upstream Port

8. Place the test fixture Test Switch (S1) into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the SOF packets from the host controller.

9. Verify that all packets from the data generator are NAK'd by the port under test. Record the Pass / Fail in EL_18.

10. On the data generator select the Edit menu, then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the IN-ADD1.PDA setup file. Press OK to load it.

11. Verify that all packets are NAK'd while signaling from the data generator is about at the 400 mV nominal threshold. The oscilloscope should look like the following figure.



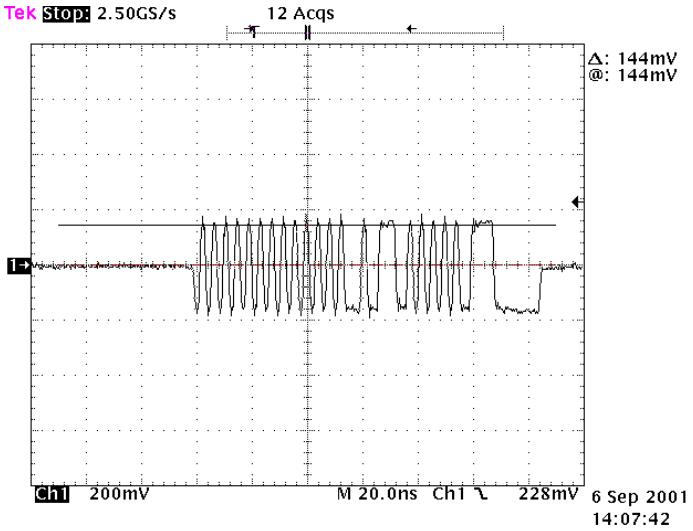
Receiver Respond with NAK to IN from Data Generator

12. Adjust the output level of each channel as follows:

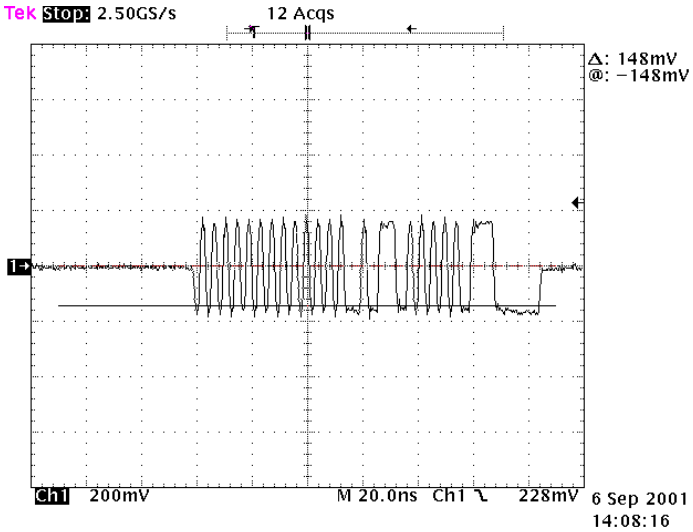
13. Select the Setup menu. Then press High from the Level Condition function. Adjustment of the output level is best done with the keypad in 50mV while monitoring the actual level on the oscilloscope. Use the up and down arrow buttons to select the channel to change

14. Reduce the amplitude of the data generator packets in 50mV steps while monitoring the NAK response from the hub on the oscilloscope. The adjustment should be made to both channels such that Ch0 and Ch1 are matched, as indicated on the data generator readout. Reduce the amplitude until the NAK packets begins to be intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.

15. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The measurement is best made by turning on the Fit To Screen function in the Horizontal menu of the oscilloscope to maintain sufficient sampling rate. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_17.

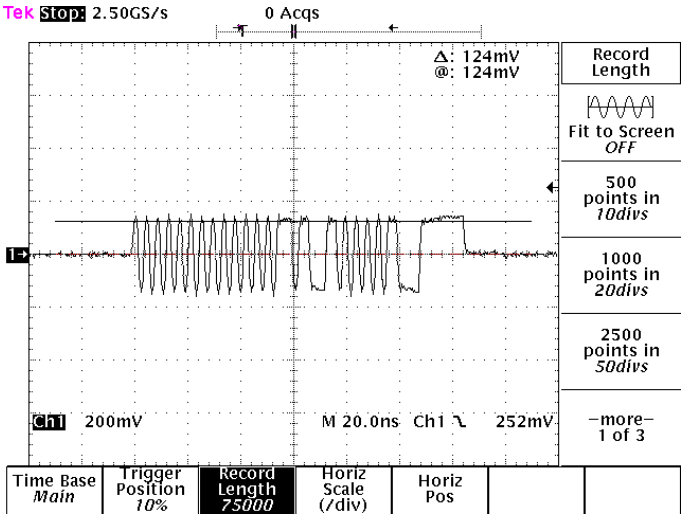


16. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_17. As long as the receiver continue to NAK the data generator packet above +/- 150mV, it is considers pass the test. Record PASS/FAIL in EL_17.

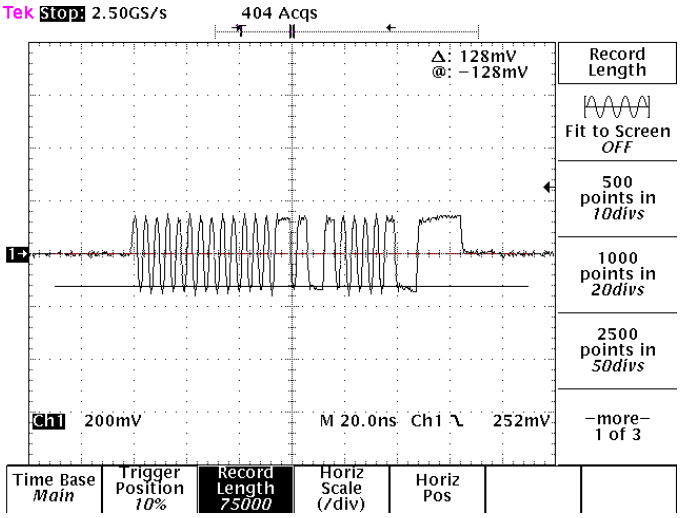


17. Turn Fit To Screen to off in order to be able to monitor 8 to 9 packet pairs. Now further reduce the amplitude of the packet from the data generator in small steps. Still maintaining balance between Ch0 and Ch1 until the receiver just cease to respond with NAK. This is the squelch level of the receiver.

18. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The measurement is best made by turning on the Fit To Screen function in the Horizontal menu of the oscilloscope to maintain sufficient sampling rate. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16.



19. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16. As long as the receiver continue to NAK the data generator packet below +/- 100mV, it is considers pass the test. Record PASS/FAIL in EL_16.



20. Cycle power on the hub to prepare for the subsequent test.

Note: With certain devices making an accurate zero-to-peak measurement of the In packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the In packet at the test fixture could be significantly higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

4.10 Hub Repeater Test – Downstream Facing Ports (EL_42, EL_43, EL_44, EL_45, EL_48)

This section requires two sets of differential probes, one for monitoring packets at the upstream facing port while the other one for monitoring packets at a downstream facing port. One

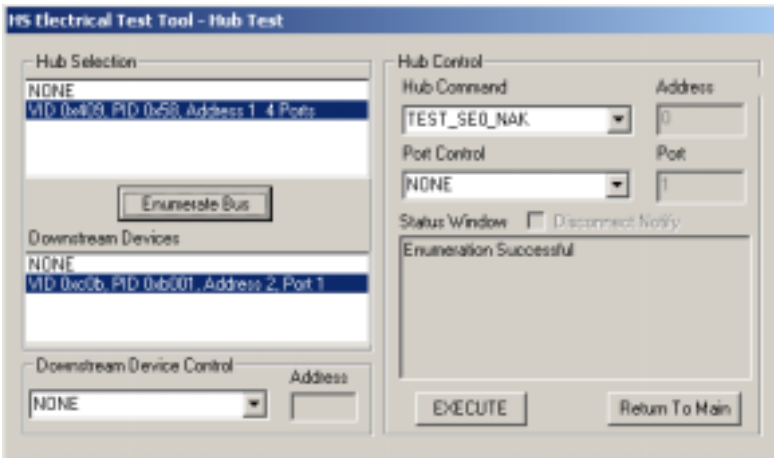
differential probe is needed at Channel 1 of the oscilloscope. A second differential probe is needed at Channel 4. A Host Signal Quality fixture and a Device Signal Quality fixture are needed.

Note: Although most hubs have multiple downstream ports, it is acceptable to only test one port for the economy of test time.

1. Connect the Device Signal Quality test fixture between the upstream facing port of the hub and the host controller port. Attach the Channel 1 diff probe to J7 of the fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

2. Connect the Host Signal Quality test fixture between the downstream port under test of the hub and a known-good high-speed device. Attach the Channel 4 diff probe to J7 of the fixture. Ensure the + polarity on the probe lines up with D+ on the fixture. Connect a known-good high-speed device to the Init port of this test fixture. Apply power to the hub and the known good device.

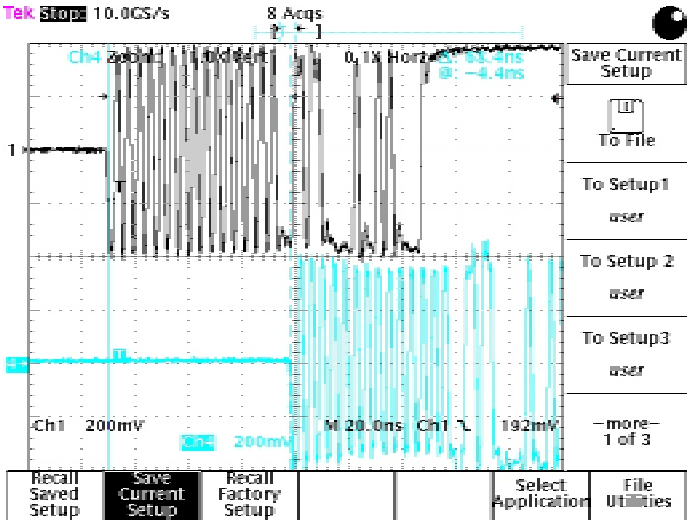
3. Click the Enumerate Bus button once. The hub under test should be enumerated with the hub's VID shown together with the USB address. Likewise the known good device should be enumerated with it's VID shown together with the hub port in which it is connected.



Hub and DS Device Enumerated

4. Recall the REPEATER.SET oscilloscope setup.

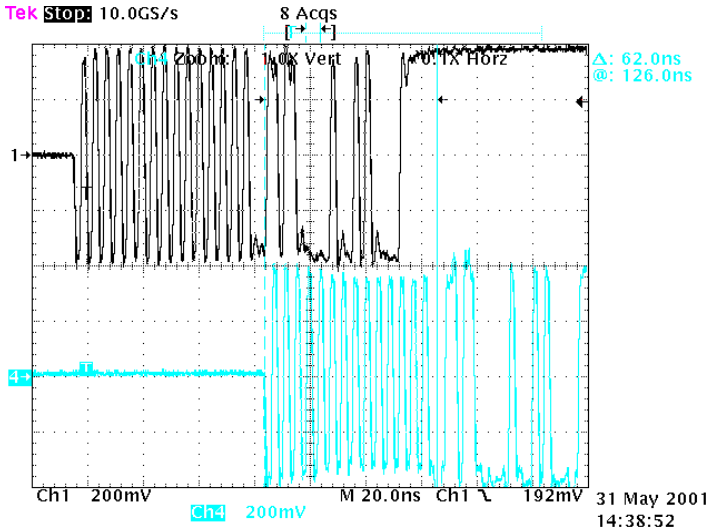
5. Using the oscilloscope, verify SOF (Start Of Frame) packets are being transmitted on the downstream facing port (on Channel 4). Capture a SOF packet and pause the acquisition with the RUN / STOP button. The captured oscilloscope acquisition should appear as follows.



Packet Delay – Downstream Facing Repeater

6. Measure the delay between the start of packet between the hub's upstream facing port (Channel 1) and the hub's down stream facing port under test (Channel 4) as in the cursor positions in the figure. This is the delay of the SOF packet through the hub. Verify this is no more than 79uS (36 bits plus 4nS). Record the result in EL_48.

7. Count the number of bits in the sync field on Channel 4. Each falling or rising edges counts as one bit (consecutive zeros in NRZI format), up to and include the first no transition (due to the first one that follows the consecutive zeros in NRZI format). Refer to the lower trace (Ch 4) in following figure for example. In this case, the downstream SOF (Ch 4) only has 30 bits in the sync field because it truncates 2 bits from the 32 bits total on the upstream SOF (Ch 1). Determine the number of sync bit truncated by the hub. Record the result into EL_42.



Sync Bits – Downstream Facing Repeater

8. Verify also that the sync field in Channel 4 is not corrupted, when compared to that in Channel 1 except the truncation of consecutive zeros (as determined in step 7). Record the result in EL_43.

9. Measure the time of the EOP width of the packet in Channel 1. Measure the time of the EOP width of the packet in Channel 4. Determine the number of bits of each by dividing the measurement by 2.08nS. Verify the number of bits in Channel 4 does not have 4 more bits (EOP dribble) than that in Channel 1 (which should be 40 bits). Record the result in EL_44.

10. Verify also that the EOP in Channel 4 is not corrupted. Record the result in EL_45.

4.11 Hub Repeater Test – Upstream Facing Port (EL_42, EL_43, EL_44, EL_45)

This section also requires two sets of differential probes, one for monitor packets at the upstream facing port while the other one for monitor packets at a downstream facing port. In order to be able to trigger on a packet from the device, the diff probe on Channel 4 now needs to be placed nearer to the device than the hub port. This is accomplished by using a fixture that allows probing near the device. Please note that the two test fixtures in this section are interchanged with respect to the connections in section 4.10.

1. Connect the Host Signal Quality test fixture between the upstream facing port of the hub and the host controller port. Attach the Channel 1 diff probe to J7 of the fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

2. Connect the Device Signal Quality test fixture between the downstream port under test of the hub and a known-good high-speed device. Attach the Channel 4 diff probe to J7 of the fixture. Ensure the + polarity on the probe lines up with D+ on the fixture. Connect a known-good high-speed device to the Test port of this test fixture. Apply power to the hub and the known good device.

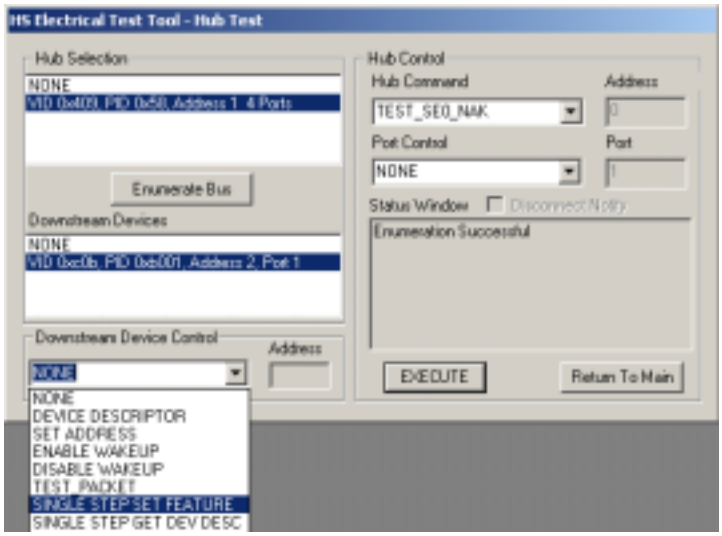
3. Click the Enumerate Bus button once. The hub under test should be enumerated with the hub's VID shown together with the USB address. Likewise the known good device should be enumerated with the it's VID shown together with the hub port in which it is connected.

4. Recall the HUBUP.SET oscilloscope setup.

5. Using the oscilloscope, verify SOFs (Start Of Frame) packets are being transmitted on the downstream facing port (on Channel 4). You may need to lower the trigger level to somewhat below 400mV.

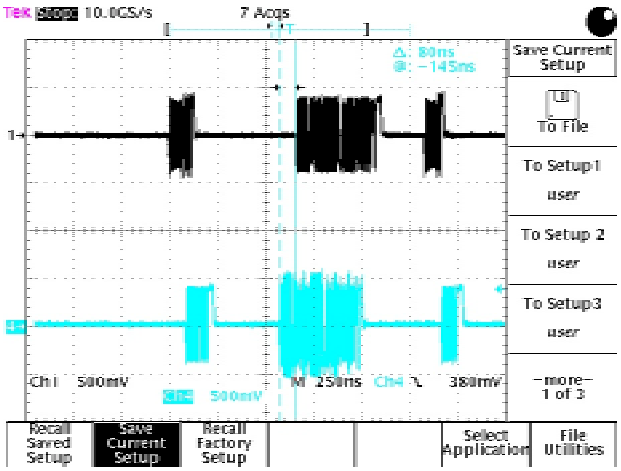
6. Now raise the oscilloscope trigger level slowly until it just stop being triggered on the SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the hub and the length of cable used on the fixture. Ensure the RUN / STOP of the oscilloscope is set to RUN.

7. In the HS Electrical Test Tool – Hub Test menu select SINGLE STEP SET FEATURE from the Downstream Device Control drop down menu and click EXECUTE once.



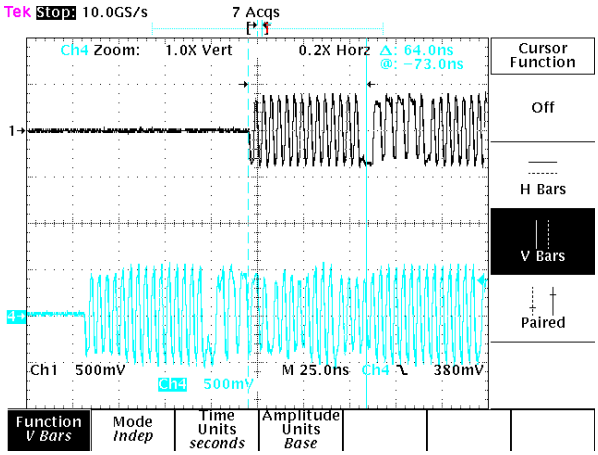
SINGLE STEP SET FEATURE – Downstream Device

8. The captured oscilloscope sample should appear as the figure below. If the oscilloscope doesn't trigger on the hub traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 5. Press STOP on the oscilloscope trigger.



Packet Repeated to Upstream – Top Trace

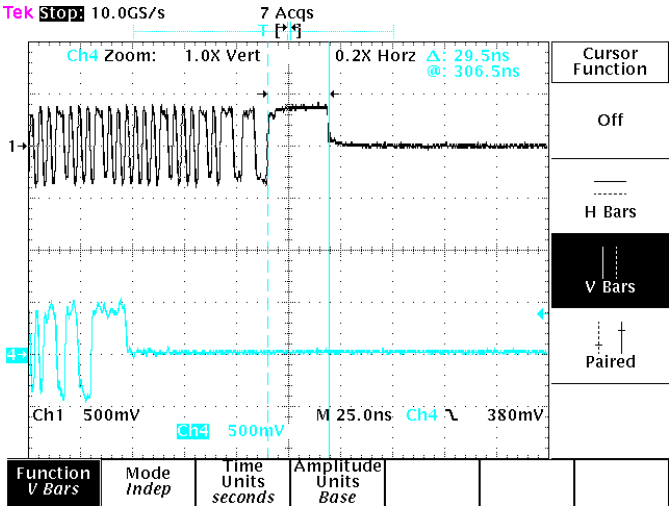
9. Count the number of bits in the sync field on the packet in Channel 1. Each falling or rising edges counts as one bit (consecutive zeros in NRZI format), up to and include the first no transition (due to the first one that follows the consecutive zeros in NRZI format). Refer to the top trace (Ch 1) in the following figure that has 30 bits in the sync field for example. Verify the truncation of the sync field is no more than 4 bits (the number of sync bits in channel 1 should not be more than 4 bit less than that in channel 4). Record the result in EL_42.



Sync Bit Truncation – No More than 4 Bits

10. Verify also that the sync field in Channel 1 is not corrupted, when compared to that in Channel 4 except the truncation of consecutive zeros (as determined in step 9). Record the result in EL_43.

11. Measure the time of the EOP width of the packet in Channel 1. Measure the time of the EOP width of the packet in Channel 4. Refer to the following figure for reference. Determine the number of bits of each by dividing the measurement by 2.08nS. Verify the number of bits in Channel 1 is no more than 4 bits than that in Channel 4 (which should be 8 bits). Record the result in EL_44.



EOP Width – No More Than 4 Added Bits

12. Verify also that the EOP in Channel 4 is not corrupted. Record the result in EL_45.

13. Disconnect both differential probes. Disconnect the connection on the hub's downstream facing port.

4.12 Hub CHIRP Timing – Upstream Facing Port (EL_28, EL_29, EL_31)

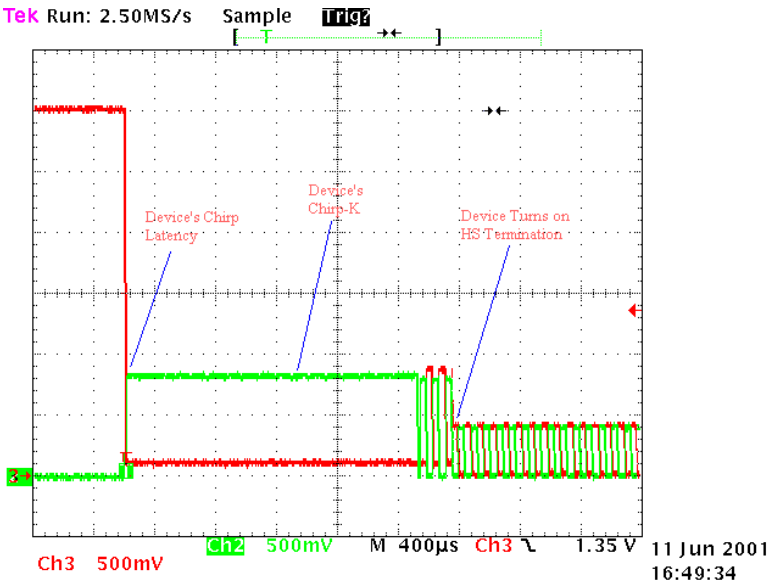
This test applies only to the upstream facing port of the hub under test.

1. Attach the Init port of the Device High-speed Signal Quality test fixture into a USB 2.0 compliant port of the HS host controller.

2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J7. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.

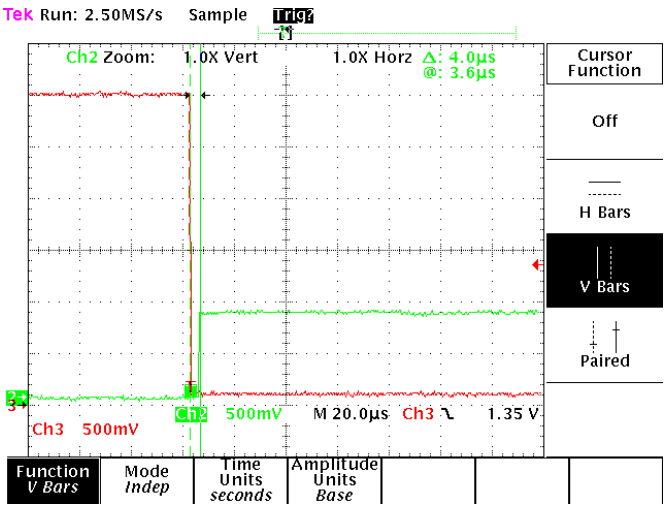
3. Recall the CHRP2&3.SET oscilloscope setup.

4. Attach the TEST port of the fixture to the upstream port of the hub. Apply power to the hub. Click Enumerate Bus and capture the CHIRP handshake as in the figure below.



Hub Chirp (Speed Detection)

5. Measure the hub's CHIRP-K latency ($T_{WTRSTFS}$) in respond to the reset from the upstream host port. Verify this timing is 2.5uS ≤ $T_{WTRSTFS}$ ≤ 3.0mS. Record the result in EL28.



Hub Chirp-K Latency

6. Measure the hub's CHIRP-K duration. Verify this assertion time is 1.0mS (T_{UCH}) ≤ CHIRP-K duration ≥ 7.0mS (T_{UCHEND}). Record the result in EL_29.

7. Following the host assertion of alternate sequence of Chirp-K and Chirp-J, the hub must respond by turning on its high-speed terminations. This is evident by a drop of amplitude of the alternate Chirp-K and Chirp-J sequence from the 800mV nominal to the 400mV nominal. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the hub turns on the high-speed terminations. Verify this is less than or equal to 500us. Record the measurement in EL_31.

8. In addition to turning on its high-speed terminations, the hub must also disconnect the D+ pull-up resistor in respond to the host's assertion of alternate sequence of Chirp-K and Chirp-J. The evidence is a slight drop of the D+ level during the Chirp-K from the host. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the D+ pull-up resistor is disconnected. Verify this is less than or equal to 500us. Record the measurement in EL_31.

4.13 Hub Suspend/Resume/Reset Timing – Upstream Facing Port (EL_27, EL_28, EL_38, EL_39, EL_40)

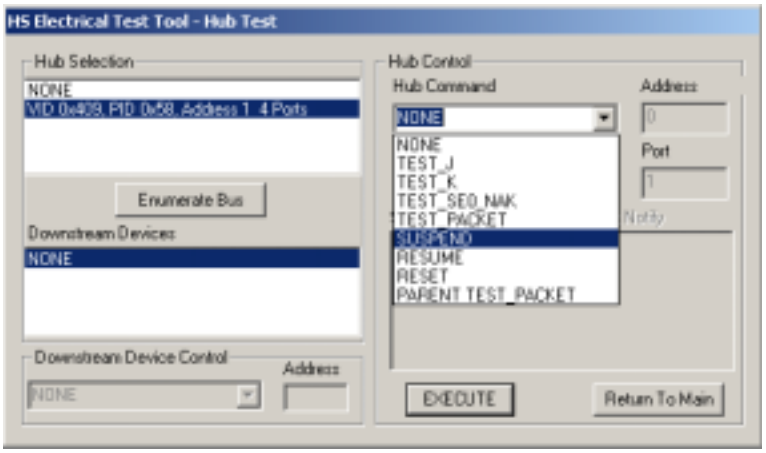
1. Plug the Init port of the Device High-speed Signal Quality test fixture into a high-speed capable port of the test bed computer.

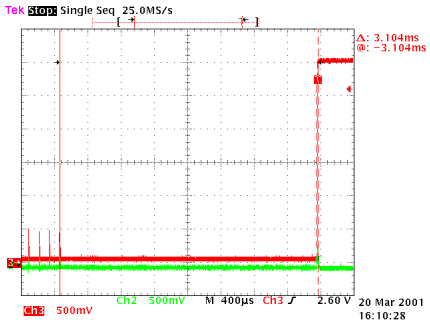
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J7. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.

3. Attach the TEST port of the fixture to the upstream port of the hub. Apply power to the hub. Click the Enumerate Bus button once. The hub under test should be enumerated with the hub's VID shown together with the USB address.

4. Recall SUSP2&3.SET oscilloscope setup.

5. On the HS Electrical Test Tool – Hub Test menu, select SUSPEND from the Hub Command drop down menu. Click EXECUTE once to place the hub into suspend. The captured suspend transition should appear as in the figure below.





Response to Suspend from Host - Upstream Facing Port

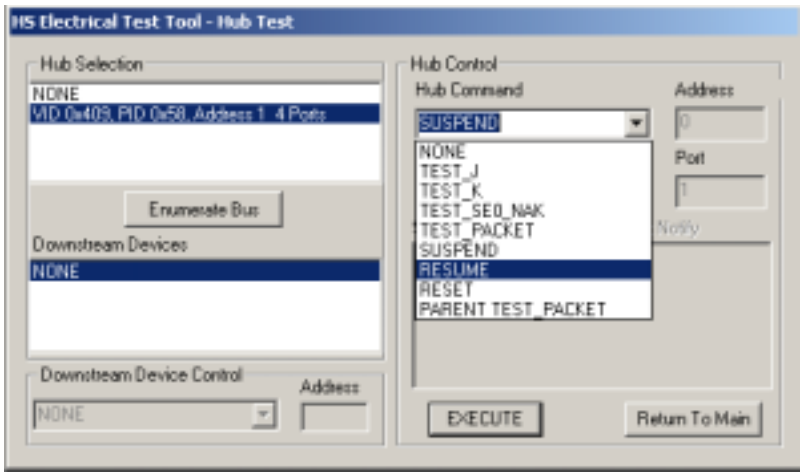
6. Measure the time interval from the end of last SOF packet issued by the hub to when the hub attached its full speed pull-up resistor on D+. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. Verify this time is between 3.000mS and 3.125mS (T_{TWTHS}). Record the result in EL_38.

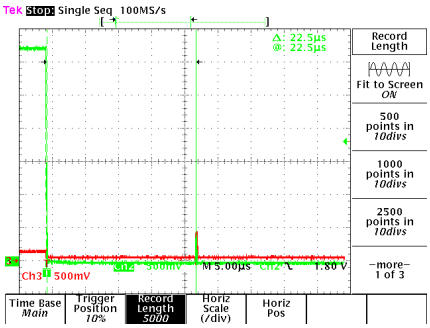
7. Ensure the oscilloscope is armed. Press Force Trigger to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V. Record the Pass / Fail result in EL_39.

The following steps verify the Resume response of the hub under test.

8. Recall RESUM2&3.SET oscilloscope setup. Ensure the oscilloscope is armed.

9. On the HS Electrical Test Tool – Hub Test menu, select RESUME from the Hub Command drop down menu. Click EXECUTE once to resume the hub from suspend. The captured resume transition should appear as in the figure below.





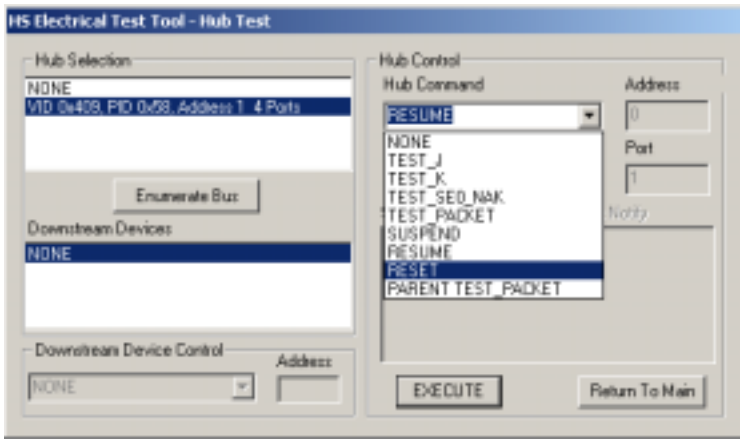
Hub Resumes to High-speed

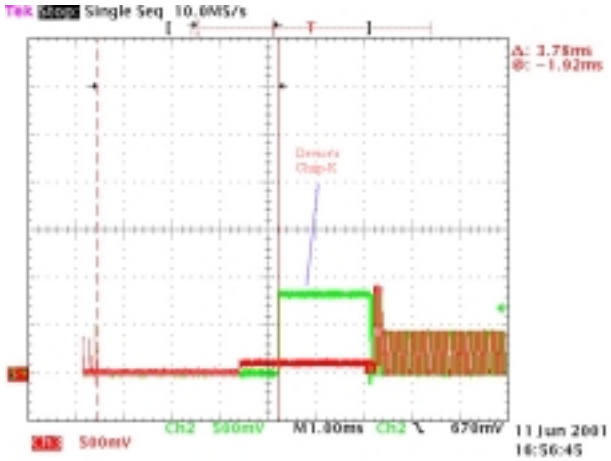
10. The hub should resume the high-speed operation, which is indicated by the presence of high-speed SOF packets (with 400mV nominal amplitudes) following the K State driven by the host controller. The presence of SOF at 400mV nominal amplitude indicates the hub resumes back to high-speed operation. Record the Pass / Fail result in EL_40.

The following steps verify the hub resumes back to high-speed operation after being reset from operating in high-speed.

11. Recall RSTFHS.SET oscilloscope setup.

12. On the HS Electrical Test Tool – Hub Test menu, select RESET from the Hub Command drop down menu. Click EXECUTE once to reset the hub operating in high-speed. The captured resume transition should appear as in the figure below.





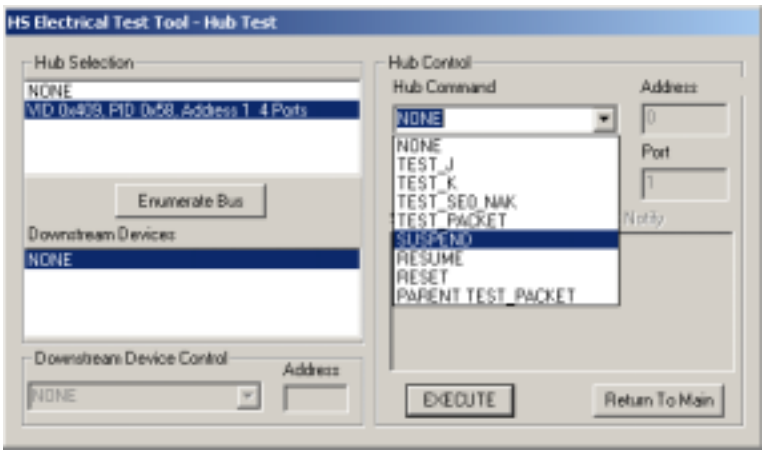
Hub's Chirp-K in Respond to Reset from High-speed

13. The device should transmit a chirp handshake following the reset. Measure the time between the beginning of the last SOF before the rest and the start of the device Chirp-K. Verify this is between 3.1mS and 6mS. Record the Pass / Fail result in EL_27.

The following steps verify the hub's chirp response after being reset from suspend.

14. Recall the RSTRSUSP.SET oscilloscope setup.

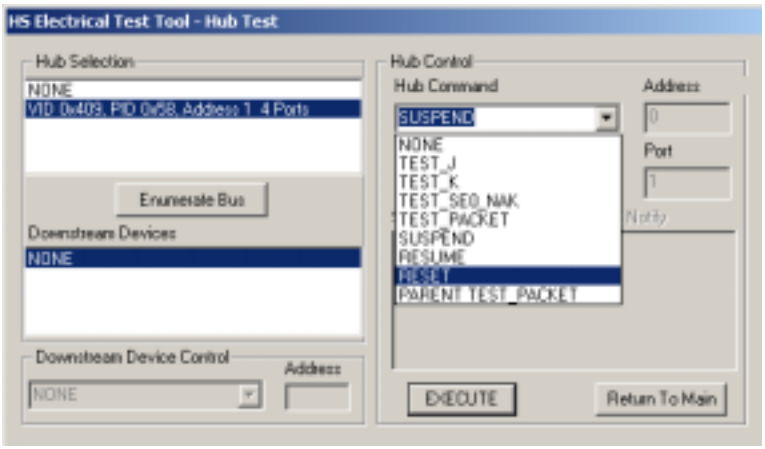
15. On the HS Electrical Test Tool – Hub Test menu, select SUSPEND from the Hub Command drop down menu. Click EXECUTE once to place the device into suspend.



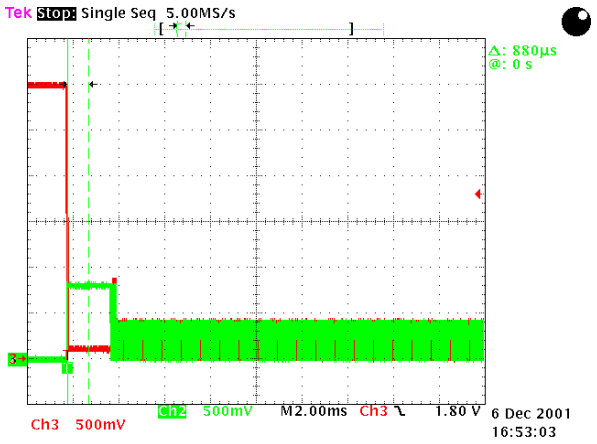
Hub Suspend

16. Ensure the oscilloscope is armed. Press Force Trigger to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V.

17. Ensure the oscilloscope is armed. On the HS Electrical Test Tool – Hub Test menu, select RESET from the Hub Command drop down menu. Click EXECUTE once to reset the device in suspend. The captured reset from suspend transition should appear as in the figure below.



Hub Reset From Suspend



Device Reset from Suspend

18. The hub responses to the reset with the Chirp-K. Measure the time between the falling edge of the D+ and the start of the device chirp-K. Verify this is between 2.5us and 3ms. Record the Pass / Fail result in EL_28.

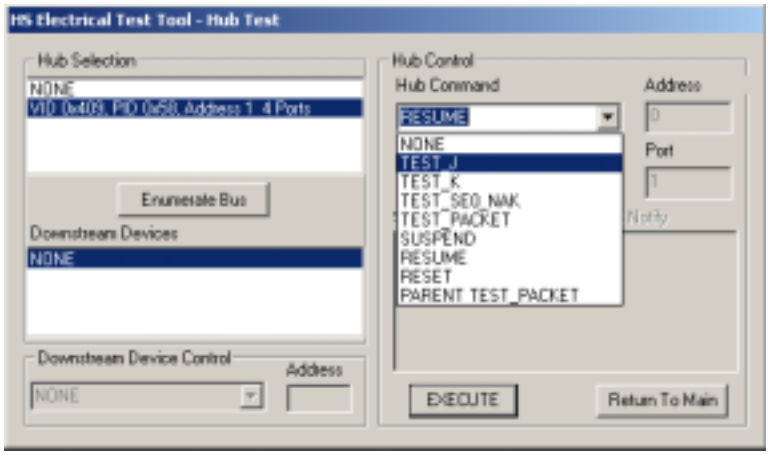
4.14 Hub Test J/K, SE0_NAK – Upstream Facing Port (EL_8, EL_9)

1. Attach the 5V power supply to J8 of the Device High-speed Signal Quality test fixture.

2. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is off.

3. Connect the Test port of the Device High-speed Signal Quality test fixture into the upstream facing port of the hub under test. Connect the Init port of the test fixture to a port of the Test Bed Computer. Apply power to the hub. Click Enumerate Bus button once. Verify that it is enumerated in the HS Electrical Test Tool – Hub Test menu.

4. On the HS Electrical Test Tool – Hub Test menu select TEST_J from the Hub Command drop down menu. Click EXECUTE once to place the hub into TEST_J test mode.



5. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.

6. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8. Return the Test switch to the NORMAL position.

7. Cycle the hub power. This restores the hub to normal operation.

8. On the HS Electrical Test Tool – Hub Test menu click Enumerate Bus, select TEST_K from the Hub Command drop down menu. Click EXECUTE once to place the hub into TEST_K test mode.

9. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.

10. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8. Return the Test switch to the NORMAL position.

11. Cycle the hub power. This restores the hub to normal operation.

12. On the HS Electrical Test Tool – Hub Test menu click Enumerate Bus once. Select TEST_SE0_NAK from the Hub Command drop down menu. Click EXECUTE once to place the hub into TEST_SE0_NAK test mode.

13. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.

14. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9. Return the Test switch to the NORMAL position.

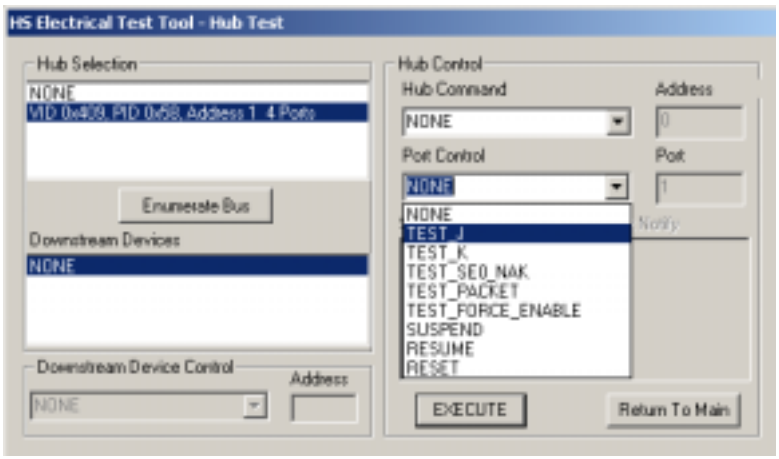
15. Cycle the hub power to prepare the hub for the subsequent tests.

4.15 Hub Test J/K, SE0_NAK – Downstream Facing Ports (EL_8, EL_9)

1. Attach the 5V power supply to Host Signal Quality test fixture (J8) and verify the green Power LED (D1) is lit. Place the TEST Switch (S1) in the Test position. Verify the yellow TEST LED is lit.

2. Attach the test fixture into the downstream facing port under test. Apply power to the hub.

3. On the HS Electrical Test Tool – Hub Test menu click Enumerate Bus once. Select TEST_J from the Port Control drop down menu. Enter the port number and click EXECUTE once to place the port under test into TEST_J test mode.



4. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.

5. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.

6. On the HS Electrical Test Tool – Hub Test menu click Enumerate Bus once. Select TEST_K from the Port Control drop down menu. Enter the port number and click EXECUTE once to place the port under test into TEST_K test mode.

7. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.

8. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.

9. On the HS Electrical Test Tool – Hub Test menu click Enumerate Bus once. Select TEST_SE0_NAK from the Port Control drop down menu. Enter the port number and click EXECUTE once to place the port under test into TEST_SE0_NAK test mode.

10. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.

11. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.

12. Repeat step 2 through 11 for the remaining ports.

Note: A specific port fails to enter the specific test mode after test mode commands have been issued to the hub a number of times. Cycle power on the hub will alleviate this problem.

Appendix A

A.4 Hub High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2 Vendor and Product Information

	Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.
Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Pass/Fail	Comments
LS SQ (Downstream)		
FS SQ (Upstream and Downstream)		
Inrush (Upstream)		
Drop / Droop (Downstream)		
Interop		

P = PASS

F = FAIL

N / A = Not applicable

A.4.4 Hub High-speed Signal Quality – Upstream Facing Port (EL_2, EL_46, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb / s ±0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.11.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_46 A hub upstream repeater must meet Template 1 transform waveform requirements measured at TP3.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.5 Hub High-speed Signal Quality – Downstream Facing Ports (EL_2, EL_3, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ±0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- ❑ Pass

- ❑ Fail
- ❑ N/A

Comments:

EL_3 A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measured at TP2 (each hub downstream port).

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5

PASS					
FAIL					
NA					

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.6 Hub Jitter – Downstream Facing Ports (EL_47)

EL_47 A hub downstream facing repeater must meet Template 1 transform waveform requirements measured at TP2 (each hub downstream port).

Reference documents: *USB 2.0 Specification*, Section 7.1.14.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.7 Hub Disconnect Detect (EL_36, EL37)

EL_37 A USB 2.0 downstream facing port must not detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is <= 525 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_36 A USB 2.0 downstream facing port must detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≥ 625 mV.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.8 Hub Packet Parameters – Upstream Facing Port (EL_21, EL_22, EL_25)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32 bit SYNC field.

Reference documents: *USB 2.0 Specification,* Section 8.2.

Data Packet SYNC field

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (Note, that a longer EOP is waiverable)

Reference documents: *USB 2.0 Specification,* Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.9 Hub Receiver Sensitivity – Upstream Facing Port (EL_16, EL_17, EL_18)

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

Note: A waiver may be granted if the receiver does not indicate Squelch at +/-50mV of 150mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification*, Section 7.1.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100 mV differential amplitude.

Note: A waiver may be granted if the receiver indicate Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification*, Section 7.1.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.10 Hub Repeater Test – Downstream Facing Ports (EL_42, EL_43, EL_44, EL_45, EL_48)

EL_48 A hub repeater may not delay packets for more than 36 bit times plus 4ns.

Reference documents: *USB 2.0 Specification*, Section 7.1.14.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_42 Hub repeaters must not truncate more than 4 bits from a repeated SYNC pattern.

Reference documents: *USB 2.0 Specification*, Section 7.1.10.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_43 Hubs must not corrupt any repeated bits of the SYNC field.

Reference documents: *USB 2.0 Specification*, Section 7.1.10.

- ❑ Pass
- ❑ Fail

- ❑ N/A

Comments:

EL_44 A hub may add at most 4 random bits to the end of the EOP field when repeating a packet.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_45 A hub must not corrupt any of the valid EOP bits when repeating a packet.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.11 Hub Repeater Test – Upstream Facing Port (EL_42, EL_43, EL_44, EL_45)

EL_42 Hub repeaters must not truncate more than 4 bits from a repeated SYNC pattern.

Reference documents: *USB 2.0 Specification*, Section 7.1.10.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_43 Hubs must not corrupt any repeated bits of the SYNC field.

Reference documents: *USB 2.0 Specification*, Section 7.1.10.

- ❑ Pass

- ❑ Fail
- ❑ N/A

Comments:

EL_44 A hub may add at most 4 random bits to the end of the EOP field when repeating a packet.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_45 A hub must not corrupt any of the valid EOP bits when repeating a packet.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.12 Hub CHIRP Timing – Upstream Facing Port (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.13 Hub Suspend/Resume/Reset Timing – Upstream Facing Port (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period on the bus.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

Note: It is not feasible to measure the hub transition back to high-speed operation within two bit time from the end of the resume signaling. The presence of SOF at nominal 400mV amplitude following the resume signaling is sufficient for this test.

Reference documents: USB 2.0 Specification, Section 7.1.7.7.

- ❑ Pass
- ❑ Fail
- ❑ N/A

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last uSOF transmitted before the reset begins.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

comments:

A.4.14 Hub Test J/K, SE0_NAK - Upstream Facing Port (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Test	D+ Voltage (mV)	D- Voltage (mV)
J		
K		

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be 0V ±10 mV when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

	Voltage (mV)
D+	
D-	

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.15 Hub Test J/K, SE0_NAK – Downstream Facing Ports (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Port	1		2		3		4		5	
Test	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
TEST_J										
TEST_K										

- ❑ Pass

- ❑ Fail
- ❑ N/A

Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be 0V ±10 mV when terminated with precision 45 Ω resistors **to ground.**

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Port	1		2		3		4		5	
Signal	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
Measure WRT Ground (mV)										

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments: