

Universal Serial Bus
Implementers Forum
Host High-speed
Electrical Test Procedure for
Tektronix TDS7254,
TDS/CSA7404, TDS6604 and
TDS6404

Revision 1.2

April 1, 2003

Revision History

Rev	Date	Filename	Comments
0.8	26-Jun-2001	Host HS Test.DOC	Initial draft revision
0.81	12-Jul-01	Host HS Test.DOC	Changed el_17 on page 36 to reference Section 7.1.6.2.
0.9 (Beta)	Aug-31-2001	Host HS Test.DOC	Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification
1.0	Dec-23-2001	Host HS Test.DOC	Edit for final release. Delete TDR section.
1.1	Sept-9-2002	HS System Test.DOC	Added Legacy free test instructions
1.2	April-1-2003	Host HS Test Tektronix.DOC	Update procedure for Tektronix TDS7040, TDS7254, CSA7404 and TDS6604 for use with TDSUSB Compliance test software

Please send comments via electronic mail to techsup@usb.org

USB-IF High-speed Electrical Test Procedure
© Copyright 2001-2002, USB Implementers Forum, Inc.
All rights reserved.

DISCLAIMER OF WARRANTIES

THIS SPECIFICATION IS PROVIDED "AS IS" AND WITH NO WARRANTIES OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, NO WARRANTY OF NONINFRINGEMENT, NO WARRANTY OF MERCHANTABILITY, NO WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, NO WARRANTY OF TITLE, AND NO WARRANTY ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE, ALL OF WHICH WARRANTIES ARE EXPRESSLY DISCLAIMED.

WITHOUT LIMITING THE GENERALITY OF THE FOREGOING, USB-IF AND THE AUTHORS OF THE SPECIFICATION DO NOT WARRANT OR REPRESENT THAT USE OF THE SPECIFICATION WILL NOT INFRINGE THE INTELLECTUAL PROPERTY RIGHTS OF OTHERS. USERS OF THE SPECIFICATION ASSUME ALL RISK OF SUCH INFRINGEMENT, AND AGREE THAT THEY WILL MAKE NO CLAIM AGAINST USB-IF OR THE AUTHORS IN THE EVENT OF CLAIMS OF INFRINGEMENT.

USB-IF IS NOT LIABLE FOR ANY CONSEQUENTIAL, SPECIAL OR OTHER DAMAGES ARISING OUT OF THE USE OF THE SPECIFICATION.

LICENSE FOR INTERNAL USE ONLY

USB-IF HEREBY GRANTS A LICENSE TO REPRODUCE AND TO DISTRIBUTE THIS SPECIFICATION FOR INTERNAL USE ONLY. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, IS GRANTED HERewith, AND NO LICENSE OF INTELLECTUAL PROPERTY RIGHTS IS GRANTED HERewith.

All product names are trademarks, registered trademarks, or servicemarks of their respective owners.

Table of Contents

1	Introduction	5
2	Purpose.....	5
3	Equipment Required	5
3.1	Equipment Setup.....	6
3.1.1	Test Equipment Setup Diskettes.....	6
3.1.2	TDS7000/6000 Digital Sampling Oscilloscope	7
3.2	Operating Systems, Software, Drivers, and Setup Files.....	7
3.2.1	Operation Systems.....	7
3.3	Special Purpose Software.....	7
3.3.1	Test Equipment Setup Files	8
4	Test Procedure	8
4.1	Test Record.....	8
4.2	Vendor and Product Information	8
4.3	Legacy USB Compliance Tests	9
4.4	Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7).....	9
4.5	Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55).....	14
4.6	Host Disconnect Detect (EL_36, EL_37)	21
4.7	Host CHIRP Timing (EL_33, EL_34, EL_35).....	23
4.8	Host Suspend/Resume timing (EL_39, EL_41)	25
4.9	Host Test J/K, SE0_NAK (EL_8, EL_9).....	28
A.4	Host High-speed Electrical Test Data	31
A.4.2	Vendor and Product Information	31
A.4.3	Legacy USB Compliance Tests	32
A.4.4	Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7).....	32
A.4.5	Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55).....	34
A.4.6	Host Disconnect Detect (EL_36, EL_37)	35
A.4.7	Host CHIRP Timing (EL_33, EL_34, EL_35).....	36
A.4.8	Host Suspend/Resume timing (EL_39, EL_41)	37
A.4.9	Host Test J/K, SE0_NAK (EL_8, EL_9).....	37

1 Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

This test procedure is an update of the USB-IF Host Electrical High-speed Test Procedure written for the Tektronix TDS694C and the USB-IF MatLab scripts. This updated procedure is written to support Tektronix TDS7404, TDS7254, TDS6604 and TDS6404 running TDSUSB2 Compliance Test Application Software. TDSUSB2 software is used in place of the MatLab scripts and NI GPIB DAQ software.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Host USB-IF High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Hub USB-IF High-speed Electrical Test Procedure and Device USB-IF High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Equipment Required

The commercial test equipment listed here are base on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

Digital Sampling Oscilloscope:

- Tektronix TDS7404 or TDS7254 Digital Phosphor Oscilloscope (DPO)

This procedure also supports Tektronix TDS7254, CSA7404 and TDS6604/TDS6404 oscilloscope models.

- Tektronix P6247 or P6248 or equivalent differential probe, qty = 1
- Tektronix P6245 FET probes, qty = 2
- Tektronix TCA to BNC adapters, qty = 3
- TDS7000 Deskew Fixture, part number: 067-0405-xx, shipped as a standard accessory to the oscilloscope.
- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent
 - Mini-clip DMM lead – one each of black and red color
- High-speed USB Electrical Test Fixtures
 - Tektronix TDSUSBF signal quality test fixture, qty = 1
 - Disconnect test fixture, qty = 1 (source: USB-IF)
 - *5V test fixture power supply, qty = 1
 - *Female Serial B to female Serial A adaptor, qty = 1

* included with Tektronix TDSUSBF test fixture
- Known good HS device – any HS capable device that is on the USBIF integrators list.
- Miscellaneous Cables
 - 1M USB cable, qty = 1
 - 1.5M USB cable, qty = 1
 - Modular AC power cord, qty = 2
- High-speed Signal Quality Analysis Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. The OS on this computer is Windows 2000 or XP Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

Note: The Tektronix USB compliance test software operates internally to the oscilloscope and automatically configures the oscilloscope settings and so external GPIB control of the oscilloscope is not required. One can consolidate the High-speed Signal Quality Analysis Computer and the High-speed USB Test Bed Computer into one single PC.

3.1 Equipment Setup

3.1.1 Test Equipment Setup Diskettes

Some tests described in this procedure are not automated by the Tektronix TDSUSB2 Compliance Test Software application. For those tests, the application includes setup files for the test equipment used in this procedure. The setup files simplify equipment setup. Copy the HS Scope Setup files to floppy disks. Insert the Tek TDS7000/6000 setup floppy diskette into the Tektronix TDS7254/7404 or 6000 oscilloscopes.

3.1.2 TDS7000/6000 Digital Sampling Oscilloscope

Before turning on the oscilloscope. Attach a P6247 or P6248 differential probe to Channel-1. Attach two P6245 FET probes, one to Channel-2 and one to Channel-3. The probe assignment will be used through out the entire test procedure. Turn on the oscilloscope to allow for 20 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the TDS7000/6000 (in the Utility menu) if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

A higher resolution view of the USB signaling is possible by turning on the scope's Hi Resolution mode. On the scope's menu bar, select Horiz/acq > Horizontal/ Acquisition Setup > Acquisition > Hi Res.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes will be cancelled later as a part of the test procedure process. The offset of the differential probe will be adjusted by the step identified in the test procedure.

For P6247/P6248 differential probes, the following setting will be used through out the entire test procedure:

- DC Reject <OFF> (P6247 only)
- BW <Full> (P6247 only)
- Attenuation < $\div 1$ >

The use of a Tip Saver accessory on the P6247 or P6248 probe is highly recommended to prolong probe tip life. Please note that the Tip Saver will wear out after repeated use and start degrading signal quality measurements. Replace the Tip Saver when measurements made without it provide better results.

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operation Systems

Microsoft Windows 2000 or XP Professional is required on the High-speed Electrical Test Bed Computer. Microsoft Windows 2000 or XP Professional is required on the High-speed Signal Quality Analysis Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.
- Proprietary EHCI Driver Stack - The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation purposes, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.
- Tektronix TDSUSB2 Compliance Test Application software

3.3.1 Test Equipment Setup Files

These are 3 ½ inch floppy diskettes that contain the setup files for the test equipment. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these setup disks.

HS Scope Setup Disk – Contain setup files for Tektronix TDS7000/6000 DSO (Digital Storage Oscilloscope).

4 Test Procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date
2. Vendor name

3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the host controller under test must also pass the following compliance tests applicable to the EHCI Host Controller:

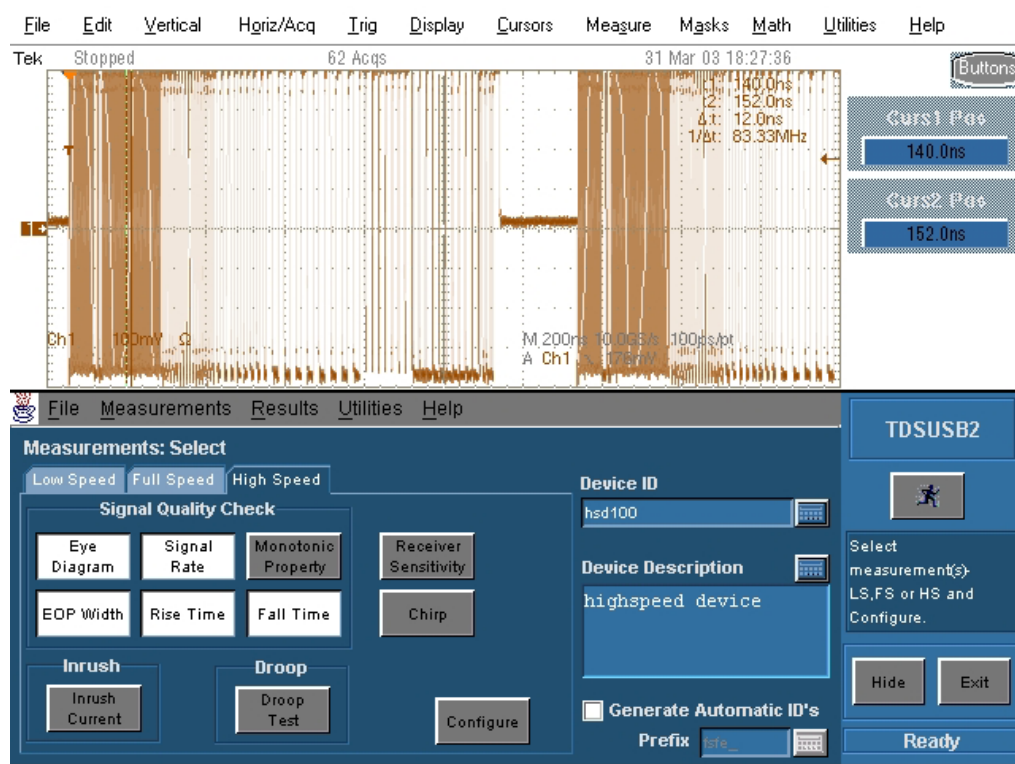
- Low speed signal quality
- Full speed signal quality
- Drop/Droop
- Interoperability

Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.

4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

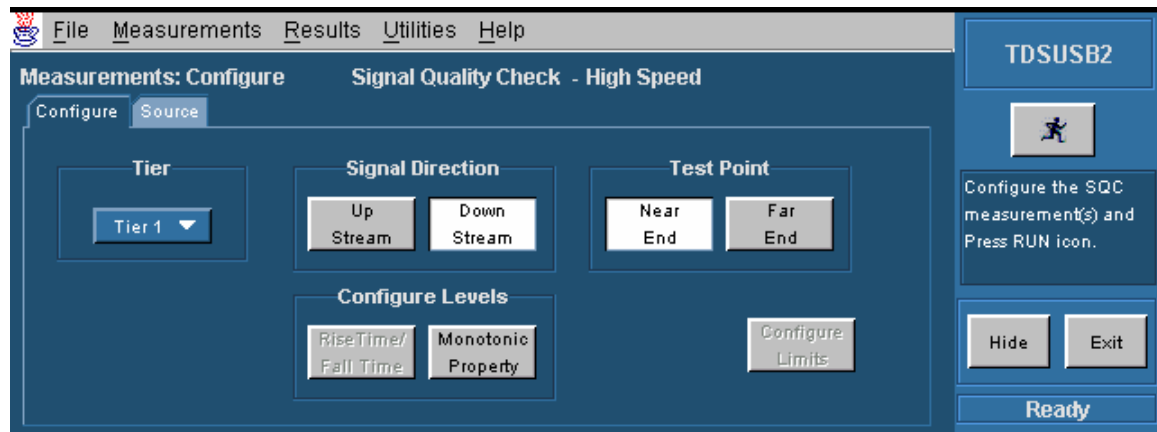
1. Attach the differential probe to J17 of the TDSUSBF test fixture, Host SQ segment. Ensure + on probe lines up with D+ on fixture. Turn on the oscilloscope if not have already done so. Allow about 20 minutes for warm up. Connect the short USB cable from the Host SQ fixture segment to the host port under test.
2. Launch the TDSUSB software application on the TDS7404 or TDS7254 oscilloscope by selecting with a mouse or touch screen, File: Run application: USB2.0 compliance test package.
3. Press default setup button on the oscilloscope front panel.
4. In the applications menu bar select, file: recall default.
5. Within the Measurement select menu of the USB2.0 compliance test application, select the High Speed tab.
6. Within the Signal Quality area of the application, select the High Speed Signal Quality tests: Eye Diagram, Signal Rate, Rise time, Fall Time, and EOP Width.


- The Monotonic property test is available but not required as it may generate false failures due to slight variations in the signal edge due to high frequency noise and/or scope quantization error.

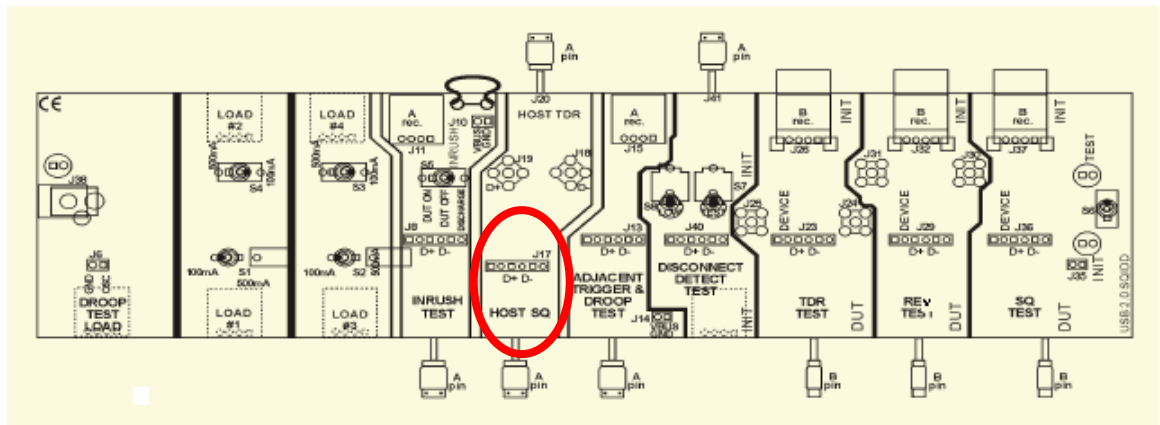
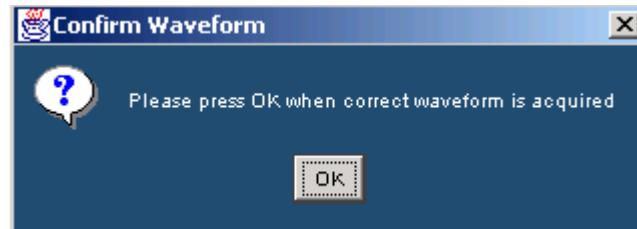


Tektronix TDSUSB Software

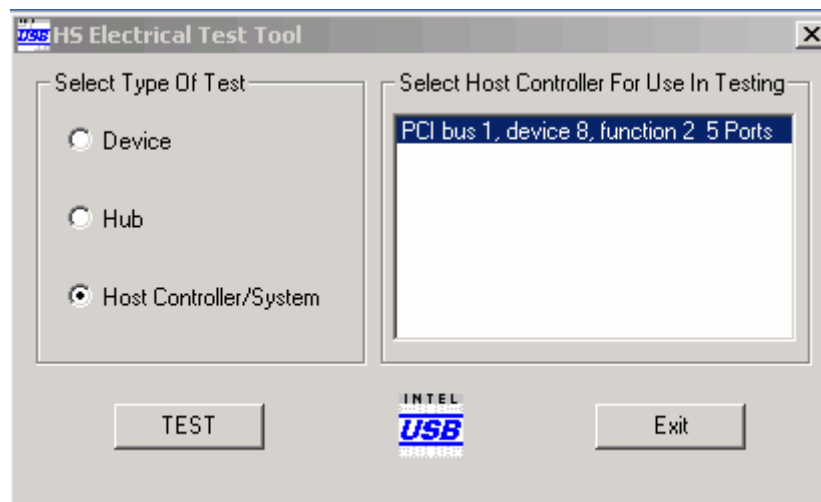
- Enter a device ID (e.g. TIDxxxxxx USNE.tsv) into the device ID dialog box and a device description into the device description dialog box.
- Press "Configure" Button to configure TDSUSB according to the system under test.



9. Press the  icon. Verify that the scope display is NOT reporting “clipping”. If it is, adjust the vertical amplitude until the “clipping” message does not appear. Do not press OK on the screen until the correct waveform is displayed.
10. Press OK when the correct waveform is acquired. Press OK when done.

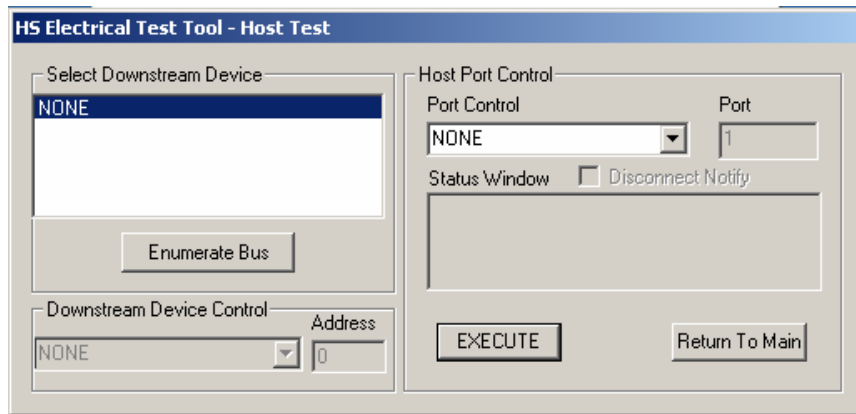


11. Invoke the High-speed Electrical Test Tool software on the high-speed computer under test. The main menu appears and shows the USB2.0 host controller.

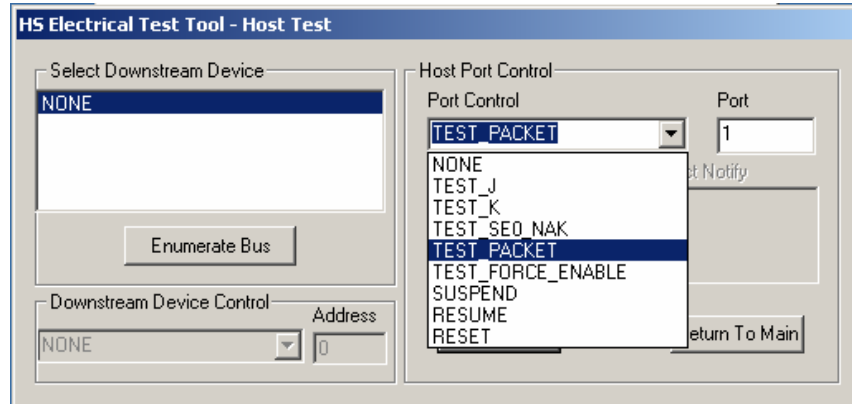


Main Menu

12. Select Host Controller/System and click the TEST button to enter the Host Test menu.

Host Test Menu

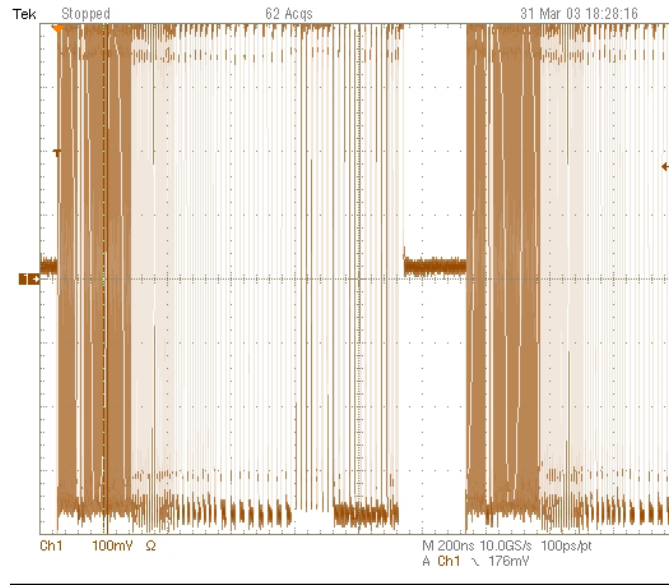
13. Connect the Test port of the Host High-speed Signal Quality test fixture into the port under test of the Host controller.
14. Select TEST_PACKET from the Port Control drop down menu. Enter the port number of the port being tested and click Execute. This forces the port under test to continuously transmit test packets

TEST_PACKET

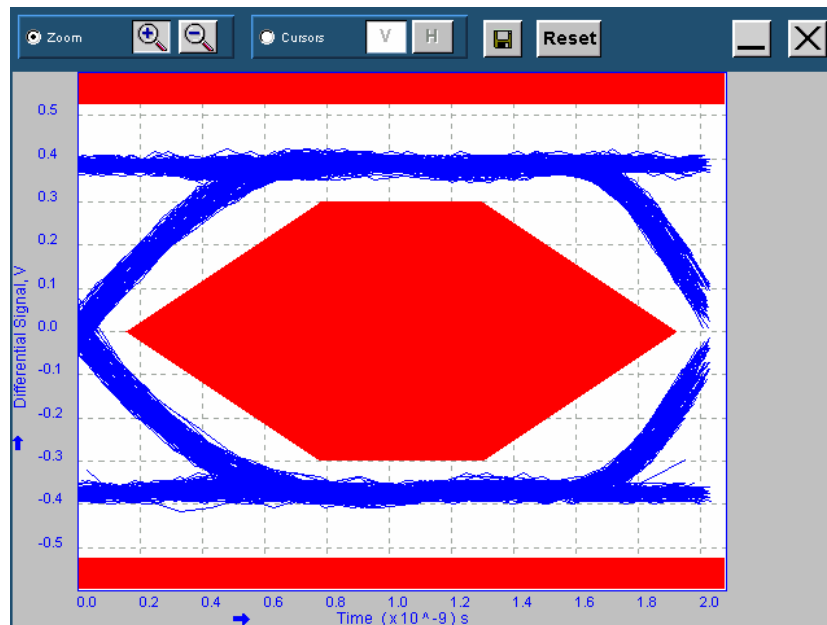
15. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change to the trigger hold-off.
16. Once the test packet is displayed properly, press OK in the application dialog box.
17. The Tektronix USB application generally triggers and displays the correct test packet without the need to place cursors. Should cursors be required they may be enabled by selecting within the application, File: Preferences: Advanced and clicking the optional Packet Identification by user using Cursors.

18. If cursors measurement is enabled on the oscilloscope place the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure for reference. Press OK on the USB2 application dialog box to begin acquisition and analysis of the test packet.

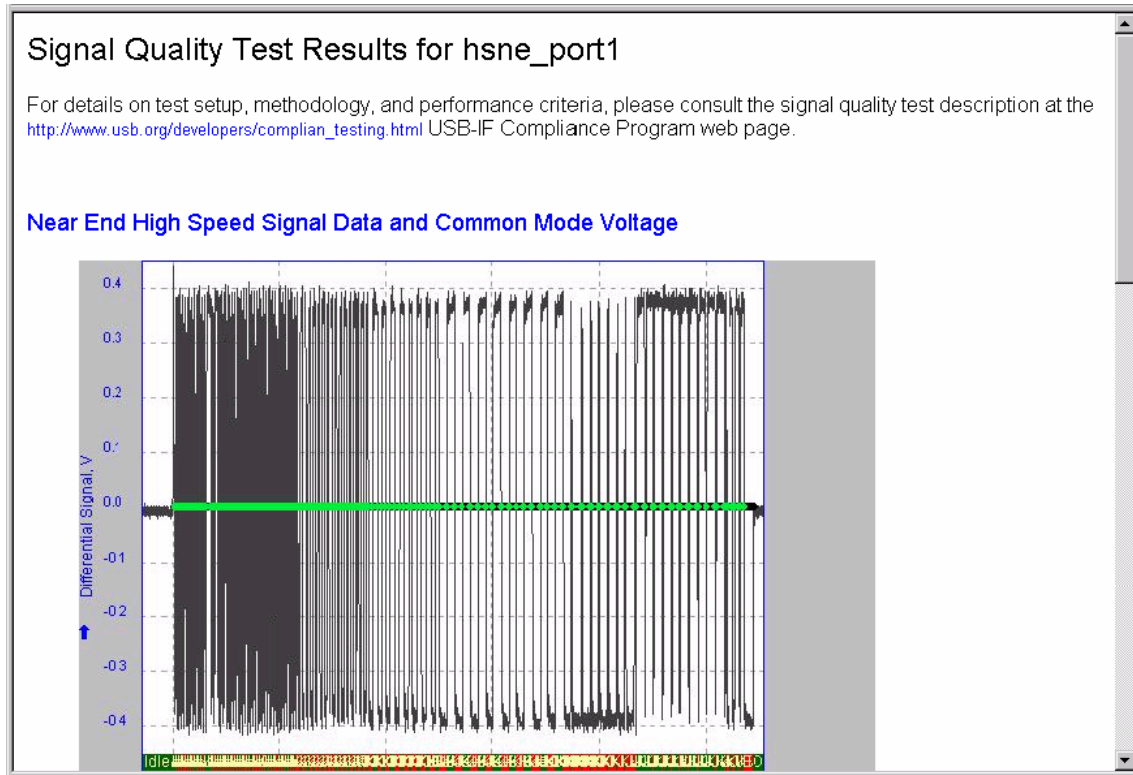
High-speed Test Packet



19. Verify the Signal Eye, EOP Width, and Signaling Rate all pass.



HTML Report for High Speed Signal Quality Test



20. Record the test result in EL_2, EL_3, EL_6, and EL_7.

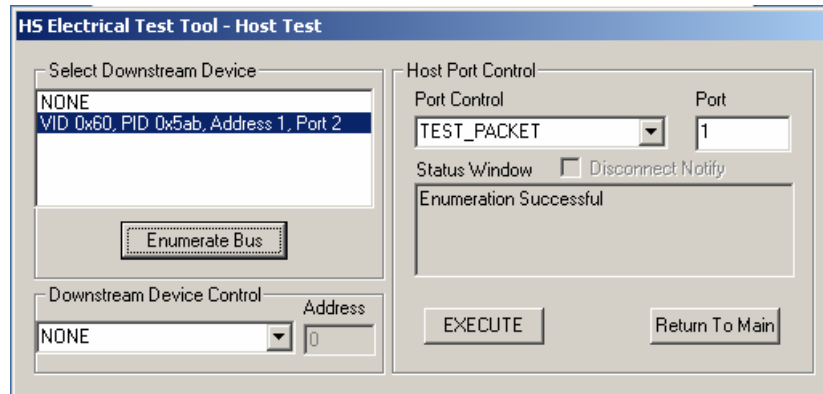
21. Remove the TDSUSB test fixture from the port.

22. Repeat steps 9 through 19 for all remaining ports.

Save all files created during the tests. Remove the Host Signal Quality test fixture from the port under test.

4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

1. Connect the TDSUSB Device Signal Quality test segment's short dongle (DUT Port) into B receptacle of a known good high-speed device. Apply power to the known good device. Using a 1M USB cable, connect the INIT side of the fixture to the Port Under Test.

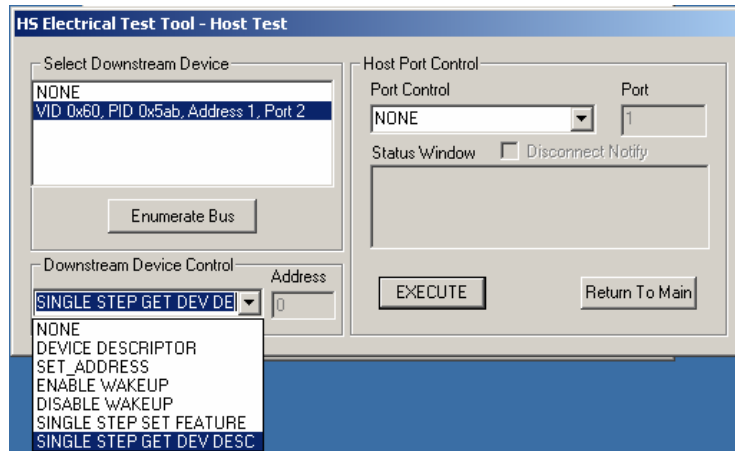


Known-Good Device Enumerated

Note: The use of the TDSUSBF Device High-speed Signal Quality test fixture segment makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

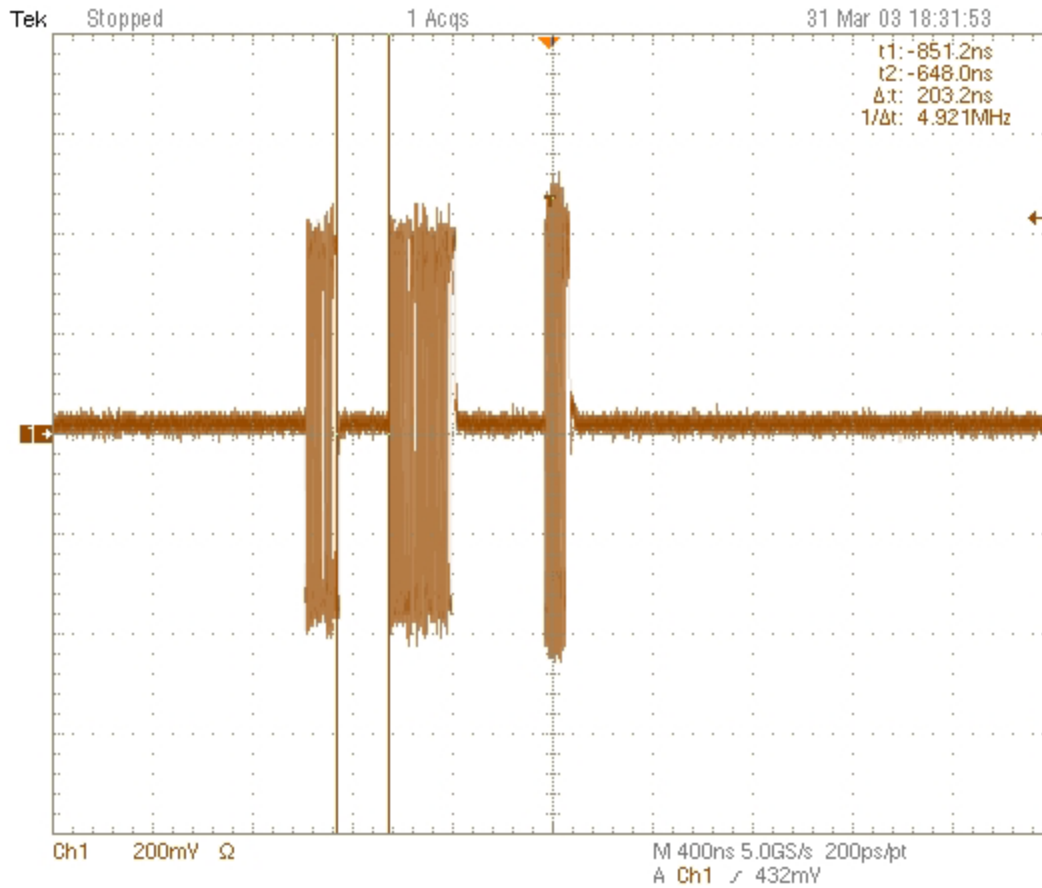
2. Attach the differential probe to J36 on the fixture near the device connector. Ensure + on probe lines up with D+ on fixture.
3. Recall the PACKPARAM.SET oscilloscope setup.
4. Verify that the Test Init switch is in the Init position. Connect the TDSUSBF Device Signal Quality test fixture segment (Init Port) into host controller port under test with a short USB cable. Click Enumerate Bus and verify that the device enumerates properly.
5. Using the oscilloscope, verify SOFs (Start Of Frame packets) are being transmitted on port under test. You may need to lower the trigger level to somewhat below 400mV to obtain a trigger.
6. Now raise the oscilloscope trigger level slowly until it doesn't trigger on SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the device used and length of cable used on the fixture. Ensure the RUN/STOP of the oscilloscope is set to RUN.

In the Host Test menu of the High-speed Electrical Test Tool software, ensure the device under test is selected (highlighted). Select SINGLE STEP GET DEV DESC from the Downstream Device Control menu and click Execute once.



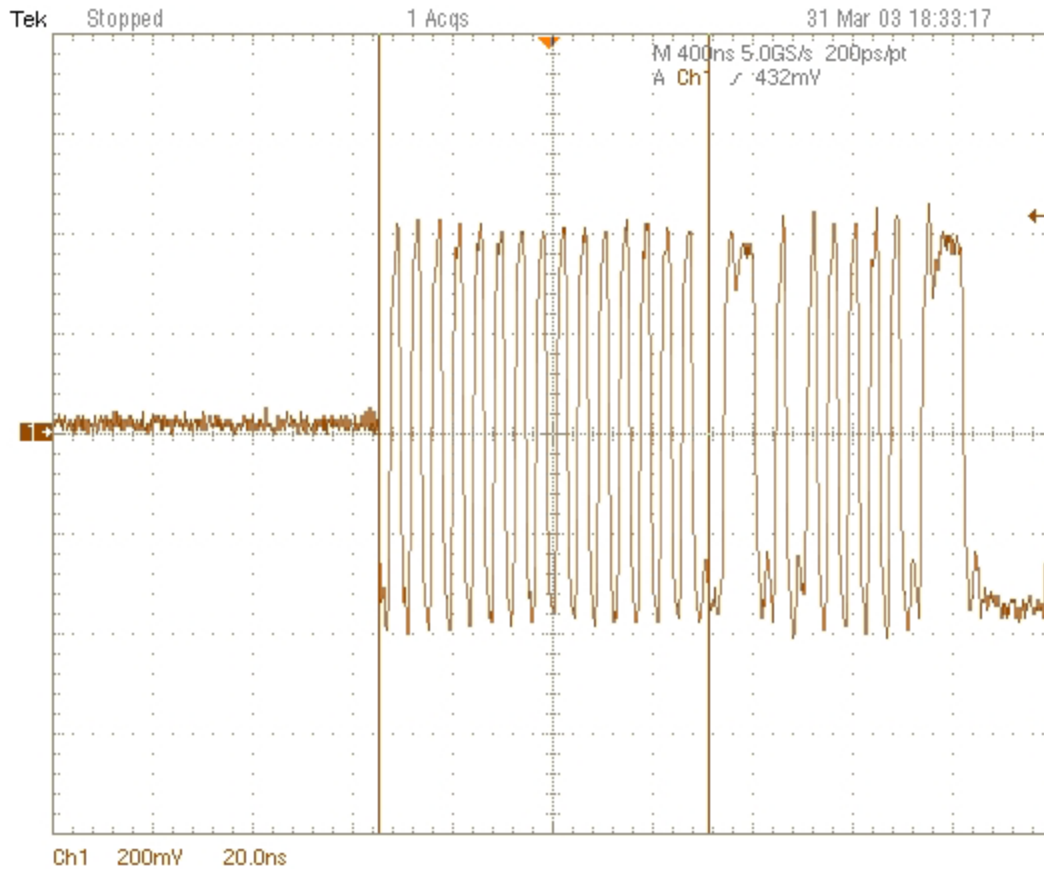
Device Single Step Get Descriptor

7. The oscilloscope capture should appear as follows. Press STOP on the oscilloscope to prevent a miss-trigger from random noise. If the oscilloscope doesn't trigger on the device traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 10.



Packet from Host and Device

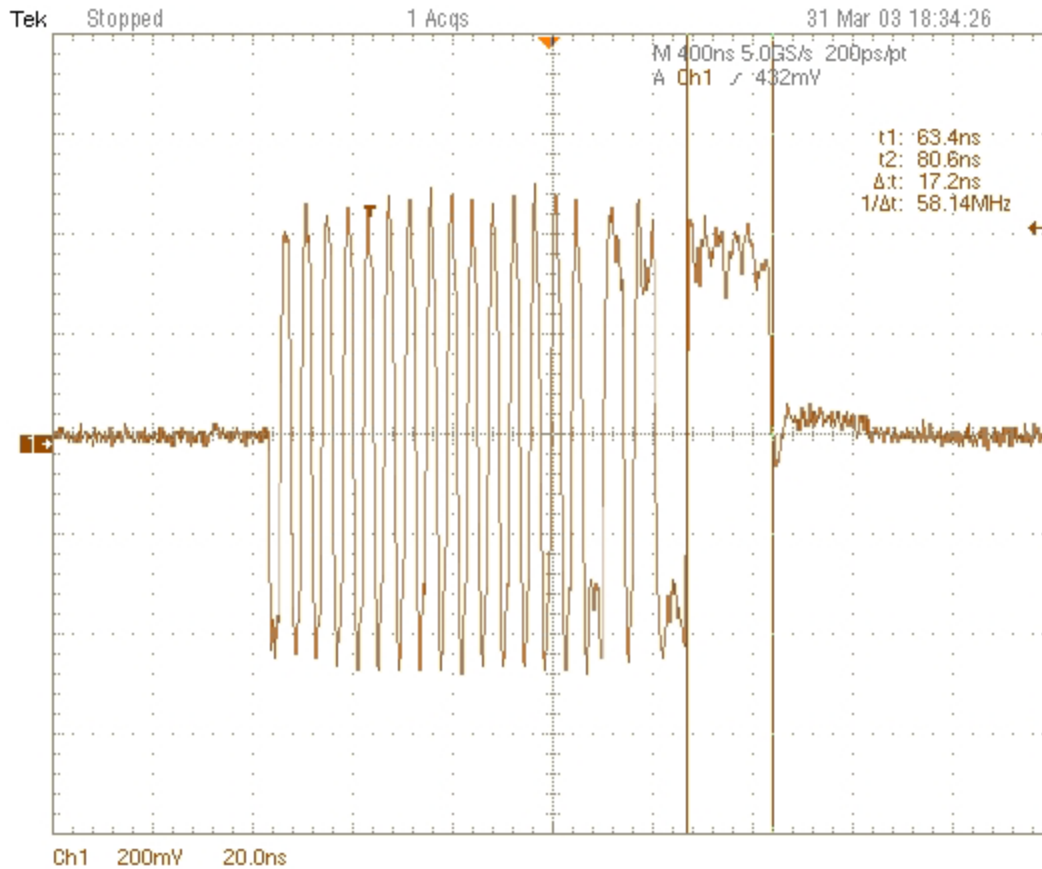
8. Use the zoom function of the oscilloscope, measure the sync field length (number of bits) of the first and second packets on the oscilloscope and verify that they are both 32 bits per EL_21. Refer to the figure below for reference. Note that Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero). Count both rising and falling edges until the first two consecutive 1's and include the first 1. There must be 32 bits. Record the number in EL_21.



Host Packet Sync Field

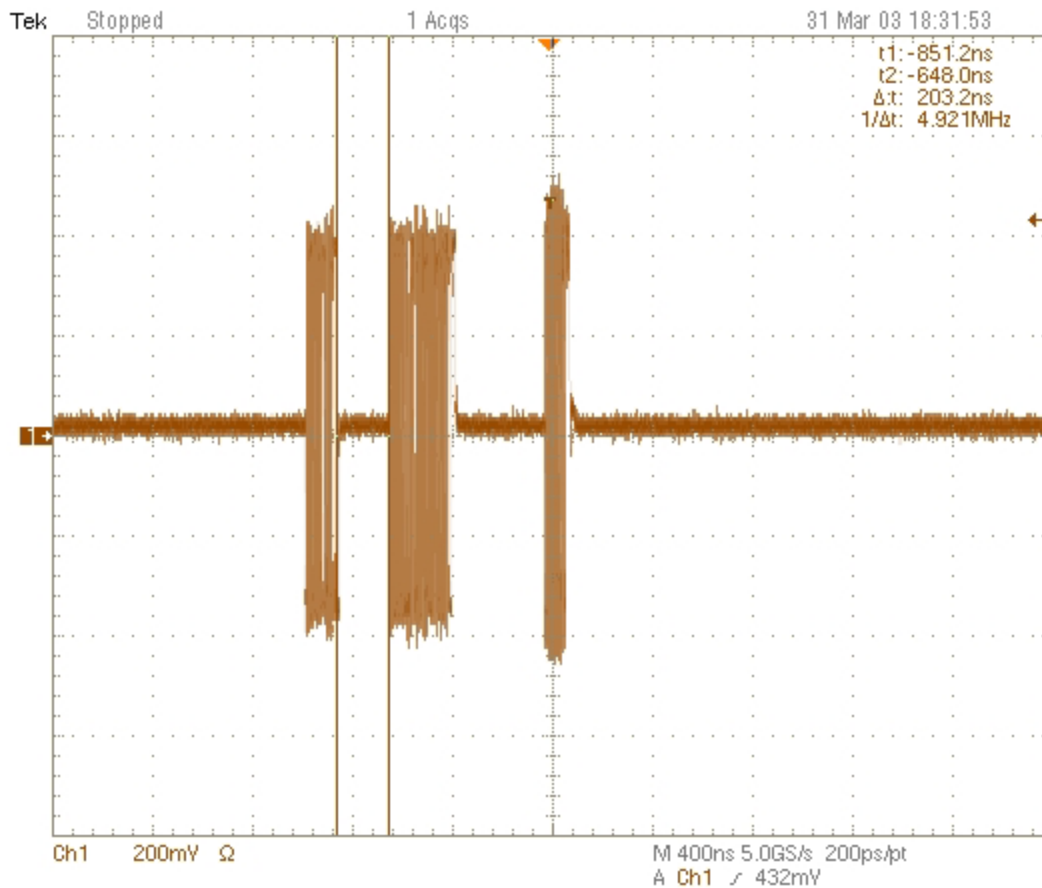
9. Measure the EOP length (number of bits) of the second packet on the oscilloscope and verify that it is 8 bits per EL_25. It is advisable to use the cursors to measure the EOP pulse width to determine the number of bits, based on 2.08nS/bit (480Mbps). Record the result in EL_25.

Please note that the EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The figure below illustrates the positive going pulse.



Host Packet EOP

Measure the inter-packet gap between the first two packets shown on the oscilloscope. These are back-to-back packets from the host. Compute the bits by dividing the time measure by 2.08nS. The requirement is it must be between 88 bits and 192 bits. (EL_23). Record the computed number of bits in EL_23. The oscilloscope should appear as shown in the following figure.



Inter-packet Gap – Between Packets from Host

Ensure the oscilloscope is armed (press run/stop button).

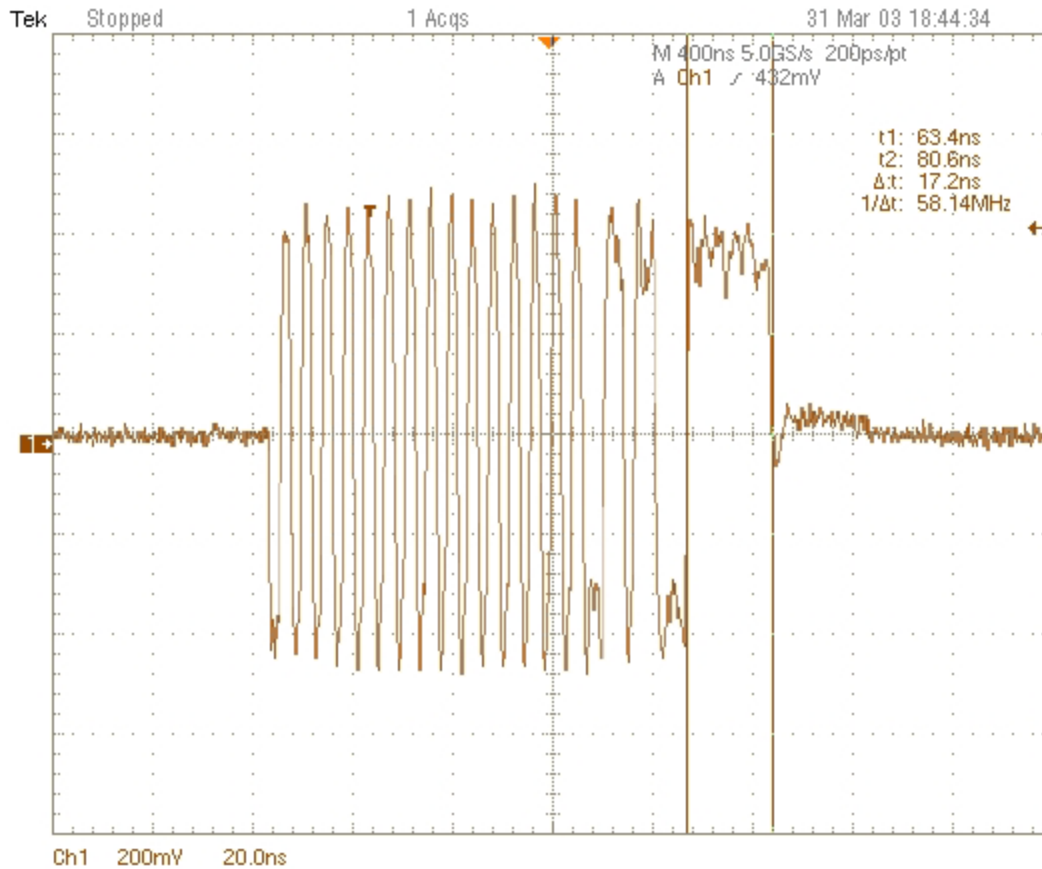
On the Host Test menu click Execute once. The oscilloscope capture should appear as the figure below. Pause the oscilloscope with the run/stop button.

Measure the inter-packet gap between the second and the third packets shown on the oscilloscope. The second (of higher amplitude) is a device packet and the third is the host response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.

NEED HOST RESPONSE PICTURE

Inter-packet Gap – Host Respond to Device

Set the oscilloscope to RUN. Adjust the trigger if necessary until the oscilloscope is continuously being triggered by the SOF packets. Stop the oscilloscope. Measure the time period of the EOP width. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be 40 bits. Record the result in EL_55.



EOP Width – SOF Packet

Repeat step 4 through 15 for the remaining ports.

Remove the Device Signal Quality test fixture and the known good device from the host controller port under test.

4.6 Host Disconnect Detect (EL_36, EL_37)

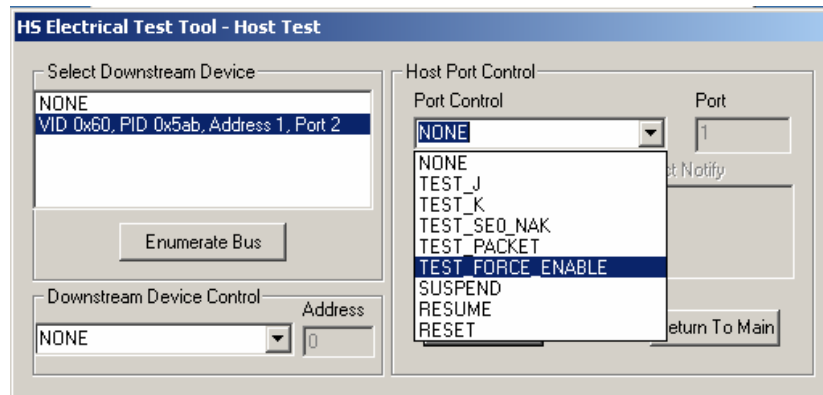
This section uses the Disconnect test fixture to verify the disconnect thresholds of the port under test by simulated disconnect condition. (Contact the USB-IF to acquire this fixture. The TDSUSBF test fixture does not support this test.)

When the TEST switch on the test fixture is in the Test position, the port under test is subjected to a threshold <525mV. The port should not detect a disconnection.

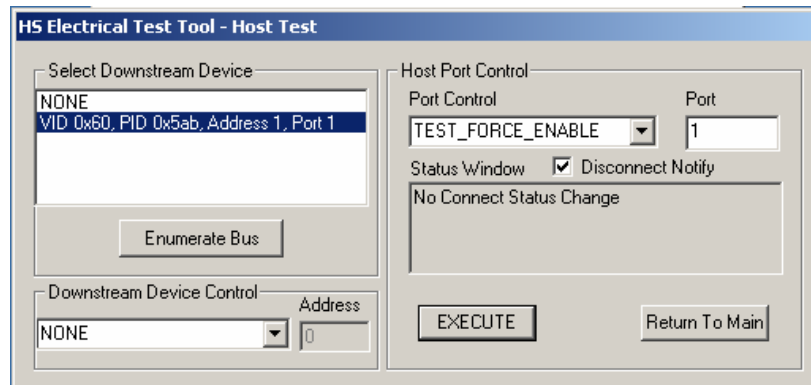
When the TEST switch is in the Normal position, the port under test is subjected to a threshold >625mV. The port should detect a disconnection.

1. Attach the 5V power supply to Disconnect test fixture (J8).
2. Attach the differential probe to J7. Ensure the + tip on probe lines up with D+ on the fixture. Recall the DISCDETE.SET oscilloscope setup.

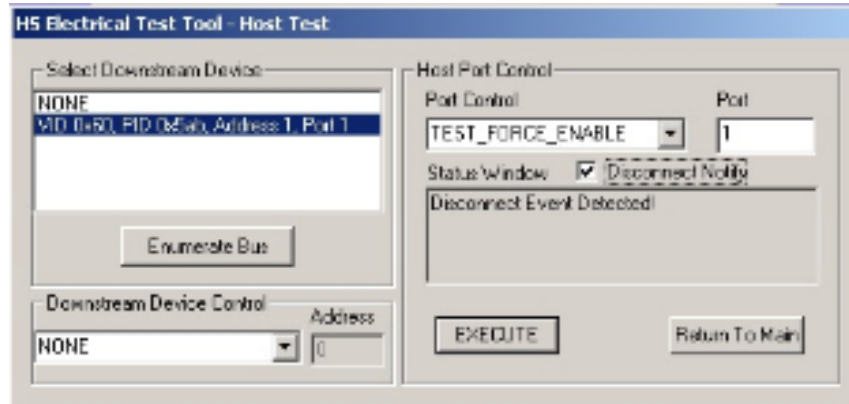
- Set the TEST switch to the Test position. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is also lit. This sets the test fixture to emulate a must-not-disconnect threshold.
- Attach the Test port of the test fixture to the port under test. In the Host Test menu of the High-speed Electrical Test Tool software select TEST_FORCE_ENABLE from the Port Control window. Enter the port number and click Execute once and ensure the operation is successful in the Status Window.



- Click the Disconnect Notify check box to monitor the disconnect status in the Status Window.



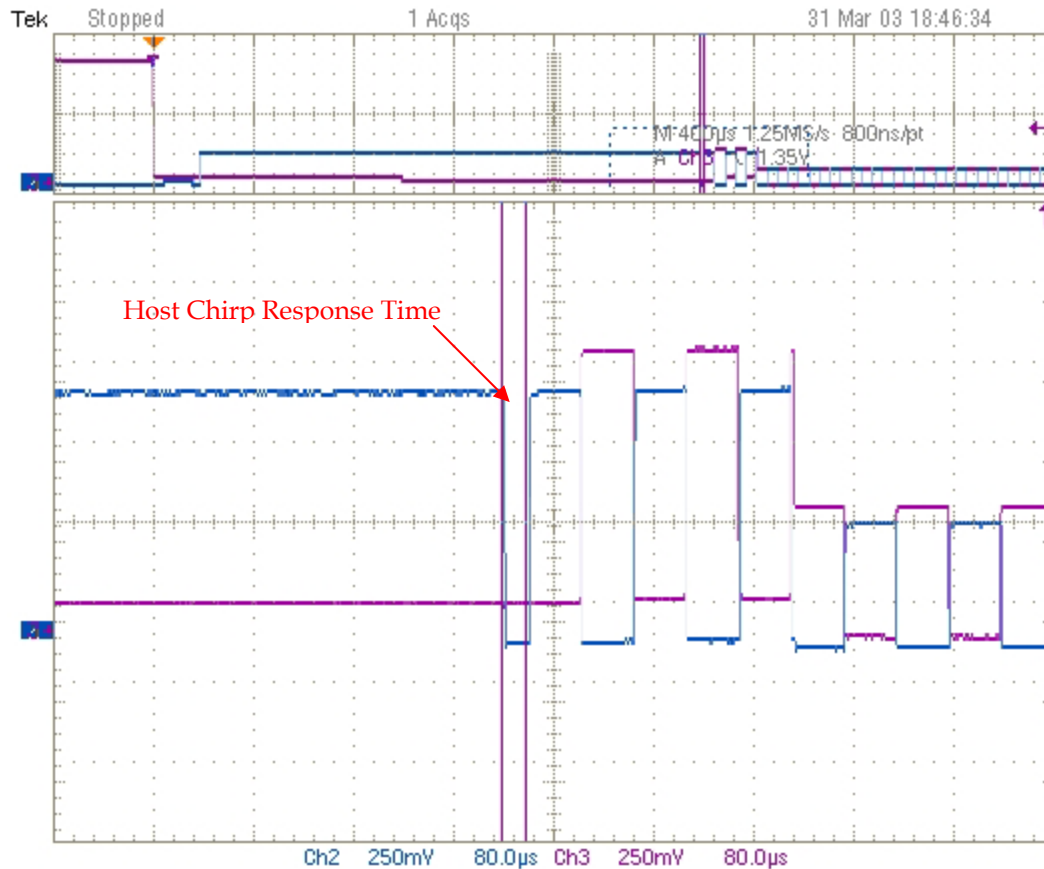
- Using the oscilloscope, verify the SOF packets are being transmitted from the port under test. The differential amplitude should be less than $\pm 525\text{mV}$. Verify that the Status Window does not display Disconnect Event Detected. Record the pass/fail result in EL_37.
- Set the TEST switch of the Disconnect test fixture to the Normal position and verify the yellow TEST LED (D2) is not lit.
- Use the oscilloscope to monitor the differential amplitude of the SOF. It should be greater than $\pm 625\text{mV}$. Verify that the Status Window now displays the Disconnect Event Detected. Record the pass/fail result in EL_36.



9. Return the TEST switch on the fixture back to the TEST position and verify the yellow TEST LED (D2) is lit.
10. Repeat step 4 through 9 for all the remaining ports.
11. Remove the Disconnect test fixture from the port under test before proceeding.

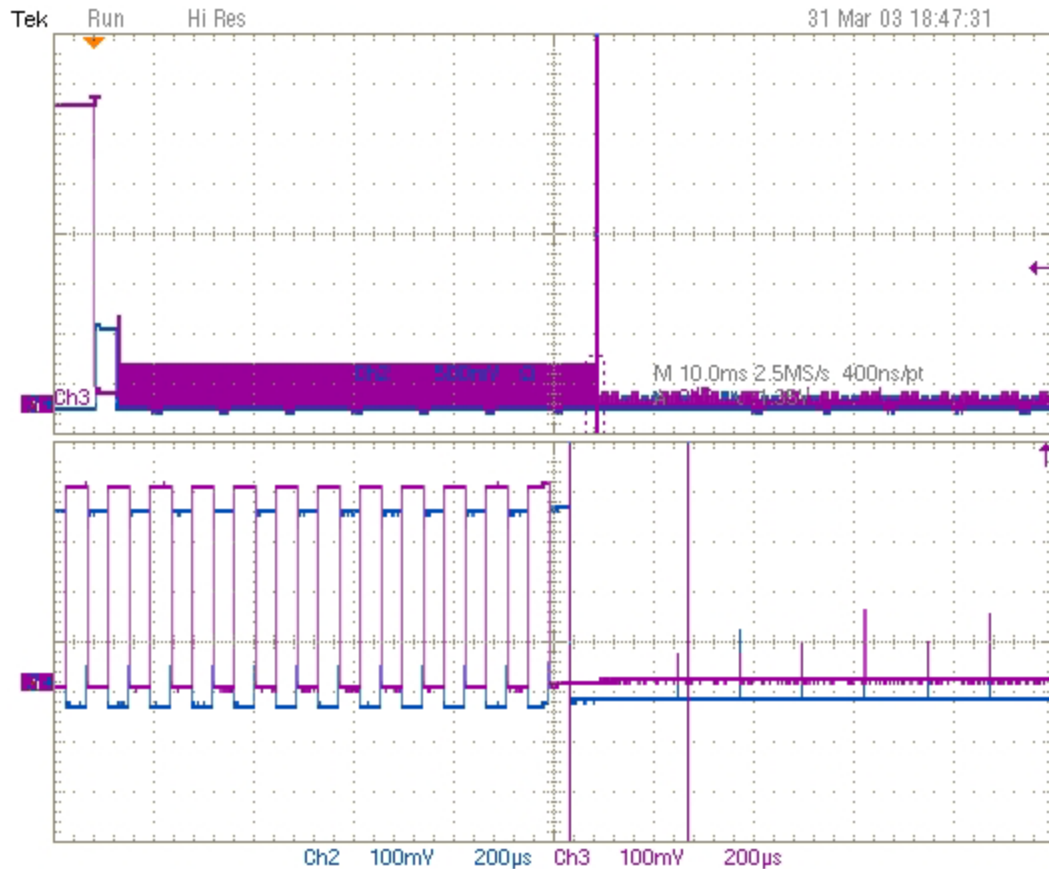
4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds.
3. Launch the TDSUSB software application on the TDS7404 or TDS7254 oscilloscope by selecting with a mouse or touch screen, File: Run application: USB2.0 compliance test package.
4. In the applications menu bar select, file: recall default.
5. Within the USB2.0 compliance test application, select the High Speed tab.
6. Select Measurement > Select > Chirp on the TDSUSB2 application.
7. Click Enumerate Bus using the High Speed Electrical Test Tool and capture the CHIRP handshake as in the figure below.



High Speed Chirp

8. Measure the host's Chirp response timing (T_{WTRSTS}). This is the time between the device's de-assertion of Chirp-K and the start of alternate Chirp-K and Chirp-J sent by the host. Verify this timing is $T_{WTRSTS} \leq 100\mu S$. Record the result in EL_33.
9. Measure and record the durations of the individual Chirp-K and Chirp-J states and verify both are between $40\mu S \leq T_{DCHBIT} \leq 60\mu S$ (EL_31). Record the measurement in EL_34.
10. Recall the SOFCHP23.SET oscilloscope setup.
11. Unplug the known good device and then reattach it.
12. Ensure the oscilloscope trigger is armed.
13. Click Enumerate Bus once. The oscilloscope capture should appear as follows.



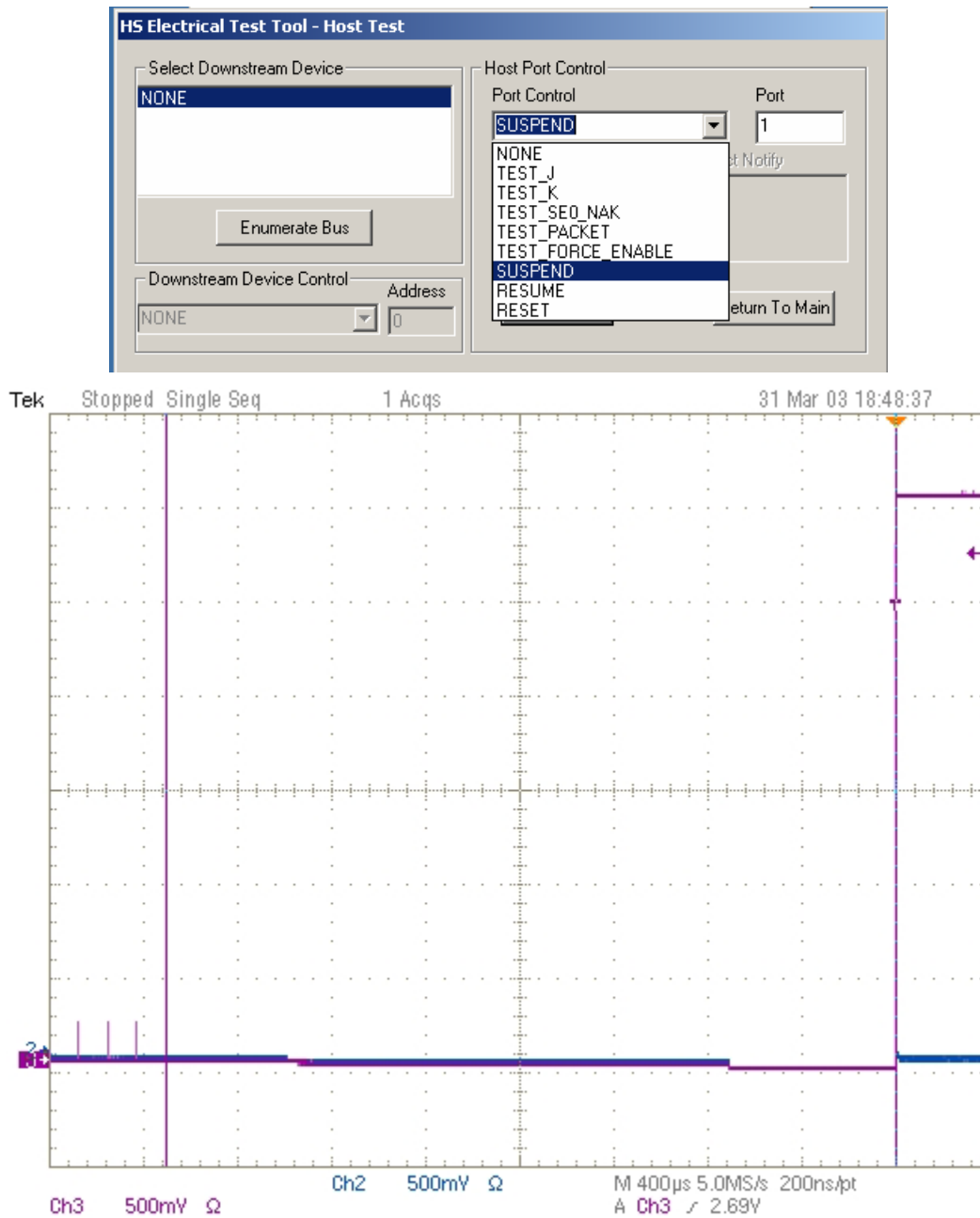
Time between SOF and Last Chirp- (J or K)

14. Measure the time from the end of host Chirp-J/K to the first SOF sent out by the host. Verify this is $100\mu\text{s} \leq T_{\text{DCHSE0}} \leq 500\mu\text{s}$. Record in EL_35.
15. Repeat step 5 through 13 for the remaining down stream facing ports.

4.8 Host Suspend/Resume timing (EL_39, EL_41)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the host port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds to the outside pins of J36.
3. Recall the SUSP2&3.SET oscilloscope setup and verify the oscilloscope is armed.
4. Attach the INIT port of the fixture into the port under test at the host controller.

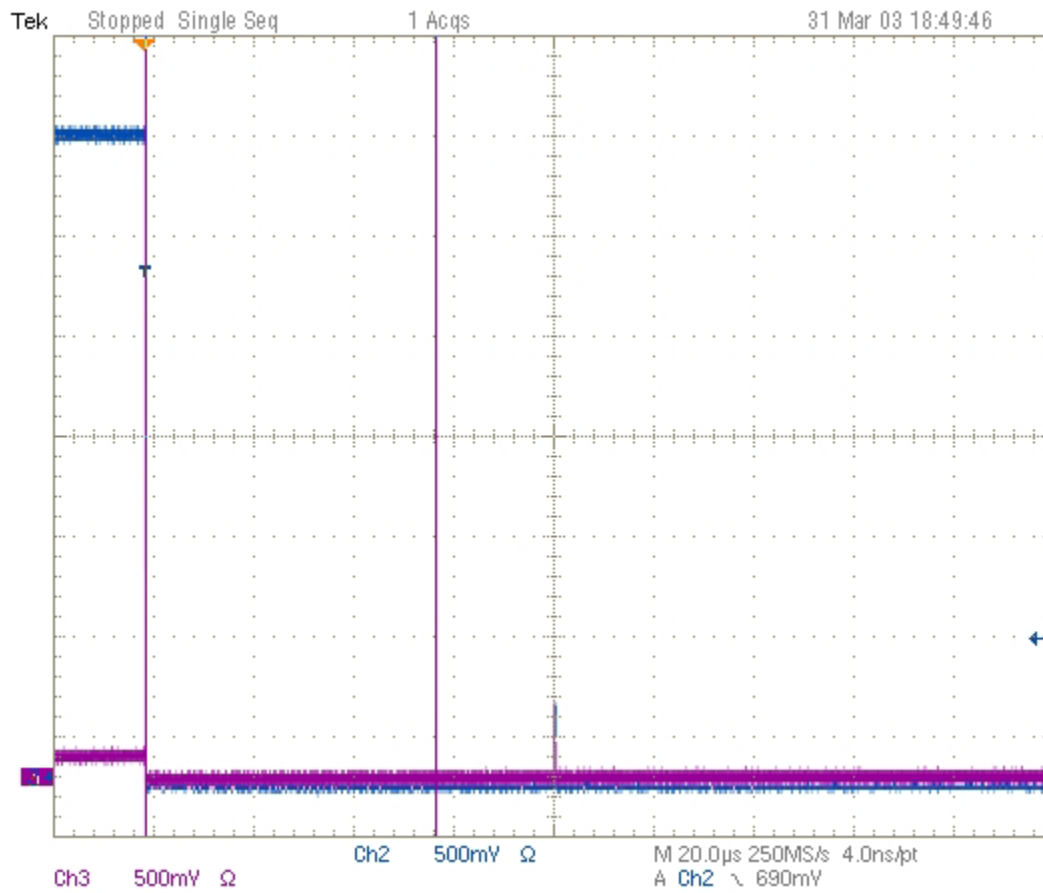
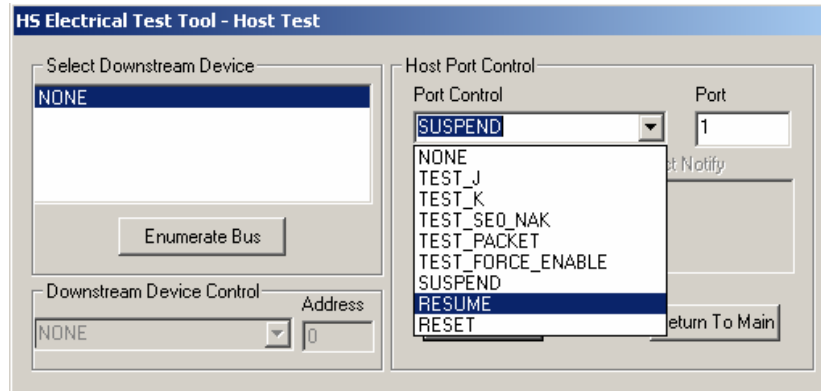
- On the Host Test menu, select SUSPEND from the Port Control drop down menu and enter the port number. Click Execute once to place the port into suspend. The captured suspend transition should appear as in the figure below.



Device Enters Suspend

- Observe the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+ (transition to full speed J-state). This time should be between 3.000mS and 3.125mS. No measurement is required as this sequence verify the host supports Suspend state. Record the Pass/Fail result in EL_39.

7. Recall the RESUM2&3.SET oscilloscope setup and verify the oscilloscope is armed.
8. On the Host Test menu, select RESUME from the Port Control drop down menu and enter the port number. Click Execute once to resume the port. The captured suspend transition should appear as in the figure below.



Time to First EOP from Start of HS Idle

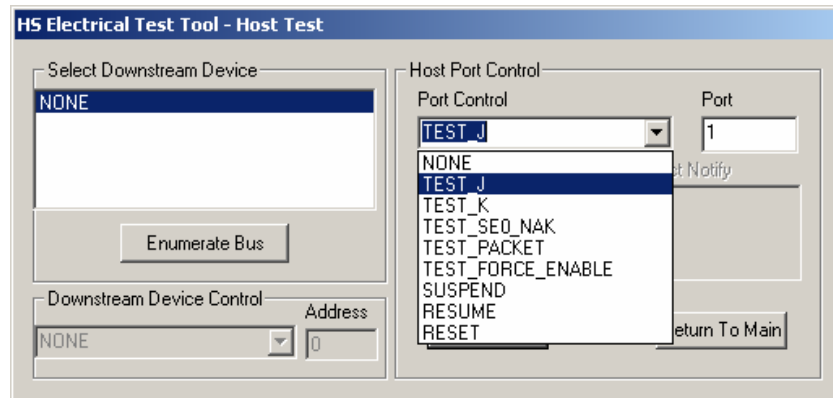
9. Measure the time from the falling edge of D+ to the first SOF issued by the host (EL_41) as shown in the figure below. Record the results in EL_41.

Note: Repeat the suspend and resume a number of times and verify the time from the falling edge of D+ to the first SOF issued by the host never exceeds 3mS.

10. Repeat step 4 through 9 for all the remaining ports.
11. Unplug the known good device from the test fixture. Click Enumerate Bus once before proceeding. Remove the FET probes from the test fixture.

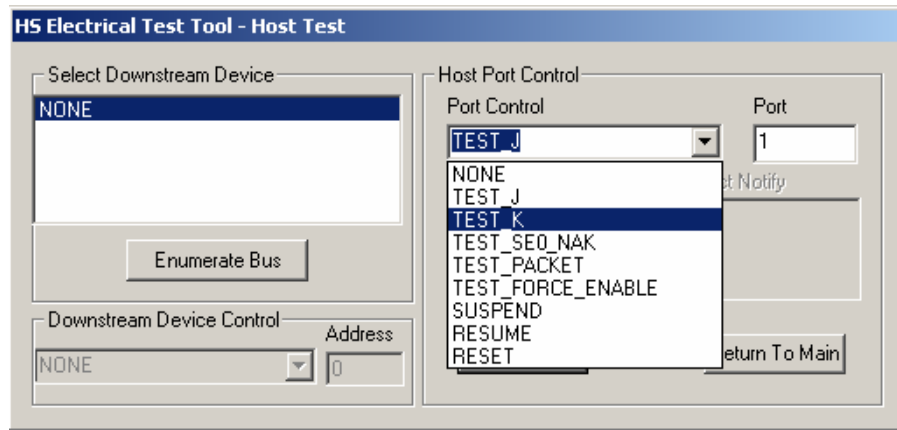
4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

1. Connect the short USB cable dongle of the HS Device SQ segment of the TDSUSBF test fixture into the upstream facing port of the known good high-speed device. Connect the Init port of the test fixture to the port under test. Apply power to the device. Ensure that the Test Init switch is in the Init position.
2. Select TEST_J from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_J test mode.



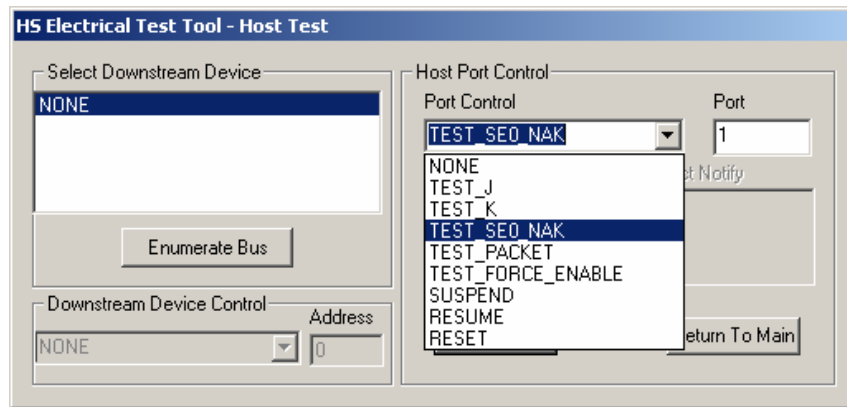
Host Port TEST_J

3. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground (outside pins of J36 are the ground pins). Record in section EL_8.
4. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground. Record in section EL_8.
5. On the Host Test menu, select TEST_K from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_K test mode.



Host Port TEST_K

6. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_8.
7. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground. Record in section EL_8.
8. On the Host Test menu, select TEST_SE0_NAK from the Port Control drop down menu. Enter the port number and click Execute once to place the port under test into TEST_SE0_NAK test mode.



Host Port TEST_SE0_NAK

9. Using a DVM measure the DC voltage on the D+ line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_9.
10. Using a DVM measure the DC voltage on the D- line at J36 with respect to ground (Outside pins of J36 are ground pins). Record in section EL_9.
11. Repeat step 2 through 11 for the remaining ports.

Appendix A

A.4 Host High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2 Vendor and Product Information

	Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.
Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Downstream Ports					Comments
	P1	P2	P3	P4	P5	
LS SQ						
FS SQ						
Drop/ Droop						
Interop						

P = PASS

F = FAIL

N/A = Not applicable

A.4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s $\pm 0.05\%$.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_3 A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measured at TP2 (each host downstream port).

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

- ☐ Pass
- ☐ Fail

☐ N/A

Comments:

A.4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification*, Section 8.2.

SOF SYNC field

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

Data Packet SYNC field

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (Note, that a longer EOP is waivable)

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_23 Hosts transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

--

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_55 Hosts transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

A.4.6 Host Disconnect Detect (EL_36, EL_37)

EL_37 A USB 2.0 downstream facing port must not detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≤ 525 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

--

EL_36 A USB 2.0 downstream facing port must detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≥ 625 mV.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

A.4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

EL_33 Downstream ports start sending and alternating sequence of Chirp K's and Chirp J's within 100us after the device Chirp K stops.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_34 Downstream port Chirp K and Chirp J durations must be between 40us and 60us duration.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_35 Downstream ports begin sending SOFs within 500us and not sooner than 100us from transmission of the last Chirp (J or K).

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

A.4.8 Host Suspend/Resume timing (EL_39, EL_41)

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL_41 After resuming a port, the host must begin sending SOFs within 3ms of the start of the idle state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.7.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

A.4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV $\pm 10\%$ when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Port	1		2		3		4		5	
Test	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
TEST_J										
TEST_K										

☐ Pass

☐ Fail

☐ N/A

Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be $0V \pm 10 \text{ mV}$ when terminated with precision 45Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Port	1		2		3		4		5	
Signal	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
Measure WRT Ground (mV)										

☐ Pass

☐ Fail

☐ N/A

Comments: