Universal Serial Bus Implementers Forum Host High-speed Electrical Test Procedure for LeCroy

Revision 1.0
Dec. 3, 2003

Revision History

Rev	Date	Filename	Comments
0.9 (Beta)	May-23-2003	Host HS Test for lecroy.DOC	Primary version of High Speed Test Procedure adapted to Agilent test equipment based on the test procedure created by USB-IF (version 0.9)
1.0	Dec-3-2003	Lecroy hs host rev 1.doc	Approved by USB-IF

Please send comments via electronic mail to techsup©usb.org

USB-IF High-speed Electrical Test Procedure

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Host HS Tests for LeCroy

I Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Host USB-IF High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Hub USB-IF High-speed Electrical Test Procedure and Device USB-IF High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Equipment Required

The commercial test equipment listed here are based on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

- Digital Storage Oscilloscope:
    - WaveMaster or SDA from LeCroy Corporation
        - LeCroy D300 or equivalent differential probe, qty = 1
        - LeCroy HFP2500 Active probe, qty = 2

• 3 1/2 Digital Multimeter – Agilent 972A or equivalent

- Mini-clip DMM lead - one each of black and red color

• High-speed USB Electrical Test Fixtures

- LeCroy USB 2.0 test fixture (model number TF-USB) or equivalent, qty = 1

• Miscellaneous Cables

- 1M USB cable, qty = 1
- 1.5M USB cable, qty = 1
- Modular AC power cord, qty = 2

• High-speed USB Test Bed Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. This OS on this computer is Windows 2000 Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

3.1 Equipment Setup

3.1.1 Digital Sampling Oscilloscope

Before turning on the oscilloscope, attach the differential probe to Channel 1. Make sure the 10x attenuator is attached at the tip of the differential probe. Attach the HFP2500 probes to channels 2 and 3. These probe assignments will be used through out the entire test procedure. Turn on the oscilloscope to allow for 10 minutes of warm up time prior to use.

Note: In certain test situations, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operating Systems

Microsoft Windows 2000 Professional is required on the High-speed Electrical Test Bed Computer. Microsoft Windows 2000 Professional is required on the High-speed Signal Quality Analysis Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computerS.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer. The software USBHSET.exe can be downloaded from the UFB-IF web site at www.USB-IF.org and installed on the test bed computer. This same software must also be installed on the oscilloscope running the LeCroy USB2.0 test software.

- Matlab v6.5 release 13 installed on the oscilloscope running the LeCroy USB2.0 test software. This can be obtained from The Mathworks at www.mathworks.com.

- LeCroy USB2.0 (part number USB2)test software for the oscilloscope

4 Test procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date
2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the host controller under test must also pass the following compliance tests applicable to the EHCI Host Controller:

- Low speed signal quality
- Full speed signal quality
- Drop/Droop
- Interoperability

Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.

4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

1. Select “USB2” from the analysis menu of the oscilloscope. In the USB test wizard, select “host” for the mode and select “HS Signal Quality” in the “Test” dialog box. Enter the path and file name for the intermediate result file in the “Result File Name” dialog box.

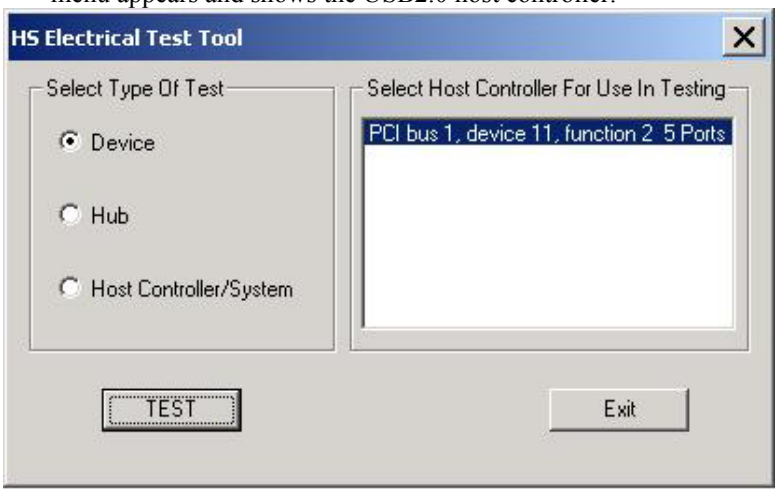
2. Attach the 5V power supply to the USB test fixture and verify that the “power” LED is lit.

3. Verify the green Power LED is lit, and the yellow Test LED is not lit.

4. Connect the host port under test to the A cable on [SQ Host] section of the test fixture.

5. Attach the differential probe to J30 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

6. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



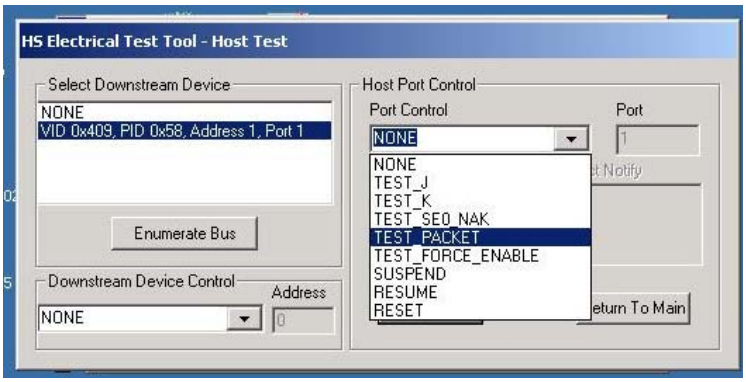
High Speed Electrical Test Tool – Main Menu

7. Select host and click the [TEST] button to enter the HS electrical test tool host test menu.

8. Press “Next” in the USB test wizard menu to start Matlab. If the oscilloscope enters the calibration stat, wait until this finishes and then press “next” again in the USB test wizard.

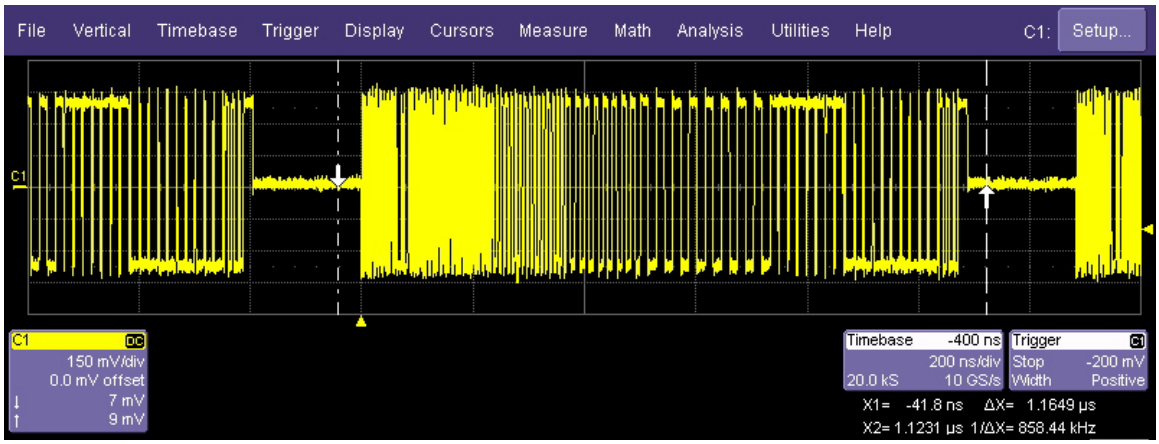
9. Select TEST_PACKET from the host Command drop down menu and click [EXECUTE]. This forces the host

under test to continuously transmit test packets.



10. Place the INIT/Test Switch on the fixture in the TEST position. Verify the yellow TEST LED is lit.

11. using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the cursors so that they are on either side of the test packet on the screen if necessary.



Test packet from host showing cursor placement

12. Enter a descriptive file name in the [Result File Name] dialog box. Note that the default directory is D:\Applications\USB2\Results and the file name has the extension *.tsv which is the intermediate result file for the MatLab scripts. The same file name (with a .HTM extension) is used for the HTML report file.

13. Press the [Next] key in the LeCroy USB 2.0 test wizard. The MatLab analysis script will be invoked to measure the signal quality. The following two plots will appear on the Windows desktop:

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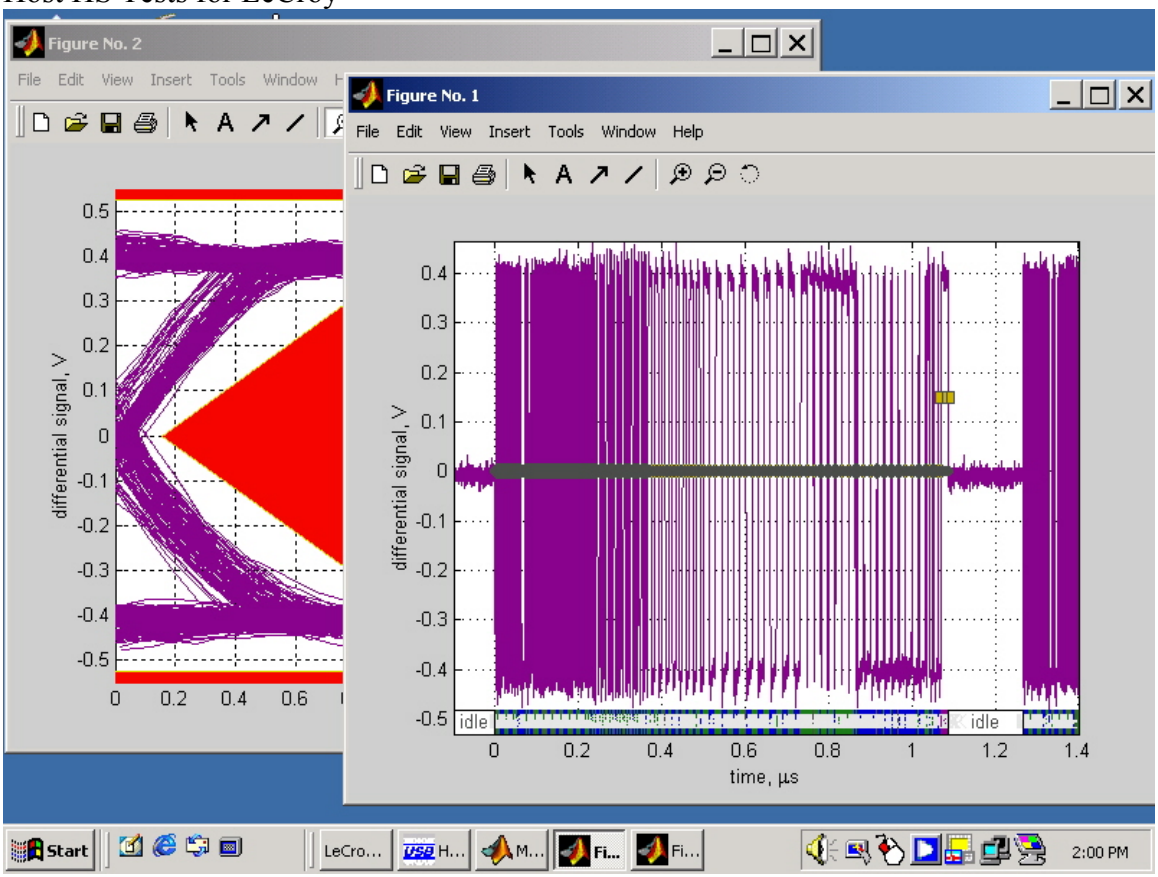
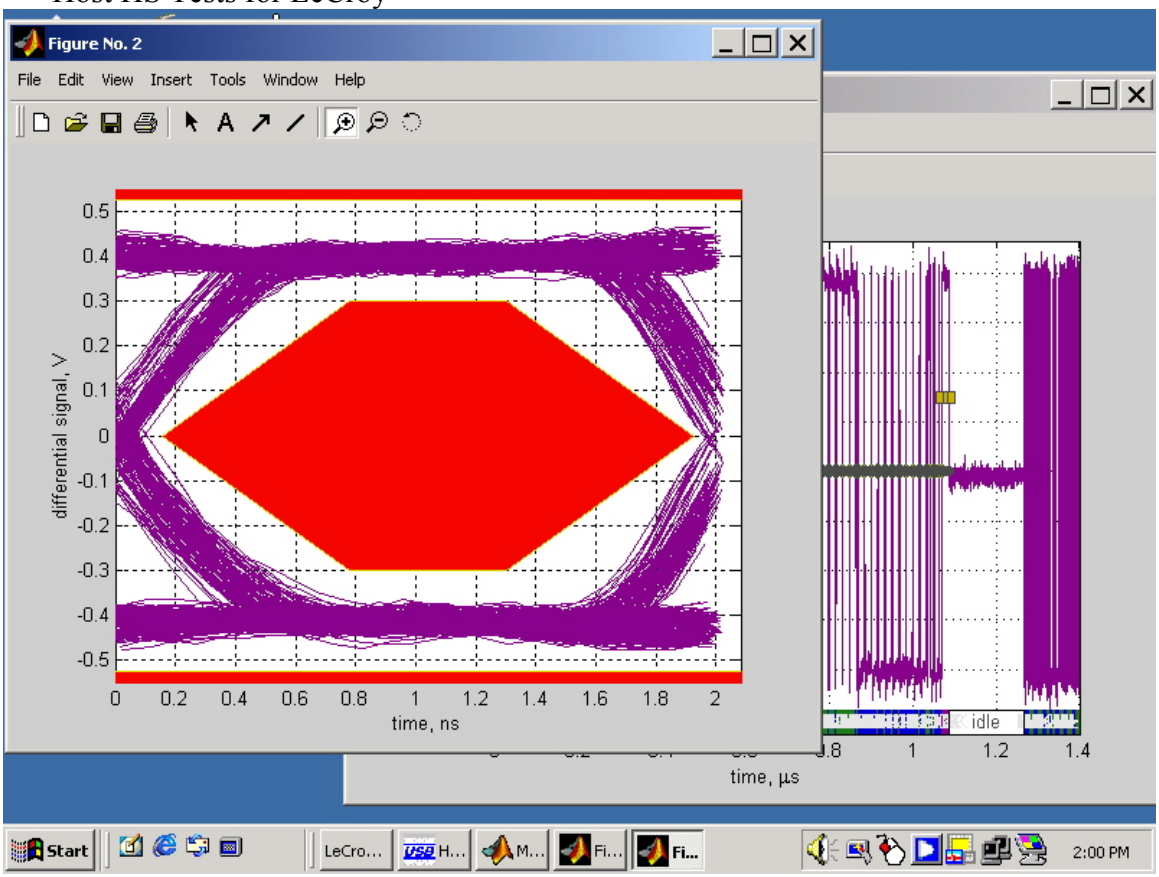




14. The results displayed are also recorded to an HTML report located in the directory specified in the "Data Path" control in the test wizard (D:\Applications\USB2\Results by default). Open this file and verify the Signal eye, EOP Width, and Signaling Rate all pass.

15. Note: if there is any irregularities in the captured waveform such as an incorrect EOP width, the Matlab plots shown above will not be displayed and the HML report will not be generated. Check the probe connections to make sure there are no problems.

16. Record the test result in EL_2, EL_3 or EL_4, EL_6 and EL_7. Save all files created during the tests

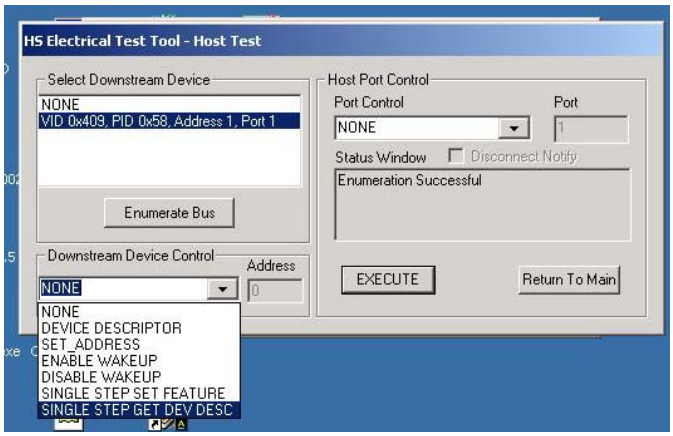
17. Return the INIT/Test switch of the test fixture back to the Normal position and verify the yellow TEST LED is not lit.

4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

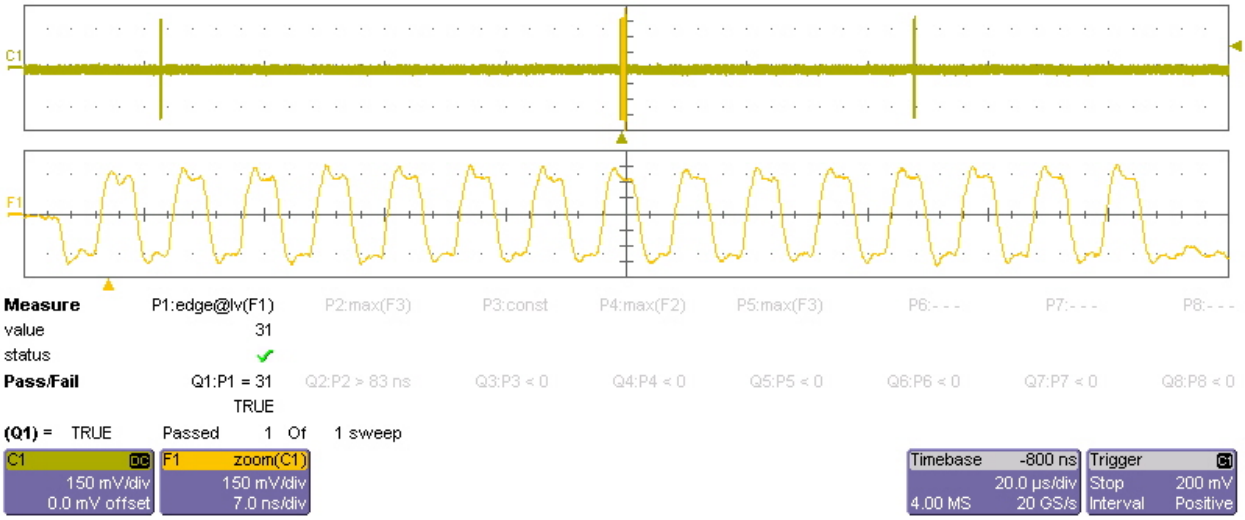
1. Select Host in the [Mode] control and HS Packet Parameters in the [Test] control of the USB Test Wizard.
2. Connect the Device Signal Quality section of the test fixture [TEST PORT] into B receptacle of a known good high-speed hub. Apply power to the known good hub (referred to as device herein).

Note: The use of the Device High-speed Signal Quality test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the differential probe to J19 on the fixture near the device connector. Ensure + on probe lines up with D+ on fixture.
4. Connect the Device Signal Quality section of the test fixture [INIT PORT] into the host controller port under test. Click [Enumerate Bus] and verify that the device enumerates properly.
5. Press [next] in the USB test wizard to start the test.
6. press “enumerate bus” in the high speed electrical test tool. If theoscilloscope goes into calibration mode, wait until this finishes and then press [next] in the USB test wizard.
7. In the Host Test menu of the High-speed Electrical Test Tool software, ensure the device is selected (highlighted). Select SINGLE STEP GET DEV DESC from the Downstream Device Control menu and click [EXECUTE] once.

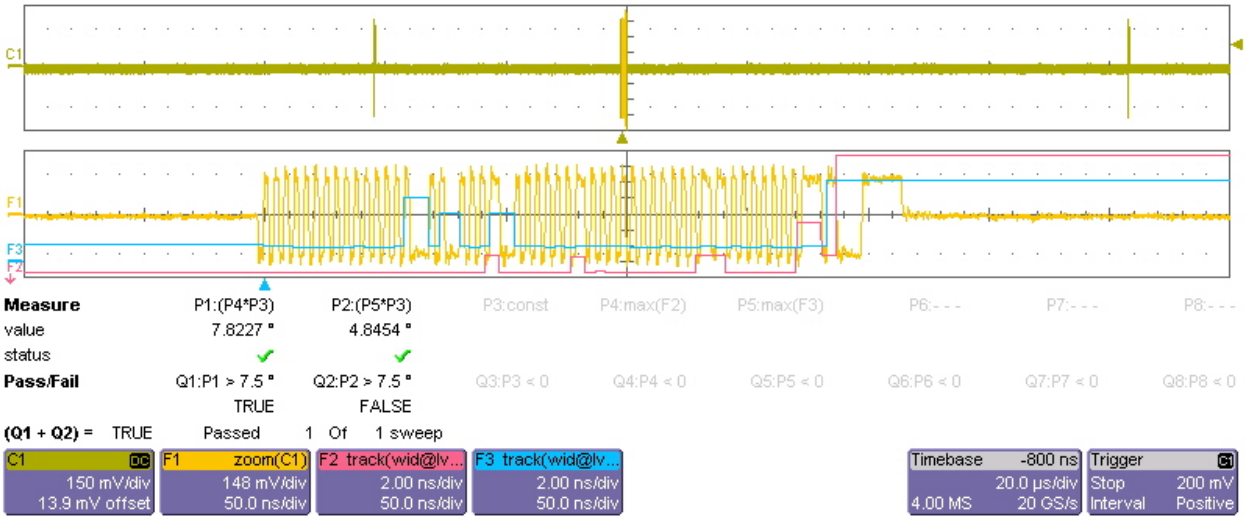


8. The oscilloscope capture should appear as follows.

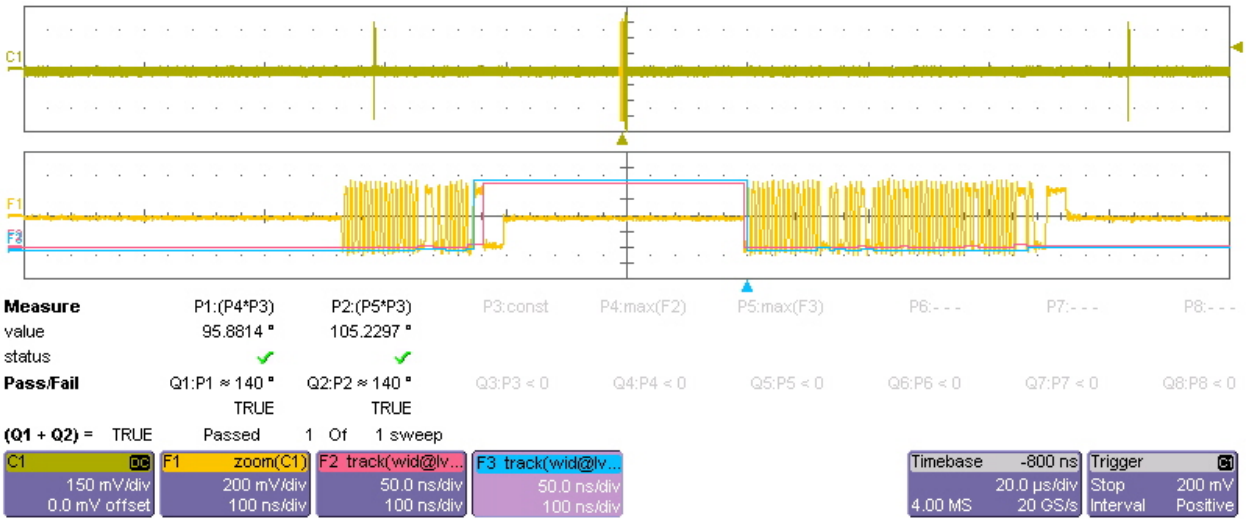


9. P1 indicates the sync field length in bits which should indicate 31 edges which corresponds to 32 bits. Record the number (P1 + 1) in EL_21.

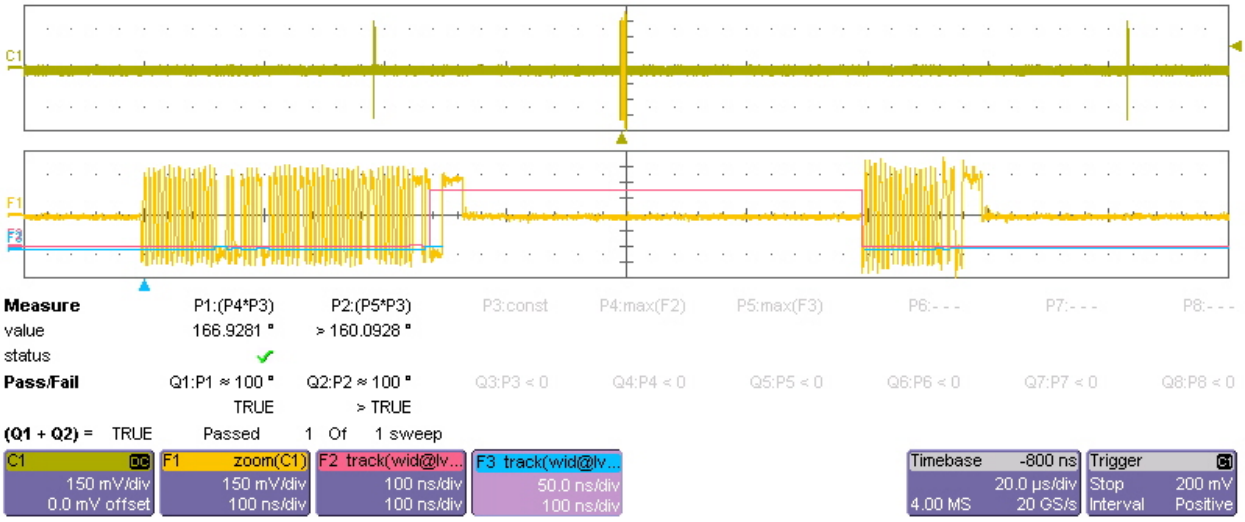
10. Press Next in the test wizard to measure the EOP length (number of bits) of the second packet on the oscilloscope and verify that it is 8 bits per EL_25. This result is shown in P1 and P2. The test passes if either one is 8 bits since the EOP can appear as negative or positive going pulses. Record the result in EL_25.



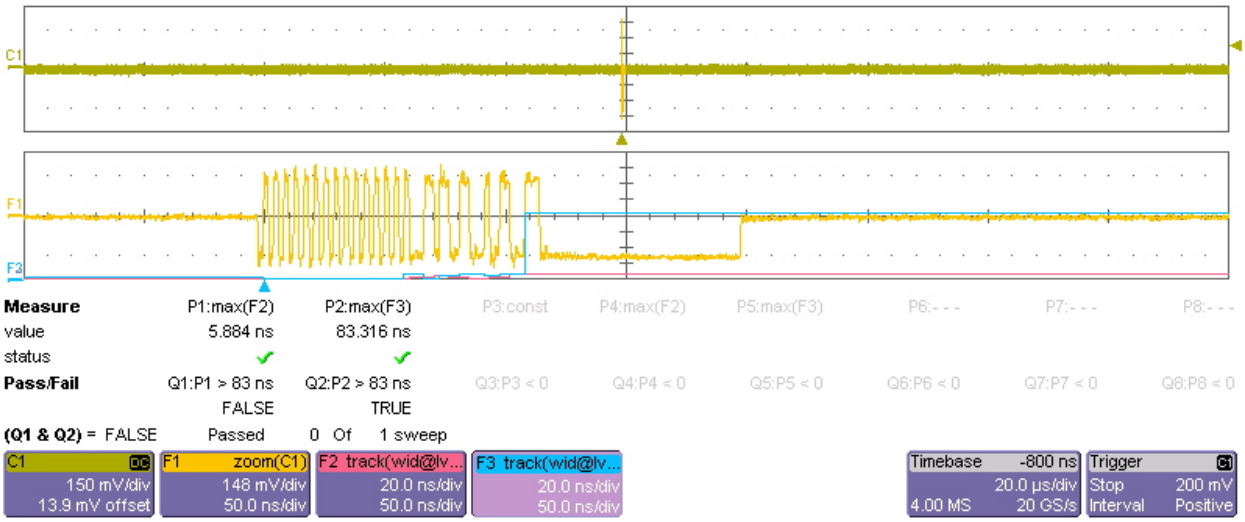
11. Press Next in the test wizard to measure the inter-packet gap between the first two packets shown on the oscilloscope by. The requirement is it must be between 88 bits and 192 bits (EL_23). This result is shown in P1 and P2 for negative and positive going pulses respectively. Record this value in EL_23. The oscilloscope should appear as shown in the following figure.



12. Measure the inter-packet gap between the second and the third packets by pressing the Next button on the test wizard. This value is reported in P1 and P2. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.



13. On the HS Test Tool, press Step twice and then Enumerate Bus.
14. Press the Next button in the test wizard to measure the SOF EOP width. This value is reported in P1 and P2. The requirement is that either the negative (P1) or positive (P2) must be 40 bits (83.2 ns). Record the result in EL_55.



15. Repeat step 4 through 14 for the remaining ports.
16. Remove the Device Signal Quality test fixture and the known good device from the host controller port under test.

4.6 Host Disconnect Detect (EL_36, EL_37)

This section uses the Disconnect test fixture to verify the disconnect thresholds of the port under test by simulated disconnect condition.

When the TEST switch on the disconnect section of the test fixture is in the Test position, the port under test is subjected to a threshold <525mV. The port should not detect a disconnection. When the TEST switch is in the

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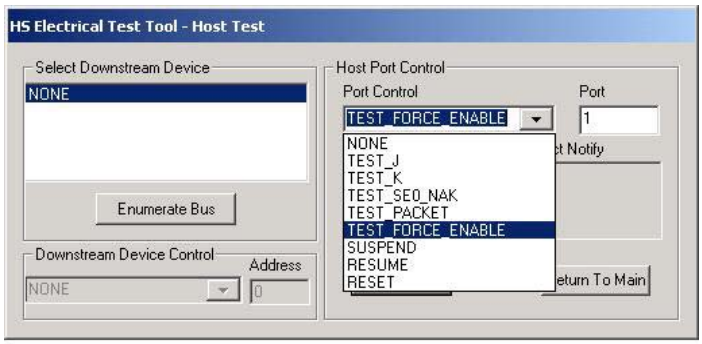
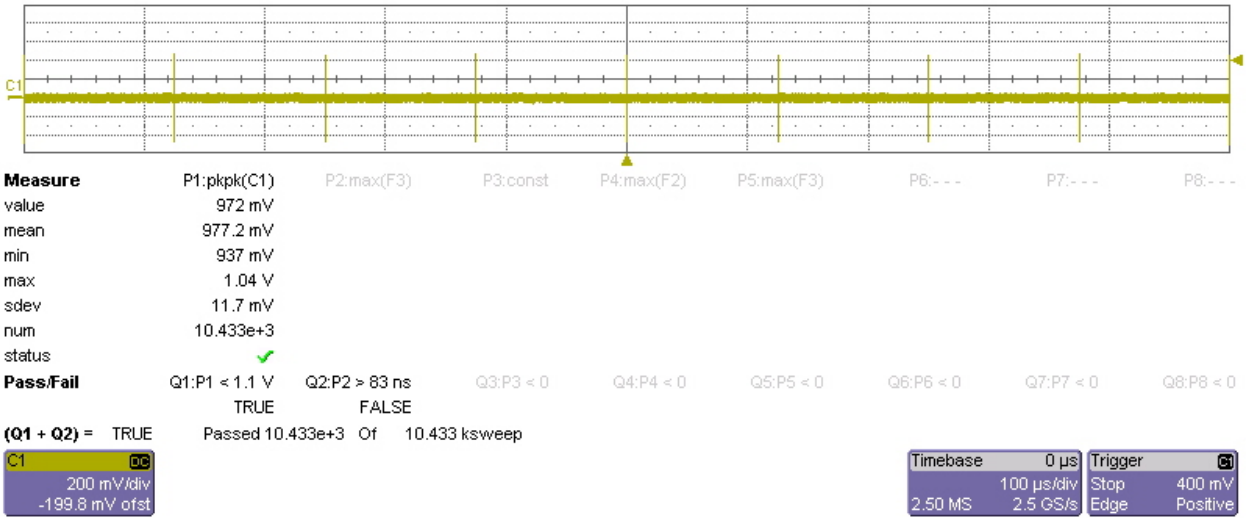
Normal position, the port under test is subjected to a threshold >625mV. The port should detect a disconnection.

1. Attach the 5V power supply to test fixture (J2).
2. Select Host in the [Mode] control and HS Disconnect in the [Test] control of the USB Test Wizard.
3. Attach the differential probe to J5 of the disconnect section of the fixture. Ensure the + tip on probe lines up with D+ on the fixture.
4. Set the two switches in the disconnect section away from the TEST and LOW positions. This sets the test fixture to emulate a must-not-disconnect threshold.
5. Attach the [INIT] 'A' cable of the disconnect section of the test fixture to the port under test. Start the high speed electrical test tool, select "host" and then "Test". Press [next] in the USB test wizard.
6. In the Host Test menu of the High-speed Electrical Test Tool software select TEST_FORCE_ENABLE from the Port Control window. Enter the port number and click [EXECUTE] once and ensure the operation is successful in the Status Window. Press [Next] in the USB test wizard.



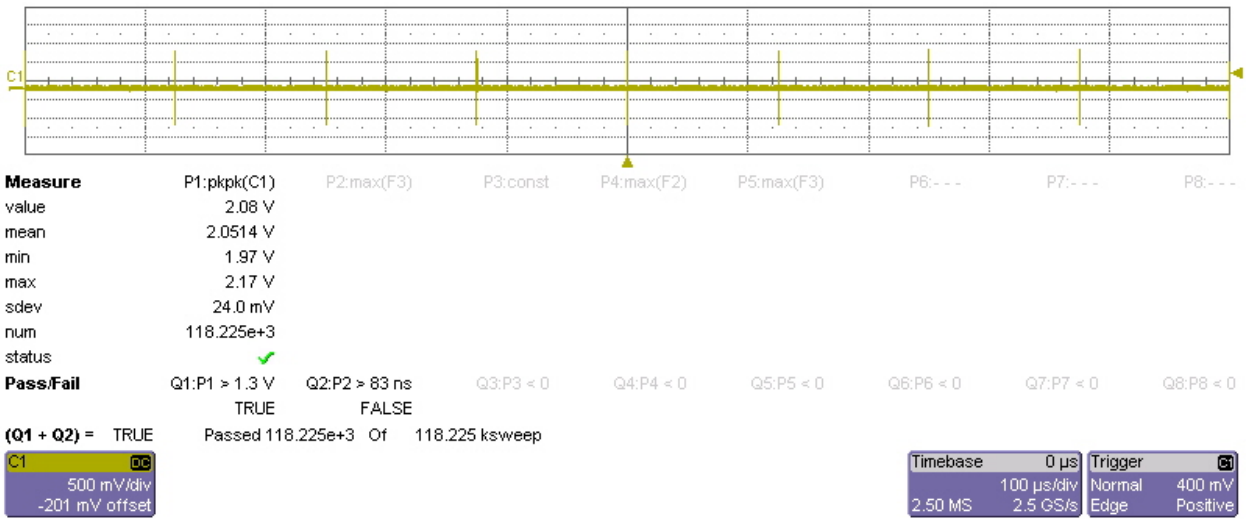
7. Click the Disconnect Notify check box to monitor the disconnect status in the Status Window.
8. Using the oscilloscope, verify the SOF packets are being transmitted from the port under test. The differential amplitude should be less than **+/-** 525mV (1.05V p-p). Verify that the Status Window does not display Disconnect Event Detected. Record the pass/fail result in EL_37.

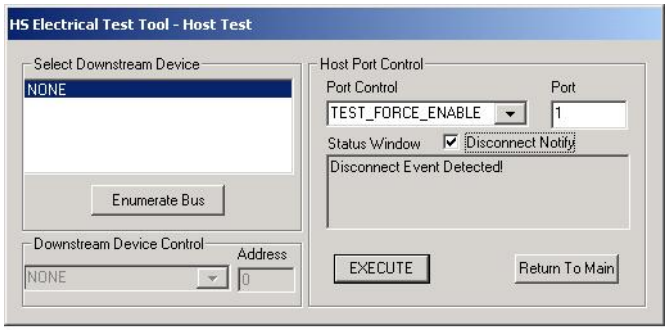


9. Move the TEST switch of the Disconnect section of the test fixture from its current position and press the

Next button on the test wizard.

10. Use the oscilloscope to monitor the differential amplitude of the SOF. It should be greater than **+/-** 625mV (1.25V p-p). Verify that the Status Window now displays the Disconnect Event Detected. Record the pass/fail result in EL_36





11. Return the TEST switch on the disconnect section of the fixture back to its original position.
12. Repeat step 4 through 9 for all the remaining ports.
13. Remove the Disconnect test fixture from the port under test before proceeding.

4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

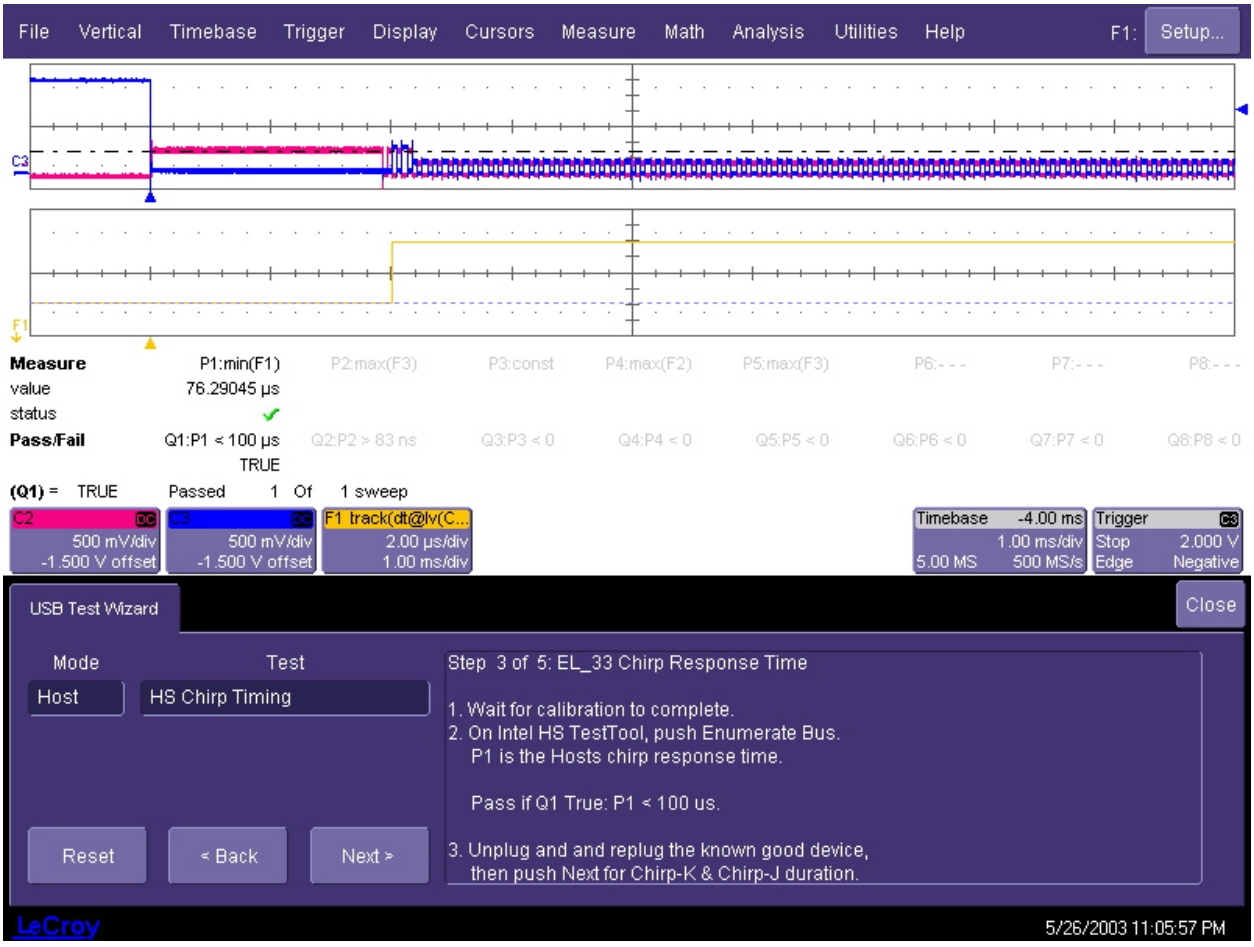
1. Select Host in the [Mode] control and HS Chirp Timing in the [Test] control of the USB Test Wizard.

2. Connect the HS port under test to the [INIT] port of the SQ Device section of the test fixture. Attach a known good device to the Device port of the SQ Device section of the test fixture. Apply power to the known-good device. Make sure the TEST/INIT switch is in the INIT position.

3. Start the HS test tool, select Host Controller/System and push Test. Click [Enumerate Bus].

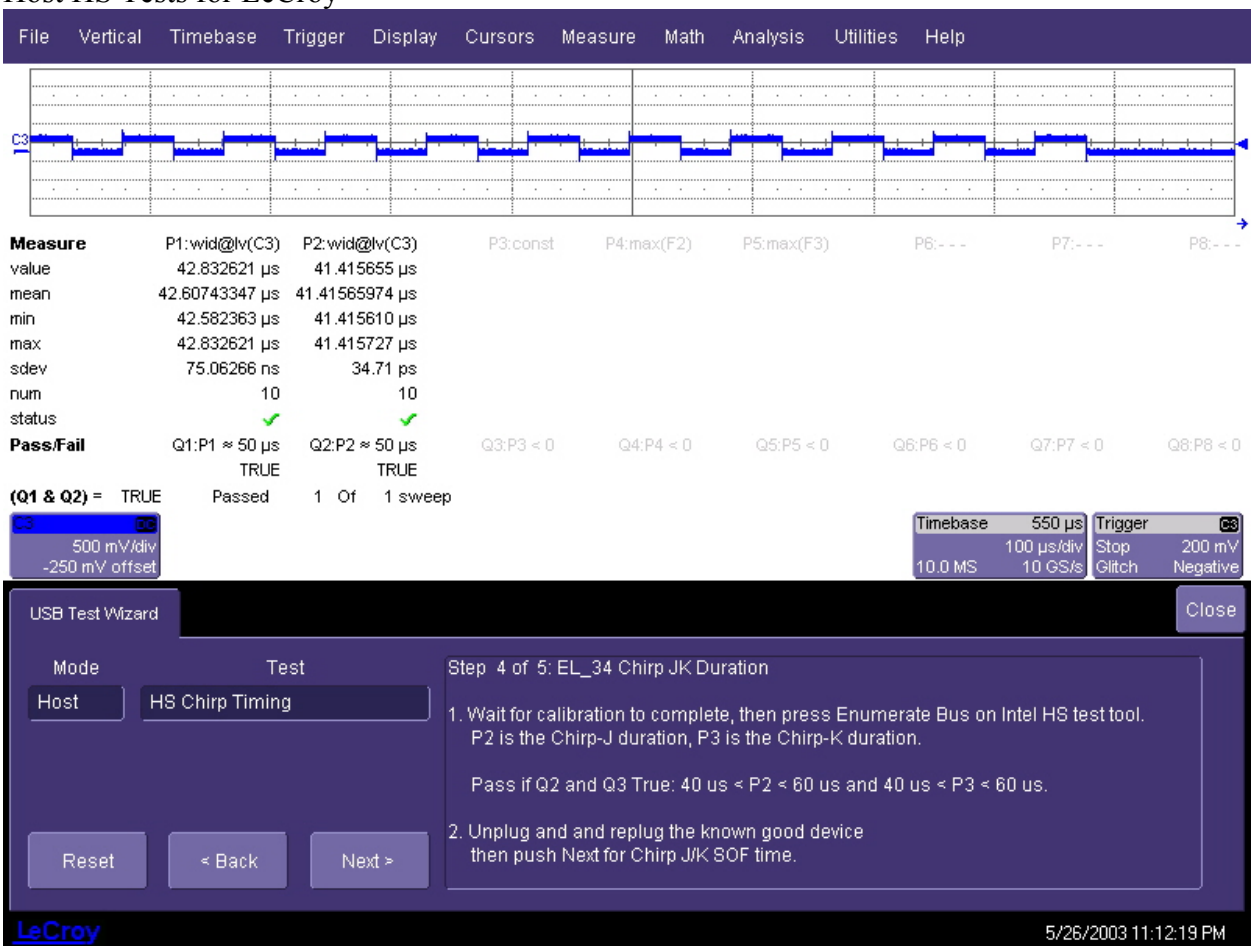
4. Connect the HFP2500 probes from channel 2 to D- of J19 on the test fixture and channel 3 to D+ of J19. Press Next in the test wizard.

5. On the HS test tool, select Enumerate bus and measure the host's Chirp response timing. This is the time between the device's de-assertion of Chirp-K and the start of alternate Chirp-K and Chirp-J sent by the host. The value of P1 indicates the chirp timing. Verify this timing is ≤ 100uS. Record the result in EL_33.



6. Unplug and re-plug the known-good device from the fixture and press Next in the test wizard.

7. Press Enumerate Bus on the HS test tool and measure the durations of the individual Chirp-K and Chirp-J states. These values are shown in P1 and P2 respectively and should be between 40 and 60 us (EL_31). Record the measurement in EL_34.



8. Unplug and re-plug the known good device from the test fixture and press Next in the test wizard.

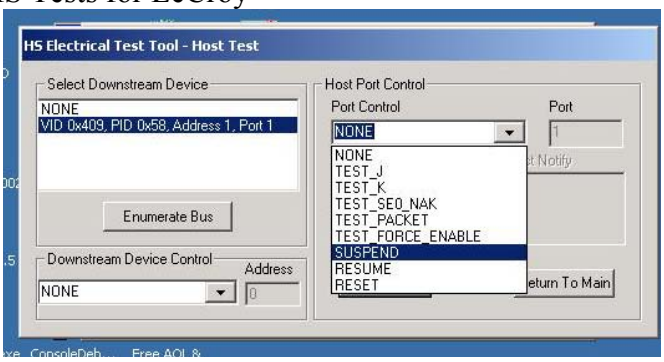
9. Press Enumerate Bus in the HS test tool.

10. The chirp J/K to SOF time is indicated by P1. This value should be between 100 and 500us. Record this value in EL_35.

11. Repeat step 2 through 10 for the remaining down stream facing ports.

4.8 Host Suspend/Resume timing (EL_39, EL_41)

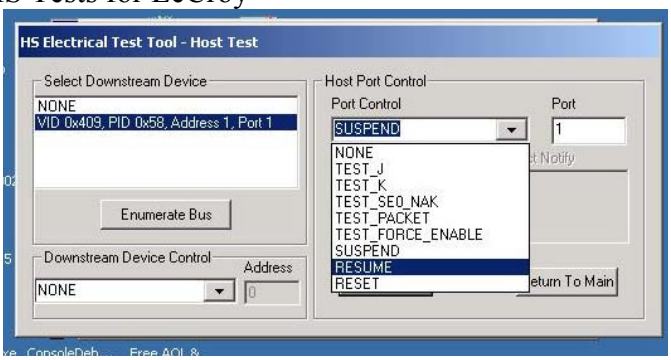
1. Select Host in the Mode control and HS Suspend Resume in the Test control of the USB Test Wizard.
2. Connect the HS port under test to the [INIT] port of the SQ Device section of the test fixture. Attach a known good device to the Device port of the SQ Device section of the test fixture. Apply power to the known-good device. Make sure the TEST/INIT switch is in the INIT position.
3. Start the HS test tool, select Host Controller/System and push Test. Click [Enumerate Bus].
4. Connect the HFP2500 probes from channel 2 to D- of J19 on the test fixture and channel 3 to D+ of J19. Press Next in the test wizard.
5. On the Host Test menu, select SUSPEND from the Port Control drop down menu and enter the port number. Click [EXECUTE] once to place the port into suspend. The captured suspend transition should appear as in the figure below.

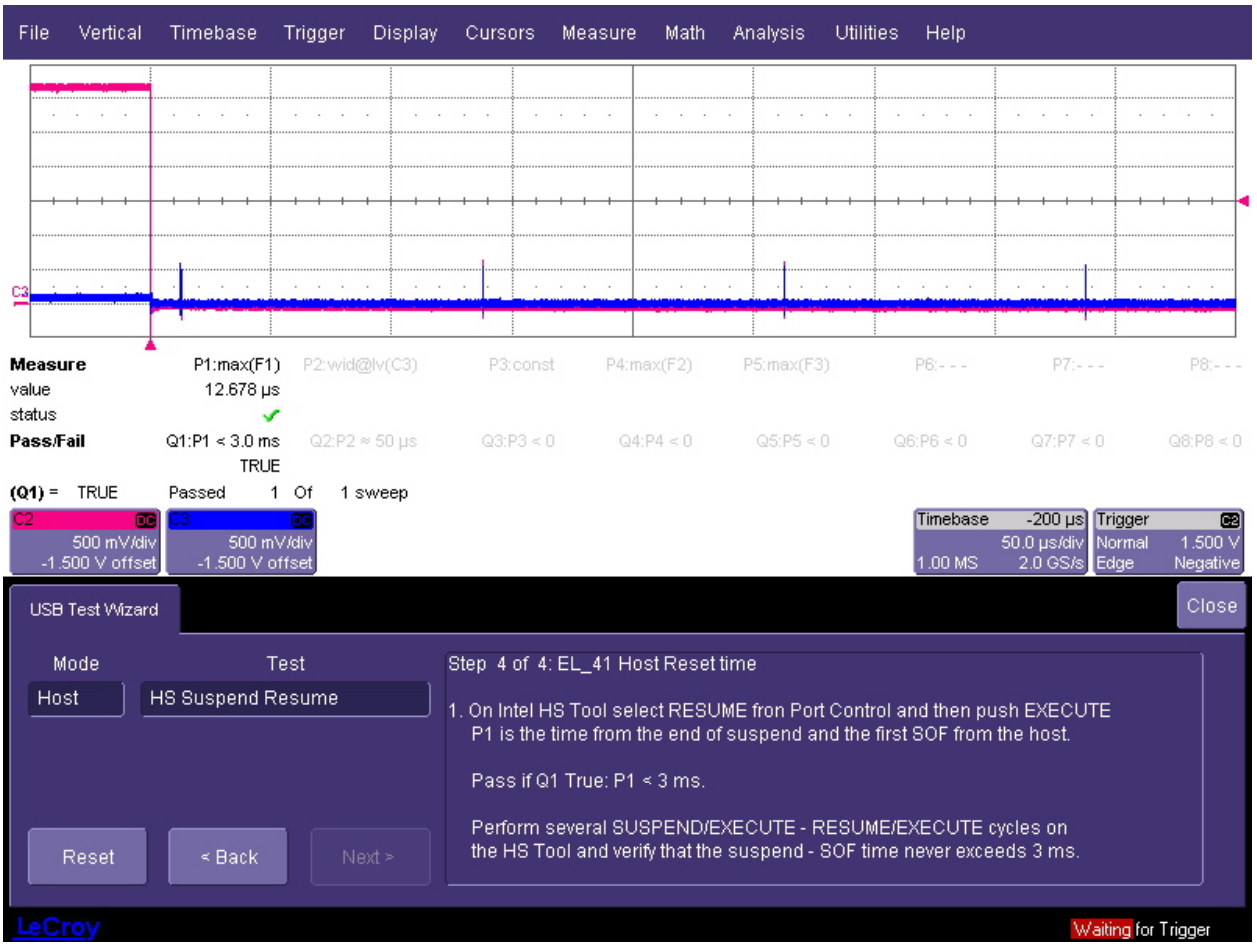


6. The parameter P1 shows the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+ (transition to full speed J-state). This time should be between 3.000mS and 3.125ms. Record the Pass/Fail result in EL_39.

7. Press Next in the test wizard.

8. On the Host Test menu, select RESUME from the Port Control drop down menu and enter the port number. Click [EXECUTE] once to resume the port. The captured suspend transition should appear as in the figure below.





9. The parameter P1 measures the time from the falling edge of D+ to the first SOF issued by the host (EL_41) as shown in the figure above. The value should be less that 3ms. Record the result in EL_41.

Note: Repeat the suspend and resume a number of times and verify the time from the falling edge of D+ to the first SOF issued by the host never exceeds 3ms.

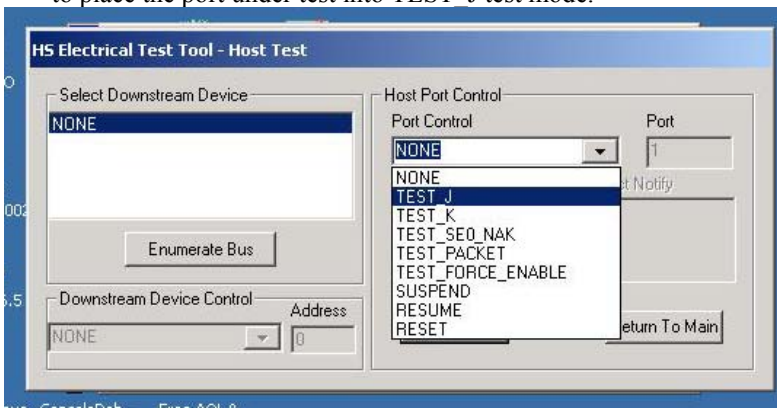
10. Repeat step 4 through 9 for all the remaining ports.

11. Unplug the known-good device from the test fixture. Click [Enumerate Bus] once before proceeding. Remove the FET probes from the test fixture.

4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

1. Attach the dongle of the SQ Host section of the test fixture to the port under test.

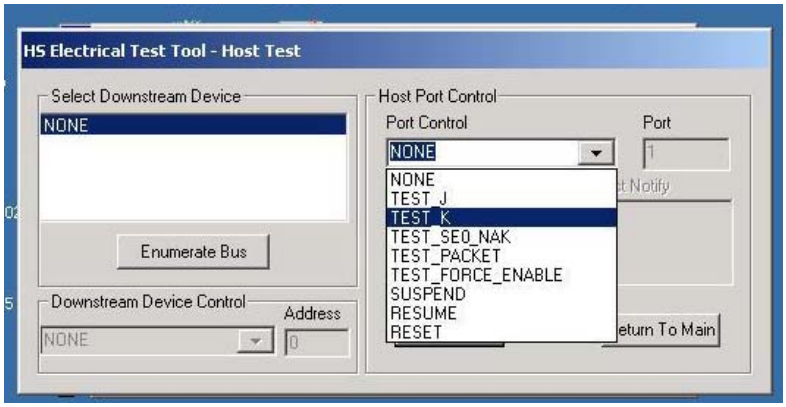
2. Select TEST_J from the Port Control drop down menu. Enter the port number and click [EXECUTE] once to place the port under test into TEST_J test mode.



3. Using a DVM measure the DC voltage on the D+ line at J30 with respect to ground (the outside pins of J30 are ground pins). Record in section EL_8.

4. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.

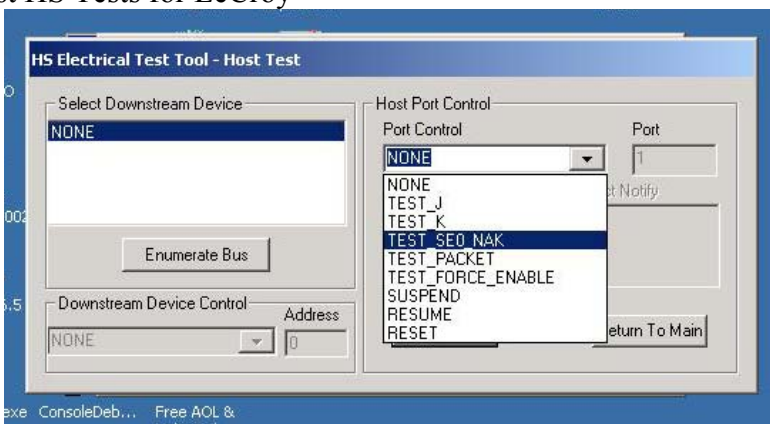
5. On the Host Test menu, select TEST_K from the Port Control drop down menu. Enter the port number and click [EXECUTE] once to place the port under test into TEST_K test mode.



6. Using a DVM measure the DC voltage on the D- line at J30 with respect to ground (the outside pins of J30 are ground pins). Record in section EL_8.

7. Using a DVM measure the DC voltage on the D+ line at J30 with respect to ground. Record in section EL_8.

8. On the Host Test menu, select TEST_SE0_NAK from the Port Control drop down menu. Enter the port number and click [EXECUTE] once to place the port under test into TEST_SE0_NAK test mode.



9. Using a DVM measure the DC voltage on the D+ line at J30 with respect to ground (the outside pins of J30 are ground pins). Record in section EL_9.

10. Using a DVM measure the DC voltage on the D- line at J30 with respect to ground (the outside pins of J30 are ground pins). Record in section EL_9.

11. Repeat step 1 through 10 for the remaining ports.

Appendix A

A.4 Host High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2Vendor and Product Information

Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.

Test Date

Vendor Name

Vendor Complete Address

Vendor Phone Number

Vendor Contact, Title

Test ID Number

Product Name

Product Model and Revision

USB Silicon Vendor Name

USB Silicon Model

USB Silicon Part Marking

USB Silicon Stepping

Tested By

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Downstream Ports					Comments
	P1	P2	P3	P4	P5	

Host HS Tests for LeCroy

LS SQ						
FS SQ						
Drop/ Droop						
Interop						

P = PASS

F = FAIL

N/A = Not applicable

A.4.4 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ±0.05%.

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:
□ Pass
□ Fail
□ N/A
Comments:

EL_3 A USB 2.0 downstream facing port must meet Template 1 transform waveform requirements measured at TP2 (each host downstream port).

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall Result:
□Pass
□ Fail
□ N/A
Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

□Pass
□ Fail
□ N/A
Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

□ N/A
Comments:

A.4.5 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification,* Section 8.2.

SOF SYNC field
□ Pass
□ Fail
□ N/A
Comment:

Data Packet SYNC field
□ Pass
□ Fail
□ N/A
Comment:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (Note, that a longer EOP is waiverable)

Reference documents: *USB 2.0 Specification,* Section 7.1.13.2

- □ Pass
- □ Fail
- □ N/A

Comment:

EL_23 Hosts transmitting two packets in a row must have an inter-packet gap of at least 88 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification,* Section 7.1.18.2.

- □ Pass
- □ Fail
- □ N/A

Comment:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification,* Section 7.1.18.2.

- □ Pass
- □ Fail
- □ N/A

Comment:

EL_55 Hosts transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol.

Reference documents: *USB 2.0 Specification,* Section 7.1.13.2

- □ Pass
- □ Fail
- □ N/A

Comment:

A.4.6Host Disconnect Detect (EL_36, EL_37)

EL_37 A USB 2.0 downstream facing port must not detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is <=525 mV.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.3.

Port	P1	P2	P3	P4	P5

PASS					
FAIL					
NA					

Overall:

□ Pass
□ Fail
□ N/A

Comment:

EL_36 A USB 2.0 downstream facing port must detect the high-speed disconnect state when the amplitude of the differential signal at the downstream facing driver's connector is ≥ 625 mV.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.3.

Port	P1	P2	P3	P4	P5
PASS					
FAIL					
NA					

Overall:

□ Pass
□ Fail
□ N/A

Comment:

A.4.7 Host CHIRP Timing (EL_33, EL_34, EL_35)

EL_33 Downstream ports start sending and alternating sequence of Chirp K's and Chirp J's within 100us after the device Chirp K stops.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□ Pass
□ Fail
□ N/A

Comment:

EL_34 Downstream port Chirp K and Chirp J durations must be between 40us and 60us duration.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□ Pass

- □ Fail
- □ N/A

Comment:

EL_35 Downstream ports begin sending SOFs within 500us and not sooner than l00us from transmission of the last Chirp (J or K).

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

- □ Pass
- □ Fail
- □ N/A

Comment:

A.4.8 Host Suspend/Resume timing (EL_39, EL_41)

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.6.

- □ Pass
- □ Fail
- □ N/A

Comment:

EL_41 After resuming a port, the host must begin sending SOFs within 3ms of the start of the idle state.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.7.

- □ Pass
- □ Fail
- □ N/A

Comment:

A.4.9 Host Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification,* Section 7.1.1.3.

Host HS Tests for LeCroy

Port	1		2		3		4		5	
Test	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
TEST_J										
TEST_K										

- □ Pass
- □ Fail
- □ N/A

Comment:

EL_9 When either D+ and D- are not being driven, the output voltage must be OV ±10 mV when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification,* Section 7.1.1.3.

Port	1		2		3		4		5	
Signal	D+	D-	D+	D-	D+	D-	D+	D-	D+	D-
Measure WRT Ground (mV)										

- □ Pass
- □ Fail
- □ N/A

Comment: