Universal Serial Bus Implementers Forum Device High-speed Electrical Test Procedure For LeCroy Revision 1.0 Dec 2, 2003

Revision History

Rev	Date	Filename	Comments
0.9 (Beta)	May-23-2003	Device HS Test for lecroy.DOC	Primary version of High Speed Test Procedure adapted to lecroy test equipment based on the test procedure created by USB-IF (version 0.9)
1.0	December-3-2003	Lecroy device hs test rev1.doc	Reviewed and approved by USB-IF

Please send comments via electronic mail to techsup©usb.org

USB-IF High-speed Electrical Test Procedure

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I Introduction

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of

peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

3 Equipment Required

- Digital Storage Oscilloscope:
  - LeCroy Wavemaster 8300, 8500, 8600, SDA3000, 50000, 6000 or WavePro7300
    - LeCroy D300 or equivalent differential probe, qty = 1
    - LeCroy active probe HFP2500, qty = 2
- 3 1/2 Digital Multimeter – Agilent 972A or equivalent
    - Mini-clip DMM lead - one each of black and red color
- Digital Signal Generator (either instrument can be used)
    - 81130A Pulse/Pattern Generator (Agilent)

      o The DSG consists of an Agilent 81130A Pulse/Pattern Generator with 2 channels of Agilent 81132A (660MHz) option.

      o 6dB attenuator (Agilent 8493C opt 006) – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2

      o 50-ohm coaxial cable with male SMA connectors at both ends, qty = 2
    - DG2040 (Tektronix)

      o 5X attenuator - for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2

      o 50-ohm coaxial cable with male SMA connectors at both ends, qty = 2
- High-speed USB Electrical Test Fixtures

  o Device high-speed signal quality test fixture LeCroy TF-USB, qty = 1
- Miscellaneous Cables
  - o 1M USB cable, qty = 1
  - o 1.5M USB cable, qty = 1
  - o Modular AC power cord, qty = 1
- High-speed USB Test Bed Computer

  This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. The OS on this computer is Windows 2000 Professional. Please refer to the High-speed Electrical Test Setup instruction for steps to configure

this computer.

3.1 Equipment Setup

3.1.1 Digital Sampling Oscilloscope

Before turning on the oscilloscope, attach the differential probe to channel 1. Attach the HFP2500 probes to channels 2 and 3. These probe assignments will be used through out the entire test procedure. Turn on the oscilloscope to allow for 10 minutes of warm up time prior to use.

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be required to establish a common ground reference.

3.1.2 Pulse/Pattern Generator

The pulse/pattern generator is needed to perform the receiver sensitivity test that is structured toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the generator about 15 minutes prior to performing the measurement.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operating Systems

Microsoft Windows 2000 Professional is required on the High-speed Electrical Test Bed Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computerS.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer. The software USBHSET.exe can be downloaded from the UFB-IF web site at www.USB-IF.org and installed on the test bed computer. This same software must also be installed on the oscilloscope running the LeCroy USB2.0 test software.
- Matlab v6.5 release 13 installed on the oscilloscope running the LeCroy USB2.0 test software. This can be obtained from The Mathworks at www.mathworks.com.
- LeCroy USB2.0 (part number USB2)test software for the oscilloscope

4 Test procedure

4.1 Test Record

Section 5 contains the test result entry form for this test procedure. Please make copies of the section 5 for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date
2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the device under test must also pass the following compliance tests applicable to high-speed capable Device:

- Full speed signal quality
- Inrush current
- Interoperability

Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.

4.4 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

Note: Please take care in determining if the device under test incorporates a captive cable, or it has a normal series B or mini-B receptacle. The former requires the signal quality measurement to be made at the far end. The latter requires the measurement to be made at the near end.

1. Select "USB2" from the analysis menu of the oscilloscope. In the USB test wizard, select "device" for the mode and select "HS NE Signal Quality" if the device has a series B or mini-B receptacle or "HS FE Signal Quality" if the device has a captive cable in the "Test" dialog box. Enter the path and file name for the intermediate result file in the "Result File Name" dialog box.

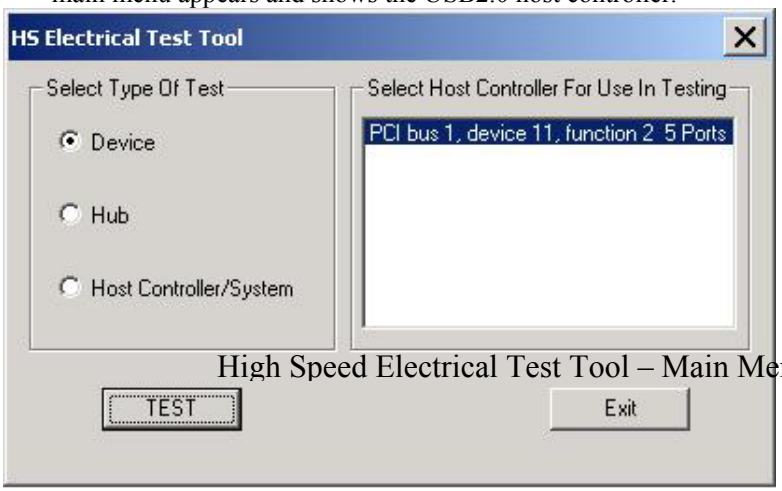
2. Attach the 5V power supply to the USB test fixture and verify that the "power" LED is lit.

4. Verify the green Power LED is lit, and the yellow Test LED is not lit.

5. Connect the [TEST PORT] of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the [INIT PORT] of the test fixture to a high-speed capable port of the Test Bed Computer. Apply power to the device.

6. Attach the differential probe to J19 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

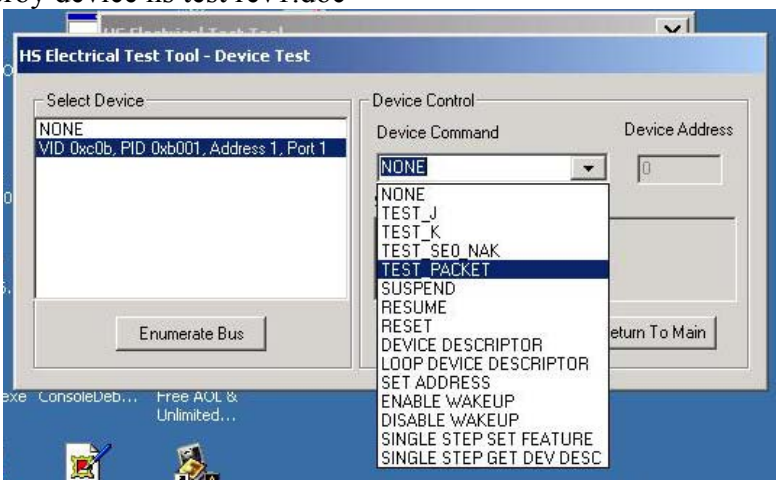
7. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



High Speed Electrical Test Tool – Main Menu

8. Select Device and click the [TEST] button to enter the HS Electrical Test Tool Device Test menu. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

9. Select TEST_PACKET from the Device Command drop down menu and click [EXECUTE]. This forces the device under test to continuously transmit test packets.



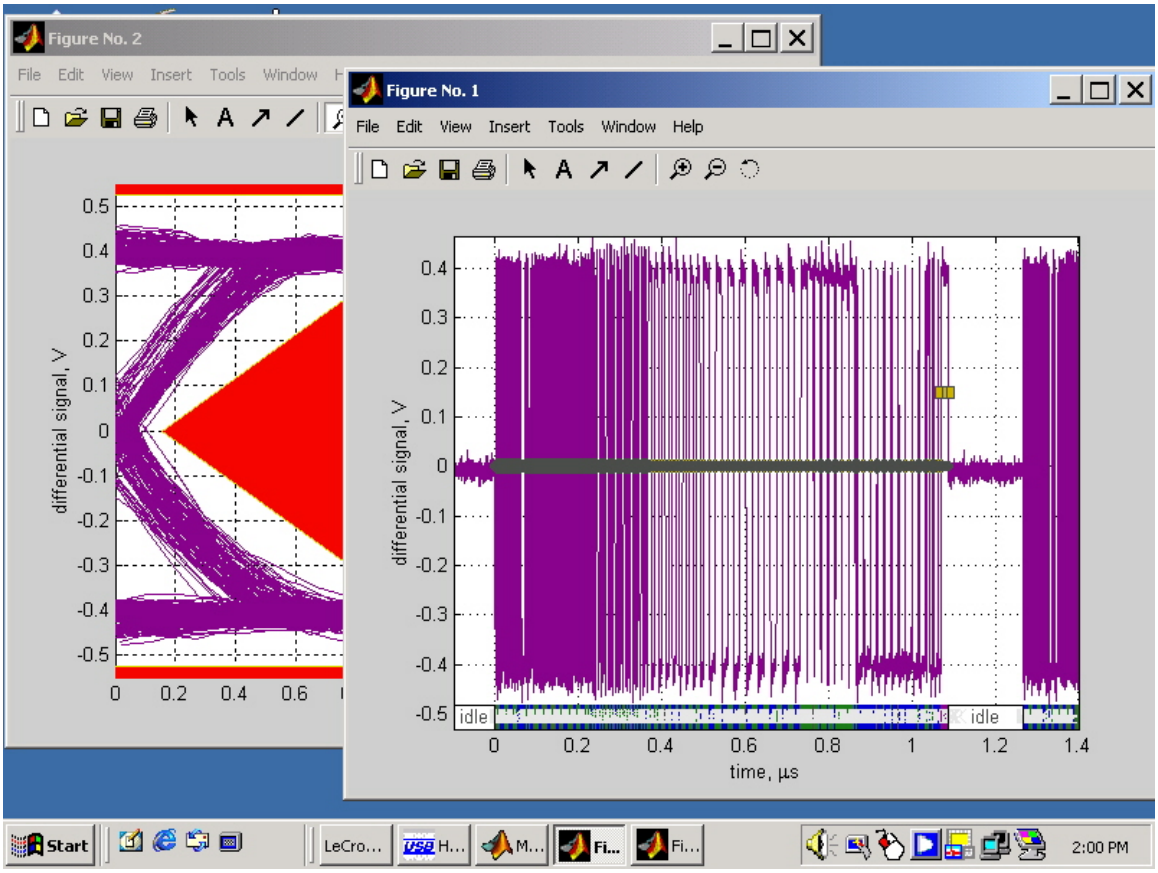
10. Place the INIT/Test Switch on the fixture in the TEST position. Verify the yellow TEST LED is lit.

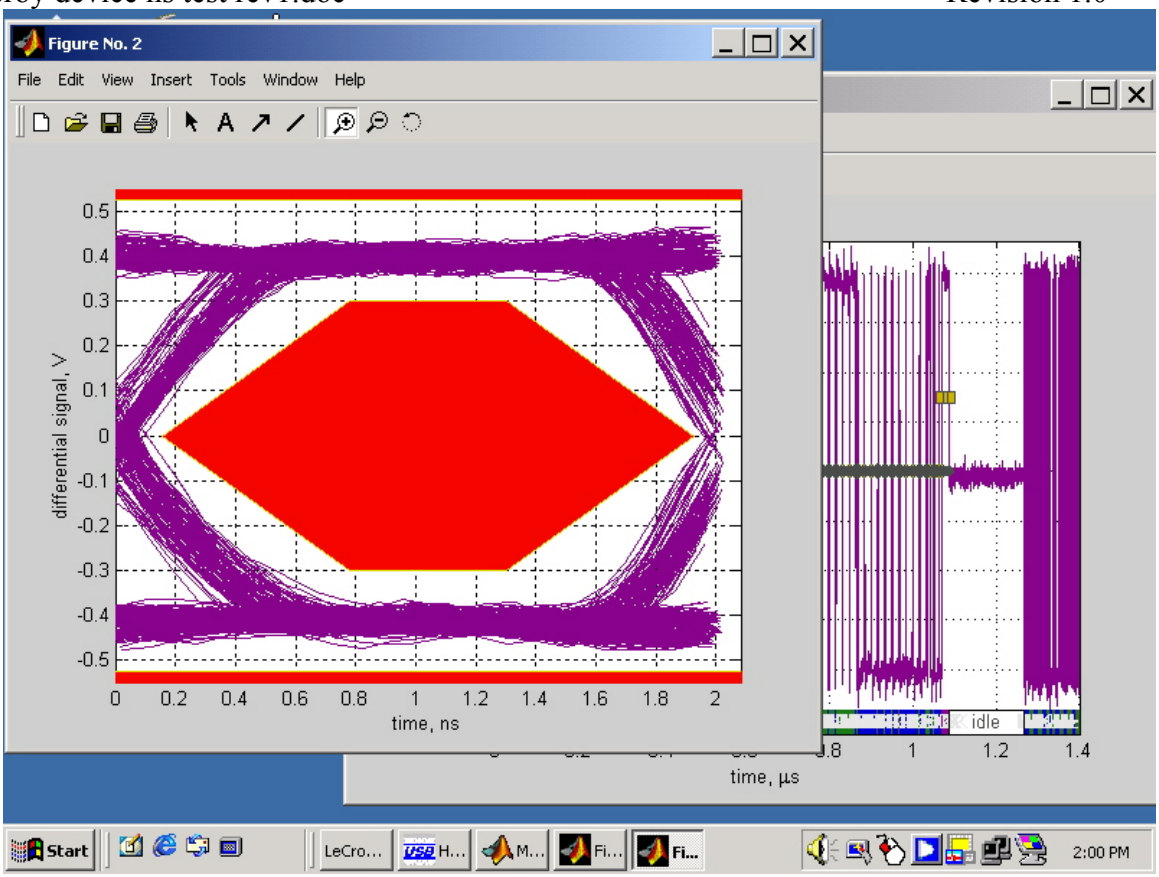
11. using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the cursors so that they are on either side of the test packet on the screen if necessary.

Test packet from device showing cursor placement

12. Enter a descriptive file name in the [Result File Name] dialog box. Note that the default directory is D:\Applications\USB2\Results and the file name has the extension *.tsv which is the intermediate result file for the MatLab scripts. The same file name (with a .HTM extension) is used for the HTML report file.

13. Press the [Next] key in the LeCroy USB 2.0 test wizard. The MatLab analysis script will be invoked to measure the signal quality. The following two plots will appear on the Windows desktop:





14. The results displayed are also recorded to an HTML report located in the directory specified in the "Data Path" control in the test wizard (D:\Applications\USB2\Results by default). Open this file and verify the Signal eye, EOP Width, and Signaling Rate all pass.

Note: if there is any irregularities in the captured waveform such as an incorrect EOP width, the Matlab plots shown above will not be displayed and the HML report will not be generated. Check the probe connections to make sure there are no problems.

20. Record the test result in EL_2, EL_4 or EL_5, and EL_6 and EL_7. Save all files created during the tests

Note: EL_4 and EL_5 requirements are mutually exclusive. If EL_4 is tested then EL_5 is not applicable, and vice versa.

21. Return the INIT/Test switch of the test fixture back to the Normal position and verify the yellow TEST LED is not lit. Cycle power on the device in preparation for subsequent tests.

4.5 Device Packet Parameters (EL_21, EL_22, EL_25)

1. Connect the [INIT PORT] of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.

2. Connect the Device Signal Quality test fixture [TEST PORT] into the B receptacle of the upstream facing

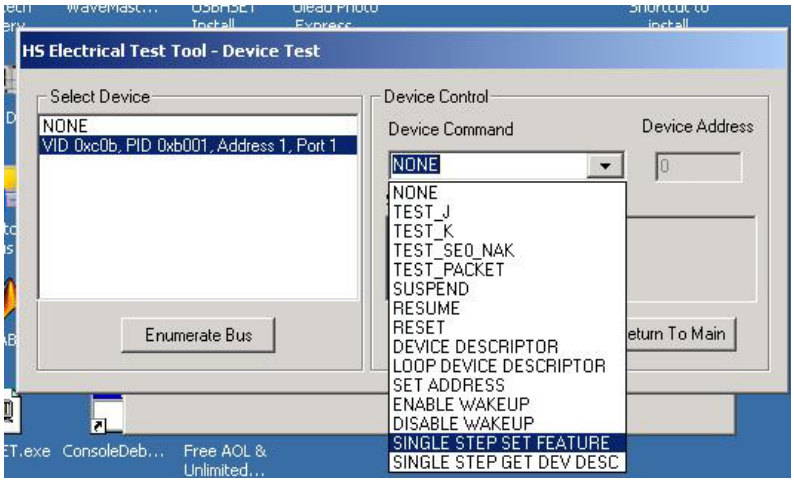
port under test of the device. Make sure that the INIT/Test switch on the fixture is in the INIT position. Verify that the device enumerates properly by selecting “enumerate bus” on the USB-IF HS test tool.

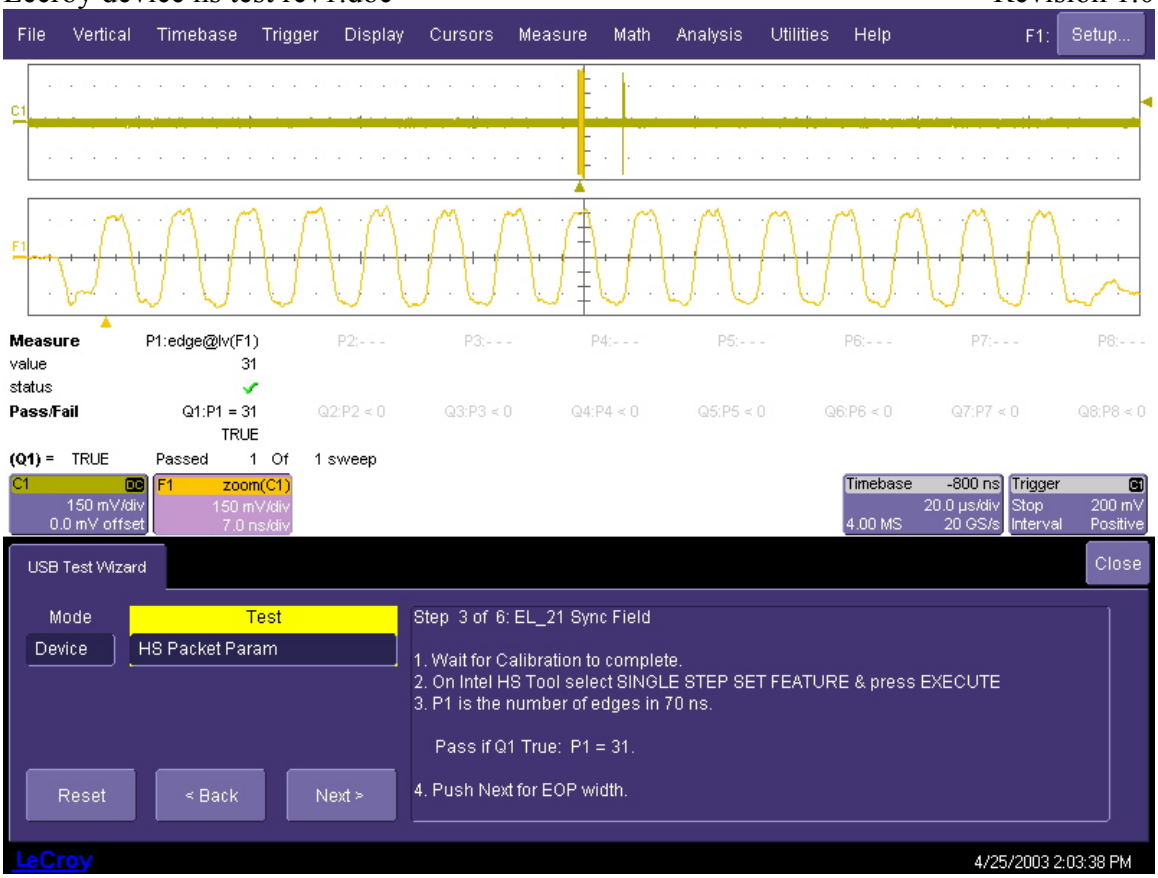
Note: The use of the Device High-speed Signal Quality test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the differential probe to J19 on the fixture. Ensure the + polarity on the probe lines up with the D+ on the fixture.

4. If necessary, wait for calibration to complete in the oscilloscope and press the “Next” button on the LeCroy USB 2.0 test wizard.

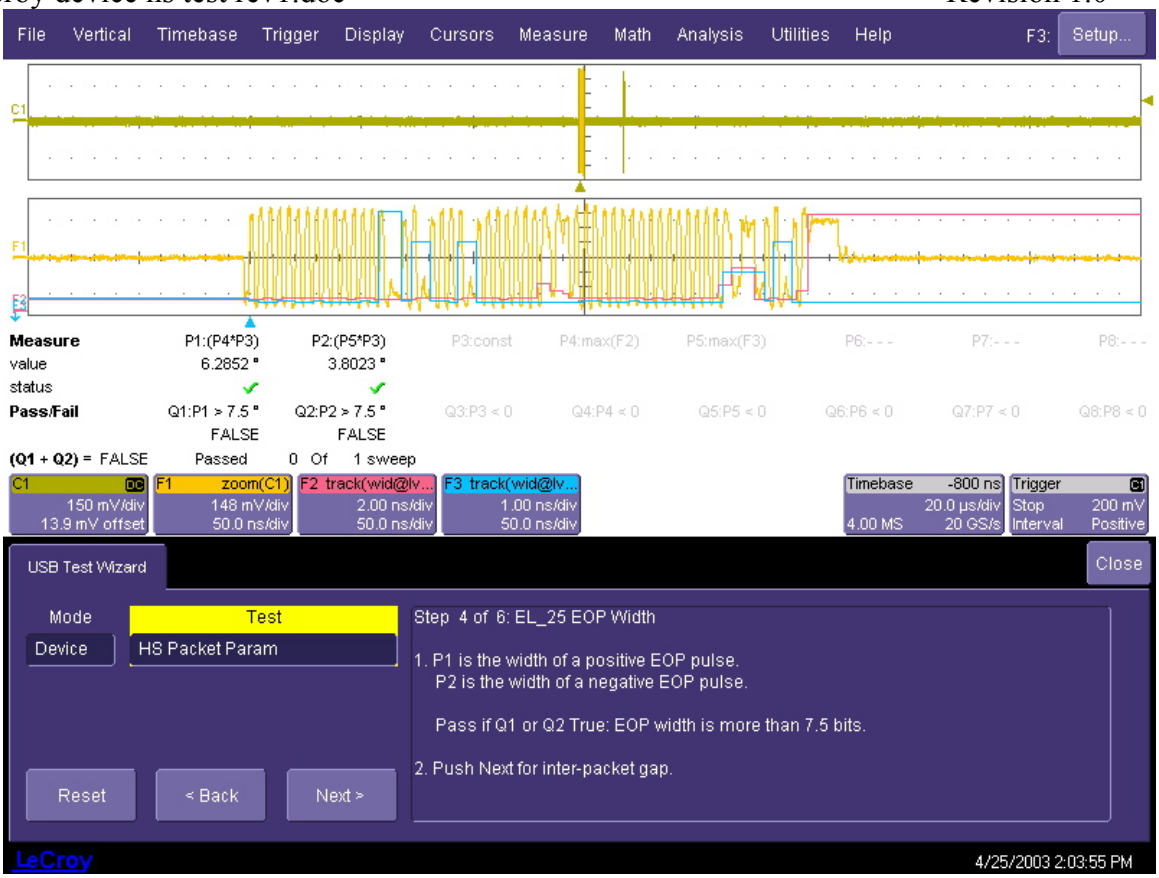
5. On the HS test tool, select SINGLE STEP SET FEATURE and press EXEXCUTE. The oscilloscope display will show 3 packets in the upper display and the sync field in the lower window. There should be 32 pulses in the sync field (31 edges).





10. Press the “Next” button on the LeCroy USB 2.0 test wizard to measure the EOP (End of Packet) width (number of bits) of the third packet on the oscilloscope and verify that it is 8 bits per EL_25.

Note: EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The test passes if either one of these is 8 bits. The oscilloscope display shows both measurements and the pass/fail determination is made on either one being 8 bits.



11. Press the “Next” button on the LeCroy USB 2.0 test wizard to measure to measure the inter-packet gap between the second (from host) and the third (from device in respond to the host’s) packets shown on the oscilloscope. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.
12. Press the “Next” button on the LeCroy USB 2.0 test wizard to measure to measure the second inter packet gap. This value should also be in the range of 8 to 192 bits. Record this value in EL_22.

15. Detach the differential probe from the Device High-Speed Signal Quality test fixture.

4.6 Device CHIRP Timing (EL_28, EL_29, EL_31)

1. Attach the [INIT PORT] of the Device High-speed Signal Quality section of the test fixture into a high-speed capable port of the HS host controller.

2. Connect one HFP2500 active probe to Channel-2 and another to Channel-3. Connect probes to the test fixture at J19 with Ch2 to D- and Ch3 to D+. Connect the probe grounds to the ground pins on either side of J19.

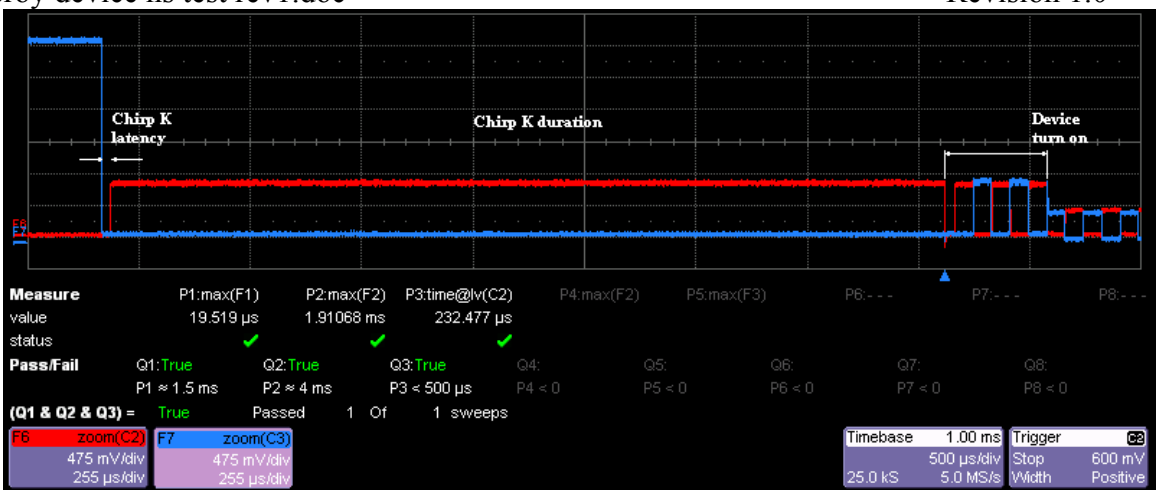
3. Select the Device mode and HS Chirp Timing for the test in the LeCroy USB 2.0 test wizard.

4. Connect the upstream facing port of the device under test into the [TEST PORT] of the test fixture.

5. Click [Enumerate Bus] and then select “Next” in the LeCroy USB 2.0 test wizard.

6. After the oscilloscope performs an automatic calibration, press the “Next” button on the test wizard.

7. Click [Enumerate Bus] in the HS Test Tool to capture the chirp handshake as shown in the figure below.



7. The chirp K latency is shown as P1 and should be between 2.5us and 3ms. Record this value in EL_28. The Chirp K duration is shown in P2 and should be between 1ms and 7ms. Record this value in EL_29. The device termination turn on time is shown in P3 and should be less than 500us. Record this value in EL_31.

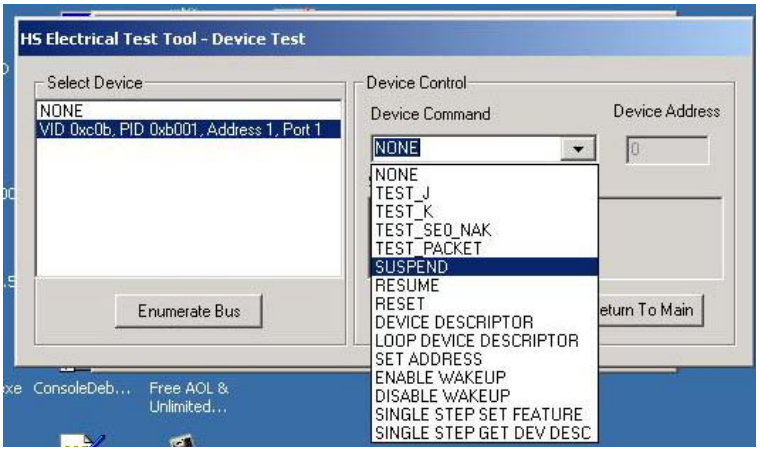
4.7 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

1. Connect the [INIT PORT] of the Device High-speed Signal Quality section of the test fixture into a high-speed capable port of the test bed computer.

2. Connect the device under test into the [TEST PORT] of the test fixture. Click the [Enumerate Bus] button once to enumerate the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

3. Connect one HFP2500 active probe to Channel-2 and another to Channel-3. Connect probes to the test fixture at J19 with Ch2 to D- and Ch3 to D+. Connect the probe grounds to the ground pins on either side of J19.

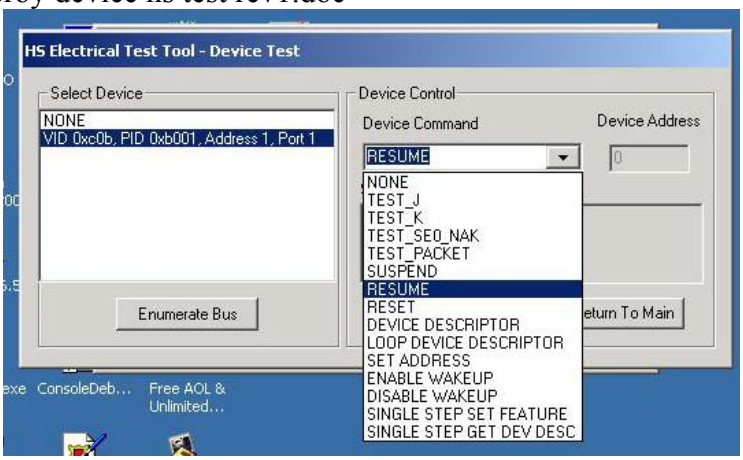
4. On the HS Electrical Test Tool - Device Test menu, select SUSPEND from the Device Command drop down menu. Click [EXECUTE] once to place the device into suspend. The captured suspend transition should appear as in the figure below.



6. The time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+ is shown in P1. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. Verify this time is between 3.000ms and 3.125ms. Record the result in EL_38.

7. Press “Next” in the test wizard to measure the suspend D voltage. The D+ should be at 3.3V nominal. The D- should be less than 0.7V. These values are in P1 and P2. Record the Pass/Fail result in EL_39.

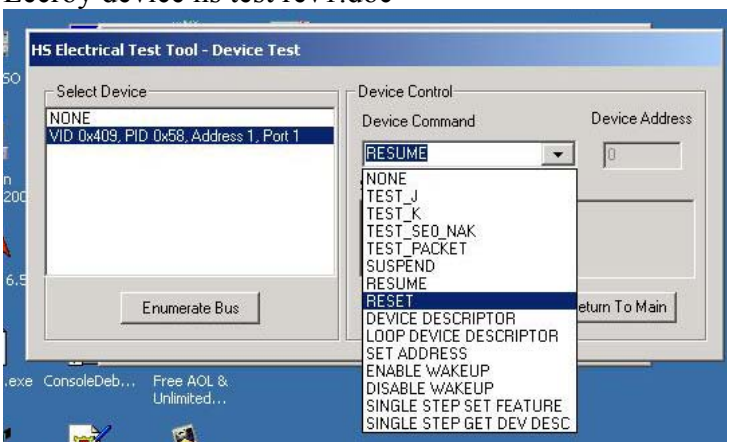
8. Press the “Next” button on the test wizard to move to the RESUME test. On the HS Electrical Test Tool - Device Test menu, select RESUME from the Device Command drop down menu. Click [EXECUTE] once to resume the device from suspend. The captured resume transition should appear as in the figure below.



10. The device should resume the HS operation, which is indicated by the presence of HS SOF packets (with 400mV nominal amplitudes) following the K State driven by the host controller. P1 indicates the resume voltage. Record the Pass/Fail result in EL_40.

11. On the HS test tool, press enumerate bus and then select “Next” in the test wizard.

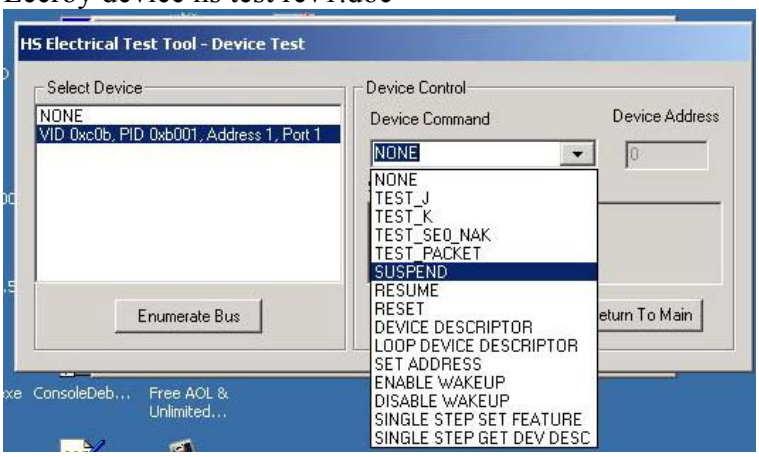
11. On the HS Electrical Test Tool Device Test menu, select RESET from the Device Command drop down menu. Click [EXECUTE] once to reset the device operating in high-speed. The captured reset response should appear as in the figure below.



14. The device should transmit a chirp handshake following the reset. The time between the beginning of the last SOF before the reset and the start of the device chirp-K is indicated by P1. Verify this is between 3.1ms and 6ms. Record the Pass/Fail result in EL_27.

15. Select “Next” on the test wizard to return to suspend.

16. On the HS Electrical Test Tool Device Test menu, select SUSPEND from the Device Command drop down menu. Click [EXECUTE] once to place the device into suspend.



18. Select “Next” in the test wizard. On the HS Electrical Test Tool .Device Test menu, select RESET from the Device Command drop down menu. Click [EXECUTE] once to reset the device in suspend. The captured reset from suspend transition should appear as in the figure below.

19. The device responses to the reset with the Chirp-K. The time between the falling edge of the D+ and the start of the device chirp-K is displayed in P1. Verify this is between 2.5us and 3ms. Record the Pass/Fail result in EL_28.

20. Disconnect the active probe from Ch2 of oscilloscope.

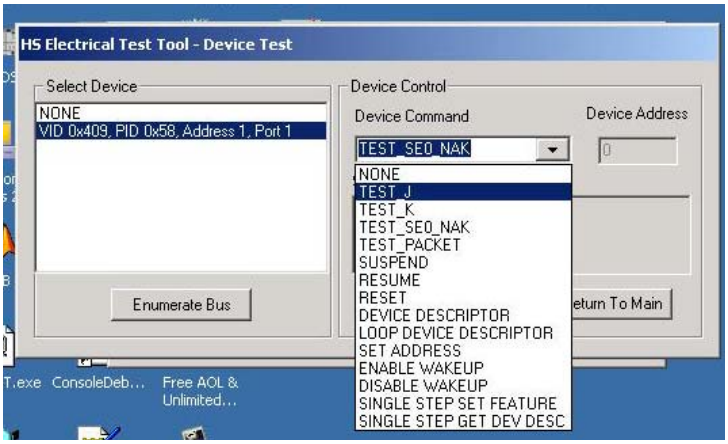
4.8 Device Test J/K, SE0_NAK (EL_8, EL_9)

1. Attach the 5V power supply to J2 of the Device High-speed Signal Quality test fixture.

2. Verify the yellow Power LED (D2) is lit, and the yellow Test LED (D8) is off.

3. Connect the [TEST PORT] of the Device High-speed Signal Quality section of the test fixture into the upstream facing port of the device under test. Connect the [INIT PORT] of the test fixture to a high-speed capable port of the Test Bed Computer. Click the [Enumerate Bus] button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

4. On the HS Electrical Test Tool - Device Test menu, select TESTJ from the Device Command drop down menu. Click [EXECUTE] once to place the device into TESTJ test mode.

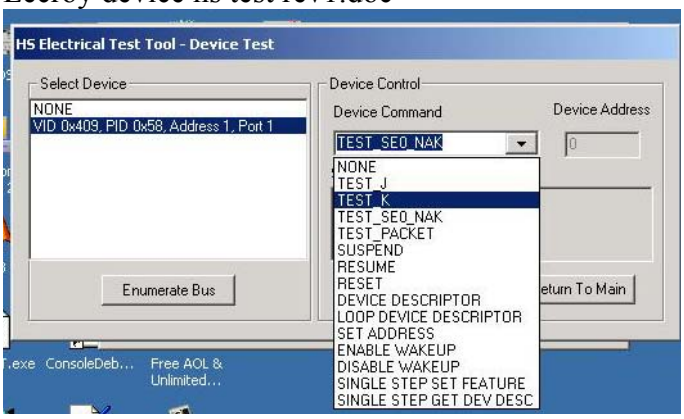


S. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J19 with respect to ground. Record in section EL_8.

6. Using a DVM measure the DC voltage on the D- line at J19 with respect to ground. Record in section EL_8.

7. Return the Test switch to the INIT position. Cycle the device power. Click [Enumerate Bus] once to force enumerate the device. This restores the device to normal operation.

8. On the HS Electrical Test Tool - Device Test menu, select TEST_K from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_K test mode.

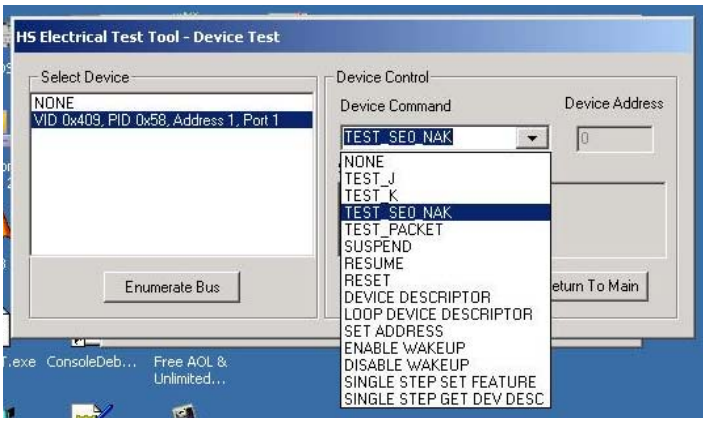


9. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J19 with respect to ground. Record in section EL_8.

10. Using a DVM measure the DC voltage on the D- line at J19 with respect to ground. Record in section EL_8.

11. Return the Test switch to the INIT position. Cycle the device power. Click [Enumerate Bus] once to force enumerate the device. This restores the device to normal operation.

12. On the HS Electrical Test Tool .Device Test menu, select TEST_SEO_NAK from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_SEO_NAK test mode.



13. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J19 with respect to ground. Record in section EL_9.

14. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_9. Return the Test switch to the INIT position.

13. Remove the Device High Speed Signal Quality test fixture. Cycle the device power to prepare it for subsequent tests.

4.9 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

This section tests the sensitivity of the receivers on a device under test. An Agilent 81130A Pulse/Pattern Generator emulates the “IN” command from the hub port to device address 1.

1. Attach the 5V power supply to the test fixture (J2) and verify the yellow Power LED (D2) is lit. Leave the TEST switch at the INIT position. The yellow TEST LED (D8) should be off.

2. Connect the [INIT PORT] of the receiver sensitivity section of the fixture to a high-speed port on the Test Bed Computer. Connect the [TEST PORT] of the receiver sensitivity section of the fixture to the device under test. Click the [Enumerate Bus] button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

3. Two sets of SMA cables are required, each with a 6dB attenuator inserted. Connect the 6dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse/Pattern Generator. Connect OUTPUT 1 to SMA2, and OUTPUT 2 to SMA1 of the Device Receiver Sensitivity test fixture using the SMA cables.

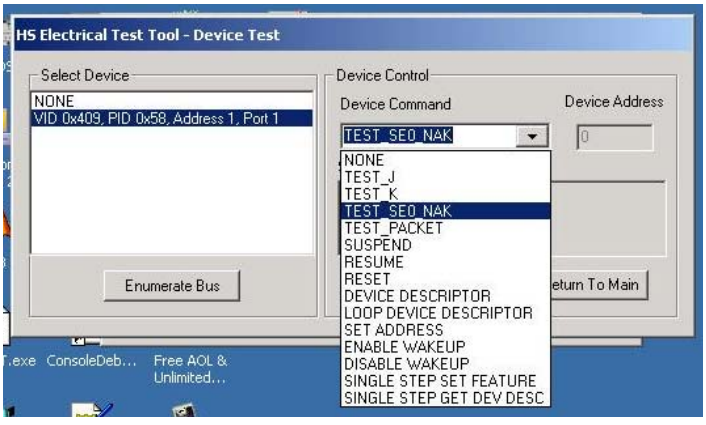
4. On the 81130A, select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen (For creating the setup files used in this section, please refer to Appendix B). Use the cursor and the rotary knob to select the [MIN_ADD1.STO] setup file. Move the cursor to [Perform Operation] and turn the knob to select [Recall]. Then press [ENTER] key to load it. This generates "IN" packets (of compliant amplitude) with a 12-bit SYNC field.

3a (alternate setup for Tektronix DG2040) Two sets of SMA cables are required, each with a 5X attenuators inserted. Connect the 5X attenuators to CH1 and CH0 of DG2040 Data Generator. Connect CH1 to SMA1, and CH2 to SMA2 of the Device Receiver Sensitivity test fixture using the SMA cables.

4a (alternate setup for Tektronix DG2040) On the DG2040, select the EDIT menu. Then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the MIN-ADD1.PDA setup file. Press OK to load it. This generates IN packets (of compliant amplitude) with a 12-bit sync field. Start the data generator with the Start/Stop button.

5. Connect the differential probe from channel 1 of the oscilloscope to J12 of the signal quality section of the test fixture. Recall the HSRcvrSensitivity.lss panel file on the oscilloscope using the File-Recall Setup menu. Use the Browse button in the Recall Panel File dialog box to select the file from the D:\Applications\USB2\Setups directory. Press the Recall Now button to select this setup file.

6. On the HS Electrical Test Tool Device Test menu, select [TEST_SE0_NAK] from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_SE0_NAK test mode.



7. Place the test fixture Test Switch (S1) into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the "IN" packets from the host controller.

8. Verify that all packets from the data generator are NAK'd by the port under test by viewing the waveform on the oscilloscope screen. The NAK packets will appear as slightly higher amplitude bursts just after (to the right) the burst from the pattern generator. Record the Pass/Fail in EL_18.

9. On the data generator select [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen (For creating the setup files used in this section, please refer to Appendix B.). Use the cursor and the rotary knob to select the IN_ADD1.STO setup file. Move the cursor to [Perform Operation] and turn the knob to select [Recall]. Then press [ENTER] key to load it.

9a (for Tektronix DG2040) On the data generator, select the Edit menu, then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the ADD1.PDA setup file. Press OK to load it.

10. Verify that all packets are NAK'd while signaling is at this amplitude.

11. Adjust the output level of each channel as follows:

12. Select the [LEVELS] softkey. If [LEVELS] is not in the menu, press [MORE] key until [LEVELS] comes up. Then move the cursor to the numeric value for [High] voltage value. Adjust the output level with the rotary knob or using the number keys while monitoring the actual level on the oscilloscope. Use the cursor arrow buttons to select the channel to change.

13. Reduce the amplitude of the data generator packets in 20mV steps (on the generator before the attenuator) while monitoring the NAK response from the device on the oscilloscope. The adjustment should be made to both channels such that OUTPUT1 and OUTPUT2 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begins to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.

12a (Tektronix DG2040) select the Setup menu. Then press High from the Level Condition function. Adjustment of the output level is best done with the keypad in 50mV while monitoring the actual level on the oscilloscope. Use the Up and Down arrow buttons to select the channel to change.

13a(Tektronix DG2040) Reduct the signal amplitude in 50mV steps (before the attenuator) while monitoring the NAK response on the oscilloscope. The adjustment should be made on both channels such that CH0 and CH1 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begin to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity level before squelch.

14. Measure the zero to positive peak of the packet from the data generator using the cursors in the lower (zoom) window of the oscilloscope display. Use the upper cursor position knob to position cursor 1 on the zero level of the waveform and the lower cursor control knob to position cursor 2 on the positive peak of the waveform. The cursor should be positioned on the plateaus of the wider pulses to avoid inflating the reading due to overshoots. The difference voltage is indicated in the "zoom(C1)" waveform box at the lower left corner of the oscilloscope screen. Record this value in EL_17.

15. Move cursor 2 to the negative peak of the waveform in the lower window of the oscilloscope screen using the lower cursor control knob again, positioning the cursor on the wider plateaus to avoid overshoots. Read the difference voltage in the waveform information box at the bottom left of the oscilloscope display. Record this value in EL_17. The receiver must continue to NAK packets above +/- 150mV to pass the test. Record Pass/Fail in EL_17.

16. Now further reduce the amplitude of the packet from the data generator in small steps. Still maintaining balance between the outputs until the receiver just ceases to respond with NAK. This is the squelch level of the receiver.

17. Measure the Zero to Positive Peak and Negative Peak of the packet from the data generator using the method described in step 14 and 15. Record the measurement in EL_16. As long as the receiver ceases to NAK the data generator packet below +/- 100mV, it is considered to pass the test. Record PASS/FAIL in EL_16.

Note: With certain devices making an accurate zero-to-peak measurement of the IN packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the IN packet at the test fixture could be considerably higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

A.4 Device High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2 Vendor and Product Information

Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.

Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Pass/Fail	Comments
FS SQ		
Inrush		
Interop		

P = PASS

F = FAIL

N/A = Not applicable

A.4.4 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ±0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.11.

□ Pass
□ Fail
□ N/A
Comments:

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

□ Pass
□ Fail
□ N/A
Comments:

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

□ Pass
□ Fail
□ N/A
Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification,* Section 7.1.2.2.

□ Pass
□ Fail
□ N/A
Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Spec~fication,* Section 7.1.2.2.

□ Pass
□ Fail
□ N/A
Comments:

A.4.5 Device Packet Parameters (EL_21, EL_22, EL_25)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification,* Section 8.2.

Data Packet SYNC field

□ Pass
□ Fail
□ N/A
Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than i92 bit times.

Reference documents: *USB 2.0 Spec~Ication,* Section 7.1.18.2.

□ Pass
□ Fail
□ N/A
Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing.

Reference documents: *USB 2.0 Spec~Ication,* Section 7.1.13.2

□ Pass
□ Fail
□ N/A
Comments:

A.4.6 Device CHIRP Timing (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.Sus and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□Pass
□Fail
□N/A
Comments:

EL_29 The chirp handshake generated by a device must be at least ims and not more than 7ms in duration.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□Pass
□Fail
□N/A
Comments:

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.5.

□Pass
□Fail
□N/A
Comments:

A.4.7 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period on the bus.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.6.

□Pass
□Fail
□N/A
Comments:

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification,* Section 7.1.7.6.

□Pass
□Fail
□N/A
Comments:

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

Note: It is not feasible to measure the device transition back to high-speed operation within two bit time from the end of the resume signaling. The presence of SOF at nominal 400mV amplitude following the resume signaling is sufficient for this test.

Reference documents: USB 2.0 Specification, Section 7.1.7.7.

□Pass
□Fail

□N/A
Comments:

EL_27 Devices must transmit a chirp handshake no sooner than 3.ims and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□Pass
□Fail
□N/A
Comments:

EL_28 Devices must transmit a chirp handshake no sooner than 2.Sus and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification,* Section *7.1.7.5.*

□Pass
□Fail
□N/A
Comments:

A.4.8 Device Test J/K, SEO_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±iO% when terminated with precision 45 Q resistors to ground.

Reference documents: *USB 2.0 Spec~Ication,* Section 7.1.1.3.

Test	D+ Voltage (mV)	D- Voltage (mV)
J		
K		

□Pass
□Fail
□N/A
Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be OV ±10 mV when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification,* Section 7.1.1.3.

	Voltage (mV)
D+	
D	

□Pass
□Fail
□N/A
Comments:

A.4.9 Device Receiver Sensitivity (EL_I6, EL_I 7, EL_I 8)

EL_i8 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

Reference documents: *USB 2.0 Specification,* Section 7.1.

□Pass
□Fail
□N/A
Comments:

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

Note: A waiver may be granted if the receiver does not indicate Squelch at +/-50mV of 150mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification,* Section 7.1.

□Pass
□Fail
□N/A
Comments:

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100 mV differential amplitude.

Note: A waiver may be granted if the receiver indicate Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification,* Section 7.1.

□Pass

□Fail

□N/A

Comments:

B.1 Procedure to create setup files for Agilent 81130A DSG

This section is for creating setup files “IN_ADD1.ST0” and “MIN_ADD1.ST0” for Agilent 81130A DSG.

B.1.1 “IN_ADD1.ST0” setup file

“IN_ADD1.ST0” setup file is for IN TOKEN with 32-bit sync field packet pattern

1.. Pressing [SHIFT] key + [STORE (RECALL)] key and selecting 0 resets 81130A to the default setting.

2. Select [MODE/TRG] softkey and use cursor and knob to set as following.
   CONTINUOUS PATTERN of

   Pulses Out 1:NRZ Out2: NRZ
   PRBS Polynom: 2^7-1
   Trigger Output at Segm1 Start

3. Select [TIMING] softkey. Move Cursor to Per and use rotary knob to change to Freq.
   Set frequency to 480MHz.
4. Select [LEVELS] softkey and use cursor and knob to set as following.

Ch1		Ch2
	Separate Outputs	
High +800mV		High +800mV
Low +0mV		Low +0mV

5. Select [PATTERN] softkey and set as following.

Segment	Length	Loopcnt	Update
1	32	1	
2	32		
3	896		
4	0		

6. Define eachsegment as following.
   Segment 1:

	1	2	3	4	5	6	7	8	9	10
CH1	0	1	0	1	0	1	0	1	0	1

CH2	1	0	1	0	1	0	1	0	1	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	1	0	1	0	1	0	1	0	1
CH2	1	0	1	0	1	0	1	0	1	0

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	0	1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	0	1	1

Segment 2:

	1	2	3	4	5	6	7	8	9	10
CH1	0	1	0	0	1	1	1	0	0	1
CH2	1	0	1	1	0	0	0	1	1	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	1

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	1	1	1	1	0	0	0	0	0	0	0	0
CH2	0	0	0	0	1	1	1	1	1	1	1	1

Segment 3: set all to 0

7. Start the data generator output by pressing [SHIFT] key, then [0] key for OUTPUT 1 and [SHIFT] key then **[+/-]** key for OUTPUT 2.

8. Insert memory card to 81130A. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Move the cursor to [Perform Operation] and turn the knob to select "Store". Then press [ENTER] key. Turn the knob to input file name as IN_ADD1, then press [ENTER] to save to memory card.

B.1.2 "MIN_ADDI.ST0" setup file

"MIN_ADD1.ST0" setup file is for IN TOKEN with 12-bit sync field packet pattern

1. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Use the cursor and the rotary knob to select the IN_ADD1.ST0 setup file. Move the cursor to [Perform Operation] and turn the knob to select "Recall". Then press [ENTER] key to load it.

2. Select [PATTERN] softkey and modify the first segment as following.

Segment 1:

	1	2	3	4	5	6	7	8	9	10
CH1	0	0	0	0	0	0	0	0	0	0
CH2	0	0	0	0	0	0	0	0	0	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	0	0	0	0	0	0	0	0	0
CH2	0	0	0	0	0	0	0	0	0	0

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	0	1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	0	1	1

3 Insert memory card to 81130A. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu,

press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Move the cursor to [Perform Operation] and turn the knob to select “Store”. Then press [ENTER] key. Turn the knob to input file name as “MIN_ADD1”, then press [ENTER] to save to memory card.