

Universal Serial Bus  
Implementers Forum  
Device High-speed  
Electrical Test Procedure for  
Tektronix TDS7254, TDS/CSA7404  
and TDS6604

Revision 1.2

April 1, 2003

## Revision History

| Rev           | Date            | Filename                        | Comments  |
|---------------|-----------------|---------------------------------|---|
| 0.8           | 26-Jun-2001     | Device HS Test.DOC              | Initial draft revision  |
| 0.81          | 12-Jul-01       | Device HS Test.DOC              | Changed el_17 on page 34 to reference Section 7.1.6.2.  |
| 0.9<br>(Beta) | Aug-31-2001     | Device HS Test.DOC              | Switch to integrated Test Tool software in place of SSTD and Test Mode software; remove redundant tests; remove TDR test; Align test assertion section number (EL_xx) to Version 1.00 of USB-IF USB 2.0 Electrical Test Specification |
| 1.0           | Dec-23-2001     | Device HS Test.DOC              | Edit for final release.   |
| 1.1           | August 27 -2002 | Device HS Test.DOC              | Edit to add procedures to accommodate testing using the Tektronix TDS7000 series oscilloscopes and TDSUSB, USB compliance test application  |
| 1.2           | April 1, 2003   | Device HS Test<br>Tektronix.doc | Edit and clean up – for publication   |
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Please send comments via electronic mail to [techsup@usb.org](mailto:techsup@usb.org)

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## 1 Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

This test procedure is an update of the USB-IF Host Electrical High-speed Test Procedure written for the Tektronix TDS694C and the USB-IF MatLab scripts. This updated procedure is written to support Tektronix TDS7404, TDS7254, TDS6604 and TDS6404 running TDSUSB2 Compliance Test Application Software. TDSUSB2 software is used in place of the MatLab scripts and NI GPIB DAQ software.

## 2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Device High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Host High-speed Electrical Test Procedure and Hub High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

## 3 Equipment Required

The commercial test equipment listed here are based on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models used to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

- Digital Phosphor Oscilloscope:
  - Tektronix TDS7404 or 7254 Digital Phosphor Oscilloscope

- Tektronix P6248 or equivalent differential probe, qty = 1
  - Tektronix P6245 FET probes, qty = 2
  - Tektronix TCA to BNC adapters, qty = 3
  - TDS7000 Deskew Fixture, part number: 067-0405-xx, shipped as a standard accessory to the oscilloscope.
- 3 ½ Digital Multimeter – Fluke Model 77 or equivalent
  - Mini-clip DMM lead – one each of black and red color
- Digital Signal Generator
  - Tektronix DG2040 Digital Signal Generator
    - 5x attenuator – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2
    - 50-ohm coaxial cable with female SMA connectors at both ends, qty = 4
- High-speed USB Electrical Test Fixtures
  - Tektronix TDSUSBF test fixture, qty = 1
    - \*5V test fixture power supply, qty = 1
    - \*Female Serial B to female Serial A adaptor, qty = 1
  - \*included with Tektronix TDSUSBF test fixture
- Miscellaneous Cables
  - 1M USB cable, qty = 5
- High-speed USB Test Bed Computer

This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. This OS on this computer is Windows 2000 or XP Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

**Note:** The Tektronix USB compliance test software operates internally to the oscilloscope and automatically configures the oscilloscope settings and so external GPIB control of the oscilloscope is not required.

### 3.1 Equipment Setup

#### 3.1.1 TDS7404 or TDS7254 Digital Phosphor Oscilloscope

Before turning on the oscilloscope. Attach a P6248 differential probe to Channel-1. Attach two P6245 FET probes, one to Channel-2 and one to Channel-3. The probe assignment will be used through out the entire test procedure. Turn on the oscilloscope to allow for 20 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the TDS7404 or 7254 (in the Utility menu) if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

The two single-end FET probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes should be cancelled using the Deskew utility of the TDSUSB software. From the TDSUSB application, select Utilities: Deskew. Follow the procedure in the applications On-Line-Help.

For P6248 differential probes, the following setting will be used through out the entire test procedure:

- Attenuation <÷1>

The use of a Tip Saver accessory on the P6248 probe is highly recommended to prolong probe tip life. Please note that the Tip Saver will wear out after repeated use and start degrading signal quality measurements. Replace the Tip Saver when measurements made without it provide better results.

**Note:** In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be required to establish a common ground reference.

### 3.1.2 DG2040 Digital Signal Generator

The DSG is needed to perform the receiver sensitivity test that is structured toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the DSG about 15 minutes prior to performing the measurement.

## 3.2 Operating Systems, Software, Drivers, and Setup Files

### 3.2.1 Operation Systems

Microsoft Windows 2000 or XP Professional is required on the High-speed Electrical Test Bed Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

## 3.3 Special Purpose Software

- The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.
- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.
- Proprietary EHCI Driver Stack - The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation purposes, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel

proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.

- TDSUSB – Tektronix USB2.0 Compliance Test Software Application

### 3.4 Test Equipment Setup Files

HS\_TDS6K\_7Kscope\_setups.zip – Contain setup files for the Tektronix TDS7404 or TDS7254 DSO (Digital Phosphor Oscilloscope). These setup files augment the TDSUSB Compliance Test Application. These setup files are used for the following tests:

- Packet Parameters (EL\_21, EL\_22, EL\_25)
- Device Suspend/Resume/Reset timing (EL\_27, EL\_28, EL\_38, EL\_39, EL\_40)

This file may be downloaded from [www.tek.com](http://www.tek.com) using the software finder utility.

DG2040.zip – Contain setup files for Tektronix DG2040 DPG (Digital Pattern Generator) and is included with TDSUSB software distribution.

## 4 Test Procedure

### 4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop as applicable) shall be retained for compliance test submission.

### 4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date
2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision



7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

### 4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the device under test must also pass the following compliance tests applicable to high-speed capable Device:

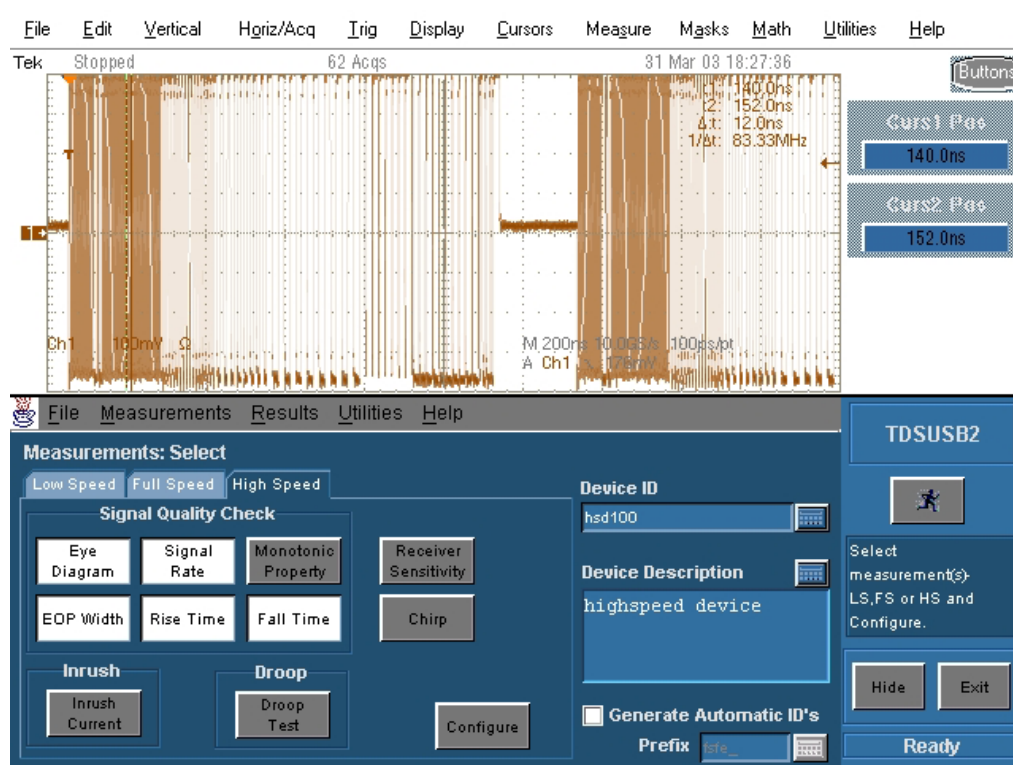
- Full speed signal quality
- Back-drive voltage
- Inrush current
- Interoperability

Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.


### 4.4 Device High-speed Signal Quality (EL\_2, EL\_4, EL\_5, EL\_6, EL\_7)

**Note:** Please take care in determining if the device under test incorporates a captive cable, or it has a normal series B or mini-B receptacle. Captive cable designs require the signal quality measurement to be made at the far end (hsfe). Detachable cable designs require the measurement to be made at the near end (hsne).

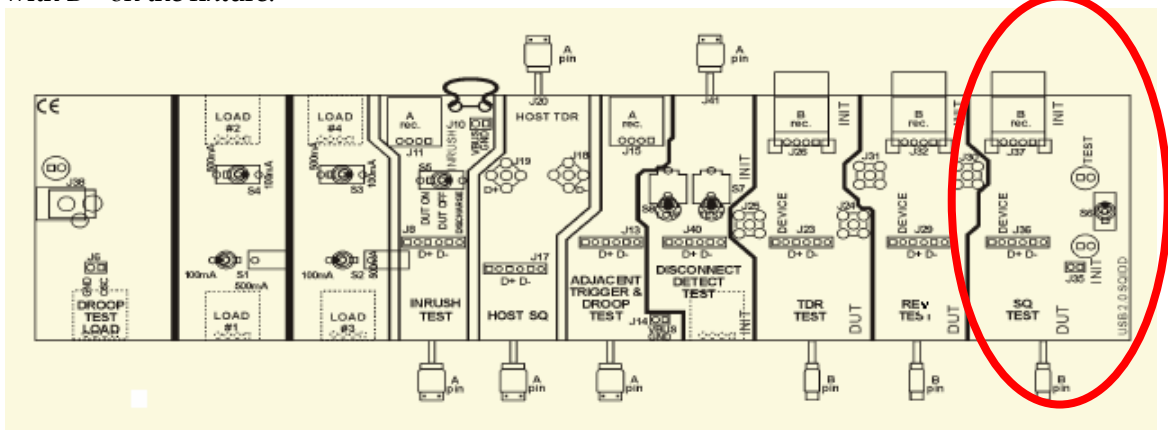
1. Turn on the oscilloscope if you have not already done so. Allow about 20 minutes for warm up.
2. Launch the TDSUSB software application on the TDS7404 or TDS7254 oscilloscope by selecting with a mouse or touch screen, File: Run application: USB2.0 compliance test package.
3. Press the Default Setup button on the oscilloscope front panel.
4. In the applications menu bar select, file: recall default.
5. Within the Measurement select menu of the USB2.0 compliance test application, select the High Speed tab.
6. Within the Signal Quality area of the application, select the High Speed Signal Quality tests: Eye Diagram, Signal Rate, Rise time, Fall Time, and EOP Width.
  - The Monotonic property test is available but not required as it may generate false failures due to slight variations in the signal edge due to high frequency noise and/or scope quantization error.



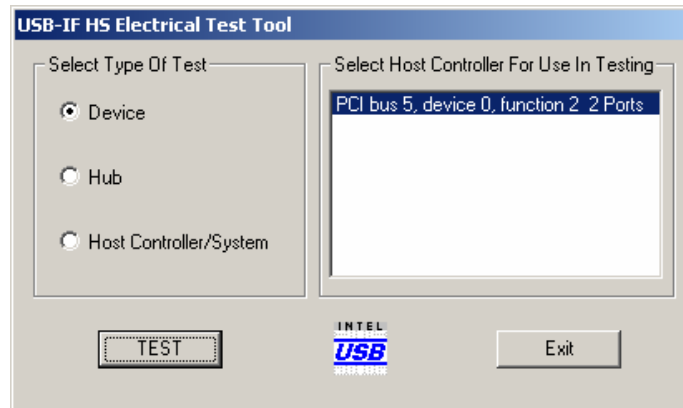
Tektronix TDSUSB Software

7. Enter a device ID (e.g. TIDxxxxxxx USNE.tsv) into the device ID dialog box and a device description into the device description dialog box.
8. Press the Configure button on the application screen. Select upstream and far end for devices with captive cables or near end for devices without a captive cable.
9. Press the  icon. Verify that the scope display is NOT reporting “clipping”. If it is, adjust the vertical amplitude until the “clipping” message does not appear. Do not press OK on the screen until the correct waveform is displayed.
10. Attach the 5V power supply to J38 of the Compliance test fixture.
11. Verify the red Power LED next to J38 and the red Init LED is lit.
12. Connect the short USB cable dongle of the Device SQ segment of the test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the Test Bed Computer. Apply power to the device.

13. Attach the differential probe to J36 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.

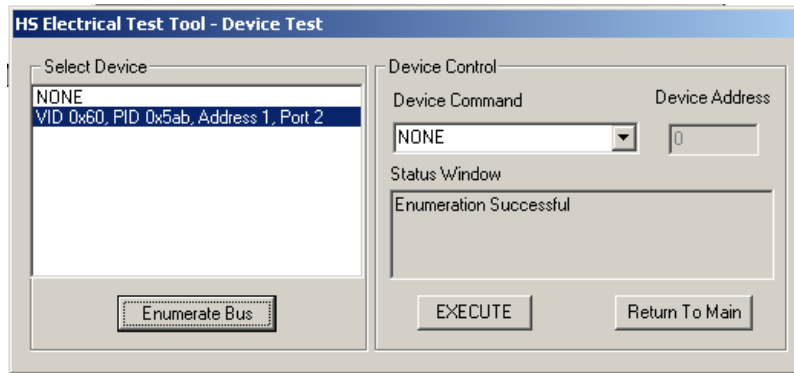


14. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



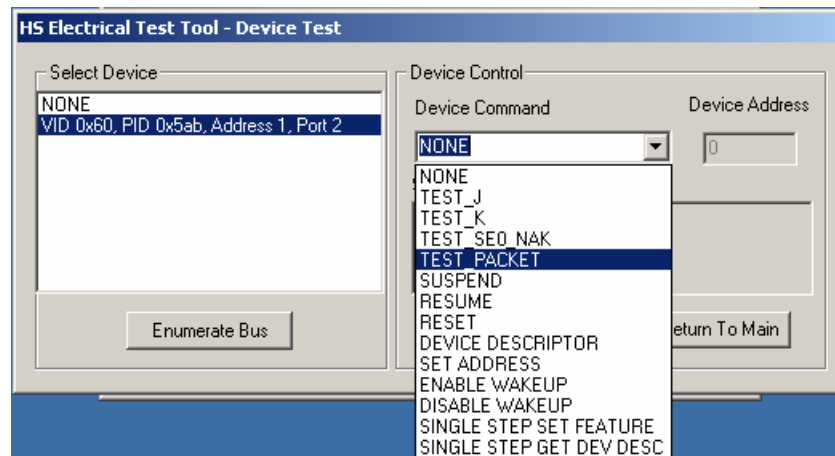
High-speed Electrical Test Tool – Main Menu

15. Select Device and click the TEST button to enter the HS Electrical Test Tool - Device Test menu. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.



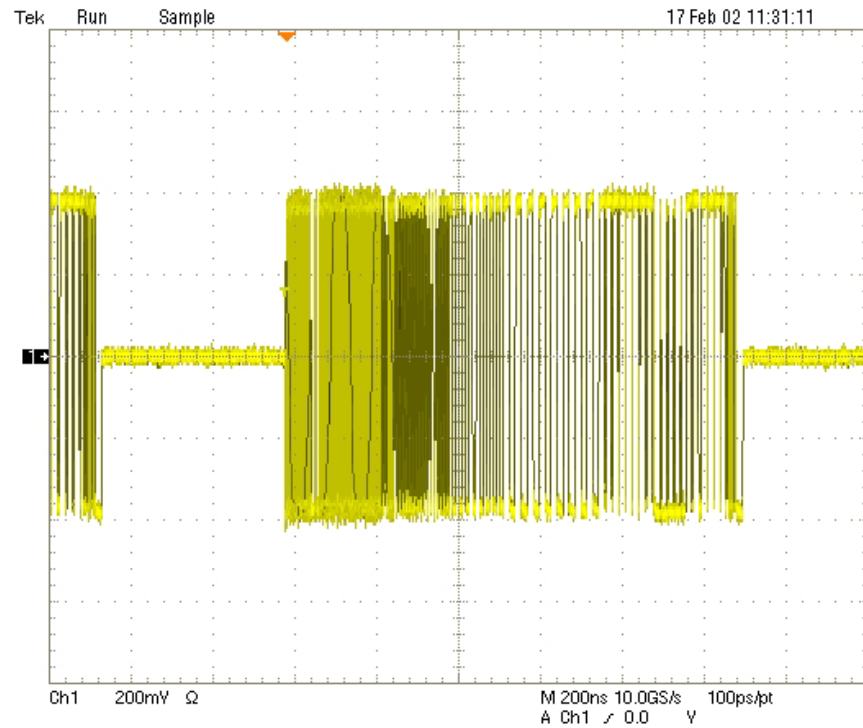
High-speed Electrical Test Tool – Device Test Menu

16. Select TEST\_PACKET from the Device Command drop down menu and click EXECUTE. This forces the device under test to continuously transmit test packets.



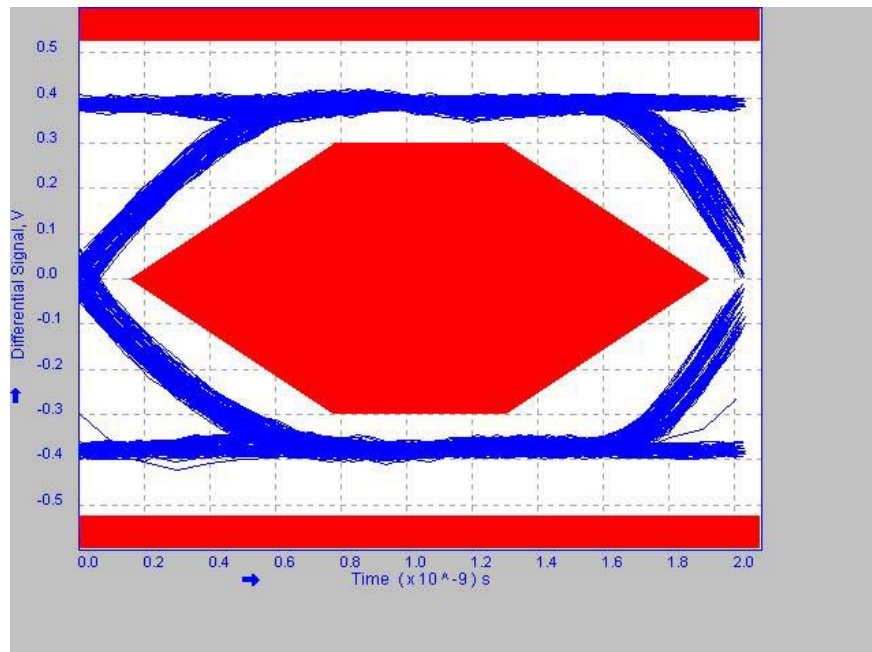
Device Upstream TEST\_PACKET

17. Place the Test Switch (S6) in the TEST position. Verify the red TEST LED is lit.
18. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change to the trigger holdoff.
19. Once the test packet is displayed properly, press OK in the application dialog box.
20. The Tektronix USB application generally triggers and displays the correct test packet without the need to place cursors. Should cursors be required they may be enabled by selecting within the application, File: Preferences: Advanced and clicking the optional Packet Identification by user using Cursors.
21. If cursors measurement is enabled (see step 17), on the oscilloscope place the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure for reference. Press OK on the USB2 application dialog box to begin acquisition and analysis of the test packet.

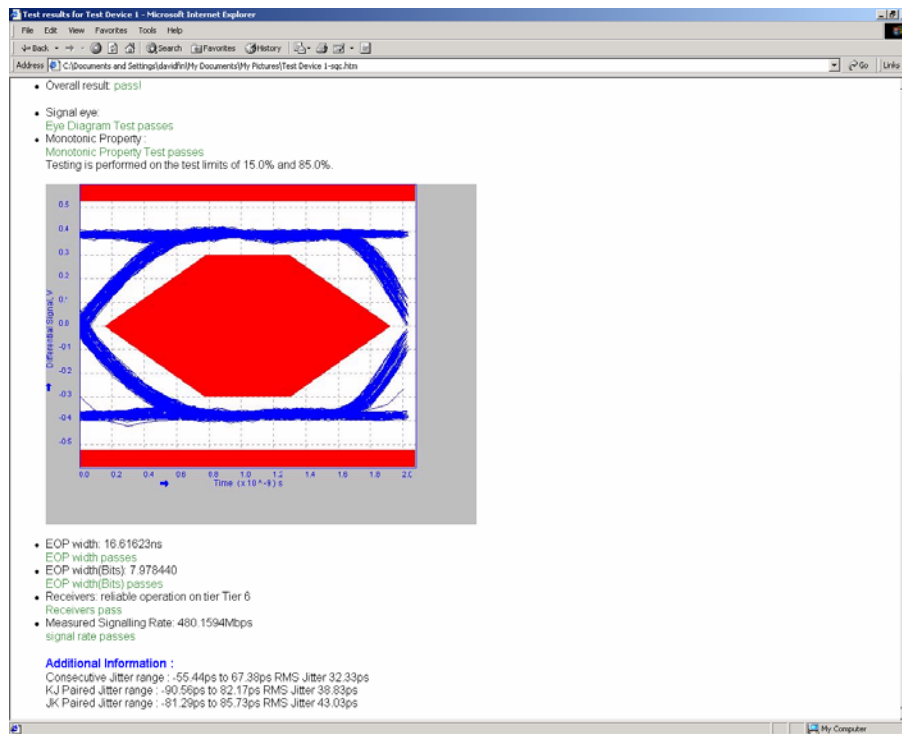


Test Packet from Device

22. Verify the Signal Eye, EOP Width, Rise and Fall time and Signaling Rate all pass. The results displayed on oscilloscope display may also be recorded to an HTML report located on the scope hard drive at the following path: C:\TekApplications\tdsusb2\report\



### High-speed Near End SQ Eye Diagram



### High-speed SQ HTML Report

23. Save all files created during the tests. Record the test result in EL\_2, EL\_4 or EL\_5, and EL\_6 and EL\_7.

**Note:** EL\_4 and EL\_5 requirements are mutually exclusive. If EL\_4 is tested then EL\_5 is not applicable, and vice versa.

24. Return the Test switch (S6) of the test fixture back to the Normal position and verify the Red TEST LED is not lit. Recycle power of the device in preparation for subsequent tests.

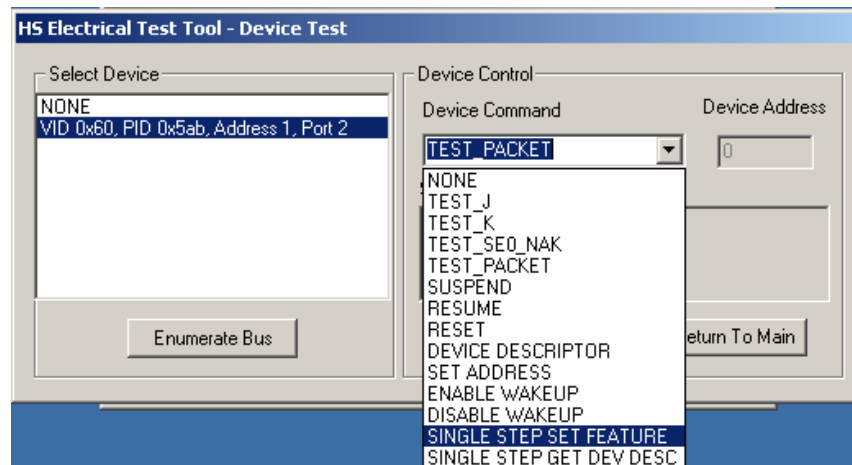
## **4.5 Device Packet Parameters (EL\_21, EL\_22, EL\_25)**

1. Connect the Init port of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.
2. Connect the short USB cable dongle of the Device SQ segment of the test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the Test Bed Computer. Apply power to the device. Verify that the device enumerates properly.

**Note:** The use of the Signal Quality segment of the compliance test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

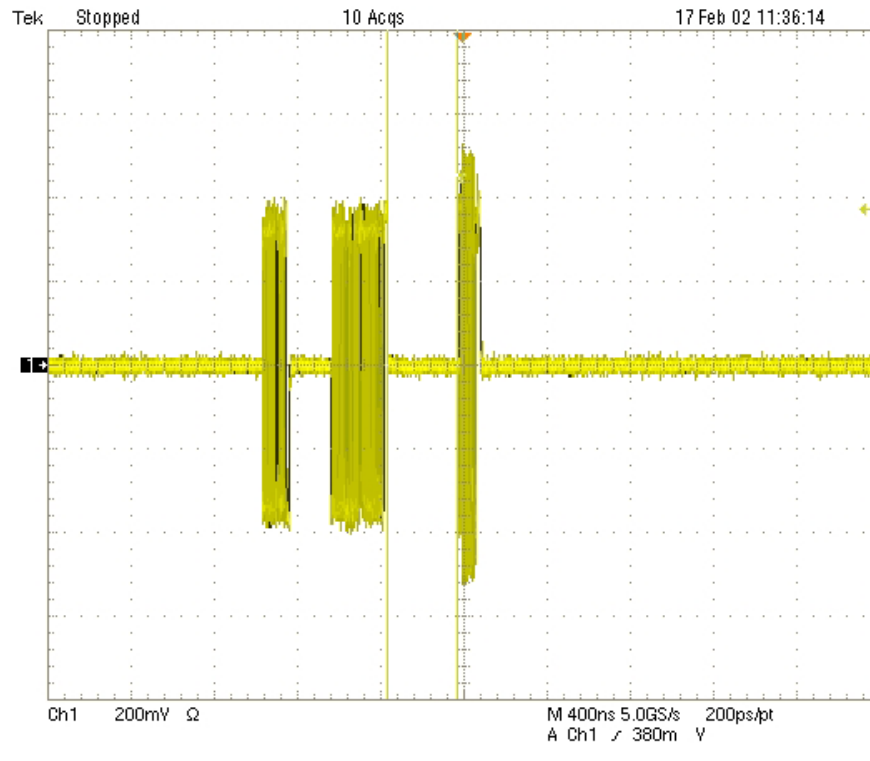
3. Attach the differential probe to J36 on the fixture near the device connector. Ensure the + polarity on the probe lines up with the D+ on the fixture.

4. Recall the PACKPARAM.SET oscilloscope setup.
5. Using the oscilloscope, verify SOFs (Start Of Frame packets) are being transmitted on the port under test. You may need to lower the trigger level to somewhat below 400mV.
6. Now raise the oscilloscope's trigger level slowly just until it does not trigger on the SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the device and the length of cable used on the fixture. Ensure the RUN/STOP of the oscilloscope is set to RUN.
7. In the HS Electrical Test Tool - Device Test menu of the High-speed Electrical Test Tool software. Ensure the device under test is selected (highlighted). Select SINGLE STEP SET FEATURE from the Device Command window and click EXECUTE once.



#### Device Single Step Set Feature

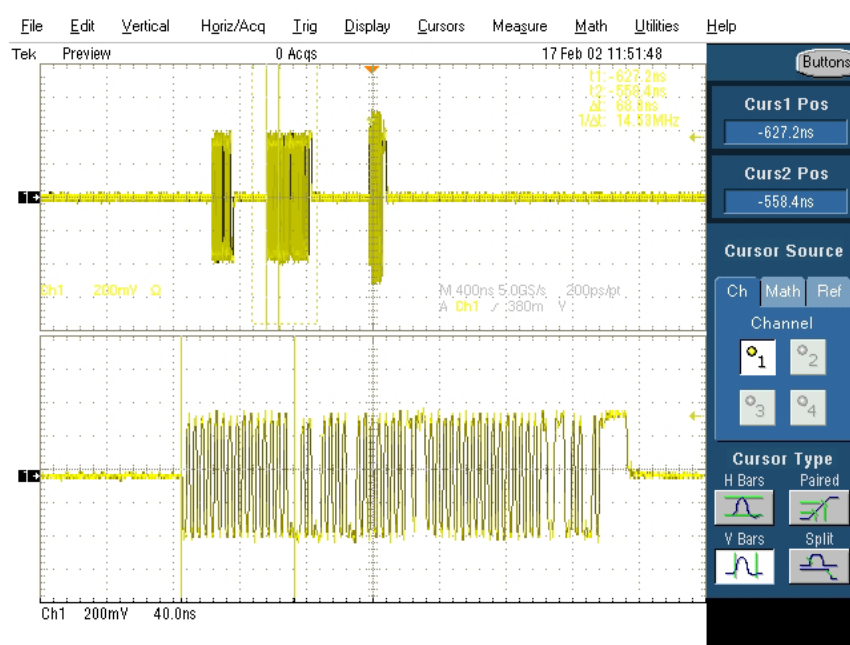
8. The oscilloscope capture should appear as follows. Press STOP on the oscilloscope to pause it from further trigger. If the oscilloscope doesn't trigger on the device traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 7. If you are unable to trigger exclusively on device traffic due to high amplitude SOFs insert a longer USB cable between the DUT and the host or modify the trigger set-up to trigger on the 8 bit EOP of a data packet.



#### Host and Device Packets

9. Use the zoom function of the oscilloscope, measure the sync field length (number of bits) of the third (from device) packet on the oscilloscope and verify that it is 32 bits per EL\_21. Refer to the figure below for reference. Note that Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero). Count both rising and falling edges until the first two consecutive 1's and include the first 1. There must be 32 bits. Record the number in EL\_21.

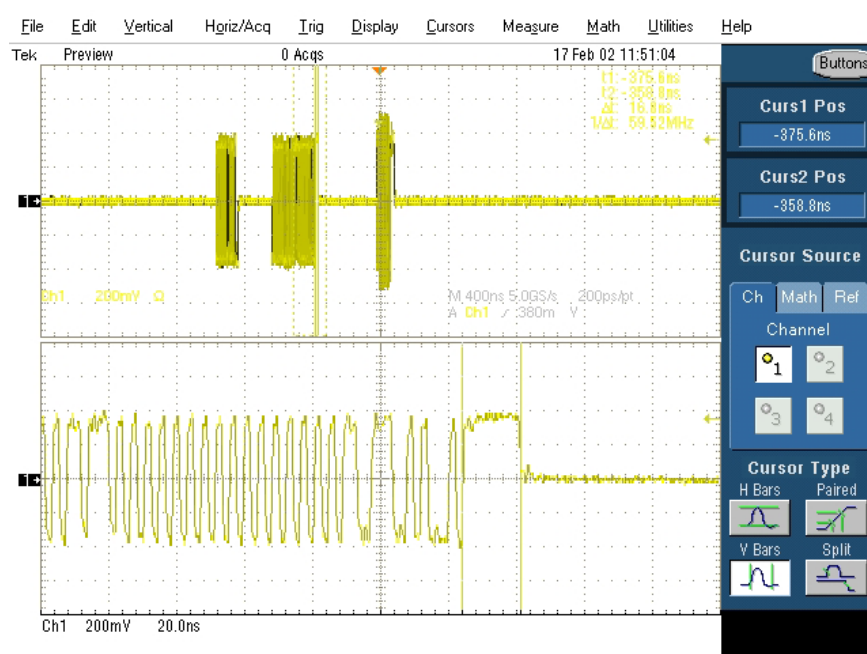




Sync Field - Device Packet

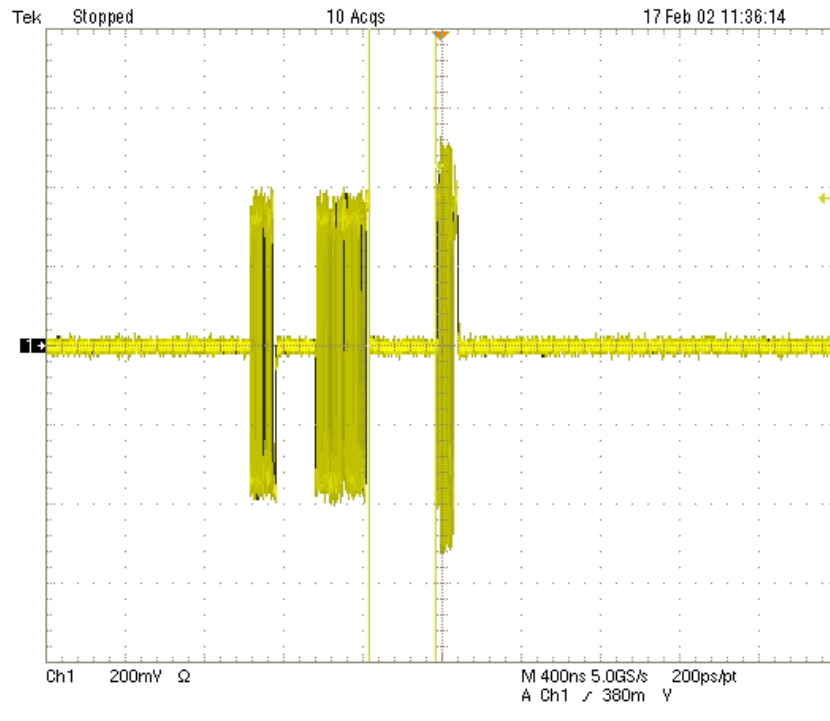
10. Measure the EOP (End of Packet) width (number of bits) of the third packet on the oscilloscope and verify that it is 8 bits per EL\_25. It is advisable to use the cursors to measure the EOP pulse width to determine the number of bits, based on 2.08ns/bit (480Mbps). Record the result in EL\_25.

**Note:** EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The figure below illustrates the appearance of a negative going EOP.



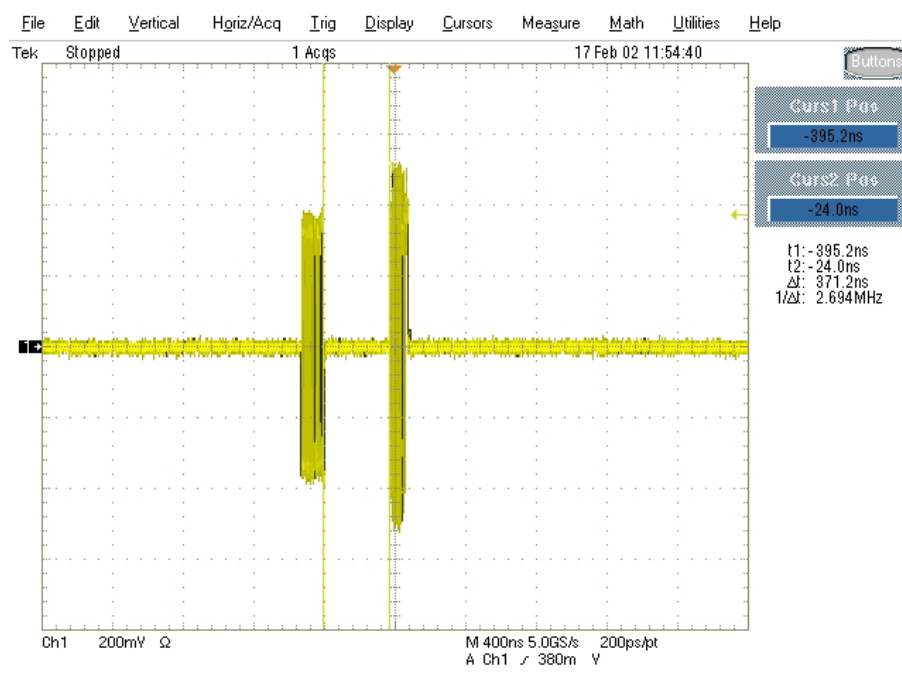
### EOP in Device's Packet

11. Measure the inter-packet gap between the second (from host) and the third (from device in respond to the host's) packets shown on the oscilloscope. The second (of lower amplitude) is from the host and the third (of higher amplitude) is a device's response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL\_22). Record the computed number of bits in EL\_22.



### Device Inter-packet Gap

12. Ensure the oscilloscope is armed. In the HS Electrical Test Tool - Device Test menu, Click the Step button once. This is the second step of the two-step Single Step Set Feature command.
13. The oscilloscope capture should appear as follows. Press STOP on the oscilloscope to pause it from further trigger.

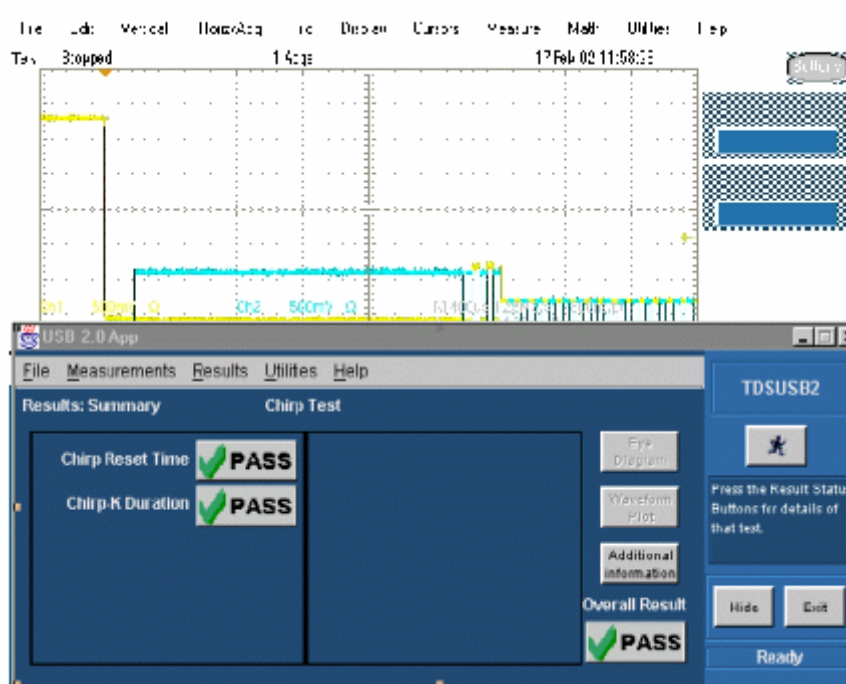


#### Single Step Set Feature – Second Step

14. Measure the inter-packet gap between the first (from host) and the second (from device in respond to the host's) packets shown on the oscilloscope. The first (of lower amplitude) is from the host and the second (of higher amplitude) is a device's response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL\_22). Record the computed number of bits in EL\_22.
15. Detach the differential probe from the Device High-Speed Signal Quality test fixture.

### **4.6 Device CHIRP Timing (EL\_28, EL\_29, EL\_31)**

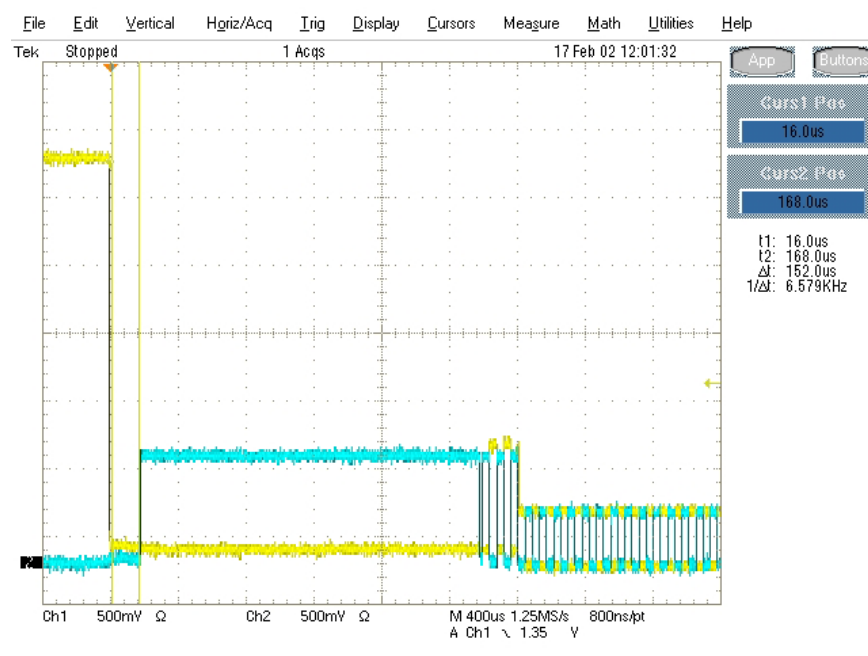
1. Connect the short USB cable dongle of the Device SQ segment of the test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the Test Bed Computer. Apply power to the device
2. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36. Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds.
3. Launch the TDSUSB software application on the TDS7404 or TDS7254 oscilloscope by selecting with a mouse or touch screen, File: Run application: USB2.0 compliance test package.
4. In the applications menu bar select, file: recall default.
5. Within the USB2.0 compliance test application, select the High Speed tab.
6. Click the Chirp button on the application.
7. Connect the upstream facing port of the device under test into the TEST port of the test fixture.
8. Click Enumerate Bus and capture the CHIRP handshake as in the figure below.



### Device Chirp (Speed Detection)

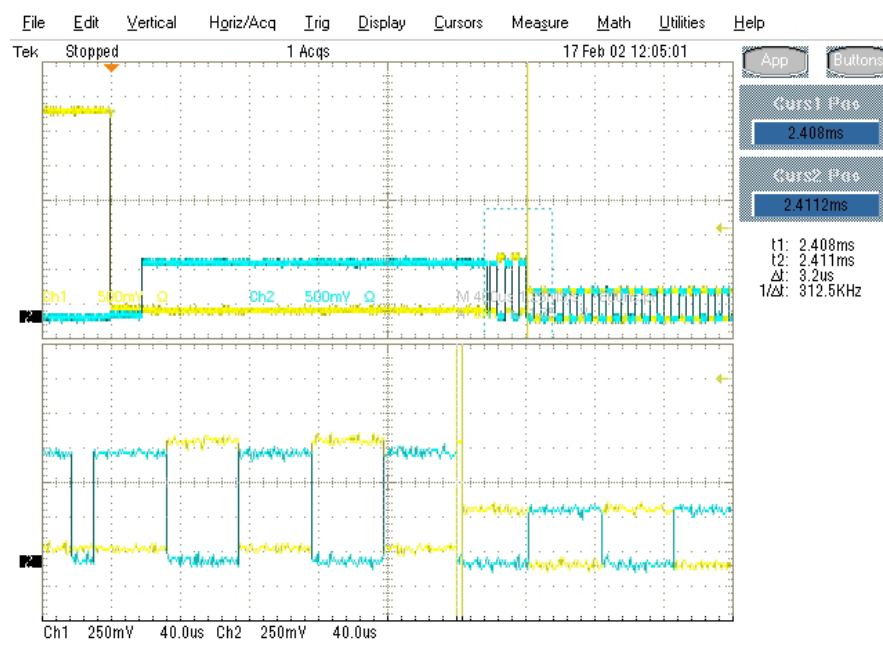
9. Check the device's CHIRP-K latency in respond to the reset from the host port. Verify this timing is between 2.5uS and 6.0mS. Record the result in \*EL\_28.

\*Note: The test specification rev 1.0 contains an error regarding EL\_28 at the time this test procedure was written. It states that the measurement time must be 2.5us to 3.0ms which is incorrect. The specification requires the CHIRP-K latency to be between 2.5uS and 6.0mS.



### Device Chirp-K Latency

10. Check the device's CHIRP-K duration. Verify this assertion time is between 1.0mS and 7.0mS. Record the result in EL\_29.
11. Following the host assertion of Chirp K-J-K-J-K-J, the device must respond by turning on its high-speed terminations. This is evident by a drop of amplitude of the alternate Chirp-K and Chirp-J sequence from the 800mV nominal to the 400mV nominal. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the device turns on the high-speed terminations. Verify this is less than or equal to 500us. Record the measurement in EL\_31.

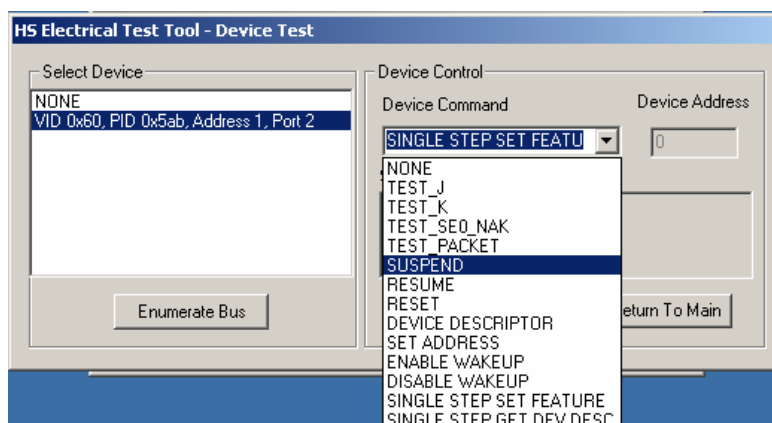


Time From Start of Last J in Chirp K-J-K-J-K-J To Device Turns on HS Termination

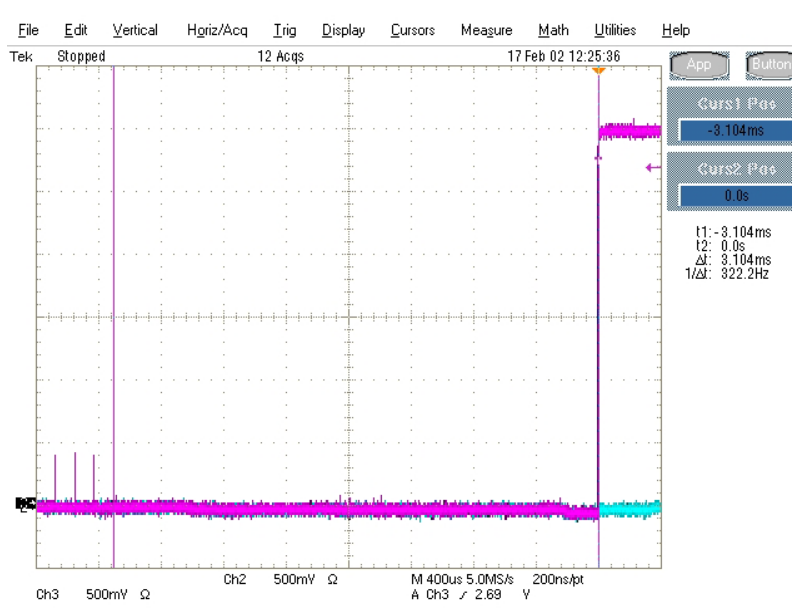
12. In addition to turning on its high-speed terminations, the device must also disconnect the D+ pull-up resistor in response to the host's assertion of Chirp K-J-K-J-K-J. The evidence is a slight drop of the D+ level during the Chirp-K from the host. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the D+ pull-up resistor is disconnected. Verify this is less than or equal to 500us. Record the measurement in EL\_31.

#### 4.7 Device Suspend/Resume/Reset timing (EL\_27, EL\_28, EL\_38, EL\_39, EL\_40)

1. Plug the Init port of the test fixture of High Speed Signal Quality test section into a high-speed capable port of the test bed computer.
2. Connect the device under test into the Test port of the test fixture. Click the Enumerate Bus button once to enumerate the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect Channel 2 and Channel 3 FET probes to the test fixture at J36 . Connect Ch2 to D- and Ch3 to D+. Connect the probe grounds.
4. Recall the SUSP2&3.SET oscilloscope setup.
5. On the HS Electrical Test Tool - Device Test menu, select SUSPEND from the Device Command drop down menu. Click EXECUTE once to place the device into suspend. The captured suspend transition should appear as in the figure below.



### Device Suspend

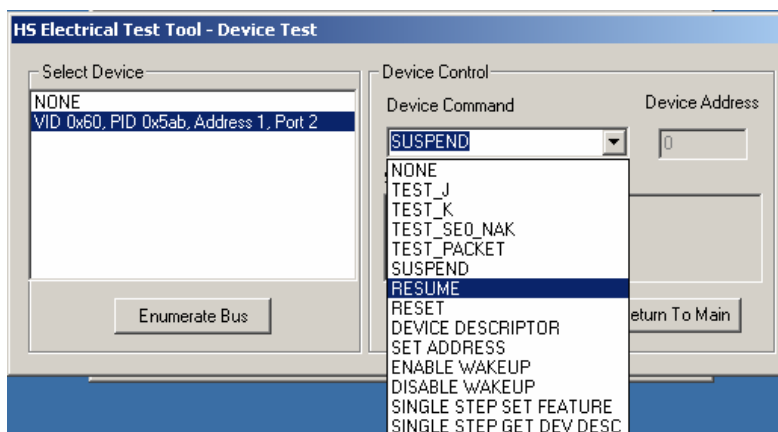


### Device Respond to Suspend from High-speed

6. Measure the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. Verify this time is between 3.000ms and 3.125ms. Record the result in EL\_38.
7. Ensure the oscilloscope is armed. Press Force Trigger to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V. Record the Pass/Fail result in EL\_39.

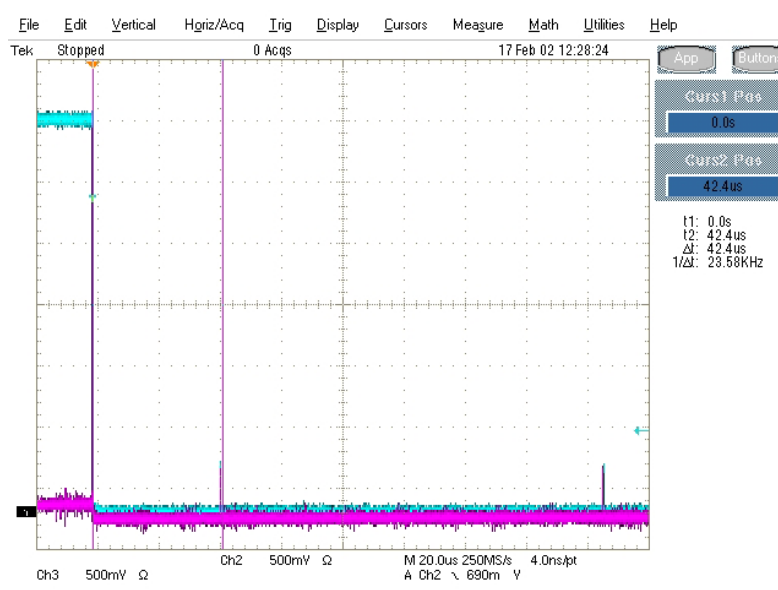
The following steps verify the Resume response of the device under test.

8. Recall the RESUM2&3.SET oscilloscope setup.
9. On the HS Electrical Test Tool - Device Test menu, select RESUME from the Device Command drop down menu. Click EXECUTE once to resume the device from suspend. The captured resume transition should appear as in the figure below.



### Device Resume

10. The device should resume the HS operation, which is indicated by the presence of HS SOF packets (with 400mV nominal amplitudes) following the K State driven by the host controller. See the following figure. Record the Pass/Fail result in EL\_40.

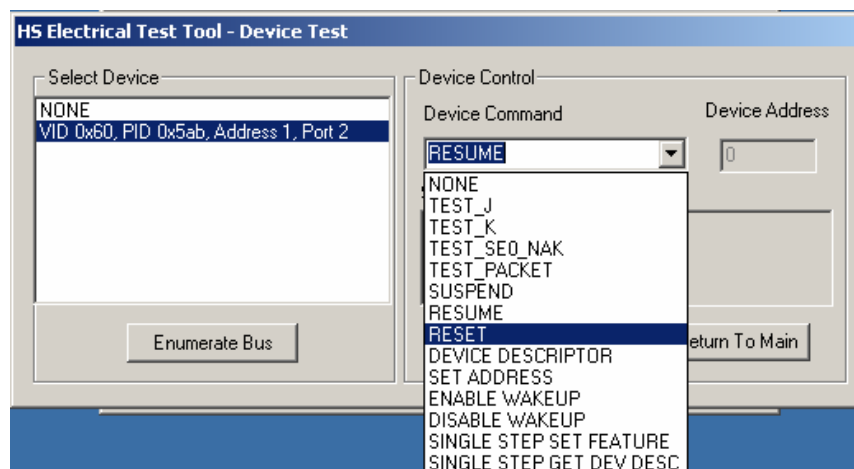


### Device Resume to High-speed

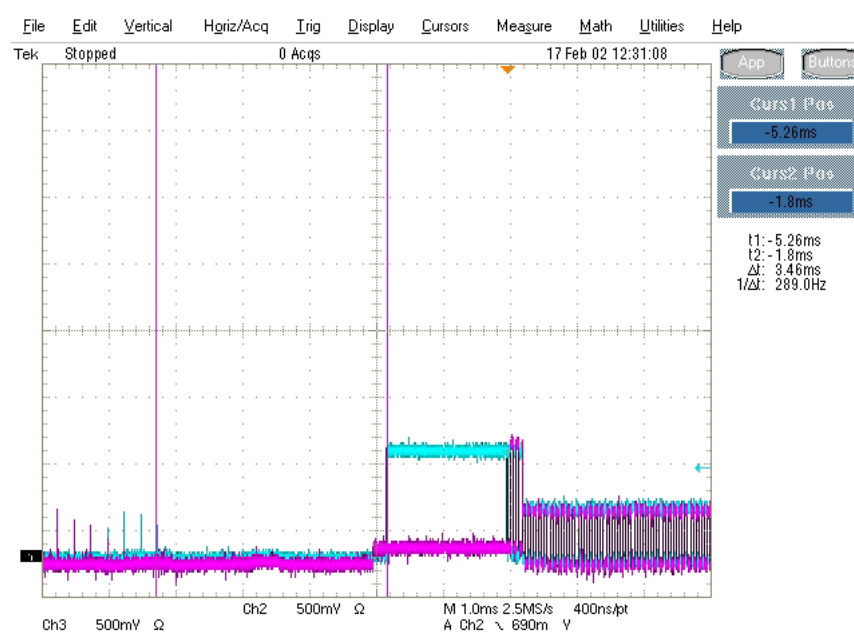
The following steps verify the device resumes back to high-speed operation after being reset from high-speed operation.

11. Recall the RSTFHS.SET oscilloscope setup.
12. Ensure the oscilloscope is armed.
13. On the HS Electrical Test Tool - Device Test menu, select RESET from the Device Command drop down menu. Click EXECUTE once to reset the device operating in high-speed. The captured reset response should appear as in the figure below.





### Device Reset

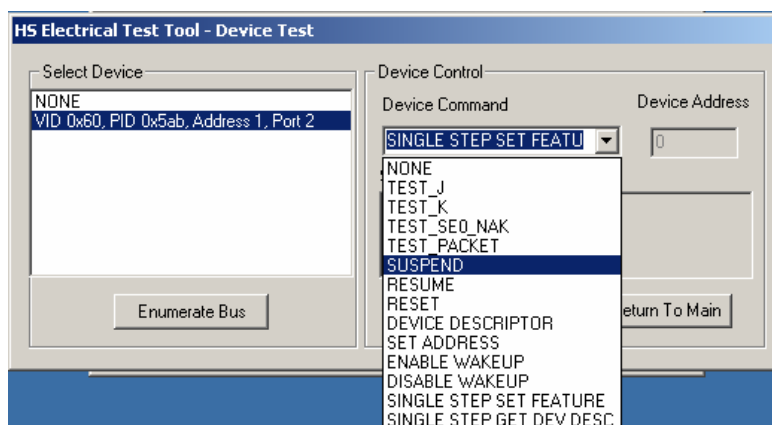


### Device Chirp-K in Response to Reset from High-speed

14. The device should transmit a chirp handshake following the reset. Measure the time between the beginning of the last SOF before the reset and the start of the device chirp-K. Verify this is between 3.1mS and 6mS. Record the Pass/Fail result in EL\_27.

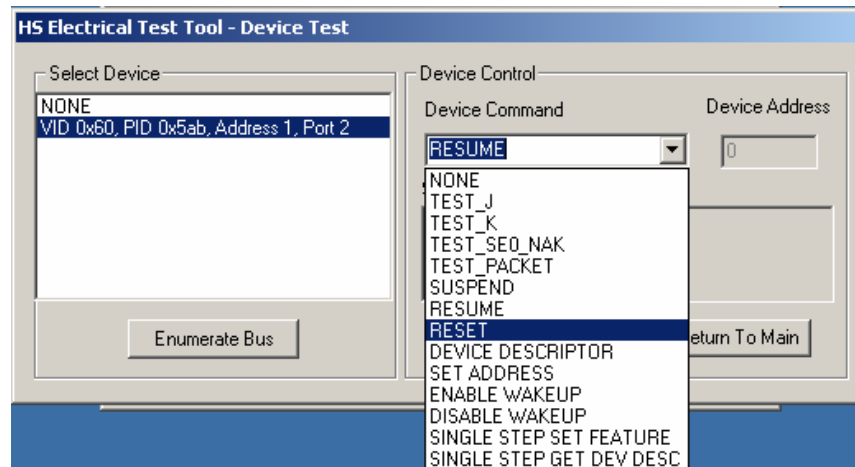
The following steps verify the device's chirp response after being reset from suspend.

15. Recall the RSTRSUSP.SET oscilloscope setup.
16. On the HS Electrical Test Tool - Device Test menu, select SUSPEND from the Device Command drop down menu. Click EXECUTE once to place the device into suspend.

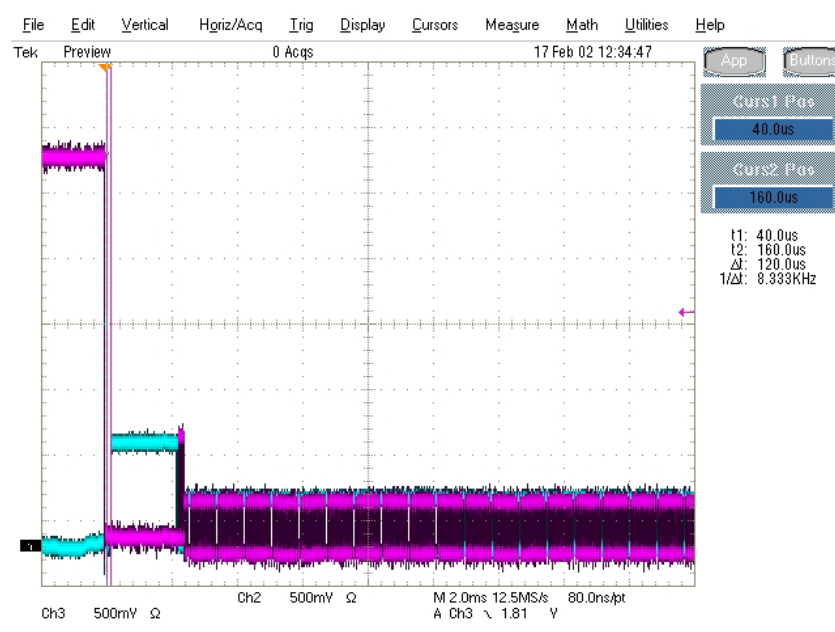


### Device Suspend

17. Ensure the oscilloscope is armed. Press Force Trigger to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V.
18. Ensure the oscilloscope is armed. On the HS Electrical Test Tool - Device Test menu, select RESET from the Device Command drop down menu. Click EXECUTE once to reset the device in suspend. The captured reset from suspend transition should appear as in the figure below.



### Device Reset



### Device Reset from Suspend

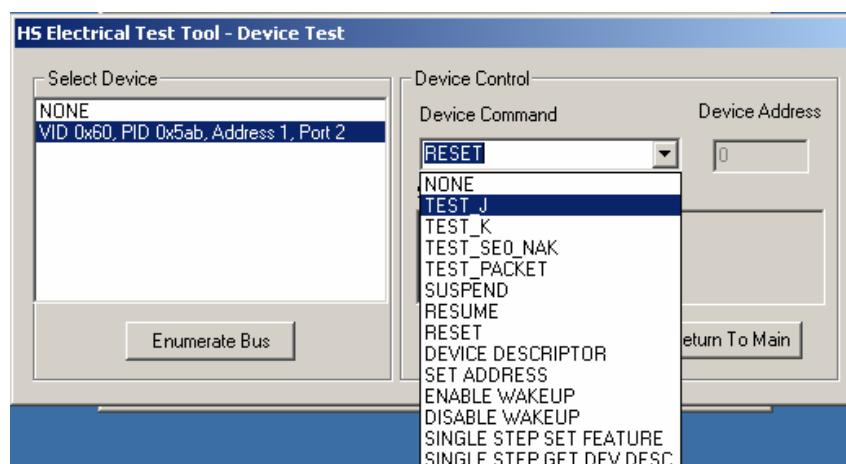
19. The device responds to the reset with the Chirp-K. Measure the time between the falling edge of the D+ and the start of the device chirp-K. Verify this is between 2.5uS and 6.0mS. Record the result in \*EL\_28.

\*Note: The test specification rev 1.0 contains an error regarding EL\_28 at the time this test procedure was written. It states that the measurement time must be 2.5us to 3.0ms which is incorrect. The specification requires the CHIRP-K latency to be between 2.5uS and 6.0mS.

20. Device Test J/K, SE0\_NAK (EL\_8, EL\_9)

1. Attach the 5V power supply to J38 of the Device High-speed Signal Quality section of the test fixture.
2. Verify the red Power LED is lit, and the red Test LED is off.

3. Connect the Test port of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the Test Bed Computer. Click the Enumerate Bus button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
4. On the HS Electrical Test Tool - Device Test menu, select TEST\_J from the Device Command drop down menu. Click EXECUTE once to place the device into TEST\_J test mode.



#### Device TEST\_J

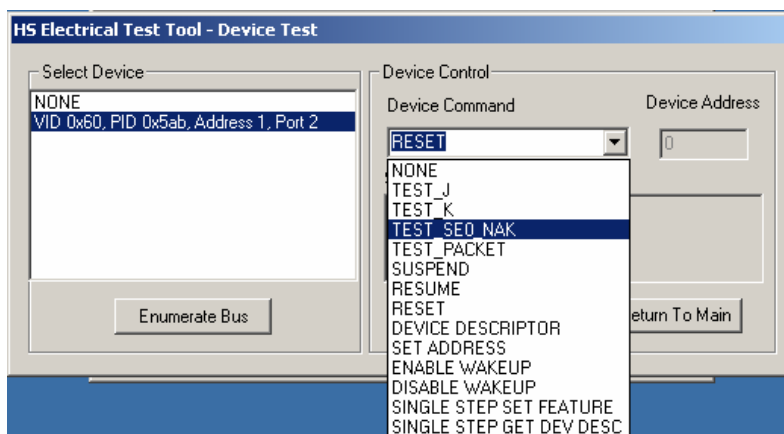
5. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL\_8.
6. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL\_8.
7. Return the Test switch to the NORMAL position. Cycle the device power. Click Enumerate Bus once to force enumerate the device. This restores the device to normal operation.
8. On the HS Electrical Test Tool - Device Test menu, select TEST\_K from the Device Command drop down menu. Click EXECUTE once to place the device into TEST\_K test mode.
9. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL\_8.
10. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL\_8.
11. Return the Test switch to the NORMAL position. Cycle the device power. Click Enumerate Bus once to force enumerate the device. This restores the device to normal operation.
12. On the HS Electrical Test Tool - Device Test menu, select TEST\_SE0\_NAK from the Device Command drop down menu. Click EXECUTE once to place the device into TEST\_SE0\_NAK test mode.
13. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL\_9.
14. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL\_9. Return the Test switch to the NORMAL position.

15. Remove the Device High Speed Signal Quality test fixture. Cycle the device power to prepare it for subsequent tests.

#### 4.8 Device Receiver Sensitivity (EL\_16, EL\_17, EL\_18)

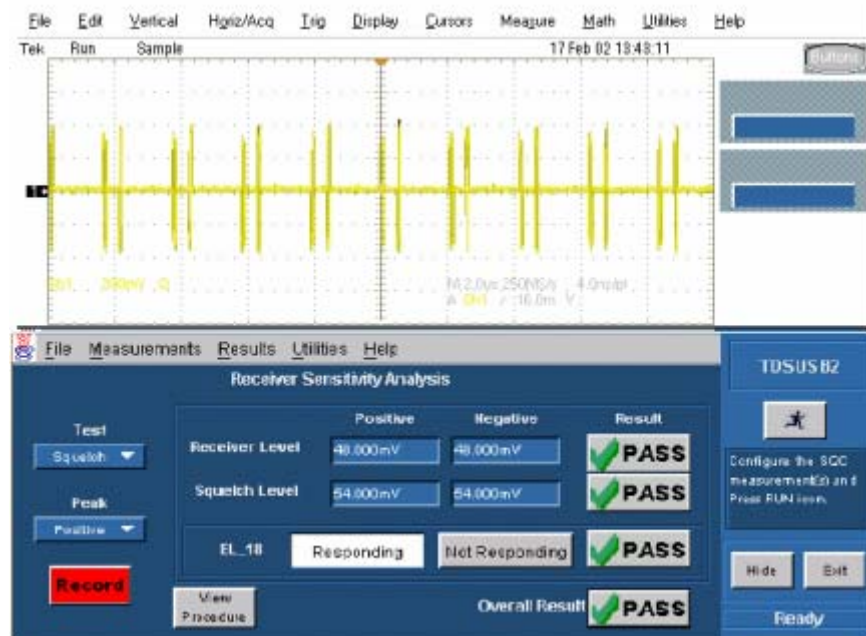
This section tests the sensitivity of the receivers on a device under test. A Tektronix DG2040 Data Generator emulates the In command from the hub port to device address 1.

1. Attach the 5V power supply to the Device Receiver test fixture J38 and verify the red Power LED is lit. Leave the TEST switch at the INIT position. The red test LED should be off and the red INIT LED should be on.
2. Connect the Init port of the fixture to a port on the Test Bed Computer. Connect the Test Port of the fixture to the device under test. Click the Enumerate Bus button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect the Tektronix DG2040 Data Generator to the Device Receiver Sensitivity test fixture using the SMA cables. Two sets of SMA cables are required, each with a 5x attenuators inserted. Connect CH 1 to SMA1, and CH 0 to SMA2, J30 and J31.
4. Connect the differential probe to the test fixture at J29. From the TDSUSB application, select Measurement: Select. Click on the High Speed tab and click Receiver Sensitivity.
5. On the DG2040, select the Edit menu. Then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the MIN-ADD1.PDA setup file. Press OK to load it. This generates IN packets (of compliant amplitude) with a 12-bit SYNC field.
6. Start the data generator output with the START/STOP button.
7. On the HS Electrical Test Tool - Device Test menu, select TEST\_SE0\_NAK from the Device Command drop down menu. Click EXECUTE once to place the device into TEST\_SE0\_NAK test mode.



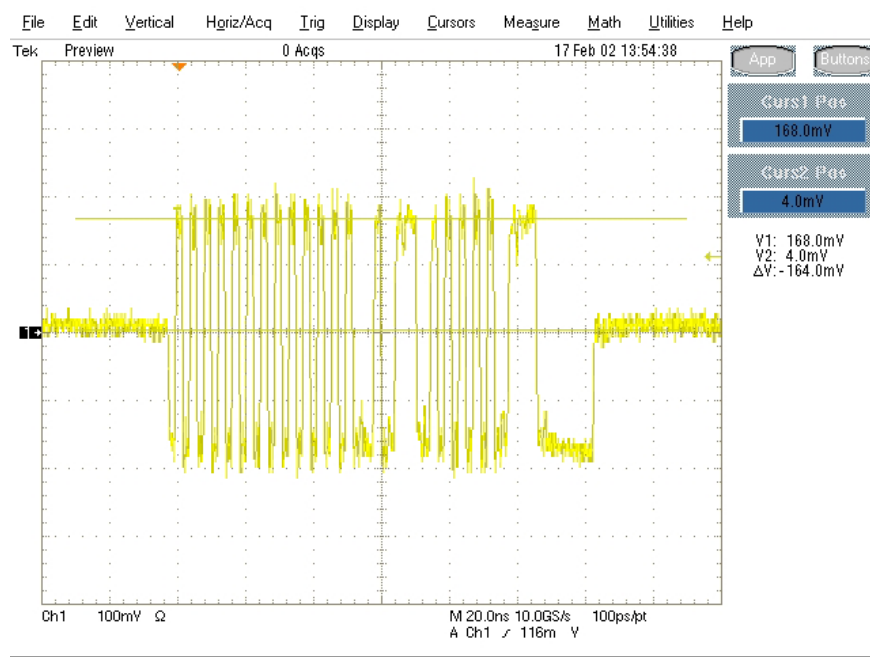
Device TEST\_SE0\_NAK

8. Place the test fixture Test Switch S6 into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the IN packets from the host controller.
9. Verify that all packets from the data generator are NAK'd by the port under test as in the following figure. Record the Pass/Fail in EL\_18.



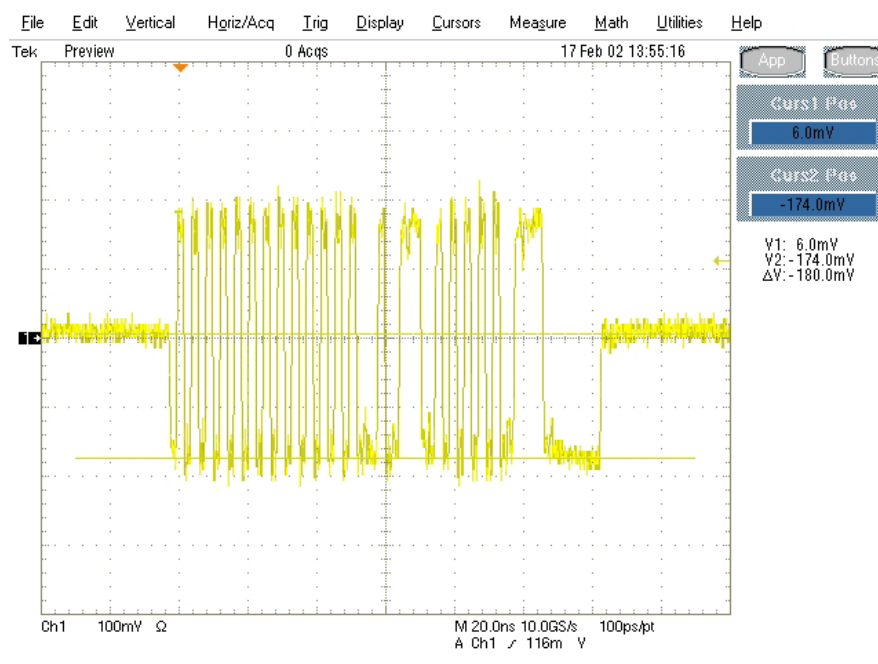
Receiver Respond with NAK to IN from Data Generator

10. On the data generator select the Edit menu, then press Load Data & Setup from the File function. The content of the floppy disk will appear on the screen. Use the jog dial to select the IN-ADD1.PDA setup file. Press OK to load it.
11. Verify that all packets are NAK'd while signaling is at this amplitude.
12. Adjust the output level of each channel as follows:
13. Select the Setup menu. Then press High from the Level Condition function. Adjustment of the output level is best done with the keypad in 50mV while monitoring the actual level on the oscilloscope. Use the up and down arrow buttons to select the channel to change.
14. Reduce the amplitude of the data generator packets in 50mV steps (on the generator before the attenuator) while monitoring the NAK response from the device on the oscilloscope. The adjustment should be made to both channels such that Ch0 and Ch1 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begins to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.
15. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Press the record button on the TDSUSB application corresponding to the receiver sensitivity level and record the measurement in EL\_17 of appendix A.



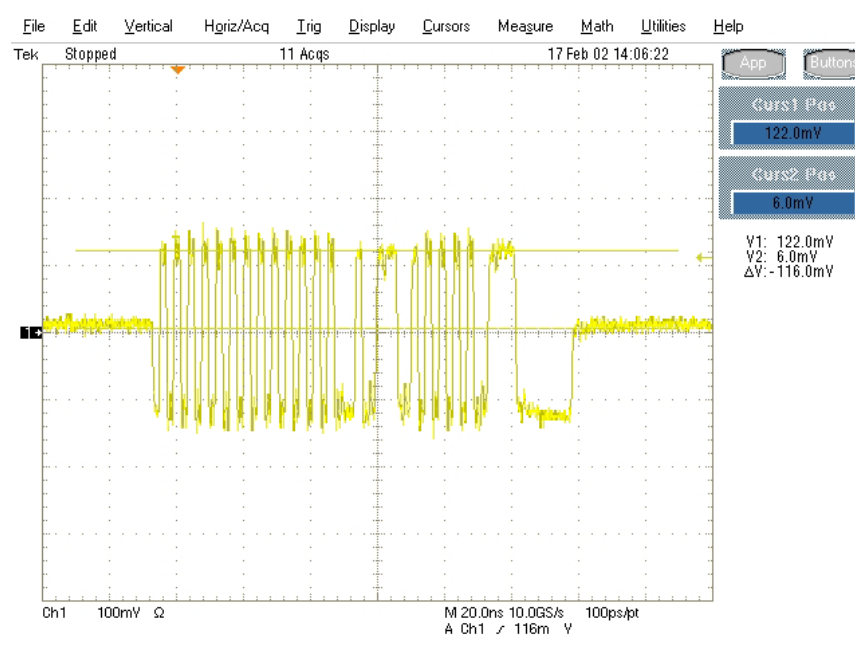
#### Measuring Differential Voltage Level – Zero to Positive Peak

16. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL\_17. As long as the receiver continue to NAK the data generator packet above +/- 150mV, it is considers pass the test. Record PASS/FAIL in EL\_17.



Measuring Differential Voltage Level – Zero to Negative Peak

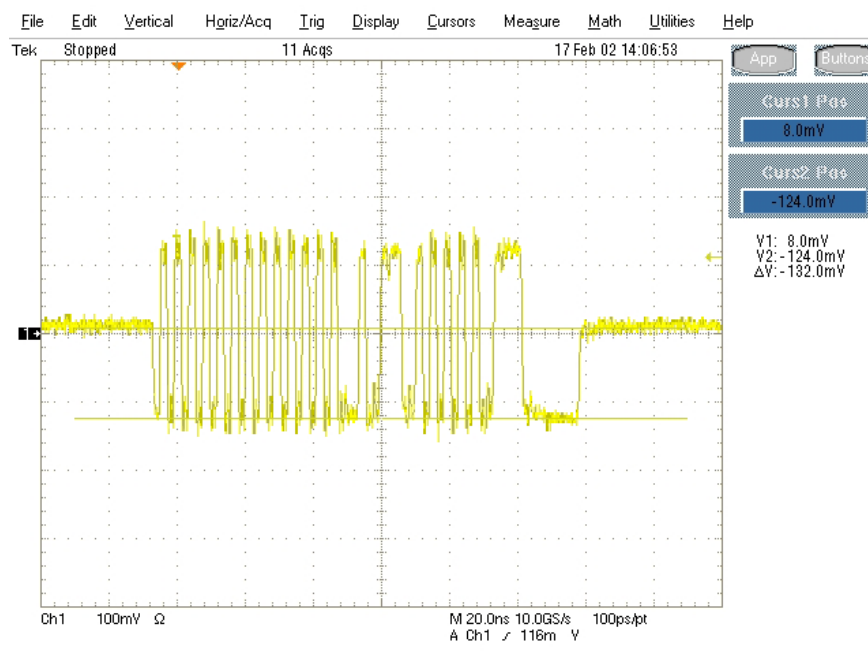
17. Now further reduce the amplitude of the packet from the data generator in small steps. Still maintaining balance between Ch0 and Ch1 until the receiver just cease to respond with NAK. This is the squelch level of the receiver.
18. Measure the Zero to Positive Peak of the packet from the data generator as in the following figure using the cursors. The measurement is best made by turning on the Fit To Screen function in the Horizontal menu of the oscilloscope to maintain sufficient sampling rate. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL\_16.





### Measuring Differential Voltage Level – Zero to Positive Peak

19. Measure the Zero to Negative Peak of the packet from the data generator as in the following figure using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL\_16. As long as the receiver ceases to NAK the data generator packet below  $\pm 100\text{mV}$ , it is considered pass the test. Record PASS/FAIL in EL\_16.



### Measuring Differential Voltage Level – Zero to Negative Peak

**Note:** With certain devices making an accurate zero-to-peak measurement of the In packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the In packet at the test fixture could be considerably higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

## Appendix A

### A.4 Device High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

#### A.4.2 Vendor and Product Information

|                            |   |
|----------------------------|---|
|                            | Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information. |
| Test Date                  |   |
| Vendor Name                |   |
| Vendor Complete Address    |   |
| Vendor Phone Number        |   |
| Vendor Contact, Title      |   |
| Test ID Number             |   |
| Product Name               |   |
| Product Model and Revision |   |
| USB Silicon Vendor Name    |   |
| USB Silicon Model          |   |
| USB Silicon Part Marking   |   |
| USB Silicon Stepping       |   |
| Tested By                  |   |

### A.4.3 Legacy USB Compliance Tests

#### Legacy USB Compliance Checklist

| Legacy Test | Pass/Fail | Comments |
|-------------|-----------|----------|
| FS SQ       |           |          |
| Inrush      |           |          |
| Interop     |           |          |

P = PASS

F = FAIL

N/A = Not applicable

### A.4.4 Device High-speed Signal Quality (EL\_2, EL\_4, EL\_5, EL\_6, EL\_7)

EL\_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s  $\pm 0.05\%$ .

**Reference documents:** *USB 2.0 Specification*, Section 7.1.11.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.2.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

#### A.4.5 Device Packet Parameters (EL\_21, EL\_22, EL\_25)

EL\_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

**Reference documents:** *USB 2.0 Specification*, Section 8.2.

##### Data Packet SYNC field

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.18.2.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.13.2

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

#### A.4.6 Device CHIRP Timing (EL\_28, EL\_29, EL\_31)

EL\_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail

☐ N/A

Comments:

EL\_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.5.

☐ Pass

☐ Fail

☐ N/A

Comments:

#### A.4.7 Device Suspend/Resume/Reset timing (EL\_27, EL\_28, EL\_38, EL\_39, EL\_40)

EL\_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period on the bus.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.6.

☐ Pass

☐ Fail

☐ N/A

Comments:

EL\_39 A device must support the Suspend state.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.6.

☐ Pass

☐ Fail

☐ N/A

Comments:

EL\_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

**Note:** It is not feasible to measure the device transition back to high-speed operation within two bit time from the end of the resume signaling. The presence of SOF at nominal 400mV amplitude following the resume signaling is sufficient for this test.

**Reference documents:** USB 2.0 Specification, Section 7.1.7.7.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.7.5.

- ☐ Pass
- ☐ Fail
- ☐ N/A

comments:

#### A.4.8 Device Test J/K, SE0\_NAK (EL\_8, EL\_9)

EL\_8 When either D+ or D- are driven high, the output voltage must be 400 mV  $\pm$ 10% when terminated with precision 45  $\Omega$  resistors to ground.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.1.3.

| Test | D+ Voltage (mV) | D- Voltage (mV) |
|------|-----------------|-----------------|
| J    |                 |                 |
| K    |                 |                 |

- ☐ Pass

- ☐ Fail
- ☐ N/A

Comments:

EL\_9 When either D+ and D- are not being driven, the output voltage must be  $0V \pm 10\text{ mV}$  when terminated with precision  $45\ \Omega$  resistors to ground.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.1.3.

|           | Voltage (mV) |
|-----------|--------------|
| <b>D+</b> |              |
| <b>D-</b> |              |

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

#### A.4.9 Device Receiver Sensitivity (EL\_16, EL\_17, EL\_18)

EL\_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.

- ☐ Pass
- ☐ Fail
- ☐ N/A

Comments:

EL\_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

**Note:** A waiver may be granted if the receiver does not indicate Squelch at  $\pm 50\text{mV}$  of 150mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.

- ☐ Pass
- ☐ Fail



☐ N/A

|           |
|-----------|
| Comments: |
|-----------|

EL\_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100 mV differential amplitude.

**Note:** A waiver may be granted if the receiver indicate Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

**Reference documents:** *USB 2.0 Specification*, Section 7.1.

☐ Pass☐ Fail☐ N/A

|           |
|-----------|
| Comments: |
|-----------|