Universal Serial Bus Implementers Forum Device High-speed Electrical Test Procedure For Agilent Infiniium

Revision 1.0

Feb 5, 2002

Revision History

Rev	Date	Filename	Comments
0.9 (Beta)	Nov-23-2001	Device HS Test for Agilent.DOC	Primary version of High Speed Test Procedure adapted to Agilent test equipment based on the test procedure created by USB-IF (version 0.9)
1.0	Feb-5-2002	Device HS Test for Agilent.DOC	Edit for final release.

Please send comments via electronic mail to techsup@usb.org

Table of Contents

1 Introduction

The USB-IF High-speed Electrical Test Procedures are developed by the USB 2.0 Compliance Committee under the direction of USB-IF, Inc. There are three High-speed Electrical Test Procedures. The Host High-speed Electrical Test Procedure is for EHCI host controllers. The Hub High-speed Electrical Test Procedure is for high-speed capable hubs. The Device High-speed Electrical Test Procedure is for high-speed capable devices.

The High-speed Electrical Compliance Test Procedures verify the electrical requirements of high-speed USB operation of these devices designed to the USB 2.0 specification. In addition to passing the high-speed test requirements, high-speed capable products must also complete and pass the applicable legacy compliance tests identified in these documents in order to be posted on the USB-IF Integrators List and use the USB-IF logo in conjunction with the said product (if the vendor has signed the USB-IF Trademark License Agreement). These legacy compliance tests are identified in the Legacy USB Compliance Test section in this document.

2 Purpose

This USB-IF High-speed Electrical Test Procedure documents a series of tests used to evaluate USB peripherals and systems operating at high-speed. These tests are also used to evaluate the high-speed operation of USB silicon that has been incorporated in ready-to-ship products, reference designs, proofs of concept and one of a kind prototypes of peripherals, add-in cards, motherboards, or systems.

This test procedure makes reference to the test assertions in the USB-IF USB2.0 Electrical Test Specification, Version 1.00.

This Device High-speed Electrical Test Procedure is one of the three USB-IF High-speed Electrical Compliance Test Procedures. The other two are Host High-speed Electrical Test Procedure and Hub High-speed Electrical Test Procedure. The adoption of the individual procedures based on the device class makes it easier to use.

3 Equipment Required

The commercial test equipment listed here are base on positive experience by the USB-IF members in executing the USB high-speed electrical tests. This test procedure is written with a set of specific models we use to develop this procedure. In time, there will be other equivalent or better test equipment suitable for use. Some minor adaptation of the procedure will be required in those cases.

- Digital Storage Oscilloscope:
  - Infiniium 54846A digital storage oscilloscope from Agilent Technologies
    - Tektronix P6247 or P6248 or equivalent differential probe, qty = 1
    - Tektronix 1103 Tekprobe Power Supply (for used with Tektronix P6247 or P6248), qty = 1
    - Agilent 1161A miniature passive probe, qty = 2

  - Short BNC cable (less than 50cm / 50ohm), qty = 1

- 3 ½ Digital Multimeter – Agilent 972A or equivalent
  - Mini-clip DMM lead – one each of black and red color
- Digital Signal Generator
  - 81130A Pulse / Pattern Generator
    - The DSG consists of an Agilent 81130A Pulse / Pattern Generator with 2 channels of Agilent 81132A (660MHz) option.
    - 6dB attenuator (Agilent 8493C opt 006) – for scaling the DSG output voltages needed for receiver sensitivity test, qty = 2
    - 50-ohm coaxial cable with male SMA connectors at both ends, qty = 2
- High-speed USB Electrical Test Fixtures
  - Device high-speed signal quality test fixture, qty = 1
  - Device Receiver test fixture, qty = 1
  - 5V test fixture power supply, qty = 1

    (When using Agilent HS test fixtures, the nomenclature of the test point will be different from Intel's test fixtures. This test procedure is written with the reference to Intel's test fixtures. Please use the following cross-reference chart when using Agilent's test fixture

Intel's Fixtures	Description of the test points	Agilent Fixtures
J7	Test Point	TP2
J8	Power Port	J5
J10	Ground	TP5
J11	Ground	TP5
SMA1	D- line	SMA2
SMA2	D+ line	SMA1

- Miscellaneous Cables
  - 1M USB cable, qty = 1
  - 1.5M USB cable, qty = 1
  - Modular AC power cord, qty = 2
- High-speed USB Test Bed Computer

  This is the computer that hosts a USB 2.0 compliance host controller for high-speed hub or device electrical test, or serves as a test bed host for a USB 2.0 host controller under test. This OS on this computer is Windows 2000 Professional. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure this computer.

3.1 Equipment Setup

3.1.1 Infiniium 54846A Digital Sampling Oscilloscope

Before turning on the oscilloscope, attach P6247 or P6248 differential probe to 1103 TekProbe Power Supply, connect a short BNC cable from 1103 to Channel-1. Make sure the saver is attached at the tip of the differential probe. When using two 1161A miniature passive probes, disconnect BNC cable from Channel-1 and connect one passive probe to Channel-1 and another to Channel-3. These probe assignments will be used through out the entire test procedure. Turn on the oscilloscope to allow for 10 minutes of warm up time prior to use. Perform the signal path compensation procedure built into the Infiniium 54846A (in the [Calibration…] section of [Utilities] pull down menu) if the ambient temperature has changed more than 5 degrees. The compensation should be performed with the probes disconnected from the oscilloscope.

The two miniature passive probes must be calibrated to minimize gain and offset errors. The offset errors of the diff probes will be cancelled later as a part of the test procedure process. The offset of the differential probe will be adjusted by the step identified in the test procedure.

For P6247 / P6248 differential probes, the following setting will be used through out the entire test procedure.

- DC Reject <OFF> (P6247 only)
- BW <Full> (P6247 only)
- Attenuation <÷1>

Note: In certain test situation, there may not be a ground connection between the DSO and the device under test. This may lead to the signal seen by the differential probe to be modulated up and down due to mid frequency switching power supply. Connecting the DSO ground to the DUT ground will be require to establish a common ground reference.

3.1.2 81130A Pulse/Pattern Generator

The 81130A is needed to perform the receiver sensitivity test that is structured toward the end of this test procedure. For energy conservation consideration, one may choose to turn on the 81130A about 15 minutes prior to performing the measurement.

3.2 Operating Systems, Software, Drivers, and Setup Files

3.2.1 Operating Systems

Microsoft Windows 2000 Professional is required on the High-speed Electrical Test Bed Computer. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

3.3 Special Purpose Software

- The following special purpose software is required. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these computers.

- High-speed Electrical Test Tool Software – To be used in the High-speed Electrical Test Bed Computer.

- Proprietary EHCI Driver Stack - The High-speed Electrical Test Tool software requires the use of a proprietary EHCI driver stack. The use of this proprietary EHCI driver stack facilitates the electrical testing that requires direct control of the command registers of the USB EHCI host controllers. The end result much more robust test bed environment. Since the proprietary EHCI driver stack is designed for debug and test validation purposes, this driver stack does not support the normal functionality as found in the EHCI drivers from Microsoft (or the device vendor). An automatic driver stack switching function has been implemented into the High-speed Electrical Test Tool for easy switching between the proprietary EHCI driver stack and that from Microsoft. Upon invocation of the HS Electrical Test Tool software, the driver stack will automatically switch to the Intel proprietary EHCI driver stack. Upon exit of the HS Electrical Test Tool software, the driver stack will automatically switch to the Microsoft EHCI driver stack.

- Infiniium USB test option (option B30 or E2645A) - For performing electrical test on USB devices.

3.4 Test Equipment Setup Files

This is 3½ inch floppy diskette that contain the setup files for the test equipment. Please refer to the High-speed Electrical Test Setup Instruction for steps to configure these setup disks. No setup disk is needed for Infiniium 54846A if Infiniium USB test option (option B30 or E2645A) is installed.

DSO Setup Disk – Contain setup files for Agilent Infiniium 54846A (This disk is not needed for the Infiniium 54846A with Infiniium USB test option or E2645A) (Digital Storage Oscilloscope)

DPG Setup – Please refer to Appendix B (Digital Pattern Generator)

4 Test Procedure

4.1 Test Record

Appendix A contains the test result entry form for this test procedure. Please make copies of the Appendix A for use as test record documentation for compliance test submission. All fields must be filled in. Fields not applicable for the device under test should be indicated as N/A, with appropriate note explaining the reason. The completed test result shall be retained for the compliance test submission.

In addition to the hardcopy test record, the electronic files from the signal quality, and power delivery (inrush, drop and droop) shall be retained for compliance test submission.

4.2 Vendor and Product Information

Collect the following information and enter into a copy of the test record in Appendix A before performing any tests.

1. Test date

2. Vendor name
3. Vendor address and phone, and the contact name
4. Test submission ID number
5. Product name
6. Product model and revision
7. USB silicon vendor name
8. USB silicon model
9. USB silicon part marking
10. USB silicon stepping
11. Test conducted by

4.3 Legacy USB Compliance Tests

In addition to the high-speed electrical tests prescribed in this document, the device under test must also pass the following compliance tests applicable to high-speed capable Device:

- Full speed signal quality
- Inrush current
- Interoperability

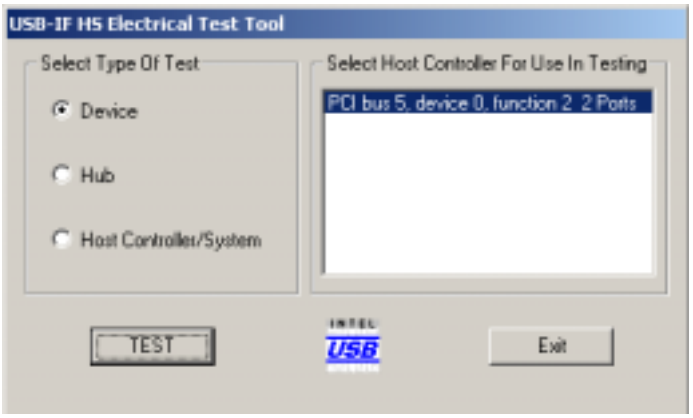
Perform all these tests and record the measurements and summarized Pass/Fail status in Appendix A.

4.4 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

Note: Please take care in determining if the device under test incorporates a captive cable, or it has a normal series B or mini-B receptacle. The former requires the signal quality measurement to be made at the far end. The latter requires the measurement to be made at the near end.

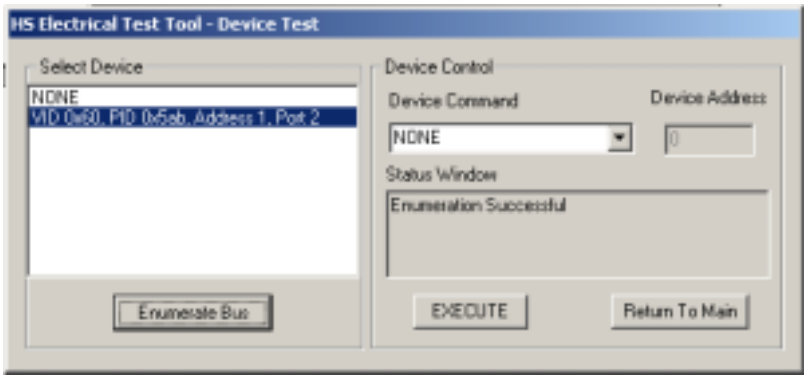
1. Turn on the oscilloscope if not already have done so. Allow about 10 minutes for warm up. Attach a P6247 or P6248 differential probe to 1103 TekProbe Power Supply. Connect 1103 and Channel-1 with a short BNC cable.
2. Recall HS_SQ_1.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu. Ensure the differential probe is not connected to anything. Set trigger to “Auto” by pressing [sweep] button of the oscilloscope. Adjust the DC level to zero using offset adjuster (OFFSET) on the 1103 Power Supply. When adjusting is done, set trigger back to “Trig’d” by pressing [sweep] button.
3. Attach the 5V power supply to J8 of the Device High-speed Signal Quality test fixture.
4. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is not lit.

5. Connect the [TEST PORT] of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the INIT PORT of the test fixture to a high-speed capable port of the Test Bed Computer. Apply power to the device.
6. Attach the differential probe to J7 of the test fixture. Ensure the + polarity on the probe lines up with D+ on the fixture.
7. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.



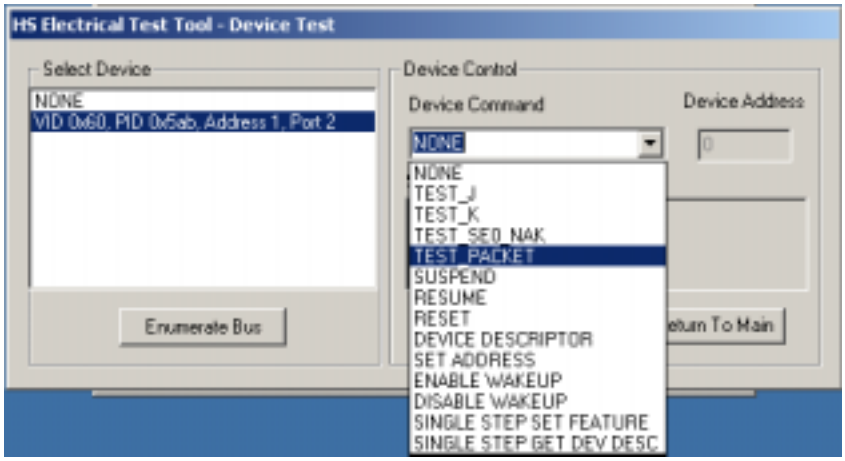
High-speed Electrical Test Tool – Main Menu

8. Select Device and click the [TEST] button to enter the HS Electrical Test Tool - Device Test menu. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.



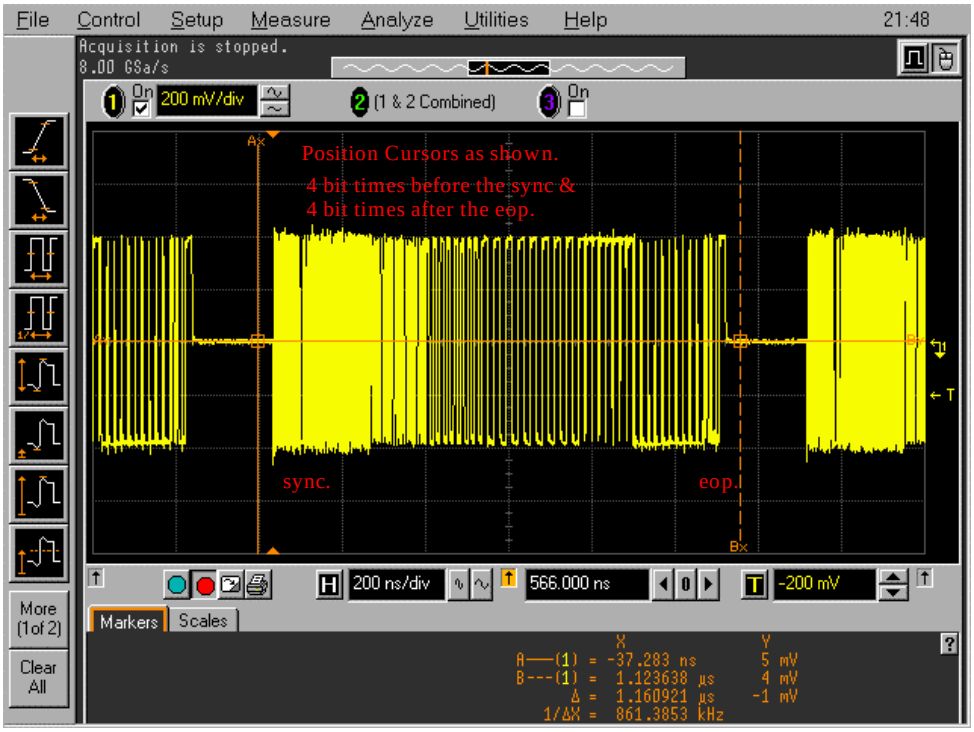
High-speed Electrical Test Tool – Device Test Menu

9. Select TEST_PACKET from the Device Command drop down menu and click [EXECUTE]. This forces the device under test to continuously transmit test packets.



Device Upstream TEST_PACKET

10. Place the Test Switch (S1) in the TEST position. Verify the yellow TEST LED is lit.
11. Using the oscilloscope, verify test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try slight change to the "trigger holdoff". "Holdoff" can be adjusted by selecting [Setup] pull down menu >> [Trigger…] >> [Conditioning…] button.
12. Pause the oscilloscope acquisitions using the [STOP] button.
13. On the oscilloscope adjust the two vertical cursors around one test packet, one just (about one bit time) before the sync field and the other just (about one bit time) after the EOP (END OF PACKET). Refer to the following figure for reference.



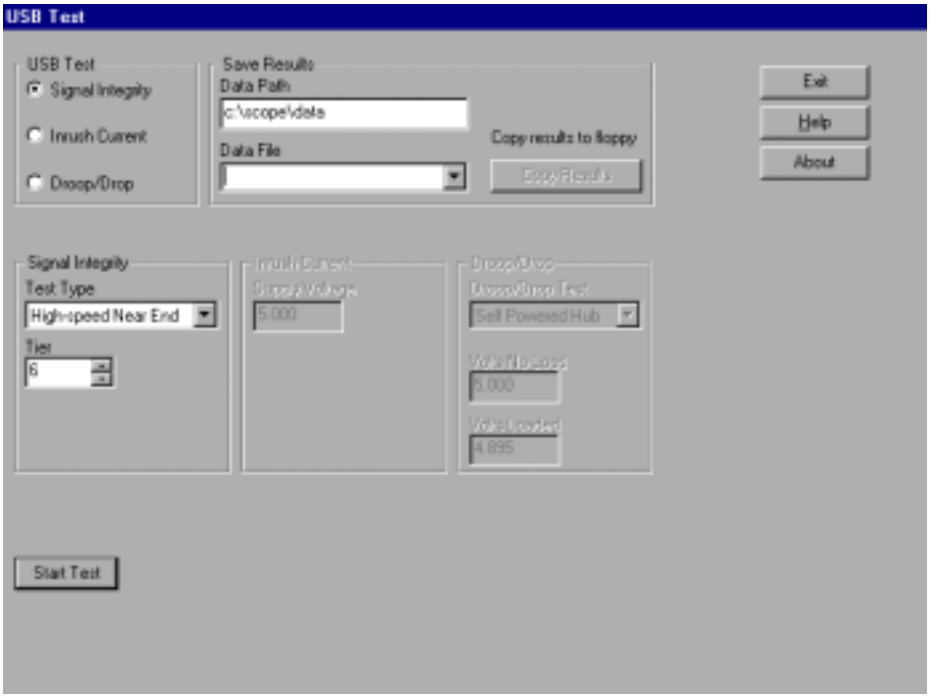
Test Packet from Device

14. From the Infiniium 54846A [Analyze] pull down menu, select [USB Test] to invoke the USB test
15. On the USB test option graphical user interface, select Signal Integrity in [USB Test] section.
16. If the device does not have a captive cable, on [Signal Integrity - Test Type] of USB test option graphical user interface select:

    High-speed Near End (Leave the [Tier] setting to 6)

    Otherwise (the device has a captive cable) select:

    High-speed Far End (Leave the [Tier] setting to 6)



USB Test Option

17. Enter a descriptive file name (e.g. TIDxxxxxxx USNE.tsv) in the [Save Results - Data File] field.
18. Click [Start Test] at the bottom of USB test option.
19. The result will be displayed on in the Internet Explorer. Verify the Signal eye, EOP Width, and Signaling Rate all pass. The results displayed in the Internet Explorer are also recorded to an HTML report located in the directory specified in the “Data Path” (e.g. c:\scope\data)

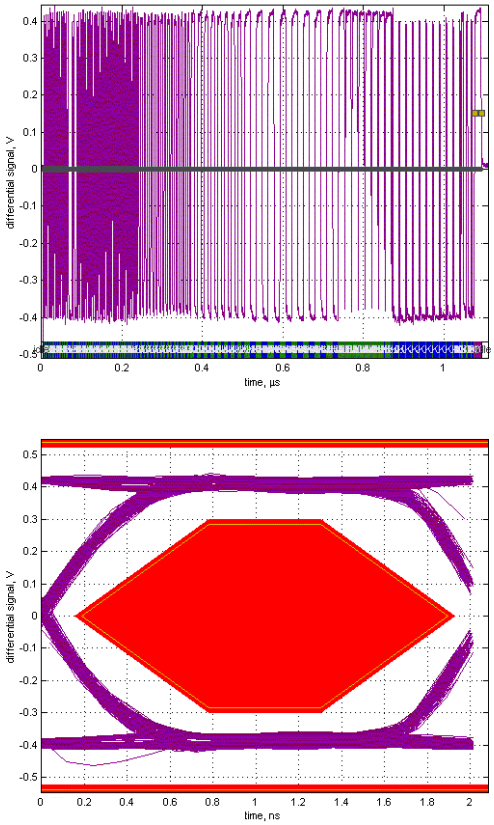
Required Tests

- Overall result: pass!
- Signal eye:
  eye passes
- EOP width: 8.00 bits
  EOP width passes
- Receivers: reliable operation on tier 6
  receivers pass
- Measured signaling rate: 480.0097MHz
  signal rate passes

Additional Information

- Consecutive jitter range: −45.3ps to 63.6ps, RMS jitter 21.6ps
  Paired JK jitter range: −38.4ps to 32.9ps, RMS jitter 17.0ps
  Paired KJ jitter range: −50.6ps to 43.3ps, RMS jitter 18.3ps

Signal Data, Eye, and Spectrogram



High-speed Near End SQ Eye Diagram

20. Record the test result in EL_2, EL_4 or EL_5, and EL_6 and EL_7. Save all files created during the tests. To save the results to a floppy disk, insert a floppy to the Infiniium's floppy drive and click on [Copy Results] after closing the Internet Explorer.

Note: EL_4 and EL_5 requirements are mutually exclusive. If EL_4 is tested then EL_5 is not applicable, and vice versa.

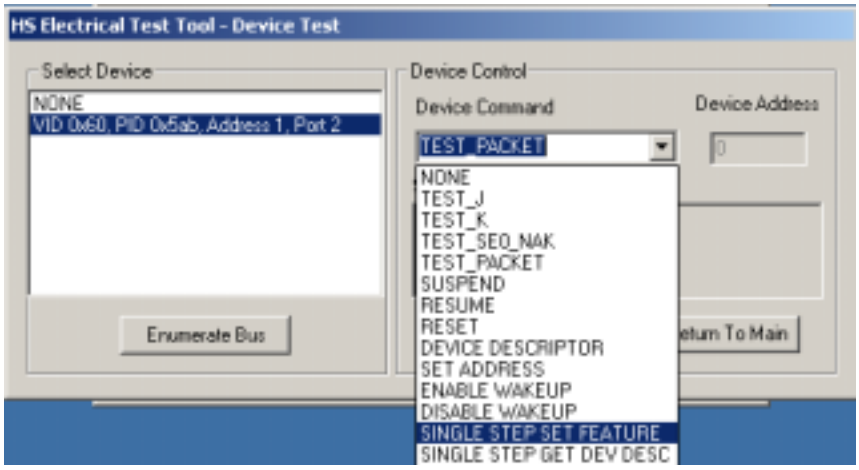
21. Return the Test switch (S1) of the test fixture back to the Normal position and verify the yellow TEST LED is not lit. Cycle power on the device in preparation for subsequent tests. Close the Infiniium USB test option by clicking [Exit] button.

4.5 Device Packet Parameters (EL_21, EL_22, EL_25)

1. Connect the [INIT PORT] of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.
2. Connect the Device Signal Quality test fixture [TEST PORT] into the B receptacle of the upstream facing port under test of the device. Verify that the device enumerates properly.

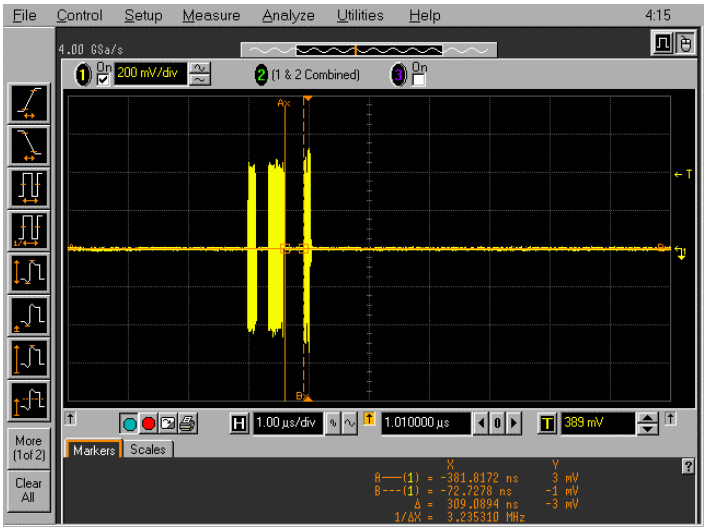
Note: The use of the Device High-speed Signal Quality test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the differential probe to J7 on the fixture near the device connector. Ensure the + polarity on the probe lines up with the D+ on the fixture.
4. Recall the PACKPARA.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.
5. Using the oscilloscope, verify SOFs (Start Of Frame packets) are being transmitted on the port under test. You may need to lower the trigger level to somewhat below 400mV.
6. Now raise the oscilloscope's trigger level slowly just until it does not trigger on the SOFs (or any host traffic). Typically this is around or slightly below 400mV, depending on the device and the length of cable used on the fixture. Ensure the oscilloscope is "RUN"ing and "Trig'd" mode. Use [Sweep] button in the front panel to adjust the mode if oscilloscope is in any other mode.
7. In the HS Electrical Test Tool - Device Test menu of the High-speed Electrical Test Tool software. Ensure the device under test is selected (highlighted). Select SINGLE STEP SET FEATURE from the Device Command window and click EXECUTE once.



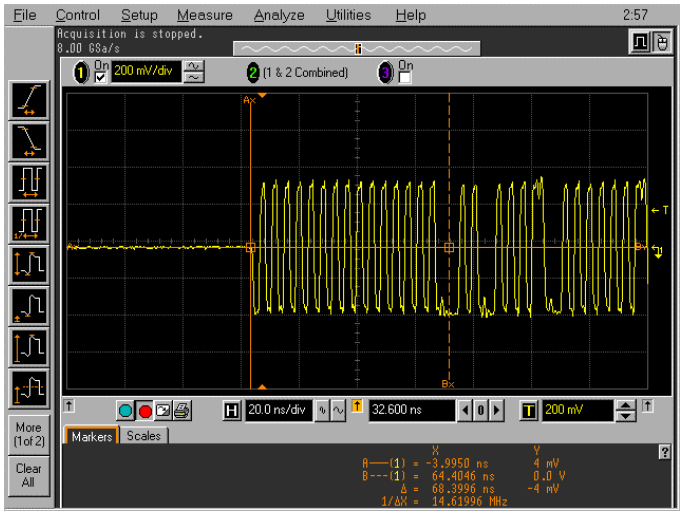
Device Single Step Set Feature

8. The oscilloscope capture should appear as follows. Press [STOP] on the oscilloscope to pause it from further trigger. If the oscilloscope doesn't trigger on the device traffic the trigger level is set too high. Lower the trigger level slightly (but not so low that it triggers on host SOFs) and repeat from step 7.



Host and Device Packets

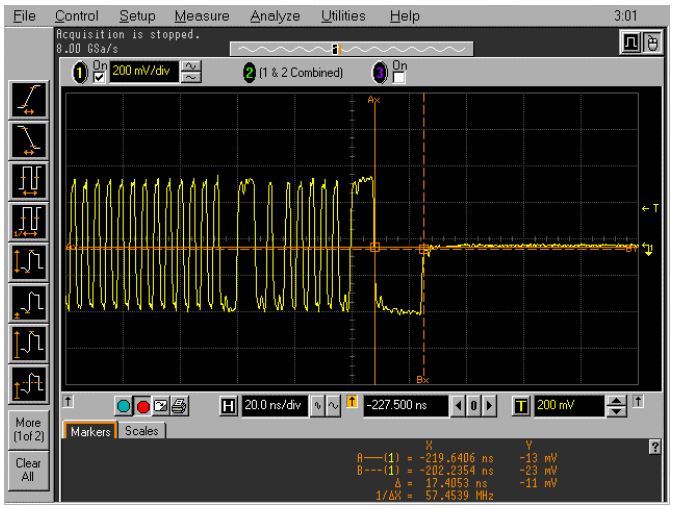
9. Use [Horizontal] knobs or the Zoom Box feature of the oscilloscope, measure the sync field length (number of bits) of the third (from device) packet on the oscilloscope and verify that it is 32 bits per EL_21 (to use the Zoom Box feature, press left button and drag oscilloscope's mouse around the given packet to draw the "Zoom Box", and click inside the box to zoom in). Refer to the figure below for the reference waveform. Note that Sync Field starts from the high-speed idle transitions to a falling edge (due to the first zero). Count both rising and falling edges until the first two consecutive 1's and include the first 1. There must be 32 bits. Record the number in EL_21.



Sync Field – Device Packet

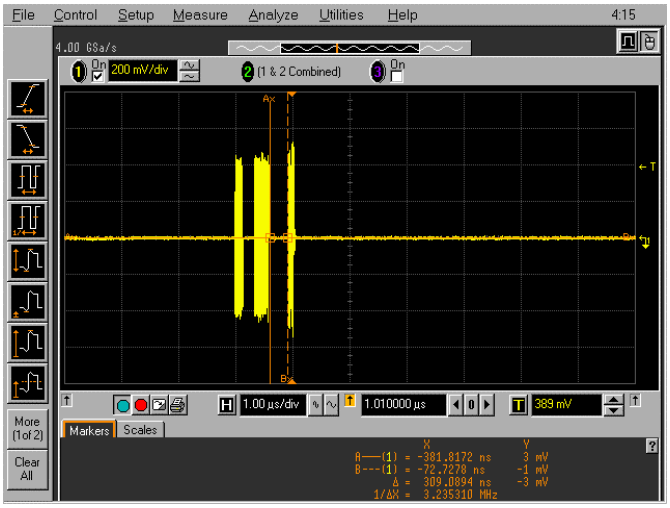
10. Measure the EOP (End of Packet) width (number of bits) of the third packet on the oscilloscope and verify that it is 8 bits per EL_25. It is advisable to use the markers to measure the EOP pulse width to determine the number of bits, based on 2.08nS / bit (480Mbps). Record the result in EL_25.

Note: EOP could appear as a negative going pulse, or a positive going pulse on differential measurement. The figure below illustrates the appearance of a negative going EOP.



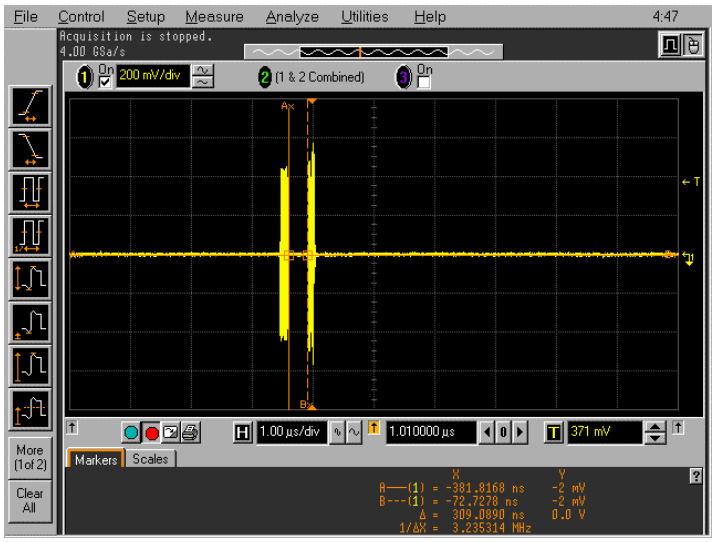
EOP in Device's Packet

11. Measure the inter-packet gap between the second (from host) and the third (from device in respond to the host's) packets shown on the oscilloscope by using the marker function of the oscilloscope. Markers can be accessed from [Measure] pull down menu or by pressing the [Marker] keys just below the display. The second (of lower amplitude) is from the host and the third (of higher amplitude) is a device's response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.



Device Inter-packet Gap

12. Ensure the oscilloscope is armed in “Trig’d” mode. In the HS Electrical Test Tool - Device Test menu, click the Step button once. This is the second step of the two-step Single Step Set Feature command.
13. The oscilloscope capture should appear as follows. Press [STOP] on the oscilloscope to pause it from further trigger.

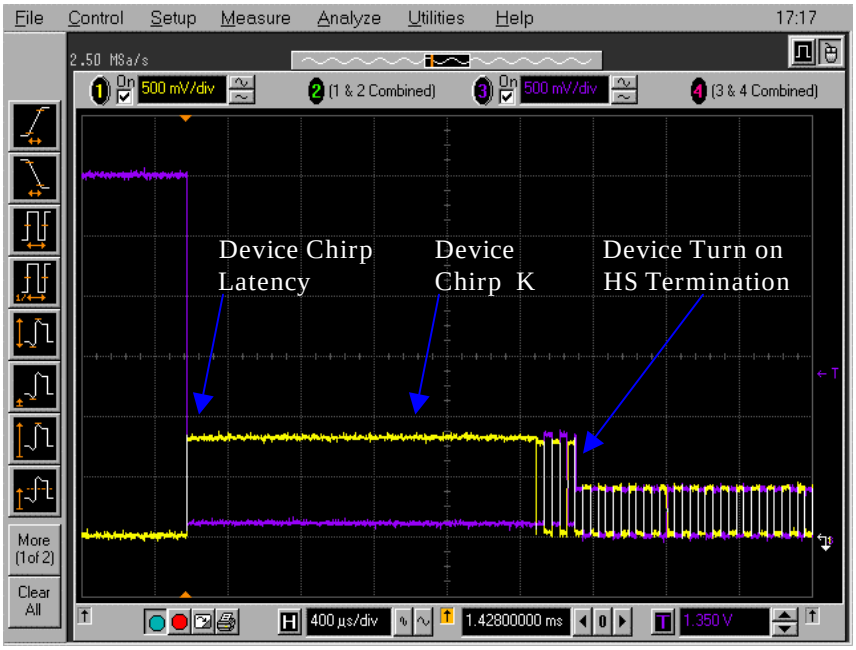


Single Step Set Feature – Second Step

14. Measure the inter-packet gap between the first (from host) and the second (from device in respond to the host’s) packets shown on the oscilloscope. The first (of lower amplitude) is from the host and the second (of higher amplitude) is a device’s response. Compute the number of bits by dividing the time measure by 2.08nS. The requirement is it must be between 8 bits and 192 bits. (EL_22). Record the computed number of bits in EL_22.
15. Detach the differential probe from the Device High-Speed Signal Quality test fixture. Disconnect the BNC cable from Channel-1 of the oscilloscope.

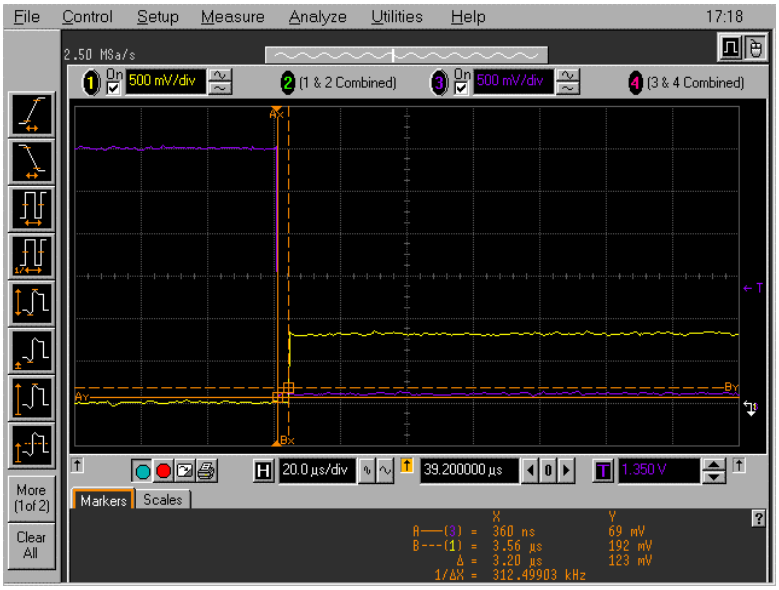
4.6 Device CHIRP Timing (EL_28, EL_29, EL_31)

1. Attach the [INIT PORT] of the Device High-speed Signal Quality test fixture into a high-speed capable port of the HS host controller.
2. Connect one 1161A miniature passive probe to Channel-1 and another to Channel-3. Connect the 1161A probes to the test fixture at J7 with Ch1 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.
3. Recall the CHRP1&3.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.
4. Connect the upstream facing port of the device under test into the [TEST PORT] of the test fixture.
5. Click [Enumerate Bus] and capture the CHIRP handshake as in the figure below.



Device Chirp (Speed Detection)

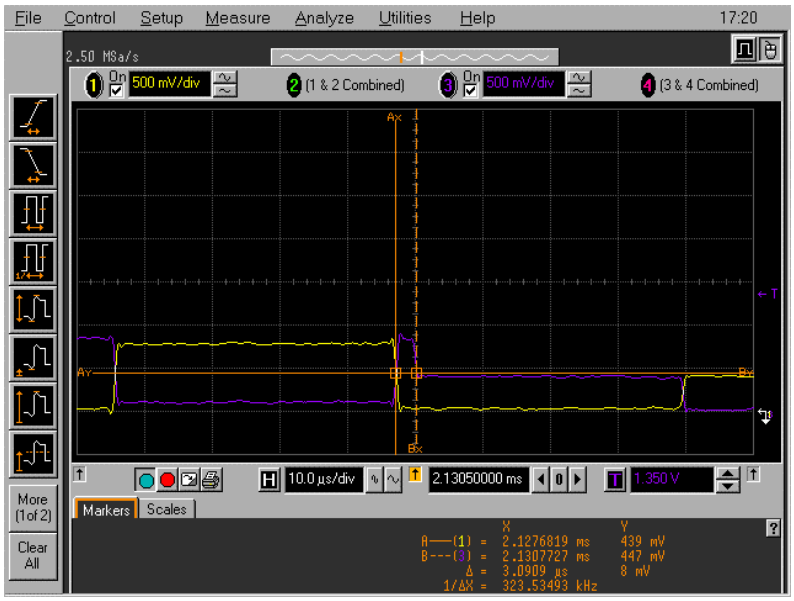
6. Use the [Horizontal] knobs or the Zoom Box feature of the oscilloscope, measure the device's CHIRP-K latency in respond to the reset from the host port. Verify this timing is between 2.5uS and 3.0mS. Record the result in EL_28.



Device Chirp-K Latency

7. Measure the device's CHIRP-K duration. Verify this assertion time is between 1.0mS and 7.0mS. Record the result in EL_29.

8. Following the host assertion of Chirp K-J-K-J-K-J, the device must respond by turning on its high-speed terminations. This is evident by a drop of amplitude of the alternate Chirp-K and Chirp-J sequence from the 800mV nominal to the 400mV nominal. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the device turns on the high-speed terminations. Verify this is less than or equal to 500us. Record the measurement in EL_31.

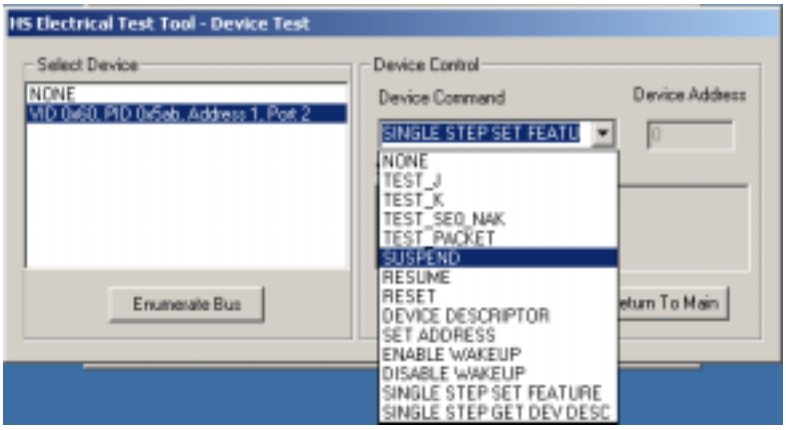


Time From Start of Last J in Chirp K-J-K-J-K-J To Device Turns on HS Termination

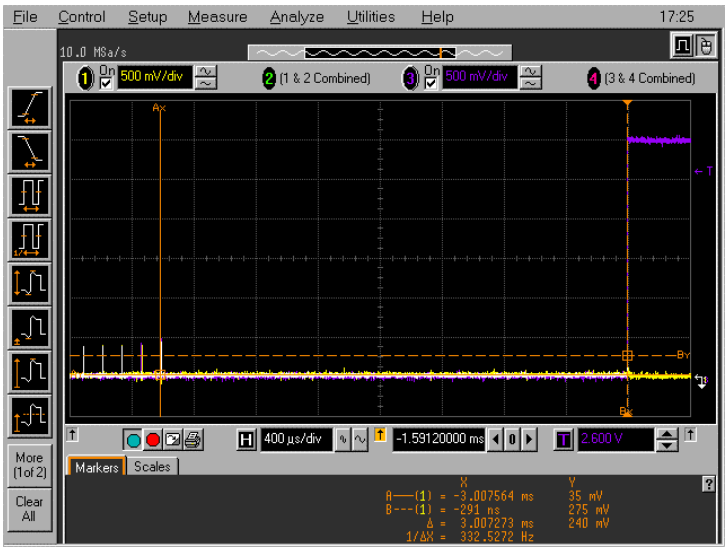
9. In addition to turning on its high-speed terminations, the device must also disconnect the D+ pull-up resistor in response to the host's assertion of Chirp K-J-K-J-K-J. The evidence is a slight drop of the D+ level during the Chirp-K from the host. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the D+ pull-up resistor is disconnected. Verify this is less than or equal to 500us. Record the measurement in EL_31.

4.7 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

1. Connect the [INIT PORT] of the Device High-speed Signal Quality test fixture into a high-speed capable port of the test bed computer.
2. Connect the device under test into the [TEST PORT] of the test fixture. Click the [Enumerate Bus] button once to enumerate the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect Channel 1 and Channel 3 1161A miniature passive probes to the test fixture at J7. Connect Ch1 to D- and Ch3 to D+. Connect the probe grounds to J10 and J11.
4. Recall the SUSP1&3.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.
5. On the HS Electrical Test Tool - Device Test menu, select SUSPEND from the Device Command drop down menu. Click [EXECUTE] once to place the device into suspend. The captured suspend transition should appear as in the figure below.



Device Suspend



Device Respond to Suspend from High-speed

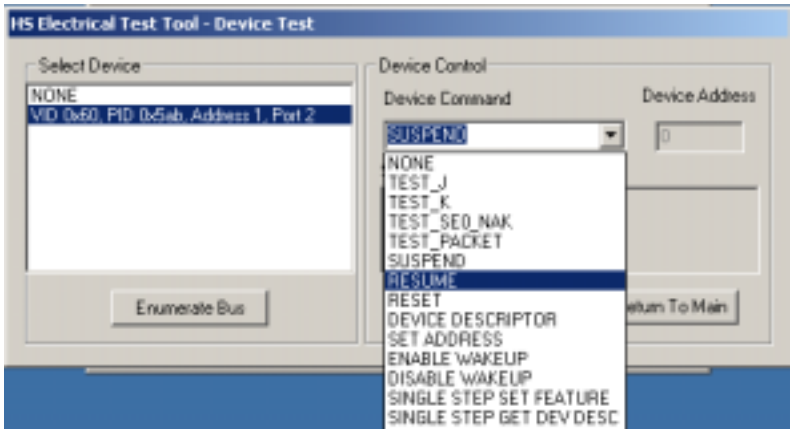
6. Measure the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. Verify this time is between 3.000ms and 3.125ms. Record the result in EL_38.

7. Ensure the oscilloscope is armed. Set trigger to “Auto” by pressing [sweep] button to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V. Record the Pass / Fail result in EL_39.

   The following steps verify the Resume response of the device under test.

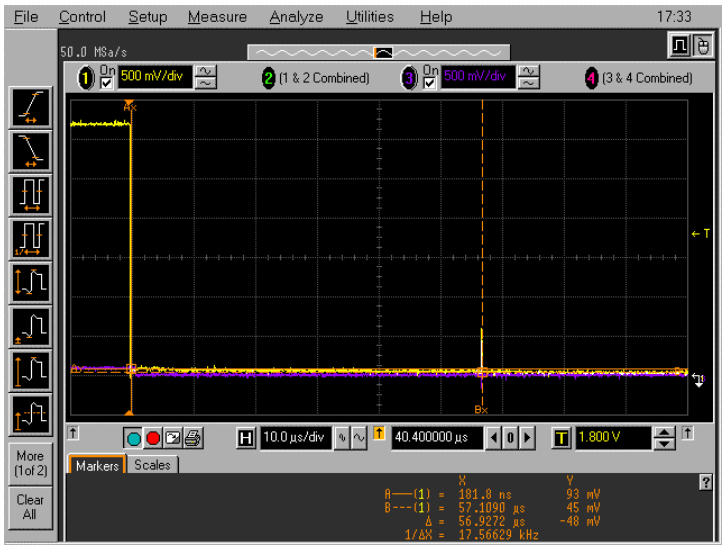
8. Recall the RESUM1&3.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.

9. On the HS Electrical Test Tool - Device Test menu, select RESUME from the Device Command drop down menu. Click [EXECUTE] once to resume the device from suspend. The captured resume transition should appear as in the figure below.



Device Resume

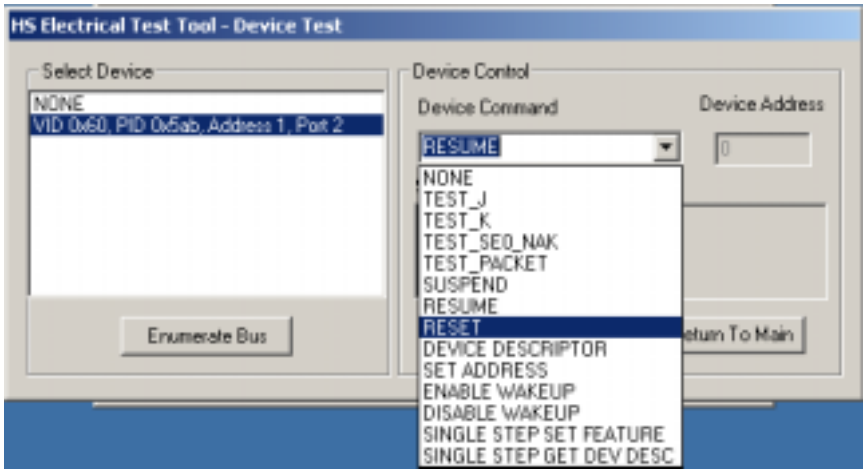
10. The device should resume the HS operation, which is indicated by the presence of HS SOF packets (with 400mV nominal amplitudes) following the K State driven by the host controller. See the following figure. Record the Pass / Fail result in EL_40.



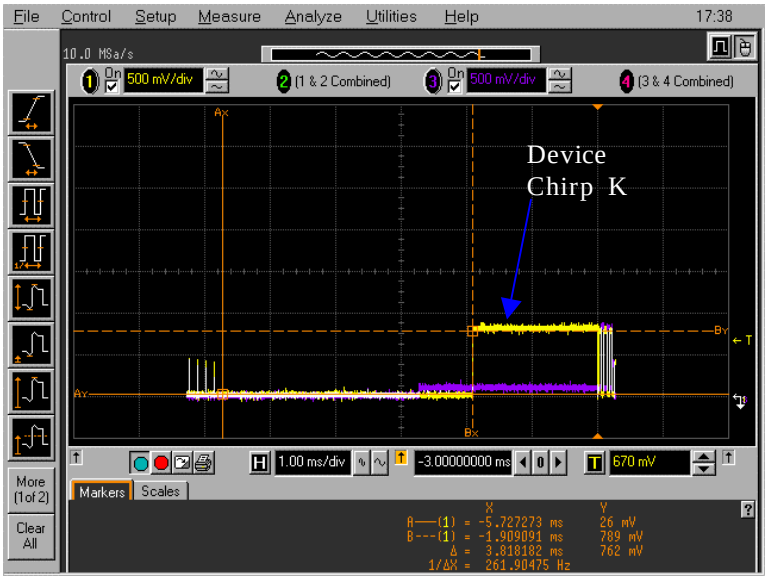
Device Resume to High-speed

The following steps verify the device resumes back to high-speed operation after being reset from high-speed operation.

11. Recall the RSTFHS1&3.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.
12. Ensure the oscilloscope is armed.
13. On the HS Electrical Test Tool - Device Test menu, select RESET from the Device Command drop down menu. Click [EXECUTE] once to reset the device operating in high-speed. The captured reset response should appear as in the figure below.



Device Reset



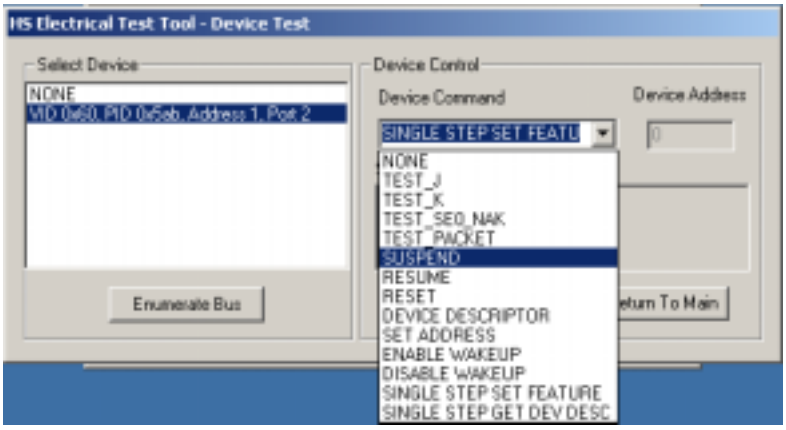
Device Chirp-K in Response to Reset from High-speed

14. The device should transmit a chirp handshake following the reset. Measure the time between the beginning of the last SOF before the reset and the start of the device chirp-K. Verify this is between 3.1mS and 6mS. Record the Pass/Fail result in EL_27.

    The following steps verify the device's chirp response after being reset from suspend.

15. Recall the RSTRSUSP1&3.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.

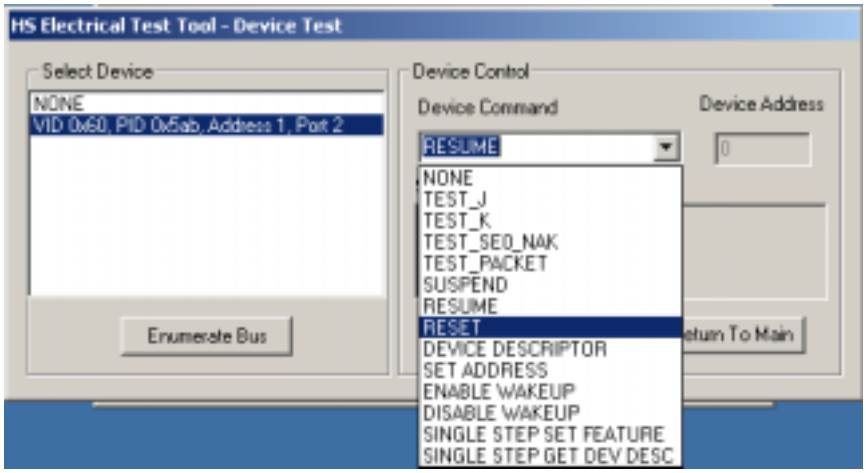
16. On the HS Electrical Test Tool - Device Test menu, select SUSPEND from the Device Command drop down menu. Click [EXECUTE] once to place the device into suspend.



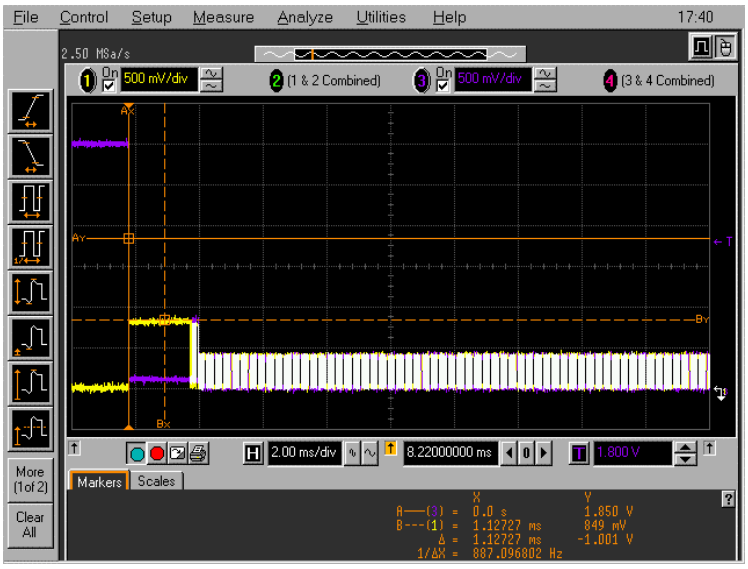
Device Suspend

17. Ensure the oscilloscope is armed. Set trigger to “Auto” by pressing [sweep] button to verify the device is still in the suspend state. The D+ should be at 3.3V nominal. The D- should be less than 0.7V.

18. Set trigger back to “Trig’d” by pressing [sweep] button. Ensure the oscilloscope is armed by pressing [RUN] button. On the HS Electrical Test Tool - Device Test menu, select RESET from the Device Command drop down menu. Click [EXECUTE] once to reset the device in suspend. The captured reset from suspend transition should appear as in the figure below.



Device Reset



Device Reset from Suspend

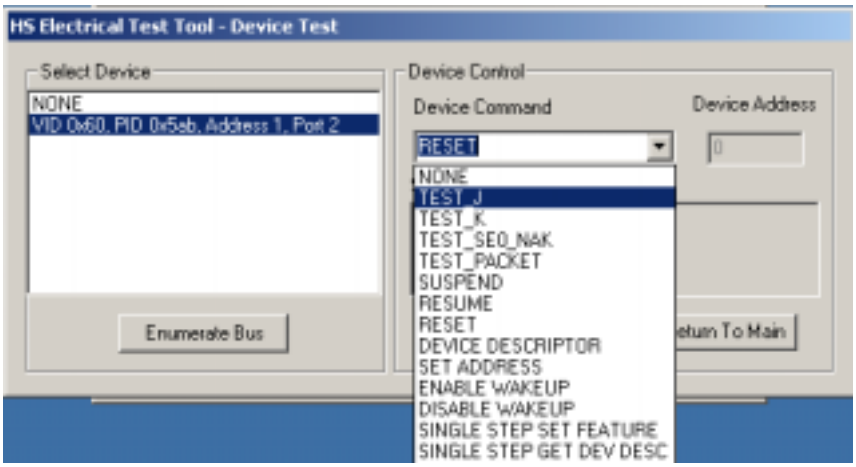
19. The device responses to the reset with the Chirp-K. Measure the time between the falling edge of the D+ and the start of the device chirp-K. Verify this is between 2.5us and 3ms. Record the Pass/Fail result in EL_28.
20. Disconnect the 1161A miniature passive probe from Ch1 of oscilloscope.

4.8 Device Test J/K, SE0_NAK (EL_8, EL_9)

1. Attach the 5V power supply to J8 of the Device High-speed Signal Quality test fixture.
2. Verify the green Power LED (D1) is lit, and the yellow Test LED (D2) is off.
3. Connect the [TEST PORT] of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the [INIT PORT] of the test fixture to a high-speed capable port of the Test Bed Computer. Click the [Enumerate Bus] button once to force

enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.

4. On the HS Electrical Test Tool - Device Test menu, select TEST_J from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_J test mode.



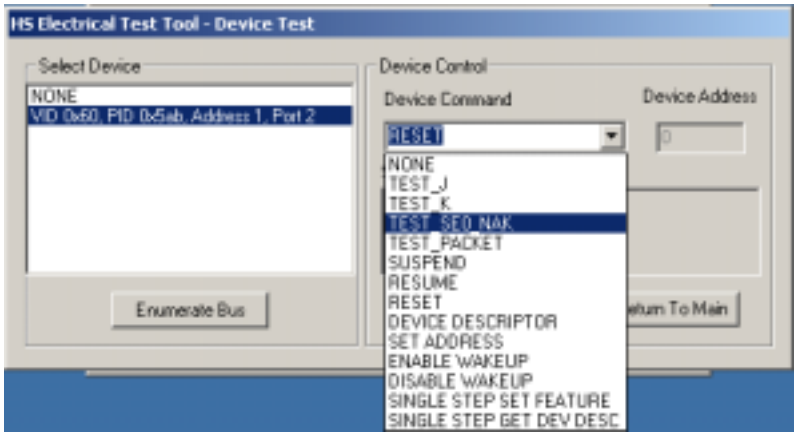
Device TEST_J

5. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
6. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.
7. Return the Test switch to the NORMAL position. Cycle the device power. Click [Enumerate Bus] once to force enumerate the device. This restores the device to normal operation.
8. On the HS Electrical Test Tool - Device Test menu, select TEST_K from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_K test mode.
9. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_8.
10. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground. Record in section EL_8.
11. Return the Test switch to the NORMAL position. Cycle the device power. Click [Enumerate Bus] once to force enumerate the device. This restores the device to normal operation.
12. On the HS Electrical Test Tool - Device Test menu, select TEST_SE0_NAK from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_SE0_NAK test mode.
13. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.
14. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9. Return the Test switch to the NORMAL position.
15. Remove the Device High Speed Signal Quality test fixture. Cycle the device power to prepare it for subsequent tests.

4.9 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

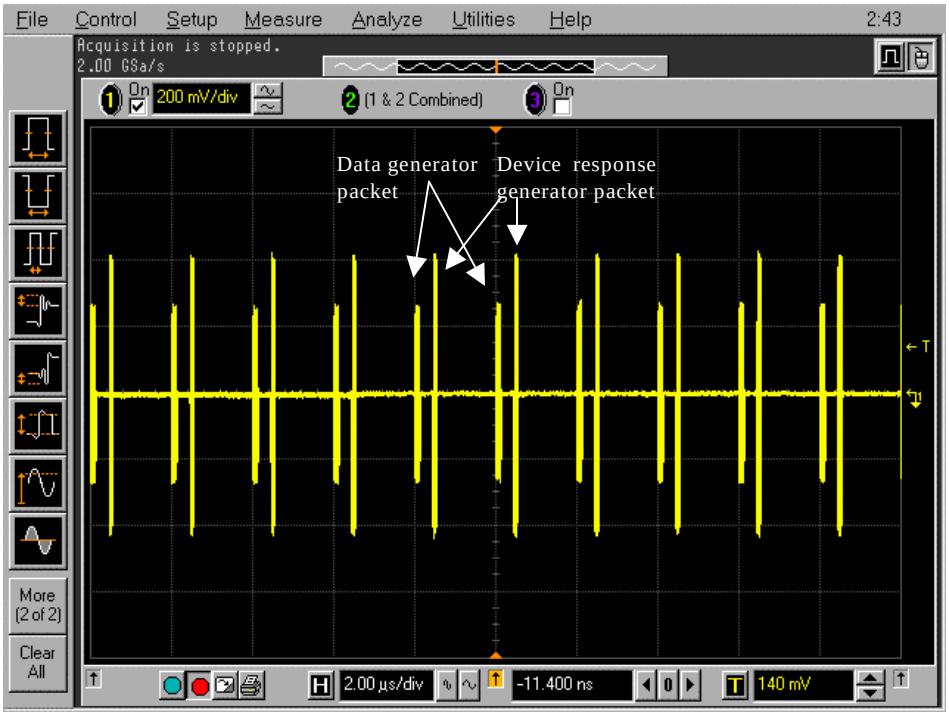
This section tests the sensitivity of the receivers on a device under test. An Agilent 81130A Pulse / Pattern Generator emulates the "IN" command from the hub port to device address 1.

1. Attach the 5V power supply to the Device Receiver test fixture (J8) and verify the green Power LED (D1) is lit. Leave the TEST switch at the Normal position (S1 position). The yellow LED (D2) should be off.
2. Connect the [INIT PORT] of the fixture to a high-speed port on the Test Bed Computer. Connect the [TEST PORT] of the fixture to the device under test. Click the [Enumerate Bus] button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Two sets of SMA cables are required, each with a 6dB attenuators inserted. Connect the 6dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse / Pattern Generator. Connect OUTPUT 1 to SMA2, and OUTPUT 2 to SMA1 of the Device Receiver Sensitivity test fixture using the SMA cables.
4. Connect Ch1 of the oscilloscope and the 1103 Tekprobe Power Supply with a short BNC cable. Connect the differential probe to the test fixture at J7. Recall the RCVRSENS.SET oscilloscope setup by selecting [Load] >> [Setup…] from the [File] pull down menu.
5. On the 81130A, select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen (For creating the setup files used in this section, please refer to Appendix B). Use the cursor and the rotary knob to select the [MIN_ADD1.ST0] setup file. Move the cursor to [Perform Operation] and turn the knob to select [Recall]. Then press [ENTER] key to load it. This generates "IN" packets (of compliant amplitude) with a 12-bit SYNC field.
6. On the HS Electrical Test Tool - Device Test menu, select [TEST_SE0_NAK] from the Device Command drop down menu. Click [EXECUTE] once to place the device into TEST_SE0_NAK test mode.



Device TEST_SE0_NAK

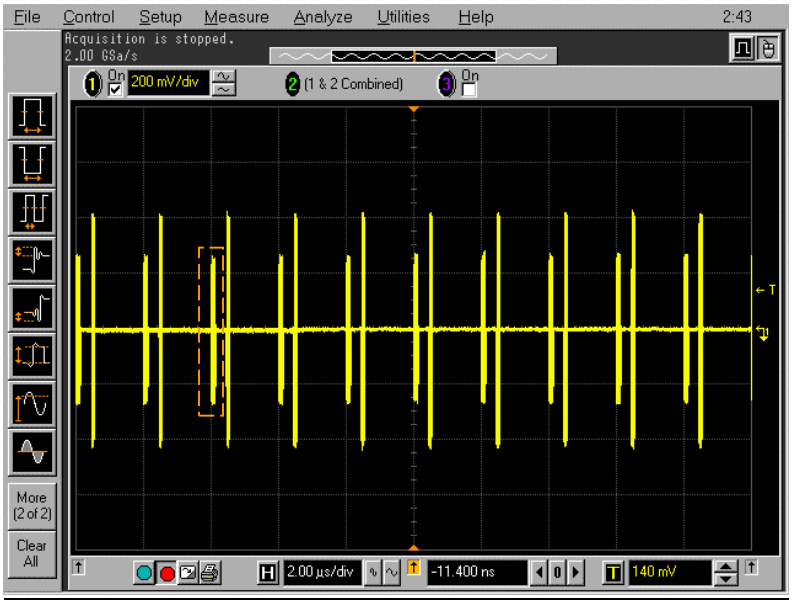
7. Place the test fixture Test Switch (S1) into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the "IN" packets from the host controller.
8. Verify that all packets from the data generator are NAK'd by the port under test as in the following figure. Record the Pass / Fail in EL_18.



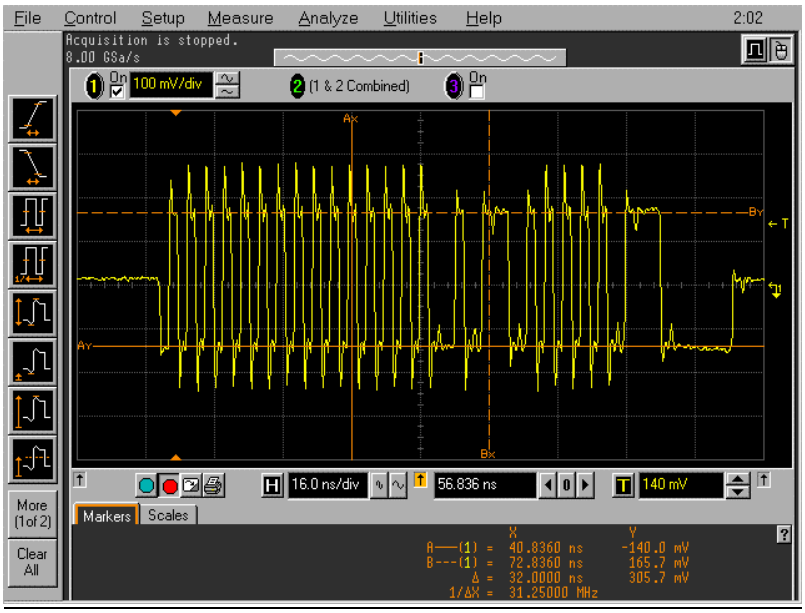
Receiver Respond with NAK to IN from Data Generator

9. On the data generator select [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen (For creating the setup files used in this section, please refer to Appendix B.). Use the cursor and the rotary knob to select the IN_ADD1.ST0 setup file. Move the cursor to [Perform Operation] and turn the knob to select [Recall]. Then press [ENTER] key to load it.
10. Verify that all packets are NAK'd while signaling is at this amplitude.
11. Adjust the output level of each channel as follows:
12. Select the [LEVELS] softkey. If [LEVELS] is not in the menu, press [MORE] key until [LEVELS] comes up. Then move the cursor to the numeric value for [High] voltage value. Adjust the output level with the rotary knob or using the number keys while monitoring the actual level on the oscilloscope. Use the cursor arrow buttons to select the channel to change.
13. Reduce the amplitude of the data generator packets in 20mV steps (on the generator before the attenuator) while monitoring the NAK response from the device on the oscilloscope. The adjustment should be made to both channels such that OUTPUT1 and OUTPUT2 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begins to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.
14. Measure the Zero to Positive Peak and Negative Peak of the packet from the data using the following method. First, use the oscilloscope mouse to draw the zoom box around the data generator packet by pressing the "left" button and dragging the mouse. Zoom in the waveform by clicking inside the "Zoom Box" (see the "Zoom Box" figure below). Repeat this step until the packet becomes adequate size for the measurement (see the "Measuring the Packet Amplitude" figure below).
15. Press [Marker A] below the oscilloscope display to turn on the markers. Click the "right" mouse button in the "Markers" section at the bottom of the oscilloscope display, and select "Markers

Manual Placement". Drag [By] to the Positive Peak and Drag [Ay] to the Negative Peak. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Read out the [Ay] and [By] values and record the measurement in EL_17 (see the "Measuring the Packet Amplitude" figure below). As long as the receiver continue to NAK the data generator packet above +/- 150mV, it is considers pass the test. Record PASS/FAIL in EL_17.



Zoom Box

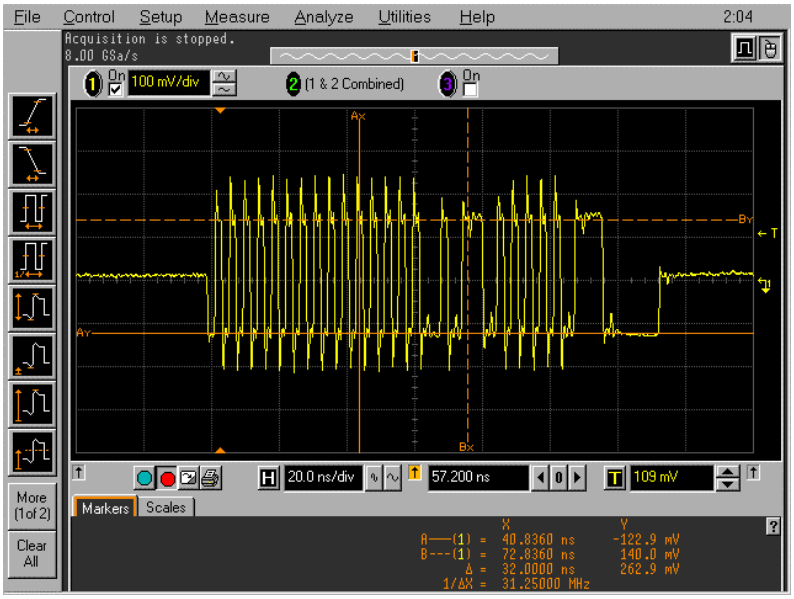


Measuring the Packet Amplitude

16. Click "right" mouse button in the main oscilloscope screen with no waveform. From the menu, select "Undo Zoom" until screen shot from step 9 comes up. Now further reduce the amplitude of the packet from the data generator in small steps. Still maintaining balance between OUTPUT1

and OUTPUT2 until the receiver just cease to respond with NAK. This is the squelch level of the receiver.

17. Measure the Zero to Positive Peak and Negative Peak of the packet from the data generator using the method described in step 15 and 16. Record the measurement in EL_16. As long as the receiver ceases to NAK the data generator packet below +/- 100mV, it is considers pass the test. Record PASS/FAIL in EL_16.



Measuring the Packet Amplitude

Note: With certain devices making an accurate zero-to-peak measurement of the In packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the In packet at the test fixture could be considerably higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

Appendix A

A.4 Device High-speed Electrical Test Data

This section is for recording the actual test result. Please use a copy for each device to be tested.

A.4.2 Vendor and Product Information

	Please fill in all fields. Please contact your silicon supplier if you are unsure of the silicon information.
Test Date	
Vendor Name	
Vendor Complete Address	
Vendor Phone Number	
Vendor Contact, Title	
Test ID Number	
Product Name	
Product Model and Revision	
USB Silicon Vendor Name	
USB Silicon Model	
USB Silicon Part Marking	
USB Silicon Stepping	
Tested By	

A.4.3 Legacy USB Compliance Tests

Legacy USB Compliance Checklist

Legacy Test	Pass/Fail	Comments
FS SQ		
Inrush		
Interop		

P = PASS

F = FAIL

N / A = Not applicable

A.4.4 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb / s ±0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.11.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.5 Device Packet Parameters (EL_21, EL_22, EL_25)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification*, Section 8.2.

Data Packet SYNC field

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing.

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.6 Device CHIRP Timing (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail

- ❑ N/A

Comments:

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.7 Device Suspend/Resume/Reset timing (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period on the bus.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

Note: It is not feasible to measure the device transition back to high-speed operation within two bit time from the end of the resume signaling. The presence of SOF at nominal 400mV amplitude following the resume signaling is sufficient for this test.

Reference documents: USB 2.0 Specification, Section 7.1.7.7.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5.

- ❑ Pass
- ❑ Fail
- ❑ N/A

comments:

A.4.8 Device Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400 mV ±10% when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3.

Test	D+ Voltage (mV)	D- Voltage (mV)
J		
K		

- ❑ Pass

- ❑ Fail
- ❑ N/A

Comments:

EL_9 When either D+ and D- are not being driven, the output voltage must be 0V ±10 mV when terminated with precision 45 Ω resistors to ground.

Reference documents: *USB 2.0 Specification,* Section 7.1.1.3.

	Voltage (mV)
D+	
D-	

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

A.4.9 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

Reference documents: *USB 2.0 Specification,* Section 7.1.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receives packets) when a receiver exceeds 150 mV differential amplitude.

Note: A waiver may be granted if the receiver does not indicate Squelch at +/-50mV of 150mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification,* Section 7.1.

- ❑ Pass
- ❑ Fail

- ❑ N/A

Comments:

EL_16 A high-speed capable device must implement a transmission envelope detector that indicates squelch (i.e. never receives packets) when a receiver's input falls below 100 mV differential amplitude.

Note: A waiver may be granted if the receiver indicate Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pins.

Reference documents: *USB 2.0 Specification*, Section 7.1.

- ❑ Pass
- ❑ Fail
- ❑ N/A

Comments:

Appendix B

B.1 Procedure to create setup files for Agilent 81130A DSG

This section is for creating setup files “IN_ADD1.ST0” and “MIN_ADD1.ST0” for Agilent 81130A DSG.

B.1.1 “IN_ADD1.ST0” setup file

“IN_ADD1.ST0” setup file is for IN TOKEN with 32-bit sync field packet pattern

1. Pressing [SHIFT] key + [STORE (RECALL)] key and selecting 0 resets 81130A to the default setting.
2. Select [MODE/TRG] softkey and use cursor and knob to set as following.

   CONTINUOUS PATTERN of

   Pulses Out 1: NRZ Out2: NRZ

   PRBS Polynom : 2^7 –1

   Trigger Output at Segm1 Start
3. Select [TIMING] softkey. Move Cursor to Per and use rotary knob to change to Freq.

   Set frequency to 480MHz.
4. Select [LEVELS] softkey and use cursor and knob to set as following.

Ch 1		Ch 2	
Separate Outputs			
High	+800mV	High	+800mV
Low	+0mV	Low	+0mV
5. Select [PATTERN] softkey and set as following.

Segment	Length	Loopcnt	Update
1	32	1	
2	32		
3	896		
4	0		

6. Define each segment as following.

   Segment 1:

	1	2	3	4	5	6	7	8	9	10
CH1	0	1	0	1	0	1	0	1	0	1

CH2	1	0	1	0	1	0	1	0	1	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	1	0	1	0	1	0	1	0	1
CH2	1	0	1	0	1	0	1	0	1	0

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	0	1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	0	1	1

Segment 2:

	1	2	3	4	5	6	7	8	9	10
CH1	0	1	0	0	1	1	1	0	0	1
CH2	1	0	1	1	0	0	0	1	1	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	1

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	1	1	1	1	0	0	0	0	0	0	0	0
CH2	0	0	0	0	1	1	1	1	1	1	1	1

Segment 3: set all to 0

7. Start the data generator output by pressing [SHIFT] key, then [0] key for OUTPUT 1 and [SHIFT] key then [+/-] key for OUTPUT 2.
8. Insert memory card to 81130A. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Move the cursor to [Perform Operation] and turn the knob to select "Store". Then press [ENTER] key. Turn the knob to input file name as IN_ADD1, then press [ENTER] to save to memory card.

B.1.2 "MIN_ADD1.ST0" setup file

"MIN_ADD1.ST0" setup file is for IN TOKEN with 12-bit sync field packet pattern

1. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Use the cursor and the rotary knob to select the IN_ADD1.ST0 setup file. Move the cursor to [Perform Operation] and turn the knob to select "Recall". Then press [ENTER] key to load it.
2. Select [PATTERN] softkey and modify the first segment as following.

   Segment 1:

	1	2	3	4	5	6	7	8	9	10
CH1	0	0	0	0	0	0	0	0	0	0
CH2	0	0	0	0	0	0	0	0	0	0

	11	12	13	14	15	16	17	18	19	20
CH1	0	0	0	0	0	0	0	0	0	0
CH2	0	0	0	0	0	0	0	0	0	0

	21	22	23	24	25	26	27	28	29	30	31	32
CH1	0	1	0	1	0	1	0	1	0	1	0	0
CH2	1	0	1	0	1	0	1	0	1	0	1	1

3. Insert memory card to 81130A. Select the [MEMCARD] softkey. If [MEMCARD] is not in the menu, press [MORE] key until [MEMCARD] comes up. The content of the memory will appear on the screen. Move the cursor to [Perform Operation] and turn the knob to select "Store". Then press [ENTER] key. Turn the knob to input file name as "MIN_ADD1", then press [ENTER] to save to memory card.