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Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the INCITS Secretariat, ITI, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

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Introduction

The SCSI Signal Modeling Standard defines a common methodology for SCSI system signal modeling. Using this methodology, SCSI systems may be modeled accurately and consistently.

The SCSI Signal Modeling Standard is divided into the following clauses:

- Clause 1 is the scope;
- Clause 2 enumerates the normative references that apply to this standard;
- Clause 3 describes the definitions, symbols, conventions and abbreviations used in this report;
- Clause 4 provides a general overview of the concepts within this report;
- Clause 5 describes the modeling methodologies;
- Clause 6 describes the model characteristics;
- Clause 7 describes model assembliages;
- Clause 8 describes the measurement and validation methodologies;
- Clause 9 describes the simulation strategies;

Annexes A, B, and C form an integral part of this Standard.

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Information technology - SCSI Signal Modeling-2 (SSM-2)

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SCSI Signal Modeling-2 (SSM-2)

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ABSTRACT

This standard defines a common methodology for modeling and simulating SCSI systems accurately and consistantly. It establishes the requirements for the exchange of perfomance information between components suppliers and system simulators. It defines the acceptable methods for extracting the electrical and perfomance attributes of the constituent parts of the SCSI parallel interface. It establishes a common methodolgy for simulating the SCSI physical environment. It is intended to be used in conjunction with the requirements within the SCSI Parallel Interface (SPI-x) family of standards.

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1 Scope

This Standard establishes a common methodology for SCSI system signal modeling. Using this methodology, SCSI systems may be modeled accurately and consistently. This Standard establishes the requirements for the exchange of signal performance information between component suppliers, system integrators, and those carrying-out simulations. This Standard defines the acceptable methods for extracting the electrical and signal performance attributes of the constituent parts of a SCSI bus segment. This Standard establishes the acceptable methods for modeling these parts. It shall be used in conjunction with the requirements within the SCSI Parallel Interface (SPI-x) family of standards.

The objectives of the SCSI Signal Modeling (SSM-2) Standard are to:

a) create a framework that shows how SCSI signal modeling fits within the context of a SCSI bus segment,
b) define the modeling parameters of the component sets,
c) define a set of elemental components of the SCSI parallel interface,
d) define a set of composite components of the SCSI parallel interface,
e) define the interface boundaries of the component sets,
f) define the general signal modeling methodologies that apply to the SCSI parallel interface,
g) define the only acceptable model types and formats for the exchange of performance information and model structure for each component,
h) define the methodology for translating between physical measurements and necessary modeling parameters, and
i) define a method for the exchange of information between component suppliers and system integrators.

2 References

2.1 Overview

The documents named in this section contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. Parties using this document are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

SCSI clause
Approved ANSI standards;
Approved and draft regional and international standards (ISO, IEC, CEN/CENELEC and ITUT); and
Approved foreign standards (including BIS, JIS and DIN).

2.2 Approved references

ANSI Standard X3.302:1998, SCSI Parallel Interface 2 (SPI-2)[1]
EIA-656-A-1999, I/O Buffer Information Specification[2]
IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronic Terms[3]
INCITS.336:2000, SCSI Parallel Interface - 3 (SPI-3)[4]
INCITS TR-23:1999, Enhanced Parallel Interface (EPI)[5]
INCITS.362-200x, SCSI Parallel Interface - 4 (SPI-4)[4]

2.3 References under development

T10/1439-DT Passive Interconnect Performance (PIP)
T10/1525-D SCSI Parallel Interface - 5 (SPI-5)

1. Available from the ANSI Customer Service Department by telephone at (212) 642-4900, by FAX at (212) 302-1286 or via the world wide web at http://www.ansi.org.
2. Available from the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834
3. Available from the Institute of Electrical and Electronic Engineers, Inc. 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331 USA
4. Available from Global Engineering at (303) 792-2181 or the INCITS Secretariat, 1250 Eye Street, NW Suite 200, Washington, DC 20005.
5. *IBID*

3 Definitions, acronyms, symbols, abbreviations, keywords, and conventions

3.1 Definitions

3.1.1 Precedence of Definitions Authority:

The precedence of authority for definitions in this section are:

1) IEEE Standard Dictionary of Electrical and Electronic Terms[1]
2) National Committee for Information Technology Standards Draft American National Standard Dictionary for Information Technology[2]
3) ANSI X3.302:1998, SCSI Parallel Interface - 2 (SPI-2)[3]

3.1.2 Accuracy: The quality of freedom from mistake or error. The degree of correctness with which a measured value agrees with the true value. Not to be confused with precision - see 3.1.77.

3.1.3 Admittance: In an *n*-terminal network, the complex current flowing to the *i*-th terminal divided by the complex voltage applied between the *j*-th terminal with respect to the reference point when all other terminals have arbitrary terminations. The inverse of impedance.

3.1.4 American Wire Gauge: Formerly the Brown & Sharpe Gage, the standard gauge for copper, aluminum, and other conductors except steel.

3.1.5 Assembly: A subordinate element of a system that is comprised of two or more components

3.1.6 Asserted: Having a current value equal to a logic 1.

3.1.7 Attenuation: A general term used to denote a decrease in signal magnitude from one point to another. Attenuation may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio. Attenuation is the reciprocal of gain.

3.1.8 Backplane: The printed circuit board that contains the interconnect traces and connectors, into which boards or plug-in units are inserted.

3.1.9 Balanced: 1) The state of impedance on a two-wire circuit when the impedance-to-ground of one wire is equal from the impedance-to-ground of the other wire. 2) A circuit, in which two branches are electrically alike and symmetrical with respect to a common reference point, usually ground.

3.1.10 Buffer: In the sense of the IBIS standard, an isolating circuit used to prevent a driven circuit from influencing a driving circuit. A transceiver, see 3.1.102.

3.1.11 Bulk cable: Cable that is not connector terminated.

3.1.12 Bus: A signal line or a set of lines used by an interface system to connect a number of devices and transfer data.

3.1.13 Cable assembly: A cable that is connector terminated. Generally, a cable that has been terminated by a manufacturer and is ready for installation.

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1. Available from the Institute of Electrical and Electronic Engineers, Inc. 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331 USA
2. Available from INCITS, Information Technology Industry Council, 1250 Eye Street NW, Suite 200, Washington, DC 20005
3. Available from the ANSI Customer Service Department by telephone at (212) 642-4900, by FAX at (212) 302-1286 or via the world wide web at http://www.ansi.org.

3.1.14 Capacitive coupling: The type of coupling in which the mechanism is capacitance between the interference source, and the signal system; that is, the interference is induced in the signal system by an electric field produced by the interfering source.

3.1.15 Circuit: An interconnection of electrical components.

3.1.16 Circuit element: A basic constituent part of a circuit, exclusive of interconnections. A component.

3.1.17 Common-mode: The instantaneous algebraic average of two signals applied to a balanced circuit, both signals referred to a common reference.

3.1.18 Common-mode noise: The noise voltage that appears equally and in phase from each signal conductor to ground.

3.1.19 Component: Items from which a system, assembly, or sub-assembly is assembled; for example, resistors, capacitors, inductors, semiconductors, etc. A circuit element.

3.1.20 Complementary metal oxide semiconductor: A semiconductor technology in which circuits are composed of paired NMOS and PMOS devices.

3.1.21 Complex dielectric constant: The complex permittivity of a physical medium in ration to the permittivity of free space.

3.1.22 Complex permittivity: For isotropic media, the ratio of the complex amplitude of the electric displacement density to the complex amplitude of the electric field strength.

3.1.23 Computer-aided engineering: The application of computers to the engineering process. The term applies to any computer system or program that manipulates data for the purpose or assisting engineering, design, procurement, maintenance, etc.

3.1.24 Conductivity: (σ) A macroscopic material property that relates the conduction current density (*J*) to the electric field (*E*) in the medium.

3.1.25 Connector terminated: A section of cable with connectors attached.

3.1.26 Contact: The electrically conductive portion of a connector associated with a single conductor in a cable.

3.1.27 De-asserted: Having a current value equal to a logic 0.

3.1.28 Device: An electron device. See 3.1.39

3.1.29 Dielectric constant: 1) That physical property which determines the electrostatic energy stored per unit volume for unit potential gradient. This value is usually is given relative to vacuum. 2) The real part of the complex dielectric constant.

3.1.30 Dielectric loss: That contribution to the attenuation constant of a propagating mode on a transmission line that represents losses associated with the dielectric properties of the insulation materials involved.

3.1.31 Differential-mode: The instantaneous algebraic difference of two signals applied to a balanced circuit, both signals referred to a common reference.

3.1.32 Differential-mode noise: The noise voltage that appears differentially between two signal wires and acts on the signal sensing circuit in the same manner as the desired signal.

3.1.33 Differential SCSI: A SCSI signal configuration that uses balanced transmission lines.

3.1.34 Discontinuity: 1) An abrupt non uniformity in a uniform transmission line that causes reflected waves. 2) An abrupt change in the cross section of the planar transmission line. Abrupt refers usually to a change in dimensions or material over a length short compared to a wavelength. Short is generally recognized as 0,1 wavelength or smaller.

3.1.35 Driver: 1) An electronic circuit that supplies input to another electronic circuit. 2) An electrical circuit whose purpose is to signal a binary state for transmitting information. Also referred to as a generator in international standards.

3.1.36 Electromagnetic compatibility: A system's ability to perform its specified functions in the presence of electrical noise generated either internally or externally by other systems.

3.1.37 Electromagnetic interference: Electromagnetic energy from sources internal or external to electrical or electronic equipment that adversely affect equipment by creating undesirable responses.

3.1.38 Electrostatic discharge: The sudden transfer of charge between bodies of differing electrostatic potential.

3.1.39 Electron device: A device in which conduction is principally by electrons moving though a vacuum, gas, or semiconductor.

3.1.40 Element: A component, subcomponent, assembly, subassembly, or part of a physical architecture or system.

3.1.41 Expander: A device that connects SCSI device segments together to form a single SCSI domain. See SDV.

3.1.42 False: One of two binary states the other of which is true. False is usually represented by 0.

3.1.43 Gain: A general term used to denote a increase in signal magnitude from one point to another. Attenuation may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio. Gain is the reciprocal of attenuation.

3.1.44 Group delay: The derivative of radian phase with respect to radian frequency $\delta\phi/\delta\omega$. Group delay is equal to the phase delay for an ideal non dispersive device or medium, but may differ greatly in an actual device or medium where there is ripple in the phase versus frequency characteristic. In practice, $\Delta\omega$ shall be sufficiently large to permit adequate measurement resolution. If $\Delta\omega$ is too large, the limit in the defining equation will not be reached, and the measured group delay will be dependent upon $\Delta\omega$. Therefore the value of $\Delta\omega$ used in a measurement shall be specified.

3.1.45 Group delay time: The rate of change, with angular frequency, of the total phase shift through a network. Group delay time is the time interval required for the crest of a group of interfering waves to travel thorough a 2-port network, where the component wave trains have slightly different individual frequencies.

3.1.46 Group velocity: The velocity of propagation of the signal envelope, provided that the envelope moves without a significant change of shape. The magnitude of the group velocity is equal to the reciprocal of the rate of change of phase constant with angular frequency.

3.1.47 Hardware description language: A computer language with special constructs and verification protocols, used to develop, analyze, validate, and document a hardware design or computer architecture.

3.1.48 High: The higher of two voltages used to convey a single bit of information. For positive logic, a logic 1.

3.1.49 Inductive coupling: The type of coupling in which the mechanism is inductance between the interference source, and the signal system; that is, the interference is induced in the signal system by a magnetic field produced by the interfering source.

3.1.50 Insulation displacement contact: A type of contact where the connection to the cable is made by mechanically piercing the cable insulation as opposed to a connection in which the cable insulation is removed to provide access to the conductor.

3.1.51 Interconnect component: Interconnect components include cables, connectors, printed circuitboards and transition regions. All interconnect components are passive.

3.1.52 Isotropic: Pertaining to a material whose electric or magnetic properties, or both, are directionally independent.

3.1.53 Logical unit: An externally addressable entity within a target and processes SCSI commands.

3.1.54 Least significant: Within a group of items that, taken as a whole, represents a numerical value, the item within the group with the smallest numerical weighting.

3.1.55 Loss tangent: The ratio of the imaginary part of the complex dielectric constant of a material to its real part.

3.1.56 Low: The lower of two voltages used to convey a single information bit. For positive logic, a logic 0.

3.1.57 Magnetic coupling: Synonomous with Inductive coupling. See 3.1.49.

3.1.58 Mhos: The reciprocal of ohms

3.1.59 Microstrip: A class of planar transmission lines consisting of one or more thin conducting strips of finite width parallel to a single extended conducting ground plane. The strips are fixed to an insulating substrate attached to the ground plane. The semi-infinite space above the strips is filled with a medium of relative permittivity an permeability equal to or less than the substrate.

3.1.60 Mode: A transmission mode.

3.1.61 Model: 1) An approximation, representation, or idealization of selected aspects of the structure, behavior, operation, or other characteristics of a real-world process, concept, or system. Models may have other models as components. 2) To serve as a model in definition 1. 3) To develop or use a model as in definition 1.

3.1.62 Most significant: Within a group of items that, taken as a whole, represents a numerical value, the item within the group with the greatest numerical weighting.

3.1.63 Multiline: A model representation of a multi-conductor component that includes the capacitive and inductive coupling among the conductors.

3.1.64 Network: Any set of devices or subsystems connected by links joining, directly or indirectly, a set of terminal nodes.

3.1.65 Netlist: A listing of the nets of a circuit, providing, usually in text format, a description of the connections among the components of the circuit.

3.1.66 Network function: Any impedance, admittance function or any other function of p that can be expressed in terms of or derived from the determinant of a network and its cofactors. This also includes voltage ratios, current ratios, and numerous other quantities.

3.1.67 Network matrix: Anyone of several matrices that relate the equivalent voltage, current, incident waves and reflected waves of an *n*-port network.

3.1.68 Network parameters: The elements of a network matrix.

3.1.69 One: A true logic state.

3.1.70 Phase angle: The measure of the progression of a periodic wave in time or space from a chosen instant or position.

3.1.71 Phase delay: The ration of total radian phase shift, to the specified radian frequency. Phase delay is nominally constant over the frequency band of operation for nondestructive delay components.

3.1.72 Phase shift: 1) The absolute magnitude of the difference between two phase angles. 2) The displacement in time of one periodic-waveform relative to other waveforms.

3.1.73 Phase velocity: The velocity of an equiphase surface normal to the direction of propagation of a traveling wave at a single frequency, and for a given mode.

3.1.74 Planar transmission line: A transmission line composed of one or more parallel plates, slabs, or sheets of conduction or insulating material, including free space, and in which one or more layers are composed of material of differing electromagnetic properties, arranged in strips of finite cross section and aligned with the axis of propagation to form the guiding structures.

3.1.75 Pole: A value of *s* that makes a transfer function in the complex variable infinity, or its corresponding point in the *s* plane.

3.1.76 Port: A place of access to a network where the network variables may be observed or measured.

3.1.77 Precision: 1) The degree of exactness or discrimination with which a quantity is stated. For example 3 decimal places versus 5 decimal places. 2) The repeatability of measurement data expressed in terms of standard deviation.

3.1.78 Primary bus: The collection of signals that provides the system with the basic mechanism for exchanging data.

3.1.79 Radio frequency: A frequency in the range of 10KHz to 100 000MHz.

3.1.80 Radio frequency interference: Degradation of a wanted signal by an electromagnetic disturbance having components in the RF range.

3.1.81 Receiver: 1) An electronic circuit that recognizes input from another electronic circuit. 2) An electrical circuit whose purpose is to recognize the binary state of transmitted information.

3.1.82 Resistivity: The reciprocal of volume conductivity measured in siemens per centimeter.

3.1.83 S parameter: One of the coefficients of the scattering matrix.

3.1.84 S plane: A two-dimensional space determined by two orthogonal axes - a real number axis and a complex number axis. A complex number "s" has a real and imaginary component represented by sigma and omega, respectively.

3.1.85 Scattering matrix: A square array used to relate incident and reflected waves for an n-port network.

3.1.86 SCSI bus segment: All the conductors and connectors required to attain signal line continuity between every driver, receiver, and terminator for each signal.

3.1.87 SCSI component: A component part of a complete SCSI system. SCSI components include but are not limited to: cables, cable assemblies, devices, terminators, boards, backplanes, controllers, and chips.

3.1.88 SCSI device: A device that contains one or more SCSI ports that are connected to a service delivery subsystem and supports a SCSI application protocol. See SAM-2.

3.1.89 SCSI port: A single attachment to a SCSI bus from a SCSI device.

3.1.90 Signal assertion: The act of driving a signal to the true state.

3.1.91 Signal negation: The act of performing a signal release or of driving a signal to the false state.

3.1.92 Single line: A model representation of a multi-conductor component that does not include the capacitive and inductive coupling among the conductors.

3.1.93 Single-ended SCSI: A SCSI signal configuration that uses unbalanced transmission lines.

3.1.94 Skin depth: Of a conducting material, at a given frequency, the depth at which the surface current density is reduced to 1/*e* of its value at the surface.

3.1.95 Skin effect: The tendency of alternating current to concentrate in the areas of lowest impedance.

3.1.96 Small Computer System Interface: A data-transfer interface used to connect multiple peripheral devices such as disk derives, tapes, or printers to computer systems while taking up only one slot in the computer. Previously this was known as Shugart Associates Systems Interface.

3.1.97 Simulation Program with Integrated Circuit Emphasis: An application-oriented programming language used widely to design electrical circuits.

3.1.98 State: The value assumed at a given instant by a signal or variable.

3.1.99 Stripline: A class of planar transmission line characterized by one or more conducting strips of finite width parallel to and approximately midway between tow extended conducting ground planes. The space between the planes is filled with a homogeneous insulation medium.

3.1.100 Stub: A section of transmission line joined to the main transmission line and containing a non dissipative termination.

3.1.101 System: In a hierarchical approach, a collection of interacting, interrelated, or interdependent elements forming a collective functioning entity.

3.1.102 Transceiver: A device that both transmits and receives data.

3.1.103 Transition region: The locality in a transmission system where the transmission medium changes from one entity to another.

3.1.104 Transmission line: A structure designed to guide the propagation of electromagnetic energy in a well-defined direction.

3.1.105 Transmission medium: The material on which information signals may be carried. For example: twisted wire pairs, planar transmission lines, coaxial cable, etc.

3.1.106 Transmission mode: A form of propagation along a transmission line characterized by the presence of one of the elemental type of transverse electric, transverse magnetic, or transverse electromagnetic waves.

3.1.107 Transmittance: A response function for which the variables are measured at different ports.

3.1.108 True: One of two binary states, usually represented by 1, the other of which is false.

3.1.109 Two-port parameters: The network parameters for a two-port device.

3.1.110 Unbalanced: 1) The state of impedance on a two-wire circuit where the impedance-to-ground of one wire is different from the impedance-to-ground of the other wire. 2) Unbalanced frequently signifies a circuit where one side is grounded.

3.1.111 Uniform transmission line: A transmission line that has substantially identical electrical properties throughout its length.

3.1.112 Validation: The process of evaluating a system or component to ensure compliance with the functional, performance, and interface requirements.

3.1.113 Vendor-specific: A term used to describe parameters that may vary between vendors supplying similar components.

3.1.114 Verification: Confirmation by examination (testing) with evidence that specified requirements have been met.

3.1.115 Verilog[1]: An IEEE standard C-like hardware descriptor language used to describe a digital system, for example, a computer or a component of a computer. It describes designs at a high level of abstraction such as at the architectural or behavioral level as well as the lower implementation levels.

3.1.116 Via: An electrical connection between the layers of a printed circuit board.

3.1.117 VHDL: An IEEE standard Ada-like hardware descriptor language used to describe a digital system, for example, a computer or a component of a computer. It describe designs at a high level of abstraction such as at the architectural or behavioral level as well as the lower implementation levels

3.1.118 Y parameter: The input, output, or transfer admittance matrix, y_{11}, y_{22}, y_{12}, of a four-terminal network when the far end is short-circuited.

3.1.119 Zero: 1) A false logic state. 2) Any value of ρ, real or complex for which the network function is zero. 3) A value of *s* that makes a transfer function in the complex variable zero, or its corresponding point in the *s* plane.

3.2 Acronyms

AWG	American wire gauge
CAE	Computer-aided engineering
CMOS	Complementary metal-oxide semiconductor
DUT	Device under test
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESD	Electrostatic discharge
HBA	Host bus adapter
HDD	Hard disk drive
HDL	High level design language
HVD	High voltage differential
IBIS	I/O Buffer Interface Specification
IDC	Insulation displacement contact
ISI	Inter-symbol interference
LSB	Least significant bit
LVD	Low voltage differential
MSB	Most significant bit

1. A registered trademark of Cadence Design Systems, Inc.

NEXT	Near end crosstalk
PCB	Printed circuit board
RF	Radio frequency
RFI	Radio frequency interference
RLGC	resistance, inductance, admittance, capacitance
SCSI	Small Computer System Interface.
SE	Single-ended
SPICE	Simulation Program with Integrated Circuit Emphasis
SPI-x	The family of SCSI Parallel Interface - x (SPI-x) standards
URL	Uniform Resource Locator
VHDL	Very high level descriptor language

3.3 Symbols and abbreviations

±	plus or minus
≈	approximately
x	multiply
+	add
-	subtract
< or LT	less than
≤ or LE	less than or equal
= or EQ	equal
> or GT	greater than
≥ or GE	greater than or equal
≠ or NE	not equal

A	ampere
c	velocity of light in a vacuum
C	coulomb
dB	decibel
F	farad
g	gram
H	henry
Hz	hertz
J	joule
m	meter
N	newton
Np	neper
Ω	ohms
s	second
s	s-parameter
T	tesla
t	time
V	volt
W	watt
Wb	weber

Δ	discrete differential
δ	partial differential -infinitesimal
Φ	radial phase
ρ	either conductance or admittance
Ω	ohm
ω	radians per second

E	electric field
J	current density

T	10^{12}
G	10^{9}
M	10^{6}
k	10^{3}
c	10^{-2}
m	10^{-3}
μ	10^{-6}
n	10^{-9}
p	10^{-12}
f	10^{-15}

3.4 Keywords

3.4.1 Expected: Describes the behavior of the hardware in the design models assumed by this document. Other hardware design models may also be implemented.

3.4.2 Mandatory: Indicates an item that is required to be implemented as defined in this document.

3.4.3 May: Indicates flexibility of choice with no implied preference.

3.4.4 Optional: Features that are not required to be implemented by this document. However, if any optional feature defined by this document is implemented, it shall be implemented as defined in this document.

3.4.5 Shall: Indicates a mandatory requirement. Implementation of all such requirements ensure inter-operability with other products that conform to this document.

3.4.6 Should: Indicates flexibility of choice with a preferred alternative; equivalent to the phrase “it is recommended”.

3.5 Conventions

Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in 3 or in the text where they first appear. Names of signals are in all uppercase (e.g., DT DATA IN), lower case is used for words having the normal English meaning.

All parametric data are specified in terms of fundamental MKSA units - meters, kilograms, coulombs, seconds - and their derivatives - ohms, henrys, mhos, farads, volts, amperes, etc.

Numbers that are not immediately followed by lower-case b or h are decimal values.

Numbers immediately followed by lower-case b (xxb) are binary values.

Numbers immediately followed by lower-case h (xxh) are hexadecimal values.

Decimals are indicated with a comma (e.g., two and one half is represented as 2,5).

Decimal numbers having a value exceeding 999 are represented with a space (e.g., 24 255).

An alphanumeric list (e.g., a, b, c or A, B, C) of items indicate the items in the list are unordered.

A numeric list (e.g., 1,2,3) of items indicate the items in the list are ordered (i.e., item 1 shall occur or complete before item 2).

In the event of conflicting information the precedence for requirements defined in this standard is:

1) text,
2) tables, then
3) figures.

4 General

4.1 Overview

This standard is a collection of definitions, concepts, and architectural descriptions intended to enable transportable and reproducible mathematical representation of electrical signals existing within a SCSI bus segment.

This document considers signal behavior within single SCSI bus segments. A SCSI bus segment is defined by the existence of two terminators electrically connected with provisions for SCSI devices to be attached to the common electrical path. A minimal bus segment consists of two terminators (of like type) and two SCSI devices (one or both of which may be an expander). The simulation of SCSI domains that include multiple segments connected together by expanders is not within the scope of this document, rather, single segment physical constructions are assumed.

For purposes of this document, the simplest SCSI bus segment is divided into discrete parts as depicted in Figure 1. The transceiver boards depicted in this figure are SCSI devices.

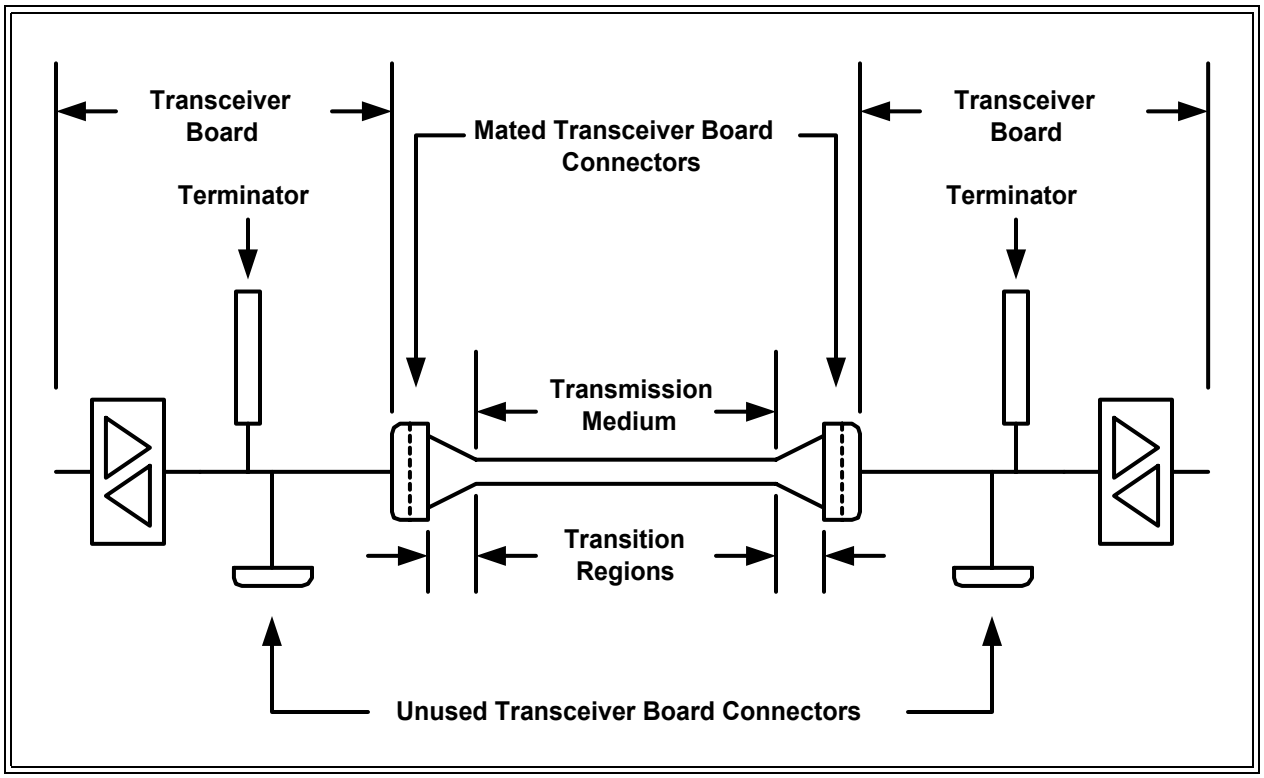


Figure 1 - Architecture for modeling minimal bus segments

Each feature identified in Figure 1 is considered a component with specific interfaces to the bus segment path.

There are more complex SCSI systems that are of major importance. Multidrop configurations are one of these. Multidrop configurations are common when using backplanes and internal cabling. The architecture depicted in figure 1 provides the basis for describing multidrop bus segments.

4.2 Signal modeling purposes

4.2.1 Overview

The results of running a simulation are modeled signals. The simulation tool inputs consists of a set of component models and a set of stimuli. Simulations are done for different reasons depending on the purpose. The details of the simulation may vary widely for the same bus segment.

The methodologies within this standard apply to several purposes. These purposes fall into two classes:

a) those that focus on different physical parts in the SCSI transmitter-receiver path as viewed by the supplier of the part
b) those that focus on the overall performance of the driver to receiver path.

For example, the description of a specific parameter for a connector or bulk cable as a part of a specification for that part falls into the first class. A system integrator using the same connector as part of a bus segment may have a very different view of what is important. The optimum approach to modeling depends strongly on the purpose.

The remainder of 4.2 describes these classes in more detail.

4.2.2 Physical components and signals

4.2.2.1 Relationship between physical and modeling terminology

The physical parts of a SCSI bus segment are generally referred to as components. Components that are not made up of lower level components are termed “elemental components”. Components that are made from lower level components are termed “composite components”. What is elemental or composite components depends on the viewpoint of the modeler. Bulk cable could be considered elemental for those making cable assemblies or composite for those manufacturing bulk cable. If a person were making the bulk cable elemental components could be the primary copper wire, the dielectric material, and the shield conductors. In order to provide a consistent view in this document a set of conventions are used to determine whether a component is elemental or composite.

From a modeling perspective there is no requirement to divide the parts of the model into a hierarchical relationship. Models can be constructed that are not physically realizable. However, if the model applies only to a portion of the SCSI bus segment the model may be referred to in a manner similar to the physical description; for example: system models, component models, etc. For composite components, standardized constructions using the elemental models are defined in this document for specific types of composite components.

Within any specific type of model a standard construction is defined that contains all the essential constituents for that type of model. These constructions are specific types of composite components that have unique delineation in the SCSI environment.

4.2.2.2 Elemental components

Elemental components are limited to the following:

a) bulk cable - passive
b) mated connectors - passive
c) un-mated connector halves - passive
d) transceivers - active
e) terminators - passive, active
f) unpopulated printed circuit boards - passive
g) instrumentation probes - passive, active

h) instrumentation - passive, active
i) cable assembly transition regions - passive

4.2.2.3 Composite components

Standard model constructions are composite components. These constructions are limited to the following:

a) cable assemblies
b) target boards
c) host bus adapter boards
d) backplanes
e) terminator modules with integral connectors

4.2.2.4 Systems

Systems are a special case of a composite component and are the next hierarchical level. It consists of a collection of standard model constructions, and possibly elemental components, that form a collective functioning entity, see 3.1.101. It is the only construction that can pass data from one transceiver to another. Systems can be either instrumented and non-instrumented. An instrumented system is one that has measurement instrumentation and probes attached. A non-instrumented system is one as it exists in service.

4.2.2.5 Signals and measurement points

Signals are time and frequency dependent voltage or current waveforms that carry information. They may be described by a set of parameters.

Signals emanate from a SCSI transmitter and propagate along the transmission medium until they reach the receiver. The parameters describing the signal change as the signal propagates. These changes are due to effects along the path**.** With a valid system model, a signal may be derived at any point along the path. The point where the signal is derived or measured shall be provided along with the signal parameters.

Signals may be calculated at any point, but certain points in the segment are designated as interoperability points. These points are where the SPI-x family of standards place requirements on the signals. Signals at points other than interoperability points are useful for a variety of purposes.

Figure 2 shows approximate positions where a SCSI device connector exists indicated by a “Y”. It is only at these points in a segment where the requirements on signals specified in SPI-x apply and only at these points where interoperability is defined by SPI-x.

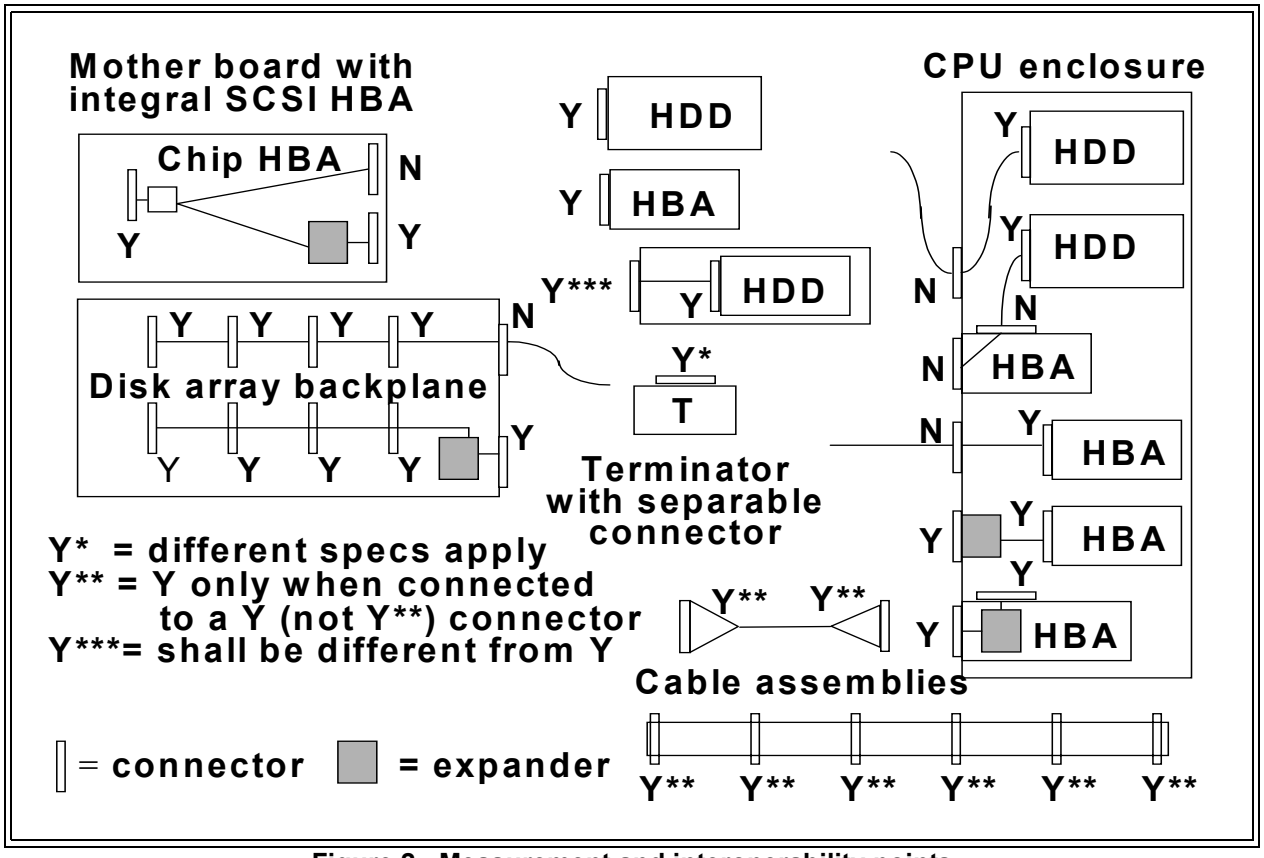


Figure 2 - Measurement and interoperability points

Note that there are many connectors possible where interoperability is not defined by SPI-x as indicated by an “N” and other conditions where the details of the configuration determine whether the connector is a defined interoperability point or not.

4.2.2.6 Run length dependent driver signals

SPI-4 defines SCSI driver signals into the transmission medium where the amplitude of the signal depends on the run length in the data pattern. This is used to help compensate for intersymbol interference that is caused by the interconnect not having a uniform frequency response. Drivers whose output depends on the run length of the data pattern will be addressed in IBIS 4.0. Simulation tools that incorporate drivers with run length dependent amplitudes were not available until 1Q2002. The methodologies in this document assume that the signals from the driver may be adequately described by the tools.

4.2.2.7 Interactions between signals on different signal lines

When a signal is traveling in one signal line it induces noise on other signal lines in the system. Such noise coupling is an important part of SCSI technology. Multiline models incorporate more than one signal line. Although good SCSI construction is designed to keep the most severely affected lines separated, this is not always possible.

Depending on the simulation goals, especially accuracy, multiline models may be required. A determination that a multiline model is not required should first be made before assuming that a single line model is adequate.

4.2.3 Viewpoints

The general utility of modeling encompasses many applications. The approach to the modeling effort depends on the viewpoint and goals of the user.

Viewpoints include: the system integrator, the elemental component supplier, and a number of others.

A system integrator may be concerned with robust operation of the segment under the conditions where the parts that comprise the segment may be removed and replaced with other parts that are nominally the same but may come from different suppliers. Such system level interchangeable parts always have separable connectors and the behavior at these connectors is the most important focus. The integrator needs to be sure that the configurations he is selling are robust and are not operating near unacceptable pitfalls. Therefore, the system integrator will focus on the signals at or near connectors and will do sensitivity characterization to variables that will be present in the composite components he is using to build his configurations.

A system integrator varies things like temperature, power supply voltage, segment loading due to different device populations, electrical length between connectors, frequency response of terminators, ambient noise, power supply transients, and the entire range of parameters allowed for the individual component performance.

A chip supplier could consider that his primary interface is the chip pads and that he would like the chip to be useful for a wide variety of printed circuit board designs. Thus, for the chip supplier, the signal coming out of the chip pads is the primary focus. The loading of the circuitry that attaches to the chip may be a critical parameter. Other area of interest to chip suppliers include effects of the chip package and effects of worst case corners of process, temperature, and supply voltage.

The kind of modeling process used, the output format, the parameters of the launched signal, and the choice of the parameters of the components that comprise the segment may all strongly depend on the viewpoint point of the user.

The signals launched from the driver as shown in Figure 2 provide the source for the propagating signal and is the only place where one can change the properties of the signals at other points in the segment for a given physical segment. This property has significant implications when modeling from the point of view of the device connector since the driver signal does not emanate directly from the device connector.

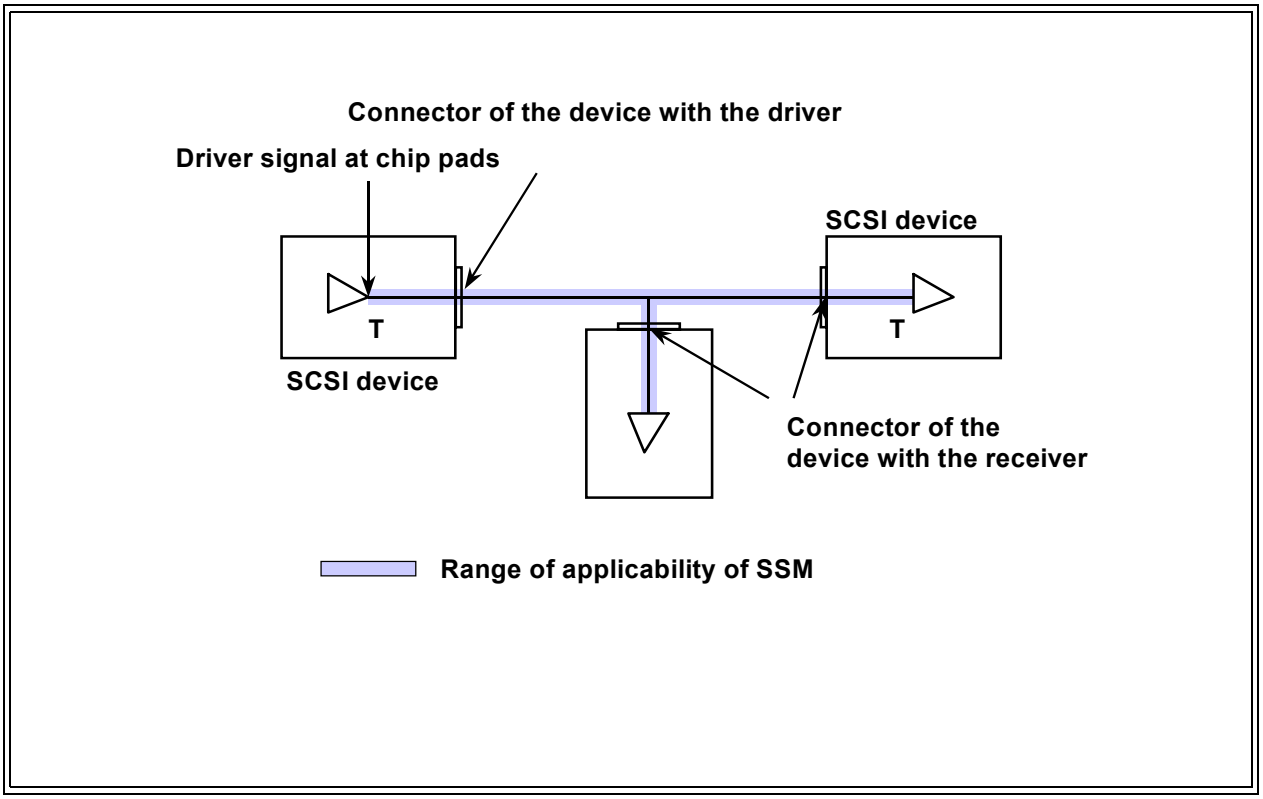


Figure 3 - SSM-2 applicability to a SCSI segment

Since SPI-x defines the properties of the signals at the device connector there are two fundamental viewpoints:

a) From the supplier of the signal
b) From the “user” of the signal or the interconnect

From a signal supplier perspective the focus may be whether a specific driver delivers a compliant signal at the device connector under a worst case loading condition. The modeling process is relatively straightforward in this case. One calculates the signal at the device connector and compares it to the specification requirements.

From the perspective of user of the signal the focus is on whether the interconnect can transport a minimal quality signal at the device connector of the SCSI device with the driver to the device connector of the SCSI device with the receiver. This requires creating a signal at the device connector that has specific properties and these required properties may not be that produced by the driver model. One would hope that good driver models would not produce minimal quality signals at the device connector. Therefore, one is faced with creating a signal launch condition at the device connector where the signal does not come from a real SCSI driver. Creating such a launch condition by artificially changing the properties of a driver model is very difficult, highly iterative, and likely to produce a significantly unrealistic condition.

Such launch conditions may easily be created in a model by placing ideal sources right at the device connector (see Figure 4) but they will not include the effects of the electrical paths on the SCSI device containing the driver. At the present state this direct launch from the device connector is the method available for this application.

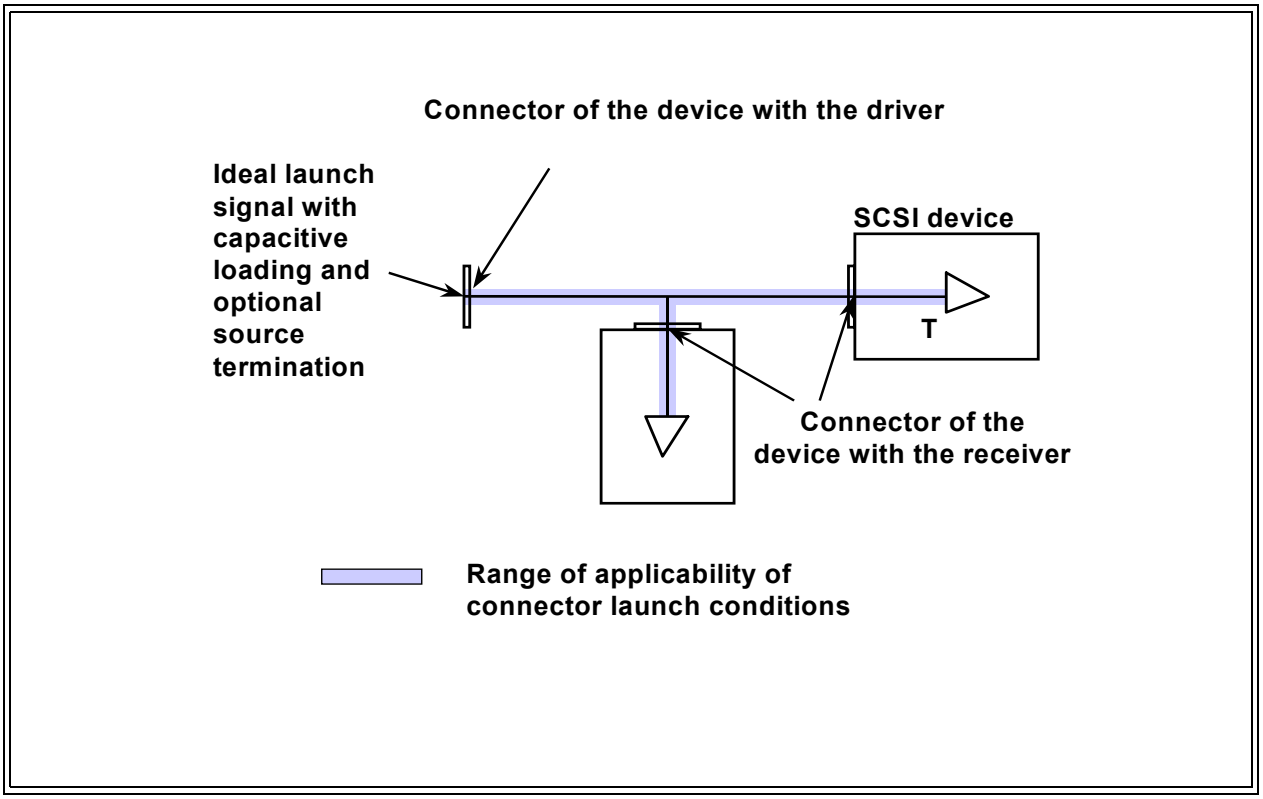


Figure 4 - Modeling architecture for launching a specific signal at a connector

4.3 Application to measurement

A major goal of the methodologies in this document is to achieve an accurate representation of signals at the precise interoperability points of real systems. By accounting for the difference between the measured signal parameters and the signal parameters at the desired physical location one may enable a practical scheme for enforcing the specifications. One important application for this capability is where it is not practical to access the physical location where the signal parameters are needed due to mechanical constraints in the system design.

A simple example is a backplane system that uses disk drives. If the signal at the pad of the SCSI chip on the disk drive is the desired location but the only accessible point is on the through pins of the backplane connector then the difference between the signals measured at the accessible point and the signals existing at the desired point is needed.

If an accurate model of the system exists one can determine the difference between the signals at the accessible point and the desired point and thereby construct an accurate representation of the signal at the desired point.

The methodologies in this document do not presently allow direct construction of a new signal at a different point in the system from the signal that is measured. The process that may be used essentially is that once the signal at a known point in the system (even if this point is not the desired point) is determined to be that predicted by the system model then signals at other points in the system may be calculated with confidence. This is not the same as directly providing a correction function for the measured signal but it significantly better than not having any idea of the error caused by inability to access the desired point.

Another important feature of applying modeling to measurement techniques is knowledge of the sensitivity of the measurement to the details of the measurement process. For example, how precisely should the position of a probe be controlled? How much disturbance to the system is being caused by the instrumentation equipment?

4.4 Practical considerations for creating models

There is an intrinsic trade-off in modeling between the accuracy of the model and the practical ability to run the required simulations. In general, the more accurate the model the more resources it consumes for simulation. When determining whether to use distributed or lumped models, a good rule of thumb is to use distributed models when the element is longer than 0,1 of the shortest wavelength and lumped in all other cases.

The resources involved are storage required for the model description, time required to assemble a complete package for simulation, and the time required for executing the simulation. Additional resources are required to create the tangible results and to interpret them.

Iteration may be required on the parameters of the model in order to achieve acceptable correlation with measurement and the conditions used to attain agreement need to be rationalized with the known properties of the system under consideration.

Lines of code required to describe the component model, frequency of use of the same component model in the same simulation, number of lines used in a multiline model, granularity used, and the number of details included are all contributors to the resources required to execute the simulation.

Good engineering judgment shall be exercised in determining the complexity of the model required for the application.

4.5 Relationship between components of the modeling environment

a) The relationships among the various components of the modeling environment are depicted in Figure 5.

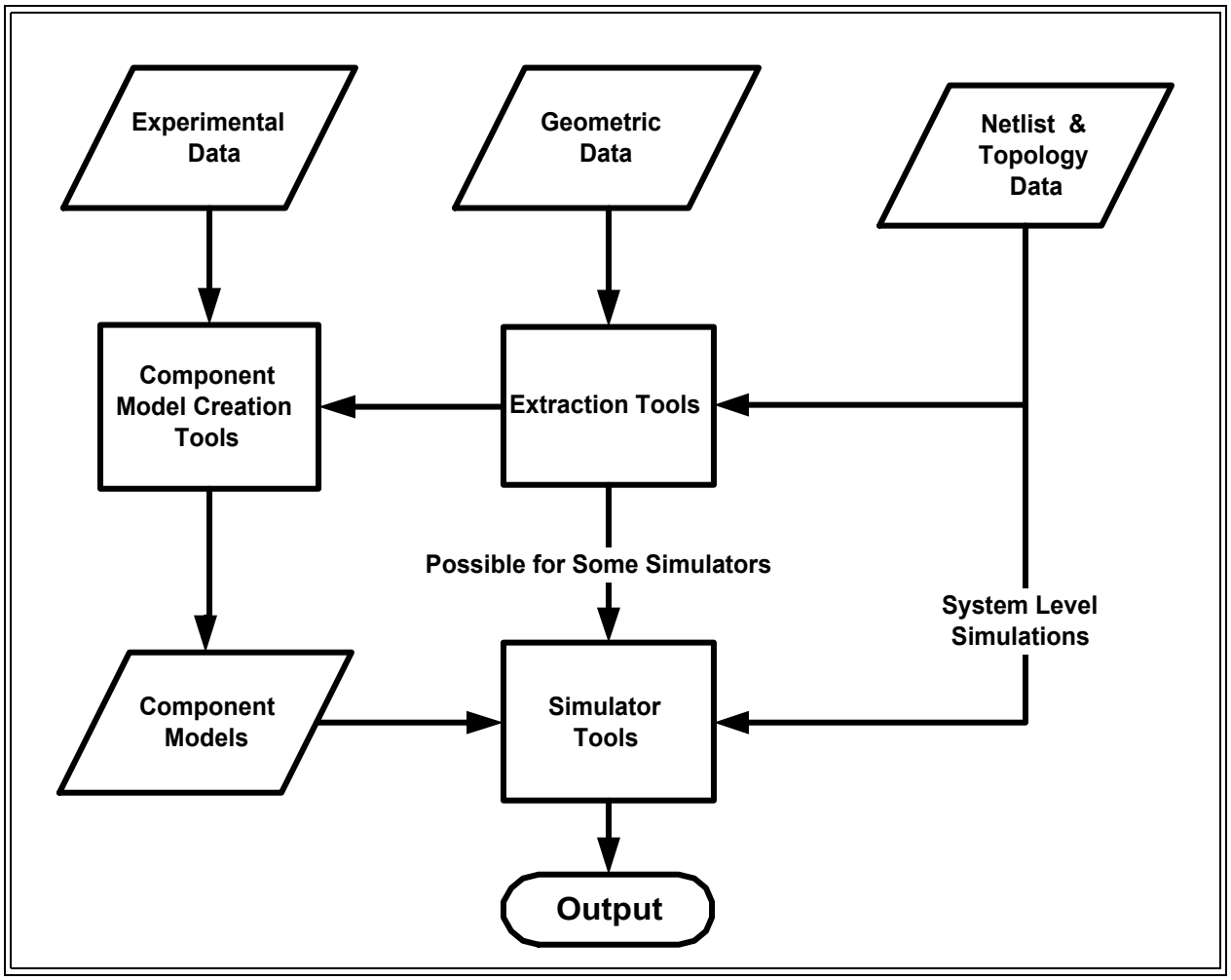


Figure 5 - Simulation environment

These simulation components are categorized as:

a) experimental data - data gathered by mechanical and electrical measurements
b) geometric data - information that describes the physical dimensions and material properties
c) netlist & topology data - geometric description of the printed circuit board topology and materials properties
d) extraction tools - software packages that use geometric data to create a parametric description of the object
e) component model creation tools - software packages that use either experimental data or the output of an extraction tool to create the component model
f) component models - either a behavioral/functional or circuit/SPICE description of a component
g) simulator tools -software packages that use any or all of the above to produce an output representing signals
h) output - results from the simulation tool

4.6 Relationship between signal specifications in standards and modeling

In many instances the signal specifications in standards and those used in modeling are essentially the same. The signal rise time parameters, however, are significantly different and this difference is described in this section.

Signal rise time describes the interval required for a signal to rise or fall between two specified limits. The rise times listed in various specifications (including SPI-x) may define threshold limits that differ from those used by simulation tools. Some interpolation or extrapolation may be required to derive values with consistent threshold limits. For example, simulation tools usually define rise time as the interval between the 0% and 100% whereas SPI-x defines rise times between the 20% and 80% points as shown in Figure 6. For the purposes of SPI-x SCSI simulation the rise times may be assumed as listed below unless otherwise specified.

a) interconnects for Single-Ended (SE) SCSI: rise time (20-80%) = 3,0 ns,
b) interconnects for Low Voltage Differential (LVD) SCSI: rise time (20-80%) = 1,0 ns.

Figure 6 shows the difference between the two methods of specifying rise time

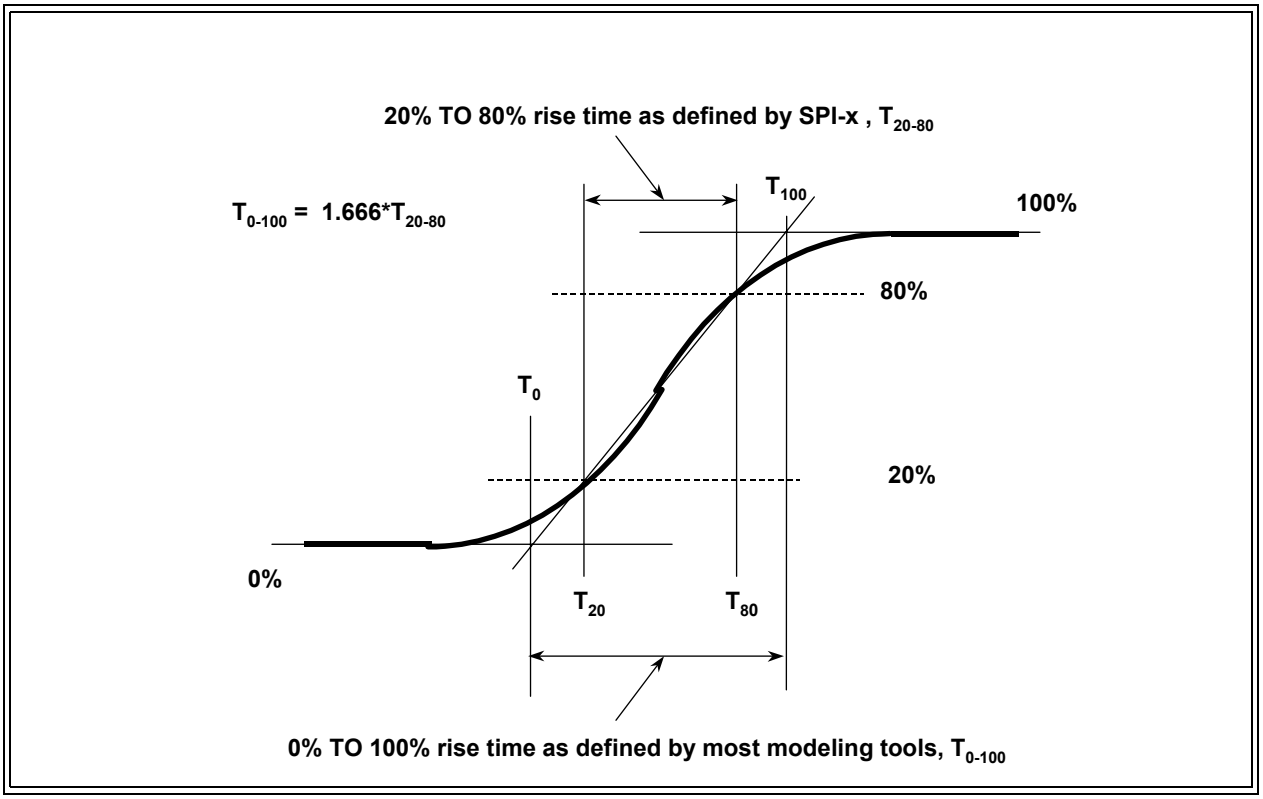


Figure 6 - Relationship between SPI-x and modeling rise times

4.7 Accuracy and model validation considerations

Accuracy is the quality of freedom from mistake or error. The degree of correctness with which a measured value agrees with the true value. Not to be confused with precision.

5 Methodologies

5.1 Overview

Models are divided between behavioral and circuit types.

Behavioral models describe the functional performance of a component. The internal physical implementation is unknown or irrelevant. Examples of behavioral models are IBIS models, which are used for the description of semiconductor devices, and Maxwell matrices which are used for the description of interconnect components.

Circuit models represent the actual internal physical implementation of a component. They consist of an arrangement of interconnected electronic and passive models and are typically implemented by a SPICE representation.

5.2 Behavioral

5.2.1 IBIS

5.2.1.1 Overview

IBIS models provide a standardized way of behaviorally representing the electrical characteristics of an device's pins, input, output, or I/O buffers, that is, without revealing the underlying circuit's structure or process information. This clause explains how to gather the information required to produce a IBIS model for a transceiver. It does not apply to terminators or connectors. It also describes the hazards to avoid when developing the IBIS file. IBIS models may created from the information obtained by direct measurement of the device itself or transistor level simulation of the device. The subsequent clauses are derived from the IBIS Forum I/O Buffer Modeling Cookbook[1], and is adapted to the requirements of SCSI devices.

The information in an IBIS file facilitates the exchange of behavioral data. It is in ASCII format and includes the data needed to model a device's input, output and I/O buffers. This information includes the I/V (current vs. voltage) and switching (V/s) characteristics. The file also includes the electrical characteristics of the package.

An output or I/O pin is characterized from the following information:

a) the output I/V characteristics when the output is logically low,
b) the output I/V characteristics when the output is the logically high,
c) the output I/V characteristics when the output is forced below ground and above the power supply rail,
d) the time it takes a buffer's output to switch logic states, and
e) the buffer's output capacitance.

An input pin is characterized from the following information:

a) the buffer's input I/V characteristics,
b) the buffer's characteristics when the input is forced below ground and above the power supply rail, and
c) the buffer's input capacitance.

1. Available from the EIA/IBIS web site at www.eigroup.org/IBIS/tools.htm

This information is described through the use of keywords which are recognized by being surrounded by square brackets. They are followed either by specific parameters or tables of data. Keywords may be either required or optional. An IBIS file contains, at the minimum, the following information, data and keywords:

a) information about the file itself and name of the device being modeled is contained under the keywords [IBIS Ver], [File Name], [File Rev], [Component] and [Manufacturer];
b) information about the package's electrical characteristics and the pin to buffer model mapping is contained under the [Package] and [Pin] keywords;
c) the [Model] keyword introduces the data set required to model each unique input, output and I/O buffer of the device. The buffer I/V curves and switching characteristics are contained under the [Pullup], [Pulldown], [GND clamp], [Power Clamp] and [Ramp] keywords. The parameters specifying the buffer type - input, output, I/O, open drain, etc. - and its input or output capacitance are contained under the [Model] keyword.

5.2.1.2 IBIS model creation

There are five steps to creating an IBIS model of a device. These steps assume that the original device model is available as a SPICE circuit model.

1) Perform the pre-modeling activities. Decide on the model complexity. Determine the voltage, temperature and process limits over which the device operates and the model will be characterized. Obtain the device related electrical characteristics, pin-out, and use information about the device
2) Extract the electrical data - I/V curves and V/s - for the output, I/O, and input buffers by transistor level simulation.
3) Format the data into an IBIS file. Check the file for conformance to the IBIS specification. This may be done by through the use of the Golden Parser. The Golden Parser is a program that checks the syntax of the IBIS file. It does not check the validity of the model. The Golden parser is available free from the Electronic Industries Alliance. It may be found at the following URL on the world wide web: http://www.eigroup.org/IBIS/tools.htm.
4) Validate the model by comparing the results from the original transistor model against the results of a behavioral simulator that uses the IBIS file as input.
5) Correlate the IBIS model output to the actual measured output of the device.

When creating the model from measured data, the same steps are taken with measured data replacing the transistor level simulation data.

5.2.1.3 Pre-modeling activities

Before creating the model, determinations shall be made regarding the IBIS version, the model's complexity, operational limits, and use. Specific information needed to generate an IBIS model of a device shall also be acquired. Some of these data are specific to the device and goes directly into the IBIS file, while other data are required to perform simulations.

5.2.1.3.1 IBIS version

All models shall be constructed using version 2.1 of the IBIS specification or higher. Version 2.1 provides for differential I/O devices, termination devices, and controlled rise-time buffers. Devices containing multi-staged or multi-IV devices or requiring diode transient times shall be constructed using version 3.2 or higher. Devices using precompensation drivers, such as those required for SPI-4, shall use IBIS version 3.2 or higher.

5.2.1.3.2 Specific device

All models shall be made to represent a specific device. Such models are based on an existing or planned parts. The strength and edge rate of the model shall be adjusted to meet the best and worst case parameters of a particular device. For example, a buffer model for a particular processor may give a worse case V_{ol} of 0,4V @ 36mA. However, if the buffer specification allows for a worst case V_{ol} of 0,6V at 36mA the model's pulldown curve shall be adjusted, or de-rated, to meet this specification. This technique permits the same IBIS model to represent a whole series of devices, and not just one particular device.

5.2.1.3.3 Corner limits

All models shall contain corner models. These include slow models - weakest drive, slowest edge - typical models, and fast models - strongest drive, fastest edge. These corners shall be determined from the environmental -temperature and voltage - conditions under which the device is expected to operate, the silicon process limits, and the number of simultaneous switching outputs (SSOs). These conditions shall match those used for specifying the device T_{co} parameter.

5.2.1.3.4 SSO effects

SSO effects shall be included. These may be determined explicitly by measuring the I/V and edge rate characteristics under SSO conditions. Alternatively, several buffers may be connected to a common power or ground rail using the method established in 5.2.1.5.4.1. The former method, including SSO effects in the models' I/V and edge rate tables, has the advantage that the resulting model is easier to verify and less dependent on any particular simulator's capability. Note however, the method described in 5.2.1.5.4.1 provides the ability to perform explicit ground bounce simulations.

The type of SSO modeling technique shall be included in the model's errata.

5.2.1.3.5 Schematics

Schematics of each of the different types of input, output and I/O buffers on the device shall be acquired. The same schematic used for simulating T_{co} shall be used. The schematic shall include ESD diodes, if present, and a representation of the power distribution of the device. The type of output structure, standard CMOS totem-pole, open-drain, etc., for each different type of output or I/O buffer on the device is determined from these schematics.

5.2.1.3.6 Clamp diode and pullup references

Different voltage references for the clamp diodes than that are used for the pullup or pulldown transistors within the device shall be determined.

5.2.1.3.7 Packaging information

All models shall include package parasitics. A separate model shall be required for each package in which the device is housed. These parasitics shall include the self resistance, inductance, and capacitance of each individual pin of the device package. The parasitics shall also include the self resistance, inductance, and capacitance of each individual bond wire within the package. Minimum, typical and maximum values shall not be used. Any coupling inductance and capacitance from any pin to any another pin, or any bond wire to any other bond wire, that is greater than 5% of the self values of the respective pin or bond wire shall be included.

BGA packages are problematical. This package type has complex interdependencies. Simple 2 dimensional and simple 3 dimensional models have been determined to be inadequate for this clause. Therefore, full 3 dimensional structural models shall be used for determining the package parasitics under this clause for all SCSI data, REQ, ACK and PARITY signal pins.

5.2.1.3.8 Signal selection

A determination shall be made as to which signals shall be used or may be ignored for modeling purposes. For example, test pads or static control signals may not need a model.

5.2.1.3.9 Die capacitance

The input, output, or I/O capacitance of each pad shall be obtained. This is recorded as established in 5.2.1.5.4.1. This is the capacitance seen when looking from the bond site on the die back into the buffer for a fully placed and routed design.

5.2.1.3.10 V_{inl} and V_{inh} parameters

Models of input and I/O buffers shall include the V_{inl} and V_{inh} parameters.

5.2.1.3.11 T_{co} measurement conditions

The loading conditions shall be obtained where the measurement of the output or I/O buffers' propagation delay from clock to output (T_{co}) is made. This shall include the load capacitance (Cref), resistance (Rref), and voltage (Vref) parameters as well as the output voltage crossing point (V_{meas}) where T_{co} is measured.

5.2.1.3.12 Buffer grouping

Separate buffer models are required for each different buffer design or structure the device uses. Group the device pins into inputs, outputs and I/Os. Determine the number of different buffer designs. Separate models are required if a signal has a different C_comp parameter or T_{co} measurement condition.

5.2.1.4 Data extraction

Upon completion of the pre-modeling activities, the device's I/V and switching information is gathered. Output and I/O buffers require both I/V curves and rise/fall times, while input buffers only need I/V curves.

Circuit simulation tools may used to obtain this information over worst-case process and temperature variations. This may be accomplished by either using the SPICE to IBIS utility (s2ibis) or by direct simulation. The s2ibis utility is a program developed by North Carolina State University available free of charge from the IBIS Open Forum[1]. Documentation, examples, and executables for various platforms are also available.

Data may also be obtained from physical measurements, but it is difficult to obtain minimum and maximum data over worst-case process and temperature variations as can be accomplished using simulation. In either case the model shall be correlated against the actual silicon measurements.

5.2.1.4.1 s2ibis extraction

In many cases, If HSPICE or other commercially available SPICE models of the device are available, the SPICE to IBIS utility (s2ibis) can be used to extract the buffers I/V and V/s curves. If the s2ibis utility is not able to accept the transistor level model, the required I/V and V/s data may be extracted directly through simulation.

5.2.1.4.2 Direct simulation extraction

The following procedures shall be used when extracting data directly from simulations.

1. Available from the EIA/IBIS web site at www.eigroup.org/IBIS/tools.htm

5.2.1.4.2.1 Extracting I/V data

The first step to extracting the required I/V curves is understanding the buffer's operation. Analyze the buffer schematic and determine how to put the buffers output into a logic low, logic high and, if applicable, high impedance state. As mentioned above, the schematic should include the R, L and C parameters associated with the on die power supply distribution and ground return paths as well as any ESD or protection diodes. The schematic should also indicate if the power clamp or ground clamp diode structures are tied to a voltage rail (voltage reference) different than that used by the pullup or pulldown transistors.

A typical simulation setup for an output or I/O buffer is depicted in Figure 7. In this example the device under test (DUT) is a standard 3-state buffer with a single push-pull output stage.

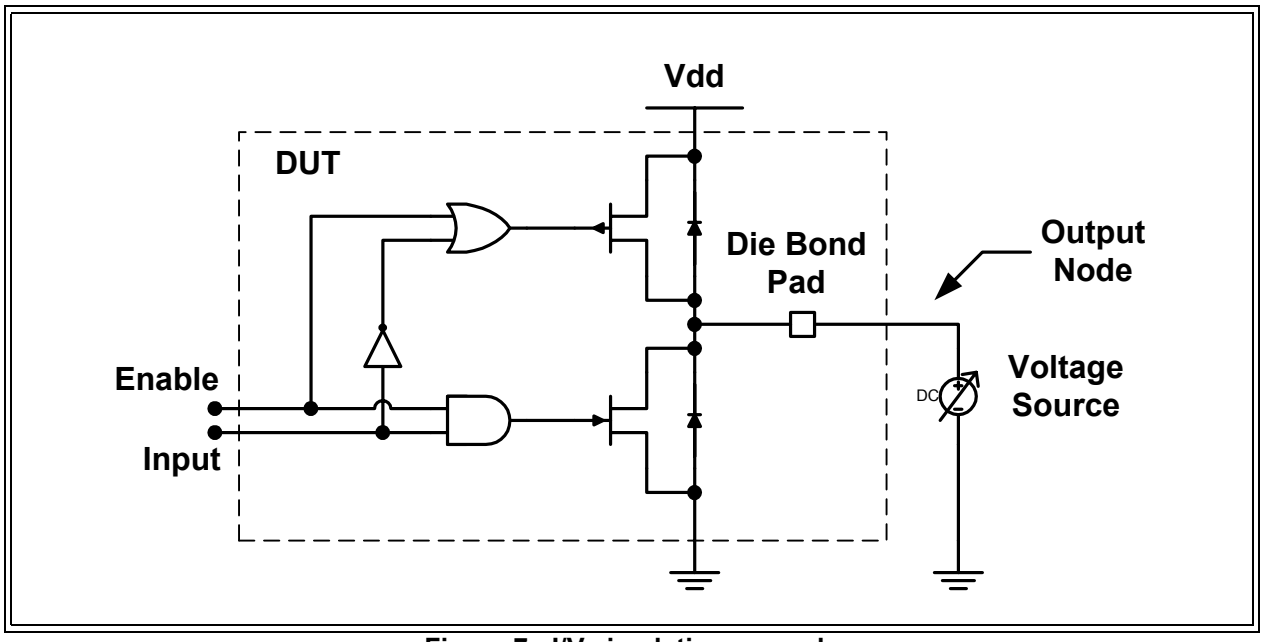


Figure 7 - I/V simulation example

All measurements shall be made at the output node (pad) as shown in Figure 7. All package lead parasitics - R_pin, L_pin, and C_pin - shall be removed. However, any series resistors present between the pad and the pullup/pulldown transistors shall be included.

The output buffer is connected to an independent voltage source. The buffer's input(s) shall be set so that the desired output state - low, high, off - is obtained. Then using a DC or transfer function analysis, the voltage source shall be swept over the range from -Vdd to Vdd x 2 while recording the current at the output node. If a DC analysis causes convergence problems, the alternative method is to perform an AC or transient analysis. The voltage source becomes a slow (100mV/ms) linear ramp function driving the output node. Both the voltage and current at the output node shall be monitored, then the resulting I/s and V/s data shall be combined into a single I/V table. While a transient function analysis may require post simulation data manipulation, an AC analysis completes much faster than a DC analysis and has less convergence or initial value problems.

5.2.1.4.2.2 Hi-Z buffers

For an I/O Hi-Z buffer four sets of I/V curves are required; one while the pulldown transistor is on, one while the pullup transistor is on, and two while the output is in a high impedance state. The data gathered while the output is low shall be used to construct the [Pulldown] table. Data gathered while the output is high shall be used to construct the [Pullup] table. Pulldown I/V data shall be referenced to ground while pullup I/V data shall be referenced to Vdd. Referencing pullup data to Vdd means that the endpoints of the sweep range are adjusted as Vdd is adjusted; refer to 5.2.1.4.2.7 for more detail. Data for the [GND Clamp] keyword shall be taken with the output in the high impedance state and is ground relative, while data for

the [POWER Clamp] keyword shall be taken with the output in a high impedance state but with the data Vdd relative. Each set of curves shall be repeated under the minimum, typical and maximum corner conditions and shall cover the entire sweep range. A Hi-Z buffer requires the following 12 I/V data sets:

a) Pulldown I/V under minimum, typical and maximum conditions, data ground relative
b) Pullup I/V under minimum, typical and maximum conditions, data Vdd relative
c) High Impedance state I/V under minimum, typical and maximum conditions, data ground relative
d) High Impedance state I/V under minimum, typical and maximum conditions, data Vdd relative

5.2.1.4.2.3 Output only buffer

An output only buffer requires two sets of curve, one with the pulldown transistor turned on, and one with the pullup transistor turned on. Pulldown I/V data shall be referenced to ground while pullup I/V data shall be referenced to Vdd. Because an output only buffer does not have a high impedance mode the power and ground clamp diode curves cannot be isolated from the transistor curves; data points beyond the rail shall be included in the pullup and pulldown I/V data. The [GND Clamp] and [POWER Clamp] keywords are not required for an output only buffer.

5.2.1.4.2.4 Open drain buffers

Open-drain or open-collector type devices only require three sets of I/V data: [Pulldown], [GND Clamp] and [POWER Clamp]. Data for the [Pulldown] table is gathered as described previously. [POWER Clamp] and [GND Clamp] data shall be gathered by turning off the pulldown transistor then performing the two I/V sweeps as described in 5.2.1.4.2.2. An open drain buffer may not require the full -Vdd to Vdd x 2 sweep range; refer to 5.2.1.4.2.6.

5.2.1.4.2.5 Input buffers

When gathering I/V data for input buffers a similar setup shall be used with the variable voltage source placed on the input node. Input buffers require only [POWER Clamp] and [GND Clamp] I/V data. The data for the [GND Clamp] keyword shall be gathered via a voltage sweep with the voltage source referenced to ground and the [POWER Clamp] data shall be gathered by a voltage sweep with the voltage source Vdd relative. If an input device includes weak resistors to power or ground their I/V curves shall be included into the respective ground clamp or power clamp I/V data.

5.2.1.4.2.6 Sweep ranges

The IBIS specification requires I/V data be supplied over the range of voltages the output could experience in a transmission line environment. For example: assuming that a device's output swings from ground to Vdd, where Vdd is the voltage given by the [Voltage Range] or [Pullup Reference] keywords, this range is from the maximum negative reflection from a shorted transmission line, to the maximum positive reflection from an open circuited transmission line or from -Vdd to Vdd x 2. However, if a device is operating in an environment where its output could be actively driven beyond these limits the I/V table shall be extended further. For example: a 3,3V I/O buffer operating in a mixed 3,3V/5,0V system. While the device's output may only drive from 0 to 3,3V, a 5V device connected to this output may drive the output node beyond 3,3V. In this case I/V data shall be supplied over a full -5,0V to +10,0V range. Similarly, an open collector or open drain device may be terminated in a voltage - Vpullup - different than given by the [Voltage Range] keyword. In this case the pullup and pulldown data shall be supplied over the range from -Vpullup to Vpullup x 2.

Semi-conductor device models may not be well behaved over these ranges. It is acceptable to lessen the actual sweep range then use linear extrapolation to get to the required endpoints. For example: in the case of a typical 5V device, the IBIS specification requires I/V data over the full -5,0V to 10,0V range. It is permissible to limit the simulation sweep to a range of -2,0V to +7,0V and then extrapolate to the final range of -5,0V to +10,0V. However, the simulation sweep range shall be of sufficient magnitude to forward bias any ESD protection diodes or the diodes intrinsic to the output transistor structures.

5.2.1.4.2.7 Pullup and power clamp sweeps relative to Vdd

Pullup and power clamp data are relative to Vdd. This shall be accomplished by adjusting the start and end points of these sweeps to follow the variations in Vdd. For example: in the case of a standard 3,3V device whose Vdd specification was 3,3V ± 10%, i.e. the operating Vdd ranged from a 3,0V minimum to 3,6V maximum, the sweep voltage would range from -3,3V to +6,6V for typical conditions. The sweep voltage would range from -3,6V to +6,3V for minimum conditions and -3,0V to +6,9V for maximum conditions. Thus the minimum conditions are obtained by subtracting 0,3V from the typical range and adding 0,3V to the maximum range. For data gathered in this manner, the corresponding voltage data point in all three data sets represents the same delta from Vdd. The 9,9V sweep RANGE remains the same for all three simulations.

5.2.1.4.2.8 Diode models

Digital I/O buffer design analysis is most concerned with the buffer's Tco parameter and output impedance. Little attention is paid to a buffer's beyond rail operation. The diode models included in buffer's schematic may only be included for layout or completeness, and are therefore most likely "perfect" diodes with no intrinsic resistance. Likewise, if a design relies on the intrinsic diode structure of the output transistors to provide output protection, the transistor models may not properly model this mode of operation. When doing simulation in these voltage regions unrealistically large power and ground clamp currents may be observed. If this exists, the diode or transistor models may be enhanced to include the proper junction or bulk resistance. With large ESD structures the metal resistance may be relatively large -- on the order of a few ohms – and this should be included in the design. If an actual device is available, the power and ground clamp I/V data may be measured directly.

5.2.1.4.2.9 Extracting the Ramp Rate or V/s Waveform Data

Simulations to obtain the ramp rate, the V/s (output voltage vs. Time) curves, or both are straightforward. For each simulation corner (minimum, typical, maximum) two V/s data sets are required; one for the buffer output switching low to high, the other is for the buffer output switching high to low. These data are then reported as a rising and falling V/s ratios (the "ramp rate") or the actual V/s data may be reported directly.

5.2.1.4.2.10 Extracting Data for the [Ramp] Keyword

If the output switching (V/s) waveform of a device may be approximated by a linear ramp - that is the data are monotonic - then the V/s data may be reported as a rising and falling ramp rate (V/s) by using the [Ramp] keyword. Data for the [Ramp] keyword are extracted using the simulation setup shown in Figure 8. This setup is described in IBIS version 2.1, and is applicable for extracting rise and fall data for a standard single stage, push-pull TTL or CMOS buffer.

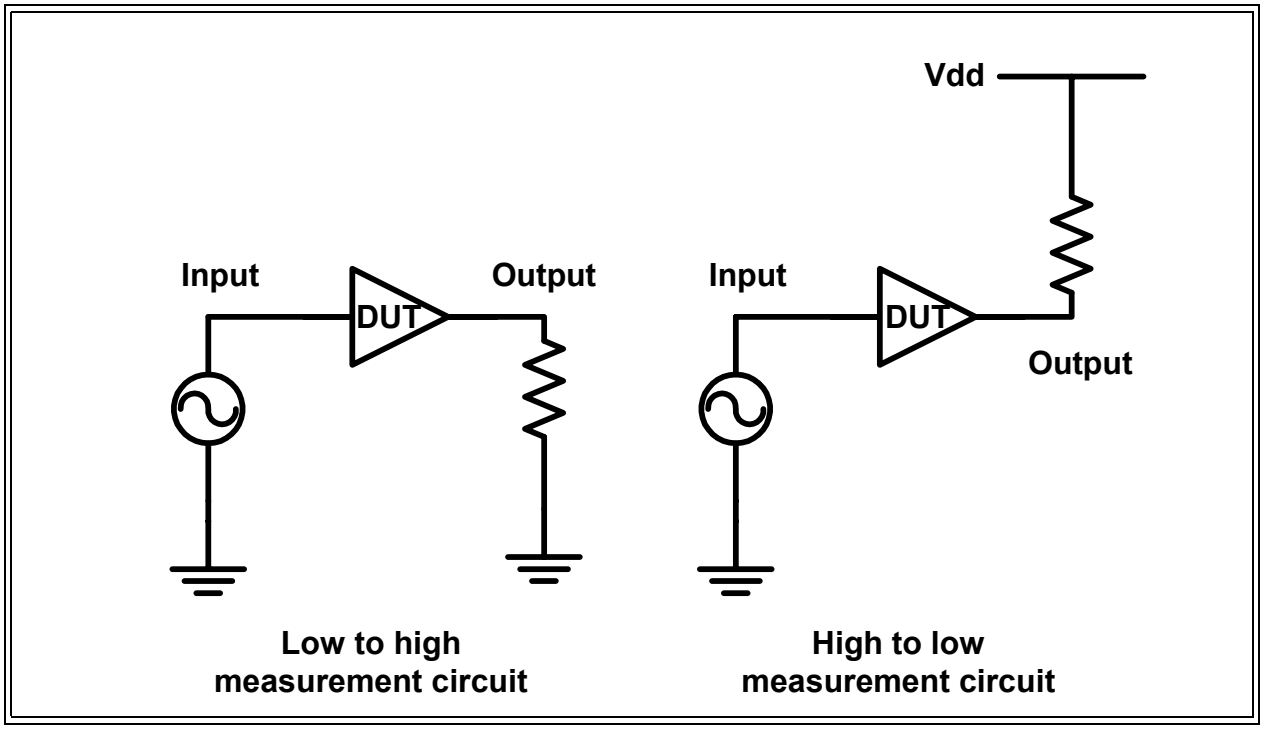


Figure 8 - Ramp data simulation example

Obtain rise and fall time data by setting the simulator for a transient analysis simulation. The control inputs of the buffer are set to enable the buffer outputs and a driving waveform is applied to the buffer input. The slew rate of the input stimulus driving waveform should match the internal slew rate of the technology (i.e. the slew rate of the pre-driver that would normally drive the final output stage). Rising edge ramp rate data are obtained by placing a load resistance from the output to ground then stimulating the buffer so that the output switches from low to high. Falling edge ramp data are captured with the load resistor tied to Vdd. Use a load resistance of 50Ω. If the device does not have enough drive capability to make a significant output transition then a higher value of load resistance may be used, but this shall be noted in the IBIS file (see the description of the [Ramp] keyword in the IBIS specification for specific details). For an open drain or ECL type devices, measure the rise and fall times into the load resistor and voltage used by the manufacture when specifying propagation delays. As with the I/V simulations the package lead (L_pin, R_pin, C_pin) parasitics shall be removed. However, simulations are performed with C_comp included in the circuit. Note that to avoid errors when trying to correlate later simulations with those used to extract rise/fall time information, use the same time step throughout the simulation and correlation procedure.

5.2.1.4.2.11 Extracting Data for the Rising and Falling Waveform Keywords

In IBIS version 2.1 V/s data may be reported directly by using the [Rising Waveform] and [Falling Waveform] keywords. These two keywords are generally required if the output switching waveform of the device is significantly non-linear (this is the case with most "controlled rise time" or "graduated turn on" style buffers). The use of these keywords is also indicated if the device incorporates a delay between the turning off of one output transistor and the turning on of the other (i.e. the V/s waveform contains a pedestal). Finally, the model creator may wish to include the V/s data directly so that the model itself includes it own verification feature. By including this "golden waveform" the model user may perform a

simulation with the buffer driving the same load as was used to generate the V/s waveforms. The results of this simulation should match the V/s waveform as given in the IBIS file, thereby verifying that the users simulator is producing the proper results.

When doing simulations to extract V/s data for the [Rising Waveform] and [Falling Waveform] keywords a variety of load circuits are used, depending on the technology of the buffer. The intent is that by picking the proper load(s) and termination voltage(s), the turn-on time, turn-off time (and overlap between the two) of the pullup and pulldown stages of the buffer can be isolated and a more accurate behavioral model construct. The recommended loads and waveforms to be collected are specified in Table 1. These have been specified by the various CAE vendors that support IBIS models.

Table 1 - Recommended load circuits and waveforms for V/s data extraction

Technology	Number of waveforms	Load circuit and waveform[a]
Standard push/pull CMOS	4	1R+1F driving 50Ω to Vdd 1R+1F driving 50Ω to Vss
Open drain CMOS	2	1R+1F into manufacturer's suggested Vterm and Rterm - pullup resistor and voltage[b]
Open source CMOS	2	1R+1F into manufacturer's suggested Vterm and Rterm - pullup resistor and voltage[b]

a. 1R = one rising waveform, 1F = one falling waveform
b. if recommended termination resistor is >100Ω, include 1R +1F driving 50Ω to Vterm

Be aware that not all CAE vendors' simulation software will use all the given waveforms. If in doubt, check with your CAE vendor.

As with the simulations for ramp rate the slew rate of the driving waveform should match the internal slew rate of the technology. For meaningful results all of the above rising and falling waveforms should be taken with the package lead parameters (R_pin, L_pin, C_pin) and fixture reactive elements (L_fixture and C_fixture) set to zero. The L_fixture and C_fixture parameters are included as parameters of the [Rising Waveform] and [Falling Waveform] keywords only for use in documenting a measurement setup or creating complex loads for simulator comparison and validation via a golden waveform.) As noted in the IBIS specification itself, it is critical that all rising and falling waveforms be time correlated. In other words, the rising (falling) edge data in each of the rising (falling) edge waveform tables shall be entered with respect to a common reference point on the input waveform used to stimulate the buffer.

In addition to the above recommended V/s waveforms, additional waveforms may be included for simulator validation purposes. These waveforms are referred to as "golden waveforms" because their intent is to supply a reference waveform that the simulator attempts to match, not raw V/s data that the simulator uses to construct the behavioral model. Unlike the recommend loads above, the load circuits used to generate golden waveforms may include reactive elements. Two popular golden waveform loads are 50,0Ω to (Vdd - GND) / 2, and a 50,0pF load to ground. The model maker may also wish to include a waveform of the buffer driving a load that represents the typical load found in the buffers intended application.

Finally, some devices may show slightly different rising and falling edge characteristics depending on how much time the buffer has had to settle from a previous output transition. Some projects may ask that the model creator extract ramp or V/s data from the second or third output transition in a series.

5.2.1.4.2.12 Minimum Time Step

As a rule of thumb, set the minimum time step so that there are between 30 to 50 data points in a rising or falling V/s curve. If the V/s waveform is especially complex more points may be required (note however that the V/s waveform tables may contain no more than 100 points). If the data are going to be reduced to a V/s under the [Ramp] keyword then fewer points may be required.

5.2.1.4.2.13 Fallback drivers

Fallback drivers shall be modeled through the use of multiple rising and falling waveform data. A set of data shall be created for the overdrive condition, and a set of data shall be created for the fallback condition using the techniques specified in 5.2.1.4.2.11 and 5.2.1.4.2.12. The complete driver is modeled through the use of the [Driver Schedule] keyword. See 5.2.1.5.4.10.

5.2.1.5 Creating the IBIS file

5.2.1.5.1 Overview

Once the I/V and switching information for a device's buffers have been obtained, these data shall be placed into the IBIS file. The file format is detailed in the IBIS specification.

An IBIS file consists of three parts, with an optional "external" package description. These three parts consist of:

1) general information about the file itself and the device being modeled,
2) the device name, pin-out, and pin-to-buffer mapping; and
3) the behavioral descriptions of each unique buffer type in that device.

Note that an IBIS file may contain a description of more than one device (i.e. parts 2 and 3 may be repeated several times within one IBIS text file). For more information refer to the description of the [Component] keyword in the specification.

5.2.1.5.2 Header Information

The first section of an IBIS file contains basic information about the file itself and the data in it. This section includes the following keywords:

Table 2 - IBIS file header information

Keyword	Required?	Description
[IBIS Ver]	Yes	The version of IBIS this file uses.
[Comment char]	No	Change the comment character. By default it is the pipe "|" character.
[File name]	Yes	The name of the IBIS file. File names shall be lower case and conform to DOS 8.3 convention. The file extension is .ibs.
[File rev]	Yes	The revision level of the IBIS file.
[Date]	No	The date the IBIS file was created.
[Source]	No	The data source for the file: data book, simulation, or measurement.
[Notes]	No	Device or file specific notes.
[Disclaimer]	No	May be legally required.
[Copyright]	No	Copyright notice

The specific revision level is set at the discretion of the model provider. The provider shall follow the syntax in Table 3 when assigning revision levels.

Table 3 - IBIS file revision levels

Revision Series	Meaning
0.x	Silicon and file in development
1.x	Pre-silicon file data from silicon model only
2.x	File correlated to actual silicon measurements
3.x	Mature product, no additional changes likely

These keywords are self-explanatory. While the [Date], [Source], etc. keywords are not required, their use is recommended. The [Notes] keyword is especially valuable, in that it may include such information as:

a) specific model use requirements and caveats;
b) simulator use information, such as what features the simulator shall support;
c) information on SSO conditions, such as under what switching conditions were the minimum, typical and maximum corners derived;
d) additional package modeling information; and
e) the model's validation level.

5.2.1.5.3 Component and pin information

This section of an IBIS file contains information regarding the device's pinout, pin to buffer mapping, and the devices package and pin electrical parameters.

Table 4 - IBIS file component and pin information

Keyword	Required?	Description
[Component]	Yes	The name of the device being modeled.
[Manufacturer]	Yes	The name of the device's manufacturer.
[Package]	Yes	The total range over which the package lead resistance, inductance, and capacitance parameters vary - minimum, typical, and maximum.
[Pin]	Yes	The pin to buffer mapping information is contained here. Additionally, the individual package lead resistance, inductance and capacitance shall be specified here.
[Package model]	No	This keyword indicates the name of the package model when an external package model, or the [Define Package Model] keyword is used within the IBIS file.
[Pin Mapping]	No	Used when data on which I/O or output pins share power and ground connections are included. This information is used by a simulator when doing simulations involving multiple outputs switching
[Diff Pin][a]	No	Used only if the device contains differential pins.

a. Not required by the IBIS specification, but a requirement for all differential SCSI device models.

These keywords are well explained in the IBIS specification. For single-ended devices the required keywords [Component], [Manufacturer], [Package] and [Pin] are all that are needed to build the model. Differential device models shall include the [Diff Pin] keyword. The [Pin] keyword is where the pins of the device are defined, and each of the buffer models created are mapped to specific pins. There shall be a buffer model - as called out by the [Model] keyword - for each non-power/ground/no-connect pin.

The values described by R_pkg, L_pkg and C_pkg are the overall minimum and maximum values of the package's lead resistance, inductance and capacitance. The numerically largest values of resistance, inductance, and capacitance are listed as the "max" values, while the numerically smallest values resistance, inductance and capacitance are listed as the "min" values.

Note the [Pin Mapping] keyword. If a particular buffer model is intended to represent that buffer in isolation, then the [Pin Mapping] keyword may be used to gang several buffers together in order to perform a simulation that includes the effects of multiple outputs switching. If the model is intended to be used with the [Pin Mapping] keyword information then that should be noted in the [Notes] section, however not all simulators support this feature.

5.2.1.5.4 Model description

The [Model] keyword starts the description of the data for a particular buffer. While a buffer model may appear quite complex, most buffers may be described using just a few of the parameters and keywords.

5.2.1.5.4.1 [Model] keyword parameters

The model description starts with the user specifying a few basic parameters. These parameters tell the simulator what type of buffer the model represents, and some characteristics of the buffer that enable simulators to do automatic error checking.

Table 5 - IBIS file [Model] parameters

[Model] parameter	Required?	Description
Model_type	Yes	Defines the buffer type - input, output, I/O, etc.
Polarity	No	Defines the signal polarity of the buffer- high true or low true.
Enable	No	Defines the signal polarity of the buffer output enable, if applicable.
Vinl	No	Defines the buffer low input logic threshold.
Vinh	No	Defines the buffer high input logic threshold.
C_comp	Yes	Defines the buffer input or output capacitance. See the following discussion on "min" and "max" values of C_comp
Vmeas	No	Tco
Cref	No	Tco
Rref	No	Tco
Vref	No	Tco

The IBIS specification contains an extensive list of possible buffer types. If an input or I/O buffer type is chosen, the Vinl and Vinh parameters shall be specified. If not, the IBIS defaults shall be verified as correct for the buffer. The Vinl and Vinh parameter are used by simulators to flag signal integrity violations and perform timing calculations. The Vmeas, Cref, Rref and Vref parameters are recommended for inclusion with all output or I/O type buffer models, since these parameters allow a simulator to do board level timing calculations.

The C_comp parameter specifies the buffer's input, output or I/O capacitance and may have a typical, minimum and maximum value. The numerically largest value of C_comp is listed as the "max" value while the numerically smallest value of C_comp is listed as the "min" value. The C_Comp "min" and "max" values do not necessarily correlate with the minimum and maximum conditions under which the I/V and switching data were gathered.

5.2.1.5.4.2 [Temperature Range] and [Voltage Range] keywords

The buffer operating temperature and voltage ranges are given by the following keywords.

Table 6 - IBIS file temperature and voltage range information

Keyword	Required?	Description
[Temperature Range]	No	The temperature range over which the min, typ and max I/V and switching data has been gathered. If not specified then 0,0 50,0 and 100,0 degrees C is assumed.
[Voltage Range]	Yes	The range over which Vdd is varied to obtain the min, typ and max pullup and power clamp data.
[Pullup Reference]	No	Allows the user to specify alternate reference (i.e. voltage rails) for any of the four I/V curves.
[Pulldown Reference]	No	Allows the user to specify alternate reference (i.e. voltage rails) for any of the four I/V curves.
[POWER Clamp Reference]	No	Allows the user to specify alternate reference (i.e. voltage rails) for any of the four I/V curves.
[GND Clamp Reference]	No	Allows the user to specify alternate reference (i.e. voltage rails) for any of the four I/V curves.

The [Temperature Range] keyword is self explanatory. The "min" and "max" temperature values listed in an IBIS file correspond to the conditions under which the "min" and "max" I/V and switching data were taken.

The [Voltage Range] keyword specifies the range over which Vdd is varied to obtain the min, typ and max conditions. In addition, this keyword supplies the default voltage reference value for the pullup and power clamp I/V curves. Normally, the [Voltage Range] keyword is all that is required. However, if a buffer uses multiple power supply rails the alternate keywords are used. Very specifically, if the model creator gathers pullup or power clamp I/V data using a voltage reference other than that called out by the Vdd keyword, then the [Pullup Reference] or [POWER Clamp Reference] keywords are used.

5.2.1.5.4.3 I/V data section

Enter the I/V data via the four I/V data keywords shown in Table 7, once the voltage references have been established.

Table 7 - IBIS file I/V data information

Keyword	Required?	Description
[Pulldown]	No	Data gathered while an output or I/O buffer is in the logic low state is entered here. This keyword is not used for input buffers.
[Pullup]	No	Data gathered while an output or I/O buffer is in the logic high state is entered here. This keyword is not used for input buffers.
[GND Clamp]	No	I/V curve when the input or output of a buffer is driven below ground, or the reference specified by the [GND Clamp Reference] keyword.
[POWER Clamp]	No	I/V curve when the input or output of a buffer is driven above Vdd, or the reference specified by the [POWER Clamp Reference] keyword.

None of the four I/V curves are mandatory. Non hi-Z buffers - buffers where separate power and ground clamp diode effects may not be isolated - require only the [Pulldown] and [Pullup] keywords. Input buffers use only the [GND Clamp] and [POWER Clamp] keywords. All four keywords are required for hi-Z buffers. The current data in the [Pullup] table is all zeros for open drain/collector buffers, or the [Pullup] keyword is omitted altogether.

Each keyword is followed by a set of data in tabular format. The gathered I/V data are entered into the appropriate tables.

5.2.1.5.4.4 [Pulldown] keyword

Data shall be gathered while the output or I/O buffer is in the low logic state. These data are entered into the [Pulldown] table. Pulldown data shall cover the range of -Vdd to Vdd x 2. For a hi-Z device, the ground clamp current is subtracted from the pulldown current and the result entered into the [Pulldown] table. This results in a pulldown I/V curve that resembles the curve in Figure 9.

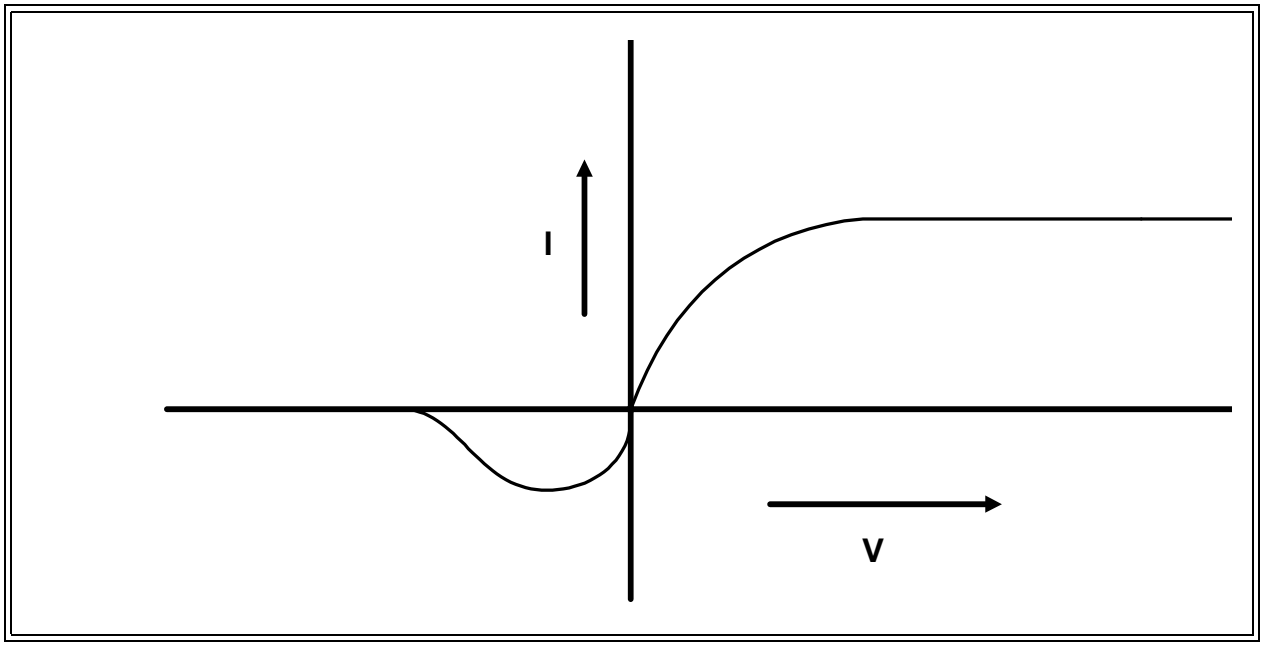


Figure 9 - IBIS pulldown I/V example

Below zero volts the magnitude of the buffer current increases, becoming more negative, but then reduces towards zero. This is acceptable. Simulators sum the ground clamp I/V curve with the pulldown I/V curve to the original pulldown I/V curve, for buffers in their active state.

5.2.1.5.4.5 [GND Clamp] keyword

Ground clamp data shall be gathered for input buffers and I/O buffers. For I/O buffers these data are gathered while the buffer is in the high impedance state and are ground relative. These data are entered into the [GND Clamp] table. The data in table shall cover the range of -Vdd to Vdd.

5.2.1.5.4.6 [Pullup] keyword

Enter into the [Pullup] table the data gathered while the output or I/O buffer was in the logic high state. If the buffer is a hi-Z device then the power clamp current is first subtracted from the pullup current and the result entered into the [Pullup] table. Pullup data shall cover the range -Vdd to Vdd x 2. The IBIS specification requires the voltage points be entered into the table using the formula in Equation 1.

$$Vtable = Vdd \angle Voutput$$

Equation 1 - [Pullup] data equation

For example, for a standard 5,0V device the values for voltage listed in the table range from +15,0V when the output is 5,0V below ground, to -5,0V when the output is 5,0V above Vdd.

5.2.1.5.4.7 [POWER Clamp] keyword

Enter the [POWER Clamp] data the into power clamp I/V data. For I/O buffers this is the Vdd relative data gathered while the buffer was in the high impedance state. The data in the table shall cover the range of Vdd to Vdd x 2.

5.2.1.5.4.8 Clamp keyword extrapolation caveats

A common error when building clamp tables involves extrapolation errors on the last data point. Most simulators extrapolate the last two data points in a table to calculate values beyond the table's range. Therefore, all curves going to zero shall have the last two data points as zero. As an example, the incorrect way to enter a diode curve described in Table 8.

Table 8 - Incorrect clamp data table entry

Voltage	Current
0,0V	0,0mA
0,6V	2,0mA

In Table 8, the simulator extrapolates the current at a bias voltage of -0,6V as -2,0mA. The correct manner to enter the data is described in Table 9.

Table 9 - Correct clamp data table entry

Voltage	Current
0,0V	0,0mA
0,4V	0,0mA
0,6V	2,0mA

A simulator will the diode curve correctly when the data is entered as in Table 9.

5.2.1.5.4.9 [Ramp] keyword and waveform tables

The last piece of information about an output or I/O buffer is the switching information. This information is contained in the keywords specified in Table 10.

Table 10 - IBIS file ramp and waveform information

Keyword	Required?	Description
[Ramp]	Yes	Ramp information in V/s
[Rising Waveform]	No	The rising transition waveform in a V/s table
[Falling Waveform]	No	The falling transition waveform in a V/s table.

The [Ramp] keyword is required, even if the [Rising Waveform] and [Falling Waveform] keywords are used. The ramp rate is not the instantaneous slew rate of the output. It indicates the time for the output transistor structures to switch from one state to another. As such, the dv portion of the [Ramp] keyword data are specified to cover the 20% to 80% voltage swing of the output. The ramp rate posted in an IBIS file is defined in Equation 2.

$$\frac{\partial V}{\partial t} = \frac{\text{20\% to 80\% points}}{\text{time to swing between points}}$$

Equation 2 - IBIS ramp rate

The ramp rate shall be recorded with 4 digits of precision.

5.2.1.5.4.10 [Driver Schedule] keyword

The [Driver Schedule] keyword describes the relative model switching sequence for referenced models to produce a multi-staged driver or in the case of SPI-4 and beyond a fallback model. This keyword shall be placed under the [Model] which acts as the top-level model. The scheduled models are then referenced from the top-level model by this keyword.

When a multi-staged buffer or fallback driver is modeled, all of its stages (including the first stage, or normal driver) have to be modeled as scheduled models.

The [Driver Schedule] keyword causes simulators to use the [Pulldown], [Pulldown Reference], [Pullup], [Pullup Reference], [Voltage Range], [Ramp], [Rising Waveform] and [Falling Waveform] keywords from the scheduled models instead of the top-level model. Consequently, these keywords will be ignored in the top-level model. Also, all other keywords not shown in the above list will be ignored in the scheduled model(s). However, both the top-level and the scheduled model(s) have to be complete models, i.e. all of the required keywords shall be present and follow the syntactical rules.

The [Driver Schedule] table consists of five columns. The first column contains the model names of other models that exist in the file. The remaining four columns describe delays: Rise_on_dly, Rise_off_dly, Fall_on_dly, and Fall_off_dly. The t=0 time of each delay is the event when a rising or falling transition is initiated. All specified delay values shall be equal to or greater than 0. There are only five valid combinations in which these delay values can be defined:

a) Rise_on_dly with Fall_on_dly
b) Rise_off_dly with Fall_off_dly
c) Rise_on_dly with Rise_off_dly
d) Fall_on_dly with Fall_off_dly
e) All four delays defined

These delay parameters have following meaning

a) Rise_on_dly is the amount of time that elapses from the initialization of a RISING edge to the t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device ON, and the t=0 time of the waveform or ramp that turns the I-V table of the PULLDOWN device OFF (if they were not already turned ON and OFF, respectively, by another event).
b) Rise_off_dly is the amount of time that elapses from the initialization of a RISING edge to the | t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device OFF, and the t=0 time of the waveform or ramp that turns the I-V table of the PULLDOWN device ON (if they were not already turned ON and OFF, respectively, by another event).
c) Fall_on_dly is the amount of time that elapses from the initialization of a FALLING edge to the | t=0 time of the waveform or ramp that turns the I-V table of the PULLDOWN device ON, and the t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device OFF (if they were not already turned ON and OFF, respectively, by another event).
d) Fall_off_dly is the amount of time that elapses from the initialization of a FALLING edge to the t=0 time of the waveform or ramp that turns the I-V table of the PULLDOWN device OFF, and the t=0 time of the waveform or ramp that turns the I-V table of the PULLUP device ON (if they were not already turned ON and OFF, respectively, by another event).

NA shall be used when no delay value is applicable. For each scheduled model the transition sequence shall be complete, i.e., the scheduled model shall return to its initial state. No [Driver Schedule] table may reference a model which itself has within it a [Driver Schedule] keyword.

The Rise_on_dly, Rise_off_dly, Fall_on_dly, Fall_off_dly parameters are single value parameters, so typical, minimum and maximum conditions cannot be described with them directly. In order to account for those effects, refer to the fastest waveform table with the delay number and then insert an appropriate amount of horizontal lead in section in those waveforms which need more delay.

Since the C_comp parameter of a multi-stage buffer is defined in the top-level model. The value of C_comp therefore includes the total capacitance of the entire buffer, including all of its stages. Since the rising and falling waveform measurements include the effects of C_comp, each of these waveforms shall be generated with the total C_comp present, even if the various stages of the buffer are characterized individually.

An example of a Driver Schedule implementation of fallback for a Ultra320 driver follows:

[Driver Schedule]

| Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

U320P-hi0.0s6.25nsNANA

U320P-lo6.25ns100msNANA

U320M-hiNANA0.0s6.25ns

U320M-IoNANA6.25ns100ms

Note: The use of a period (.) as a decimal delimiter, and concatenation of the multipliers are required by the IBIS Specification syntax.

5.2.1.5.5 External Package Models

External package models may be used when more than one package type is associated with a particular device.

5.2.1.5.6 IBIS file conformance

An IBIS file shall be checked for correct construction and syntax. The program called "ibischk2" shall be used to verify the IBIS file. This program is also called the Golden Parser[1]. The Golden Parser is available for a variety of hardware platforms and operating systems.

To run the Golden Parser, at the prompt, type:

ibischk2 <filename>

There are two versions of this program: one for DOS based systems and one for UNIX based systems. Because of the differences in line feed/carriage return characters in DOS and UNIX, an IBIS file created with a DOS text editor may fail when checked with the UNIX version of the program. Utilities such as "dos2unix" and "unix2dos" are available to convert between the DOS and UNIX texts.

5.2.1.6 IBIS model validation

Once an IBIS model has been created, it shall be validated. Validation involves:

1) creating a behavioral simulation model in a target simulator that supports IBIS from the IBIS data,
2) running the model with standard loads, and
3) comparing the results against a transistor-level reference simulation using the same loads.

Any simulator that supports IBIS may be used. Simulator vendors that support IBIS may be found on the IBIS membership roster[2].

5.2.1.7 IBIS model verification

The last step in the modeling process is to verify the model by correlating simulation results with actual silicon measurements. All models shall be verified. Verification involves measuring the I/V curves and rise/fall times of an actual device and comparing them IBIS model data as well as verifying measuring the device waveforms and comparing them to simulation waveform. IBIS models shall be meet the acceptance criteria defined in 5.2.1.8 and confirmed that they fall within the maximum and minimum values used in the IBIS model. In addition, for devices in a motherboard or other test setup driving a known load, the oscilloscope waveforms shall be compared with simulation waveforms using the same load. An oscilloscope adds a load to the circuit and the oscilloscope response affects the measured result. This shall be taken into account.

The actual device shall be used to obtain I/V curves and rise/fall time information.

1. Available from the EIA/IBIS web site at www.eigroup.org/IBIS/tools.htm
2. Available from the following web address: www.vhdl.org/pub/ibis/roster/roster.html

The following laboratory equipment is required to recover the data:

a) programmable power supply with an output capable of sinking and sourcing current while maintaining the required output voltage - the output shall be floating,
b) curve tracer,
c) digital sampling oscilloscope with at least a 4,0GHz bandwidth,
d) low capacitance probe, e.g. FET,
e) test fixture used for DC measurements,
f) motherboard or specific test fixture used for AC measurements, and
g) thermoelectronic hot/cold plate (a peltier device), to control die temperature.

The device under test (DUT) shall be mounted in a DC test fixture. The power and ground pins of the DUT shall connected to the programmable power supply. A peltier device shall be attached to the device with a very thin layer of thermal grease. The temperature shall be adjusted as desired. After the die has stabilized at the desired temperature, an output on the DUT in the desired state (high or low) shall be selected. A curve tracer shall be used to obtain the I/V characteristics of the output.

During curve tracing of a hi-Z output, the curve contains both the transistor and the diode output characteristics. Curves for the diodes alone shall be obtained by selecting and tracing the output in its high impedance state.

Devices containing time-delayed feedback may produce bad results.

The pullup and power clamp data shall be referenced to Vdd as described in the IBIS specification. These data are obtained directly by connecting the curve tracer's negative (reference) lead to the Vdd supply of the DUT, then setting the curve tracer for a negative sweep. Ascertain no ground path connects back through the AC line between the device ground and power supply ground. For standard pulldown and clamp diode curves, the negative lead shall be attached to the DUT's GND supply. A positive sweep direction shall be used. The supply shall be floating.

Note that the curve tracer may not be able to sweep the entire range required by the IBIS specification. In this case, the curves shall be extrapolated to the required range.

Capturing rise/fall time data requires either a specific test fixture or a motherboard to which the DUT can be attached. Rise/fall time measurements require an oscilloscope with at least a 4,0GHz bandwidth. The effect on the rise/fall times of the device packaging and capacitive load shall be taken into account. A probe with extremely low loading, i.e. 1,0pF or less, such as a FET probe shall be used. The probe grounding shall be less than 120mm.

An oscilloscope picture of a buffer driving a known load shall be taken. Using the known packaging parameters and measured I/V curves, a simulation model of the device shall be constructed using a best estimate of the rise/fall time. With an IBIS simulator, the rise/fall times in the model shall be adjusted until the simulation results match the oscilloscope waveforms. Greater control is obtained by lifting the pin under test from any load other than the scope probe and simulating with a package and probe model.

5.2.1.8 Acceptance criteria

The following acceptance criteria shall be used when validating the device model:

a) I/V curve data - The measured I/V curve data shall fall within the maximum and minimum values specified in the IBIS model.
b) Rise and fall time data - The measured rise and fall time data shall fall within the maximum and minimum values specified in the IBIS model.

5.2.2 Maxwell matrices

5.2.2.1 Overview

Maxwell matrices are the solutions to the fundamental equations of macroscopic electromagnetic field theory. All real (physical) electric and magnetic fields satisfy Maxwell's equations. Maxwell matrices describe a cable construction through the use of specific RLGC matrices. These matrices describe the self and coupling parameters for resistance, inductance, conductance and capacitance respectively. The form of a Maxwell Matrix is shown in 6.2.4. There is no implied physical circuit topology in a Maxwell Matrix. Maxwell Matrices may appear similar to circuit models but are truly behavioral. Although these matrices describe the construction through parameters that are usually thought of as passive circuit components, they are not directly realizable into these components, except in the case of the self terms. See, for example Electromagnetics by J. Kraus.

5.2.2.2 Empirical extraction

Empirical creates a model through direct measurement. The objective is to create a circuit model that characterizes the cable with respect to frequency. The following methodology may be used to create a multi-line model. The process for fitting empirical data follows:

1) determine the relationship of α, β, and RLGC
2) measure the cable attenuation/loss, phase angle, and impedance
3) resolve RLGC over frequency
4) plot as fitted curves RLGC versus frequency
5) resolve α to fitted curve
6) compare the α of the fitted curve with the measured α
7) if the α error is not acceptable adjust the model and repeat 6
8) apply RLGC values into a transmission line circuit model
9) simulate the transmission line model
10) compare the results of the transmission line simulation with the parameters obtained in 2, iterate if necessary.

The theoretical analysis is based on the fundamental equations that govern transmission line theory. The complex propagation constant for a transmission line is given by Equation 3:

$$\alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

Equation 3 - Complex propagation constant

The complex impedance of a transmission line is given by Equation 4:

$$Z = \sqrt{((R + j\omega L)/(G + j\omega C))}$$

Equation 4 - Complex impedance

In these equations α represents the attenuation of the signal while β represents the angular velocity. By separating the real parts from imaginary parts, the RLGC parameters can be resolved over a range of frequencies.

Based on how many parameters that are directly measured, some assumptions shall be made in order to solve all RGLC parameters. The assumptions will effect the final model accuracy.

Next the RLGC data is plotted to fitted curves. Then the RLGC values from the fitted curves are used to resolve the curve's α value.

Validation is performed by comparing the fitted α values with the actual measurements. If the error is within a reasonable range, a circuit model is created by using the RGLC values from the fitted curves. A transmission line circuit model using the RLGC values is depicted in Figure 10.

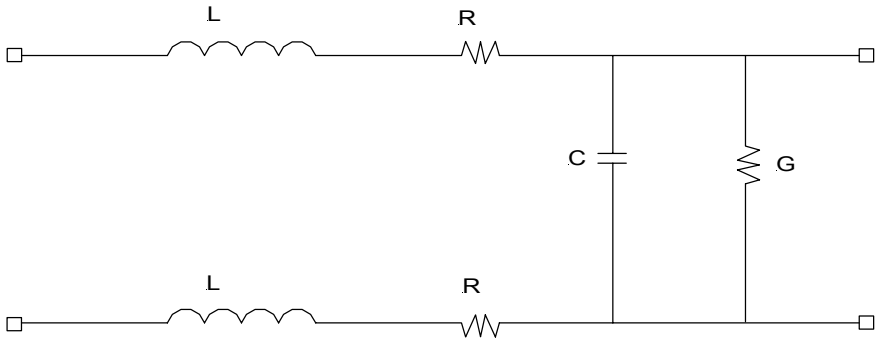


Figure 10 - Transmission line model

5.2.2.3 Validation

Validation is performed by simulating the circuit model by driving a signal and comparing the outputs with the actual measurements such as: impedance (magnitude and phase), time delay, inductance, conductance, and resistance.

5.2.3 Theoretical extraction

Theoretical extraction, in contrast, creates a model through the use of 2-D or 3-D electromagnetic simulation software instead of direct measurement. The method uses the dimensional data of the construction of the cable as well as the conductors' resistivity and the dielectric's permittivity and loss tangent to determine the RLGC characteristics. The major advantage of this method is that it can supply fully coupled multi-line models.

The process is to enter the physical parameters of the cable into the simulator. Completion of the simulation will result in a set of fully coupled RLGC matrices. However, some caveats shall be observed when using this approach.

The use of 2D extraction for twisted flat and round SCSI cables may not be practical due to the intrinsically 3D nature of these structures. 3-D extraction tools are recommended in these situations. However through experimentation, a point may be found in a 3-D structure where a 2-D representation will result in valid parametric data.

The permittivity and loss tangent values provided on raw material data sheets may not be representative of a manufactured cable. Permittivity and loss tangent versus frequency should be obtained by measuring material samples with a wide bandwidth material analyzer.

Another area for concern is how a cable structure is drawn for simulation. Simulators have a boundary that is drawn around the cable image. The simulator defines this boundary as ground. This ground shall be much larger that the cable image for the simulated results to be correct, especially if the cable in question is not shielded. The reason is that the E-field shall be perpendicular to this boundary for an accurate simulation. A good starting point is a boundary that is at least 10 times larger than the largest dimension of the cable. Experimentation is recommended. The boundary is large enough when, if by changing the boundary size, the simulated results vary minimally.

When entering cable detail into the simulation software, fine detail is not necessarily needed. These simulators determine the results through recursive partitioning algorithms. Starting with extremely fine detail results in extremely long simulation times. Depicting circular conductors as hexagons or octagons is often sufficient. The very thin lamination over insulation should be ignored. Shielded cables are often comprised of a braided shield over a wrap of aluminized mylar tape. Considering the frequencies present in SCSI cables, it is often sufficient to represent the shield as a tubular polygon representing the aluminum while ignoring the mylar and braid. The tube wall is set to the thickness of the aluminum, or may be set to zero thickness and be treated as a surface ground. This simplifies the model, speeds the overall data entry and simulation times, and the final deviation from measured data will be very small.

In 2-D simulators, with proper problem setup all odd mode simulations are correct as well as even mode capacitance. Even mode inductance values are correct if the simulations are performed using frequency independent LC matrices. However, when using the frequency dependant impedance and capacitance matrices, errors may occur in the resulting even mode inductance. Caution is advised when calculating even mode inductance (and therefore even mode impedance and even mode propagation velocity). This should not be a problem for SCSI simulations since when in differential operation all pairs in a SCSI cable operate in odd mode.

The performance of cables with twisted construction is highly complex. This is due to the structure which is usually periodic. This structure causes frequency dependent variations in impedance, phase, and attenuation. The mechanisms which causes these dependencies are not currently fully understood.

Validation should be performed with comparison to a manufactured cable. The impedance of individual pairs of the cable should be measured and the results compared to the model. The twisted regions are often of sufficient length that measured phase may also be used to further verify the simulation. In either case, if the difference between the measured and predicted profiles vary greater than acceptable limits, the simulation input data should be varied and the simulation performed again. Usually small changes in the dielectric constant will bring the results together. Note that only the self terms are determined by measurement. If the self terms are in agreement the coupled terms should also be within acceptable limits.

5.2.4 Interpreting Maxwell matrices

The following information is useful for obtaining odd mode impedance from a set of Maxwell matrices. Odd mode impedance is useful for differential SCSI. Even mode impedances do not apply since the current on the conductors in a pair will always be in opposition when signaling along the pair occurs. Most 2-D and 3-D modeling software outputs are in the form of Maxwell matrices.

An i by j Maxwell matrix, as well as any other matrix can be described as in Equation 5.

$$M = \begin{bmatrix} M_{11} & M_{12} & \dots & M_{1j} \\ M_{21} & & & Æ \\ Æ & & & Æ \\ M_{i1} & \dots & \dots & M_{ij} \end{bmatrix}$$

Equation 5 - Matrix description

The matrix is said to be square if i=j. The matrix is said to be symmetrical if $M_{ij}=M_{ji}$. In general Maxwell matrices are both square and symmetrical. A set of Maxwell matrices consist of an R_{ij}, L_{ij}, C_{ij} and sometimes a G_{ij}. These are often called RLGC matrices. These matrices fully describe the solution of Maxwell's equations for the transmission structure in question.

Suppose we have a 68 conductor or 34 pair SCSI cable, backplane, or connector described through these matrices. We would have a set of RLGC matrices that would be square and have 68 columns and 68 rows each. We want to determine the odd mode impedance of pair 14. The odd mode impedance is calculated by Equation 6.

$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}}$$

Equation 6 - Odd mode impedance

For either a symmetrical or asymmetrical matrix, the values of L_{odd} and C_{odd} are determined by a 2x2 sub-matrix bounded by $M_{2x-1,2x-1}$ and $M_{2x,2x}$ where x is the pair in question. In our example this would be $M_{27,27}$ and $M_{28,28}$. This is depicted in Equation 7.

$$Pair_{14} = \begin{bmatrix} M_{1,1} & \cdots & \cdots & \cdots & \cdots & M_{1,68} \\ \text{Æ} & & & & & \text{Æ} \\ \text{Æ} & & \begin{bmatrix} M_{27,27} & M_{27,28} \\ M_{28,27} & M_{28,28} \end{bmatrix} & & & \text{Æ} \\ \text{Æ} & & & & & \text{Æ} \\ \text{Æ} & & & & & \text{Æ} \\ M_{68,1} & \cdots & \cdots & \cdots & \cdots & M_{68,68} \end{bmatrix}$$

Where pair X is delimited by M_{II} and M_{JJ}

$$I = 2x \angle 1$$

$$J = 2x$$

Equation 7 - Pair conductor selection

The general case for determining Lodd and Codd are determined by using Equation 8.

$$L_{odd} = \left(\frac{L_{II} + L_{JJ}}{2}\right) \angle \left(\frac{L_{IJ} + L_{JI}}{2}\right)$$

$$C_{odd} = \left(\frac{C_{II} + C_{JJ}}{2}\right) \angle \left(\frac{C_{IJ} + C_{JI}}{2}\right)$$

Equation 8 - Odd mode inductance and capacitance

5.3 Circuit models

Circuit models represent the actual internal physical implementation of a component. They consist of an arrangement of interconnected electronic and passive models and are typically implemented by a SPICE representation.

An example of a circuit model would be a passive terminator. The model is defined through the use of SPICE elements representing the actual terminator resistor values and nodal connectivity. If the terminator is individually packaged, the nodal connectivity along with the inductive and capacitive values of the connector or package pins would be included.

Instrumentation probes are typically defined through the use of circuit models. Connectors could be defined through circuit models as well as behavioral models. In these cases the capacitance, resistance, inductance and nodal connectivity are defined. Probes could also have a SPICE transmission line element included. Multi-line connector models would include the inductive and capacitive coupling coefficients.

6 Models

6.1 Overview

The description of the model features for all types of components is found in 7. These models are divided into interconnect components, devices, and instrumentation. Interconnect components are passive while devices are active. Active and passive components may be either elemental or composite.

Manufacturers of SCSI components are encouraged to make simulation models available in a timely manner to control risk and facilitate useful system design validation. Manufacturers are also encouraged to make model development an integral part of their product design process and to support model availability from product announcement through end of production.

These models may be generated by a variety of means. For interconnect components this may include electromagnetic field analysis of the physical structure, or circuit extraction from a time domain reflectometer (TDR) or vector network analyzer (VNA) measurements. While for active devices the models may be generated from SPICE simulations or actual measurements of the active device parameters. The resultant models are then incorporated into higher level simulation tools to predict overall circuit performance.

When determining what is to be included in a model, the rise time of the signals which will be conducted through the structure need to be considered. Very short structures (less than 0,1 of the signal risetime, 1 nsec in this case) need not be considered in models. Consequently, TDR risetimes should be limited to above 100 picoseconds.

6.2 General requirements

6.2.1 Applicability

All models, as a minimum, shall conform to the requirements of this clause

6.2.2 Documentation

All models shall include documentation that contains the following information:

a) model name,
b) model supplier,
c) model version,
d) brief revision history,
e) model class description,
f) model limitations, dependencies, or both,
g) model creation methodology,
h) special instructions (if any) regarding use of the model or interpretation of the results,
i) validation method,
j) model support contact information, and
k) license requirements.

Additional information may be needed for each class of model and is described in the appropriate clause.

This information shall accompany the model and shall be contained in a separate ASCII text (*.txt) or Portable Document Format (*.pdf) file.

Equivalent circuit descriptions shall be contained in one or more ASCII text files. All SPICE model and library files shall contain the model name, model supplier, model version, revision history, limitations, and special instructions as part of the file.

All other textual documentation shall be contained in one or more ASCII text or Portable Document Format files. Graphical information (such as measurement and simulation results) may be contained in one or more Windows Metaformat (*.wmf) or Joint Photographic Experts Group (*.jpg) files.

The model shall also include an ASCII file named “packlist.txt” which contains a list of all the file names that belong to the model along with a brief description of the contents of each file. Complete model packages shall have all files grouped and compressed into a single file in both PC (*.zip) and Unix (*.tar) file formats.

6.2.3 Model name

To avoid duplication of names and possible confusion, it is recommended that the model name, as a minimum, be some variation of the supplier’s part number. Additionally the use of the model supplier’s vendor ID string before the model name is recommended. The vendor ID string is available at:

http://www.t10.org/lists/2vid.htm

If this URL is no longer valid, contact INCITS (www.incits.org) for the current URL.

6.2.4 Model class

All models shall be at least one of following two classes:

a) behavioral
b) circuit

Behavioral models describe the function of a component while circuit models describe the electrical structure.

IBIS models and Maxwell matrices are forms of behavioral models. IBIS models may be used to render devices, while interconnect components may rendered through Maxwell matrices.

Maxwell matrices represent the solution of Maxwell’s equations for the interconnect components. They describe the behavior of the interconnect. They consist of matrices of inductance, resistance, capacitance, and possibly dissipation. The matrices contain all mutual coupling information for the interconnect. The matrices are not necessarily directly convertible into discrete resistors, capacitors and inductors.

Circuit models describe the electrical structure. Lumped element models are examples of circuit models.

Lumped element models represent the electrical characteristics of the interconnect by single resistors, inductors, and capacitors.

Additional subclasses may be needed for each class of model. If needed, they are defined in the appropriate clause.

6.2.5 Model boundary

The model boundary defines the point where the modeled element joins another modeled element. This is the place where model measurements can be made - not to be confused with the mathematical boundary conditions used within simulation software.

6.2.6 Model limitations or dependencies

Any limitations or dependencies shall be recorded. These could include, but are not limited to:

a) minimum/maximum frequency of operation

b) voltage range over which the model is valid
c) temperature range over which the model is valid
d) states of operation

6.2.7 Model creation methodology

The model creation methodology that shall be used for each model component is defined in the appropriate clause.

6.2.7.1 Model creation stimuli

When creating behavioral models, a standard set of stimuli shall be used. The parameters of these stimuli shall be recorded in the model documentation in the model creation clause. These parameters are:

a) amplitude
b) timing
c) frequency range
d) rise time

When creating circuit models, a standard set of conditions shall be used when extracting parameters. The details of these conditions shall be recorded in the model documentation within the model creation clause. These parameters are:

a) frequency range
b) rise time
c) precision

6.2.7.2 Amplitude and timing

The general parameters regarding signal amplitudes and timings of the stimulus waveforms shall be as described in the SPI-x Standard unless otherwise specified.

6.2.7.3 Frequency range

While the spectral content of a SCSI signal depends heavily on the rise time of driver circuit and may contain measurable frequency components into the microwave region, for SSM-2 simulation purposes and model creation purposes, the frequency range shall be from 10MHz to 600MHz inclusive, unless otherwise specified.

6.2.7.4 Rise time

Signal rise time describes the time interval required for a signal to rise or fall between two specified limits. Model developers and model users alike should be aware that the rise times listed in various specifications (including SPI-x) may define threshold limits that differ from those used by simulation tools and that some interpolation or extrapolation may be required to derive values with consistent threshold limits. For example, simulators frequently define rise time as the interval between the 0% and 100% points of the steady state response, whereas SPI-x defines rise times between the 20% and 80% points. For the purposes of SPI-x SCSI simulation the rise times may be assumed as listed below unless otherwise specified.

a) interconnects for Single-Ended (SE) SCSI: rise time (20-80%) = 3,0 ns,
b) interconnects for Low Voltage Differential (LVD) SCSI: rise time (20-80%) = 1,0 ns.

6.2.8 Model validation

Each model provided shall be validated by its creator to ensure its accuracy. Accuracy is a criterion of how closely simulation results agree with physical measurements. The methods and criteria for validation defined in the appropriate clause are required as a minimum.

6.2.8.1 Accuracy requirements

Accuracy is a measure of how closely the model represents reality. For the purpose of this document, reality is what is precisely measured in the lab. A model or simulation is an idealized projection or prediction. The degree of model or simulation accuracy is constrained by time, detail, manufacturing variability, and modeling idealizations.

The correlation function is used to measure the accuracy between model and the underlying circuit model in the case of correlating IBIS models. Or between the model data and physical measurements in the case of RLGC cable models.

$$\mathrm{corr}(g,h)_j \equiv \sum_{k=0}^{N \angle 1} g_{j+k} h_k$$

Equation 9 - Correlation function

Since correlation is affected by factors described previously, it is not possible to define a uniform correlation requirement for each model described in this document. Therefore, each model type will have its own requirements specified within the clause defining that model.

6.2.8.2 Model validation stimuli

When validating behavioral models, a standard set of stimuli shall be used. The parameters of these stimuli shall be recorded in the model documentation in the model creation clause. These parameters are:

a) amplitude,
b) timing,
c) frequency range,
d) rise time, and
e) precision.

A standard set of conditions shall be used for validating circuit models. The details of these conditions shall be recorded in the model documentation within the model creation clause. These parameters are:

a) frequency range,
b) rise time, and
c) precision.

6.2.8.3 Amplitude and timing

The general parameters regarding signal amplitudes and timings of the stimulus waveforms shall be as described in the SPI-x Standard (see References) unless otherwise specified. All timing parameters are measured at the 50% level.

6.2.8.4 Frequency range

While the spectral content of a SCSI signal depends heavily on the rise time of driver circuit and may contain measurable frequency components into the microwave region, for SPI-x SCSI simulation purposes the frequency range of primary interest may be assumed as 0,0Hz to 600MHz inclusive, unless otherwise specified.

6.2.8.5 Rise time

Signal rise time describes the time interval required for a signal to rise or fall between two specified limits. Model developers and model users alike should be aware that the rise times listed in various specifications (including SPI-x) may define threshold limits that differ from those used by simulation tools and that some interpolation or extrapolation may be required to derive values with consistent threshold limits. For example, simulators frequently define rise time as the interval between the 0% and 100% points of the steady state response, whereas SPI-x defines rise times between the 20% and 80% points. For the purposes of SPI-x SCSI simulation the rise times may be assumed as listed below unless otherwise specified.

a) interconnects for Single-Ended (SE) SCSI: rise time (0-100%) = 3,0 ns,
b) interconnects for Low Voltage Differential (LVD) SCSI: rise time (0-100%) = 1,0 ns.

6.2.9 Model support contact information

6.2.10 License agreement

Licenses or Non-Disclosure Agreements may be needed as a prerequisite for obtaining the modeling information. In the case when the vendor feels his models require protection, a no-fee license/ confidentiality agreement is recommended, except in the case of IBIS models in which it shall not be required. An example of such an agreement is shown in A.4.1.

6.3 Interconnect component models

6.3.1 Overview

The passive interconnect components include cables, connectors, printed circuit boards and transition regions. An interconnect component model is a circuit representation that approximates the electrical behavior of the interconnect component.

The transition region is a locality where the transmission medium changes from one entity to another, i.e from a cable component to a connector.

Circuit simulations of interconnect components typically require models at two levels of complexity: single-line and multi-line. Single-line models describe the transmission behavior of a solitary signal path including its return path. Multi-line models describe the transmission behavior of several signal paths and their associated return paths along with the mutual coupling that exists between all the individual paths by virtue of their proximity, conductor geometry and the physical properties of the respective materials - conductivity, permittivity, permeability, etc.

Interconnect component models may be either of the behavioral or circuit model class.

6.3.2 Cables

6.3.2.1 Description

There are three types of bulk cable used within SCSI systems. These include flat ribbon cable, round shielded cable, and twisted flat cable.

6.3.2.2 Model boundary

There are two separate cable boundary categories. These are:

a) flat ribbon cable with IDC connector, - this includes twisted flat cables
b) round cable to connector

The boundary for a ribbon cable with IDC connector is the point on the cable where the insulation and copper conductor are not deformed.

The boundary for a round cable is from the beginning of the fan out required for connector attachment.

6.3.2.3 Model class

Cable models are behavioral models and shall consist of Maxwell matrices.

6.3.2.3.1 Methodology

Cable models shall be developed through the use of empirical or theoretical modeling. When completely coupled models are desired, theoretical modeling shall be used.

6.3.2.3.2 Correlation accuracy

The correlation accuracy for cable models shall be held to within 10% for flat or twisted flat cable, and to within 7% for round cable.

6.3.2.3.3 Description

The transition region is that area where a connector is attached to a cable or printed circuit board. This is an area of departure from the uniform characteristics of the cable or printed circuit board to that of the connector.

6.3.2.3.4 Model boundary

There are three separate transition region boundary categories. These are:

a) flat ribbon cable with IDC connector, - this includes twisted flat cables
   A) Connector in the middle of a flat in the body of a cable
   B) Connector at the end of a cable
b) round cable to connector
   A) Connector in the body with two fan outs
   B) Connector at the end of the cable (with only one fan out)
c) connector to printed circuit board.

The region for a ribbon cable with IDC connector is from the face of the IDC contact that touches the copper conductor to the point on the cable where the insulation and copper conductor are not deformed.

The transition region for a round cable, with the connector at the end of the cable, is from the beginning of the fan out required for connector attachment to the point of crimp, solder or weld on the connector. The transition region for a round cable, with the connector in the body of the cable, is from the beginning of the fan out required for connector attachment with the point of crimp, solder or weld on the connector to the end of the fan out on the other side of the attachment point.

The transition region for a connector to printed circuit board is from the face of the contact that touches the board trace to the end of the solder fillet, or in the case of press-fit conductors, the place where the barrel of the via is not deformed.

In each case the transition region shall be a passive circuit model taking into account an appropriate length of cable and length into the connector.

6.3.2.3.5 Model class

All transition regions models shall be circuit models.

6.3.2.3.6 Methodology

The transition region models shall be created in either Ansoft 2D or 3D Maxwell simulator software, or equivalent, as appropriate. The source shall be ± 1V differential pulsed voltage with frequency ranges as specified in 6.2.7.3 and rise times as specified in 6.2.8.5. The circuit models for the cable and connector regions shall be combined such that only one model is created for each transition region case.

6.3.2.3.7 Validation

Validation consists of manufacturing test assemblies, measuring the characteristics of the assemblies and correlating the modeling results with the measurement results. The 'risetime' of the TDR instrument should be set to 500 picoseconds.

6.3.2.3.7.1 Ribbon or twisted flat cable to IDC connectors

Validation shall performed using 1,0m and 0,5m of the cable to be modeled. In one case, the connector shall be placed in the middle of the cable with 0,5m on either side. In the other case, the connector is at the end of a 0,5m length of cable. Edge-launch SMA connectors shall be soldered to the cable wires. A 3,58 mm diameter semi-rigid coax shall connect the cable to the TDR. The voltage from the TDR shall be characterized with a high impedance probe at the connector.

6.3.2.3.7.2 Round cable to connector

Validation shall performed using 0,5m of cable and 1,0m of the cable to be modeled. The connector shall be placed on one end of the 0,5m cable and in the middle of the 1,0m length. Edge-launch SMA connectors shall be soldered to the cable wires. A 3,58 mm diameter semi-rigid coax shall connect the cable to the TDR. The voltage from the TDR shall be characterized with a high impedance probe at the connector.

6.3.2.3.7.3 Printed circuit board to connector

Validation shall be performed using 100mm of 120Ω differential printed circuit board trace. The trace may transition from one side of the printed circuit board to the other where the connector is placed on the board. The connector shall be placed at one end of the trace. Edge-launch SMA connectors shall be soldered to the trace ends. A 3,58 mm diameter semi-rigid coax shall connect the cable to the TDR. The voltage from the TDR shall be characterized with a high impedance probe at the connector.

6.3.2.3.8 Correlation accuracy

The correlation accuracy for the transition regions shall be held to within 5% for flat or twisted flat cable, and to within 10% for shielded round cable.

6.3.2.4 Connectors

6.3.2.4.1 Description

There are two types of connector models; mated connector and unmated connector. The mated connector models the mechanical and electrical contacts between two elements of an electronic system. The unmated connector models the presence of a stub on the electronic board due to an open connector.

6.3.2.4.2 Model boundary

The connector model boundaries for mated connectors are the shield for a shielded connector or the overmold for the unshielded connector and the points where the connectors attach to cable, and/or printed circuit boards. The boundaries for unmated connector are the shield for the shielded connector or the overmold for the unshielded connector, the points where the connector attach to cable, or printed circuit board, and the mating point of contacts.

6.3.2.4.3 Model class

Connectors consist of behavioral circuit models supplied in the form of LCR matrices (Maxwell matrices) or in the form of SPICE equivalent circuits. A basic connector SPICE model is made up of a collection of resistors, capacitors, inductors, and the mutuals, arranged as a circuit to simulate the electrical response of a connector.

6.3.2.4.4 Methodology

Connector parameters are extracted by Electromagnetic field solvers which extracts parameters from the 3D model structures by solving a set of equations (e.g. Maxwell's equations), or by empirical measurements which extract parameters directly from measurements in time or frequency domain.

The parameters will be extracted at frequency ranges as specified in 6.2.7.3 and rise times as specified in 6.2.7.4.

6.3.2.4.5 Validation

Validation of connector model requires data from empirical measurements to match data from the analytical results within acceptable margin.

If a physical device is available, the data for the empirical measurements can be used to correlate the model results. That will require every empirical result to have corresponding analytical result. In the case where a physical device is not available, the model results can be correlated to simple mathematical solutions.

Validation shall be performed using 12,5mm long traces on a 122Ω +/-12Ω controlled impedance printed circuit board with isolation between differential pairs.

6.3.2.4.6 Correlation accuracy

The correlation accuracy for connectors shall be held to within 10%.

6.3.3 Printed circuit boards

6.3.3.1 Model boundary

The model boundaries of PCBs are at the following locations:

a) connectors, and
b) device pins.

6.3.4 Model class

Printed circuit boards consist of behavioral models. The models are supplied in the form of Maxwell matrices . Their connectivity data are described in trace netlists.

6.3.4.1 Methodology

Listed are key data points to consider for modeling a printed circuit board. Development of both nominal and worst case models including process corner variations are encouraged. Developing multiline models are encouraged for the simulation of crosstalk.

The model development process is:

1) obtain transmission line geometries from PCB data / design requirements,
2) generate RLGC matrices for transmission line segments,
3) develop a topology from the known trace segments and components, and
4) build a netlist for each critical trace topology.

The following data from the PCB transmission line geometry are required to generate PCB trace models and may be obtained from the PCB database or design requirements.

a) trace widths,
b) thickness of traces and planes or the equivalent copper weight,
c) via barrel, pad and anti-pad diameters,
d) pad dimensions,
e) board material dielectric constants,
f) spacing within differential pairs, between differential pairs, and spacing between traces,
g) dielectric spacing between layers and planes, and
h) trace lengths of the nets to be simulated.

As indicated above, PCB trace models are obtained from RLGC matrices. These matrices are generated using a field solver that operates on the PCB transmission line geometries. Each variation in trace width or position within the board stackup requires a separate RLGC matrix. A trace segment is then derived by multiplying appropriate RLGC matrix by the segment length. A trace topology consists of a set of concatenated trace segments. Netlists are derived from the RLGC matrices and trace topologies.

6.3.4.2 Validation

Validation consists of manufacturing test coupons, measuring the characteristics of the coupons, modeling the coupon, and correlating the modeling results with the measurement results.

6.3.4.2.1 Test coupons

Test coupons provide a controlled environment for characterization. These coupons should contain examples of all significant trace, pad, and via topologies. These topologies could be examples of:

a) traces,
b) microstrip,
c) stripline,
d) broad coupled stripline,
e) offset broad coupled stripline, and
f) discontinuities.

In order to measure the topologies accurately each topology should have a section length of at least 0,5m. When including discontinuities such as pad, vias, and corners, there should be at least 0,5m of clear trace before and after the discontinuity. Launch sites on the test coupon shall use edge mount SMA connectors. Trace topology sections shall be terminated in their characteristic impedance. Traces connecting discontinuities shall have a characteristic impedances of 50Ω and be terminated in 50,0Ω.

6.3.4.2.2 Correlation accuracy

The correlation accuracy for printed circuit board models shall be held to within 12%.

6.4 Devices

6.4.1 Overview

The major devices are transceivers and terminators. Expanders are considered to be transceivers and shall be modeled as such. Each device consist of numerous circuit elements, both active and passive. To assure the correct representation of the device, the device package parameters are required to be included within the model. These parameters include the pin capacitance, pin inductance, pin resistance

6.4.2 Transceivers

6.4.2.1 Model boundary

The model boundary of transceivers are located at the package pins.

6.4.2.2 Model class

Transceivers are of the behavioral model class and shall consist solely of IBIS models.

6.4.2.3 Methodology

The methodology for deriving transceiver IBIS models are described in 5.2.1.

6.4.2.4 Validation

The model shall be verified using the methodology of 5.2.1.6 and 5.2.1.7.

6.4.2.4.1 Correlation accuracy

The correlation accuracy for transceiver IBIS models shall be held to within 2% between the IBIS model and the SPICE model from which it is derived.

6.4.3 Terminators

6.4.3.1 Description

Two variations of SCSI terminators exist, passive and active. Passive terminators consist solely of resistors, while active terminators consist of resistors and active elements such as regulators and switches. Only active terminator models are described, passive terminators are only used for single ended and HVD SCSI termination, they are not shown in the section. If passive terminations are modeled, they shall be of the circuit model class, and shall meet all other applicable sub-parts of this clause. IBIS terminator models are only a single resistor, active terminators are modeled as the composite assemblies to provide the details of the biasing voltages and/or currents used in a SCSI terminator.

6.4.3.2 Model boundary

Printed circuit board mounted terminator model boundaries are at the device pins. Plug terminator model boundaries are at the connector interface.

6.4.3.3 Model class

A terminator may be either a behavioral or circuit model.

6.4.3.4 Description

Active terminators may be used for single-ended and low voltage differential SCSI terminations. Active terminators shall correspond to one of the following configurations:

a) single-ended
b) low-voltage-differential
c) multi-mode

Single-ended terminators may only terminate a SCSI bus signal to ground. Low-voltage-differential are solely used for terminating low-voltage-differential SCSI bus signals. While multi-mode terminators include both single-ended and low-voltage-differential terminators and a mechanism for switching between them.

All models shall include packages parasitics. A separate model shall be required for each package in which the device is housed. These parasitics shall include the self resistance, inductance, and capacitance of each individual pin of the device package. The parasitics shall also include the self resistance, inductance, and capacitance of each individual bond wire within the package. Minimum, typical and maximum values shall not be used. Any coupling inductance and capacitance from the pin to another pin, or bond wire to bond wire, in the package that is greater than 5% of the self values of the respective pin or bond wire shall be included.

6.4.3.4.1 Single-ended terminator

An example of a single-ended terminator is depicted in Figure 11. The design details, location of the switch, and the frequency response are critical. Design details shall be extracted from the SPICE model of the terminator. The tolerance of the resistor in Figure 11 includes the switch. The model may require additional capacitance and inductance nodes.

Terminator models shall be capable of operating when the Termpwr voltage is in the 4,0V to 5,25V range or in the 2,7V to 5,25V range.

The source/sink current is specific to the terminators design and is critical for multi-line terminators.

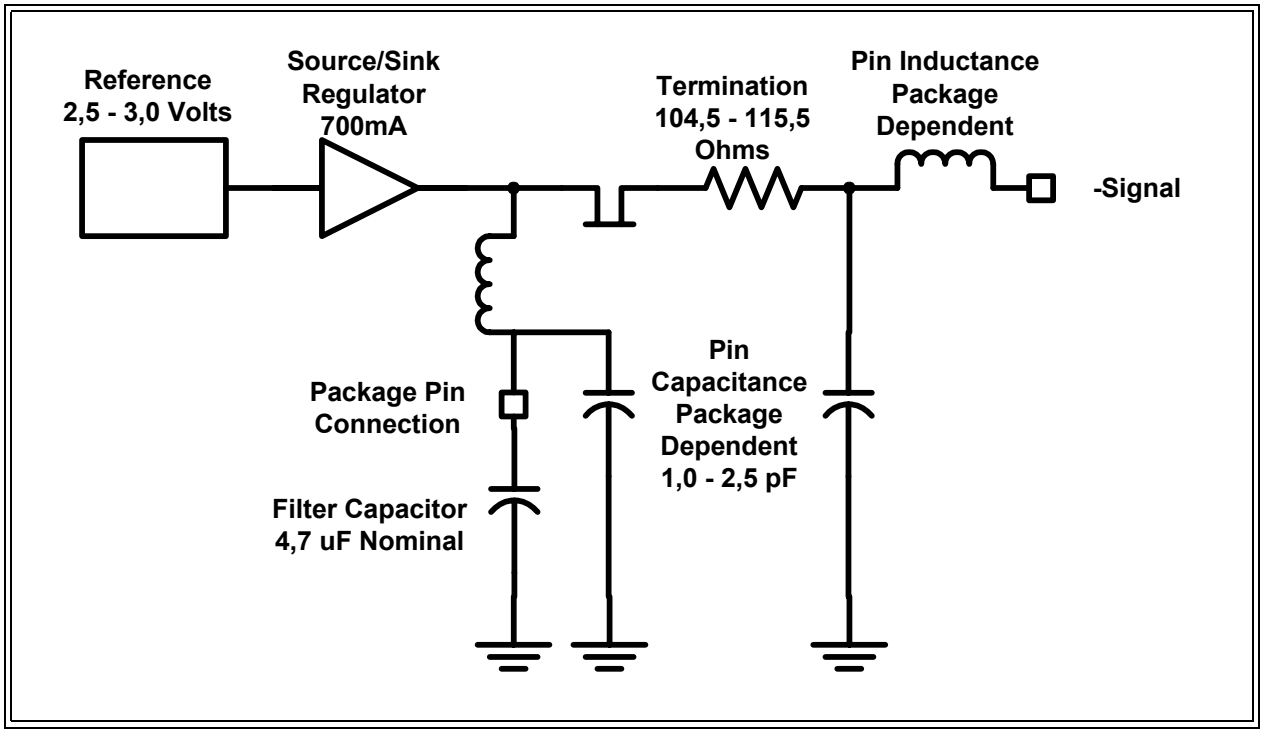


Figure 11 - Single-ended terminator

6.4.3.4.2 Low-voltage differential terminator

Low-voltage-differential terminators may be of two varieties, a Y terminator or a resistor stack terminator. The resistor stack may be constructed of discrete components and a regulator set for use in plug terminators and backplanes.

SPI-5 changes the terminator bias accuracy and adds programmable functionality. The bias measurement changed from 100 to 125mV which was defined in SPI-2 and stayed the same through SPI-4, then in SPI-5 current of 1 to 1,1mA is the bias. The differential termination impedance is 100 to 110Ω on power up for SPI-5, but can be adjusted from 55 to 130Ω. SPI-5 removes the single ended and multimode single ended, the SPI-5 adjustable terminator is a derivative of the Y terminator.

6.4.3.4.2.1 Y terminator

An example of a Y terminator is depicted in Figure 12. The design details, location of the switch, and frequency response is critical. Details shall be extracted from the SPICE models for the terminator. The tolerance of the resistor includes the switch of Figure 11. The model may require additional capacitance and inductance nodes. The pin and bond wire capacitance and inductance are specific to each package pin. If a package type is changed, these parameters shall be adjusted to reflect the new values. The voltage range is for both 4 to 5,25V and 2,7 to 5,25V terminators. The common mode source/sink current is specific to the terminators design and is not normally critical unless a multi line terminator is simulated.

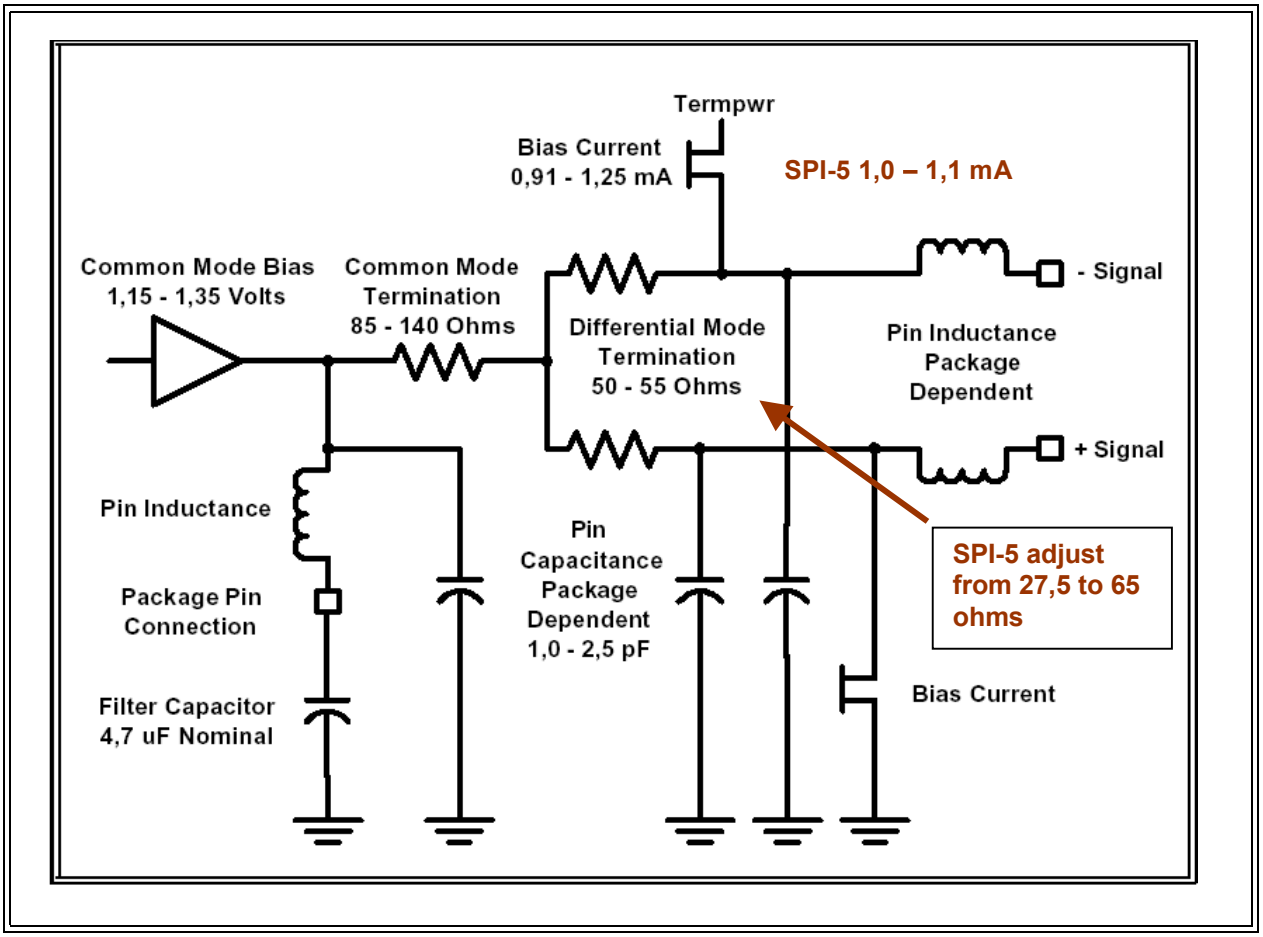


Figure 12 - LVD Y terminator

SPI-5 allows the differential mode terminators to adjust, on power up the differential mode terminating

resistors are 50 to 55Ω as in SPI-2 through SPI-4, the resistors can be adjusted from 27,5 to 65 ohms nominal value with the tolerance using domain validation to test for reflections. The bias current range is reduced in SPI-5 to 1,0 to 1,1mA.

6.4.3.4.2.2 Resistor stack terminator

An example of a resistor stack terminator is depicted in Figure 14. A resistor stack terminator requires two reference voltages from source/sink regulators. One from the bottom of the resistor stack, and one from the top of the stack. The stack consists of three resistors. In the integrated stack terminator, the series switches dramatically affect the frequency response. The reference voltages shall be source/sink with the

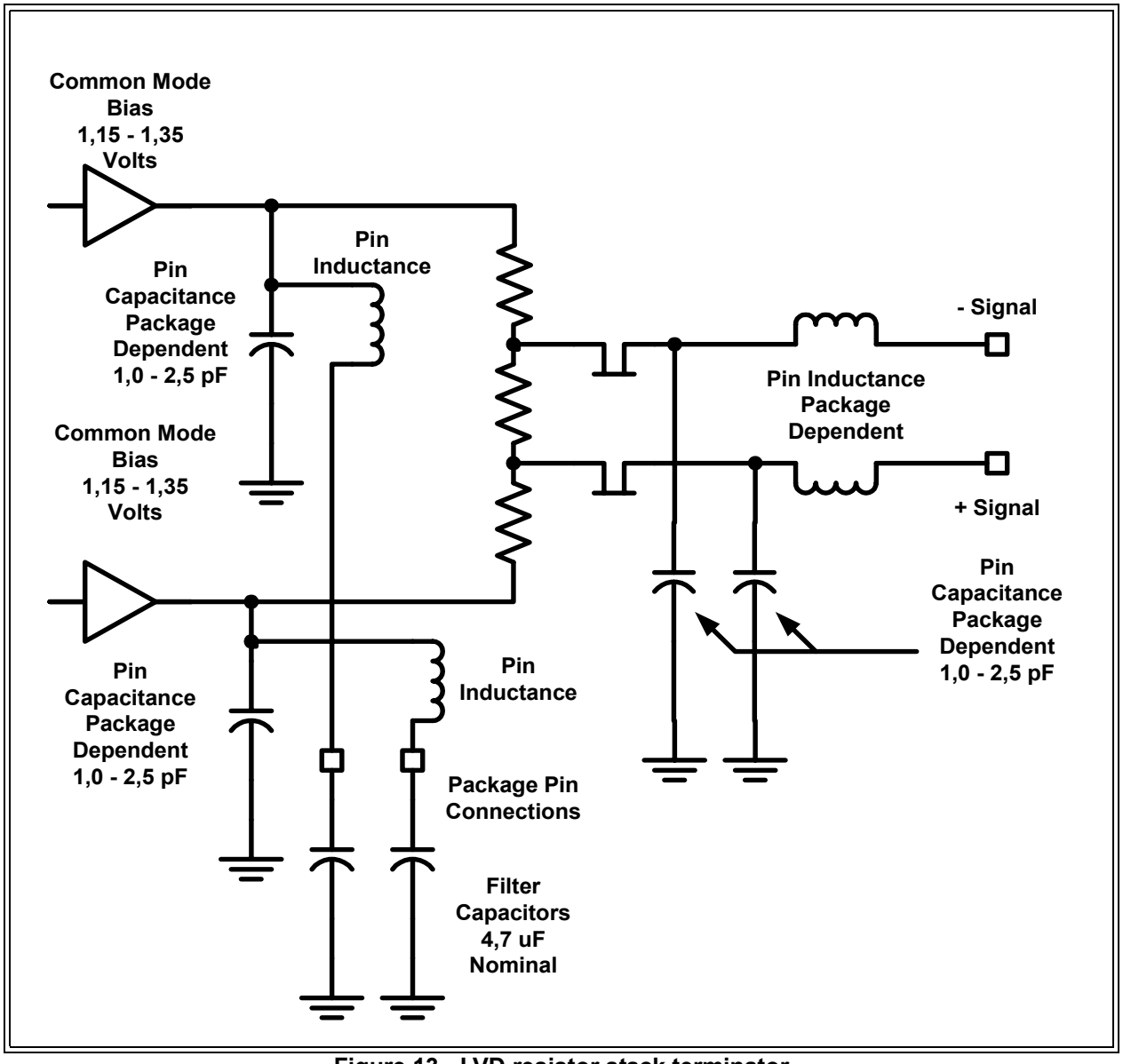


Figure 13 - LVD resistor stack terminator

correct differential for the 100 to 125 mV differential bias and have the correct offset for the 1,25V common mode bias. The parasitics and the frequency response of the components used are critical to developing a good model.

6.4.3.4.3 Multi-mode terminator

Multimode terminators combine a single-ended terminator, a ground switch for the positive signal line, and a low-voltage-differential terminator. An example of a multimode terminator is depicted in Figure 13. The low-voltage-differential section of the terminator shall be of either a Y or a resistor stack configuration.

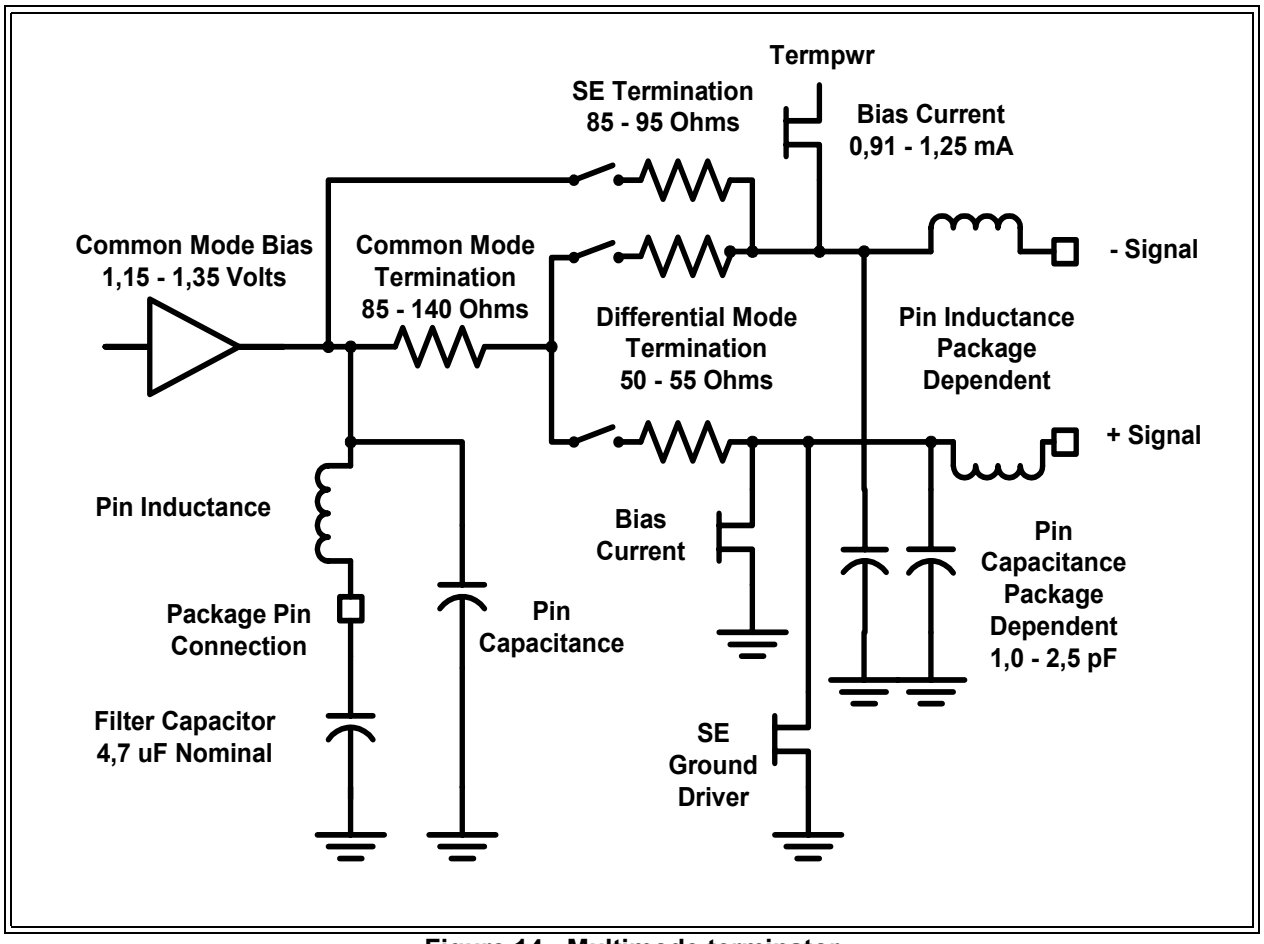


Figure 14 - Multimode terminator

6.4.4 Methodolog

Behavioral models shall be derived using the methodology of 5.2.1.

Circuit models shall consist of SPICE elements. Circuit models shall contain package parasitics.

6.4.5 Validation

Validation shall consist of testing the actual component against the model with the basic DC parameter test, open circuit voltage, load test. These verify the resistance values and regulator values. Validation shall also include AC parameter testing. This requires the use of a capacitance bridge and a network analyzer. Each terminator type shall be tested differently for the most accurate measurement of the specific internal components tested.

This data normally taken in part design validation, manufacturers models shall be verified against the device engineering data.

6.4.5.0.1 Correlation accuracy

The correlation accuracy for terminator IBIS models shall be held to within 2% between the IBIS model and the SPICE model from which it is derived.

The correlation accuracy for discrete element terminator models shall be held to within 1%.

6.5 Instrumentation models

6.5.1 Description

During validation of SPICE derived models, or models of similar construction, an instrumentation model shall be used when comparing measured data to simulation data. These instrumentation models, composed of probe and instrument models, shall be included in the model documentation, as illustrated in Figure 15[1].

Whenever a measurement is made, the connection of the instrumentation affects the measurement. This effect is twofold. The capacitance of the probe affects the loading of the circuit. Also, the bandwidths of the probe and instrument set an upper limit on the observed rise time of the signal.

6.5.2 Model boundary

The boundaries of the probe model are the connection point to the circuit or DUT, and the connection to the instrument. The boundary of the instrument is the point at which the probe is attached to the instrument.

6.5.3 Model Class

Probe models are primarily circuit models. At frequencies above 250MHz, a combination of behavioral models (transmission lines) and circuit models shall be used to depict the operation of the probe.

Instrument models shall be described by transfer functions and are therefore behavioral in nature.

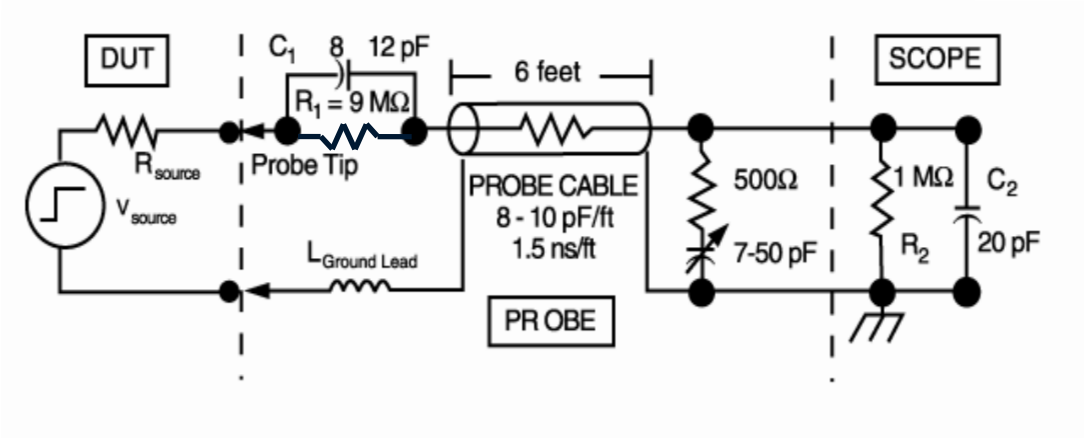


Figure 15 - Instrumentation Model

1. Probe Tutorial, Tektronix, page 10.

6.5.4 Probe models

A probe model includes probe tip, probe cable, and sub-circuit, as illustrated in Figure 15.

The values of C_1 at probe tip are typically:

a) 90pF for 1x passive probes
b) 10pF for 10x passive probes
c) 1,5pF for FET active probes
d) approximately 0,75pF for 50Ω divided probes

The values of R_1 at probe tip are typically:

a) 10kΩ to 1MΩ for passive probes
b) 10MΩ for active probes

All the below models are shown as examples only, equivalent products with their own models exist.

6.5.4.1 Models for Agilent active probe (probe tip)

A simple model for Agilent 1156A and 1158A active probe is composed of resistor R1 as well as R2 and the capacitor C1, as shown in Figure 16[1]. R2 is 100KΩ, usually. Here, R1 and C1 are dependent on the tip structures, as listed in Table 11. In addition, Table 12 summarizes the input impedance and capacitance of Agilent active probes.

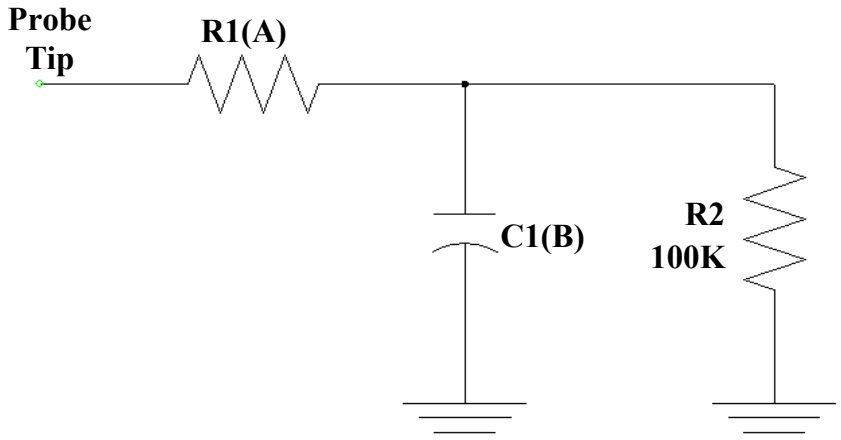


Figure 16 - Agilent 1156A Active Probe Circuit Model

Table 11 - R1 and C1 for different configurations of Agilent 1156A and 1158A active probes

Configurations	R1 (Ω)	C1 (pF)
110Ω Passive Signal Pin and Solderable Ground Socket	125	0,9
130Ω Resistive Signal Pin and Ground Blade	165	0,8

1. Agilent 1156A User's Guide

50mm Resistive Signal Leads and Solderable SMT/ Through-Hole Ground Pin	230	1,2
Socket-End 100mm Resistive Signal Lead and Solderable SMT or Through-Hole Ground Pin	275	1,8

Table 12 - Input impedance and input capacitance of Agilent active probes

Model	Frequency Range (Hz)	Input Resistance (Ω)	Input Capacitance (pF)
1156A	1,5 G	100K	0,8
1152A	2,5 G	100K	0,6
1158A	4 G	100K	0,8
85024A	3 G	1 M	<0,7
1155A	750 M	1 M	2
1157A	2,5 G	100K	0,8

6.5.4.2 Models for Agilent active differential probe (probe tip)

A simple model for Agilent N1025A active differential probe shown in Figure 17, including the mutual capacitance of 0,1pF. In addition, Table 13 summarizes the input impedance and capacitance of Agilent active differential probes.

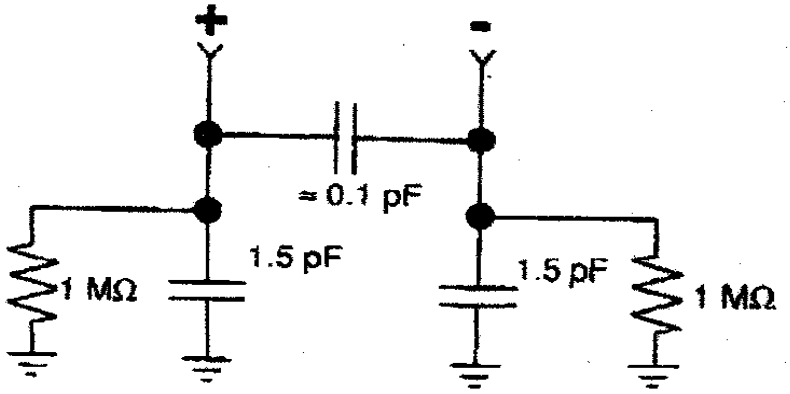


Figure 17 - Agilent 1025A Differential Probe Circuit Model

Table 13 - Input impedance and input capacitance of Agilent active probes.

Model	Frequency Range (Hz)	Input Resistance (each side to round; Ω)	Input Capacitance (each side to round; pF)	Input Capacitance (between inputs; pF)
N1025A	1,5G	1M	<1,5	<0,85
1154A	500M	1M	6	3,1
1159A	1G	1M	<1,5	<0,85
1153A	200M	1M	7	N/A

6.5.5 Methodology

The circuit description of probes and instrument transfer function shall be obtained from the equipment manufacturer.

6.5.6 Correlation accuracy

The correlation accuracy for the probe model shall be held to within 5% in the specified frequency range.

7 Standard model constructions

7.1 Host bus adapter / target board

7.1.1 Description

Host adapter boards and target boards are composite assemblies consisting of a number of model elements.

A host adapter board consists of the following elements:

a) PCB board,
b) connectors,
c) transceiver chip, and
d) terminator chip.

A target board consists of the following elements.

a) PCB board,
b) connector, and
c) transceiver chip.

7.1.2 Model boundary

The model boundaries of a host bus adapter or target board are located at the connectors. Optionally the following model boundaries may be considered:

a) transceiver chip pins, and
b) terminator chip pins.

7.1.3 Model class

Host bus adapters and target boards consist of a combination of behavioral and circuit models.

7.1.3.1 Methodology

The creation procedure for host bus adapter/target board models is:

1) request models,
2) build the netlist, and
3) simulate and review data.

When requesting models the following considerations should be kept in mind:

a) transceivers - driver and a receiver models shall both be included.
b) connectors
c) single and multiline models should both be included.
    single line models will not include crosstalk during signal integrity investigation
    multiline models may take much longer to receive
    are models for un-mated connectors necessary? (model as stubs)
d) general considerations
    the models shall work for various edge rates (slow, typical, fast)
    vendor models shall be kept in a centralized/secure location. vendors usually distribute them under NDA.
    some correlation of the models is recommended (compare simulation and lab data)
    request models well in advance of need.

7.2 Cable assemblies

7.2.1 Description

Cable assemblies consist of the following elements:

a) bulk cable
b) connectors
c) transition regions

7.2.2 Model boundary

The model boundaries for the cable assemblies are the shields for shielded cable or the jackets/over-mold for the unshielded cable and the points where the boundary of the transition model attachs to printed circuit board traces.

7.2.3 Model class

Cable assemblies consist of behavioral and circuit models.

7.2.4 Methodology

Cable assembly models shall be developed through the use of empirical data or parameter extractions or by concatening the models derived for the cable, the connector and the transition region.

7.2.5 Validation

The model shall be verified using the methodology of 5.2.2.3 .

7.2.6 Correlation accuracy

The correlation accuracy for cable models shall be held to within 10% for flat or twisted flat cable, and to within 7% for round cable.

7.3 Backplane

7.3.1 Description

Backplanes are composite assemblies consisting of a number of model elements.

A backplane consists of the following elements:

a) PCB board
b) connectors
c) transition regions

A backplane optionally consists of the following elements.

d) transceiver chip
e) expander chip
a) terminator chip

7.3.2 Model boundary

The model boundaries of a backplane are located at the connectors. Optionally the following model boundaries may be considered:

a) transceiver chip pins
b) expander chip pin
c) terminator chip pins

7.3.3 Model class

Backplanes consist mainly of circuit models. Optionally they may contain behavioral models.

7.3.4 Methodology

Listed are some key data points to consider for simulation of a backplane. Initial simulations are used to optimize PCB routing topologies. Simulating worst case scenarios require model correlation, process corners, and multiline models for crosstalk.

The process for developing the model is:

1) request models
2) build the netlist
3) simulate and review data

When requesting models the following considerations should be kept in mind:

a) transceivers and expanders
   driver and a receiver models shall both be included.
b) connectors
   single and multiline models should both be included.
   single line models will not include crosstalk during signal integrity investigation
   multiline models may take much longer to receive
   are models for un-mated connectors necessary? (model as stubs)
c) general considerations
   the models shall work for various edge rates (slow, typical, fast)
   vendor models shall be kept in a centralized/secure location. vendors usually distribute them under NDA.
   some correlation of the models is recommended (compare simulation and lab data)
   request models well in advance of the need

7.4 System models

7.4.1 SCSI System Model Example

This primary purpose of this effort is to determine which simulation tool will allow a SCSI low voltage differential (LVD) initiator board to be connected to a multi-slot SCSI backplane using a cable. The tool shall support IBIS models for the active components and RLGC models for the cables and connectors.

7.4.2 Simulation Overview

Since SCSI driver IBIS models that could perform cutback did not exist, 160M bytes per second operation was used for this phase of the simulations. New IBIS features now exist that allow cutback drivers that can be used for these simulations, but were not available when this simulation was done. Using the Cadence SpectraQuest tool, a SCSI system model was created. A SCSI initiator IBIS model was used as an SCSI signal source. An edge coupled, coplanar micro strip configuration printed circuit board model was used to

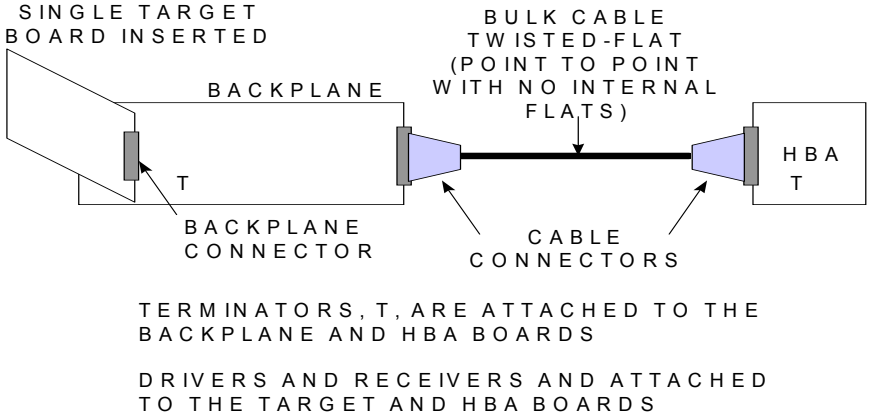
connect the SCSI initiator to a surface-mounted 68-pin SCSI unshielded receptacle connector. The PCB model had a differential impedance of approximately 120 Ω. A 2x2 RLGC model was used to represent a differential pair of conductors of a twist and flat cable. The other end of the cable is terminated in a 68-pin unshielded EBBI style plug connector. An Allegro board file from an existing six-slot SCSI DASD backplane was imported. The backplane was designed for SPI-3 SCSI operation. It has six SCA-2 connectors with an electrical spacing of about 3 inches. It uses LVD SCSI signal terminator modules at the far end of the SCSI bus and next to the initiator module. The differential impedance of the unloaded backplane is approximately 130Ω. The backplane also has a SAF-TE module for monitoring system environmental parameters. All six slots of the backplane have hard drives inserted.

The original idea was to use IBIS models for the simulation components. However, it turned to be difficult to obtain verified IBIS models from most of the vendors. The IBIS models that we received either would not import into our system or had obvious errors that took multiple iterations with the vendors to correct. None of the vendors had any data to prove that the IBIS models were in any way correlated to reality. Most of the connector models were delivered to us in Spice format. The SCA-2 connector spice models were too cumbersome to simulate in a multi-connector backplane environment in a reasonable length of time. We found that a lumped RLC model gave us comparable results to the detailed single connector spice model in our environment and reduced the simulation time significantly. Table 14 lists the components involved in the SCSI system simulation and the model types associated with them. The connector models shall be simplified multi-line models.

Table 14 - SCSI System Simulation Model Types

Device	Model Type
SCSI Initiator	IBIS
Initiator PCB	Topology
68-Pin ANSI SCSI PCB Connector	Spice / RLGC
68-Pin ANSI SCSI Cable Connector	Spice / RLGC
Twist and flat cable	RLGC
68-Pin EBBI SCSI Cable Connector	Spice /RLGC
68-Pin EBBI SCSI PCB Connector	Spice / RLGC
Backplane PCB	Topology
HDD SCA-2 Connectors	Spice / RLGC
Hard Drives	Empirical text data
SAF-TE Chip	IBIS
SCSI LVD Terminator	Spice

Figure 18 - Overview of SCSI Simulation System



7.4.3 Details of Simulation

The simulation system is shown in Figure 18. A test board using the LSI SCSI initiator integrated circuit is connected using a coaxial cable to an Arbitrary Waveform Generator (AWG). The test board is connected using a twist and flat TPE cable to the SCSI hard drive backplane. The AWG is programmed to generate a string of data consisting of 3 low periods, 1 high period, 3 low periods, 3 high periods, 1 low period, 3 high periods, 1 low period, 1 high period, 1 low period, 1 high period, 1 low period, 1 high period. A LVD oscilloscope probe is attached to the SCSI signal near the initiator cable connector.

This simulation defines the period at 25 ns, which translates to a bus speed of 160 Mega transfers per second. This string is short enough to simulate in a reasonable length of time. The expectation of this effort is to validate the models used in the simulation so that more detailed results can be obtained later. Figure 19 shows the simulation results using the above described data string. The actual waveforms are shown in Figure 20.

Figure 19 - Results of Simulation

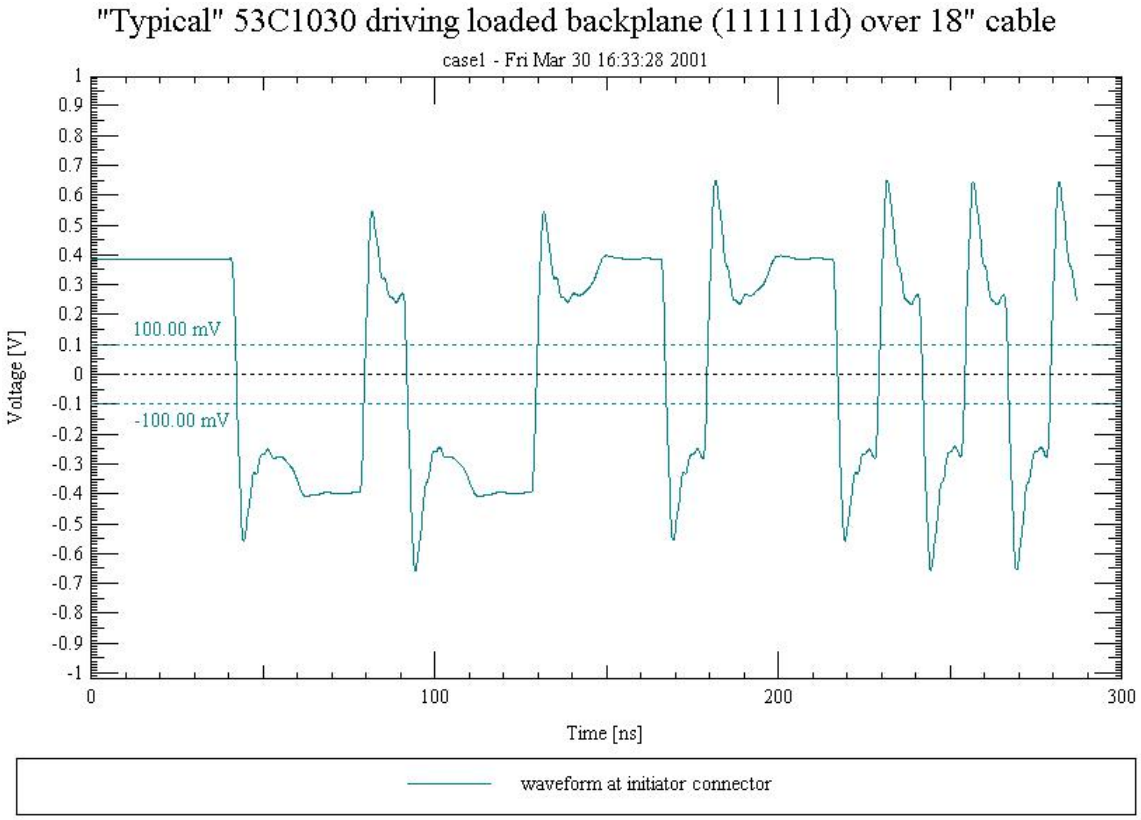
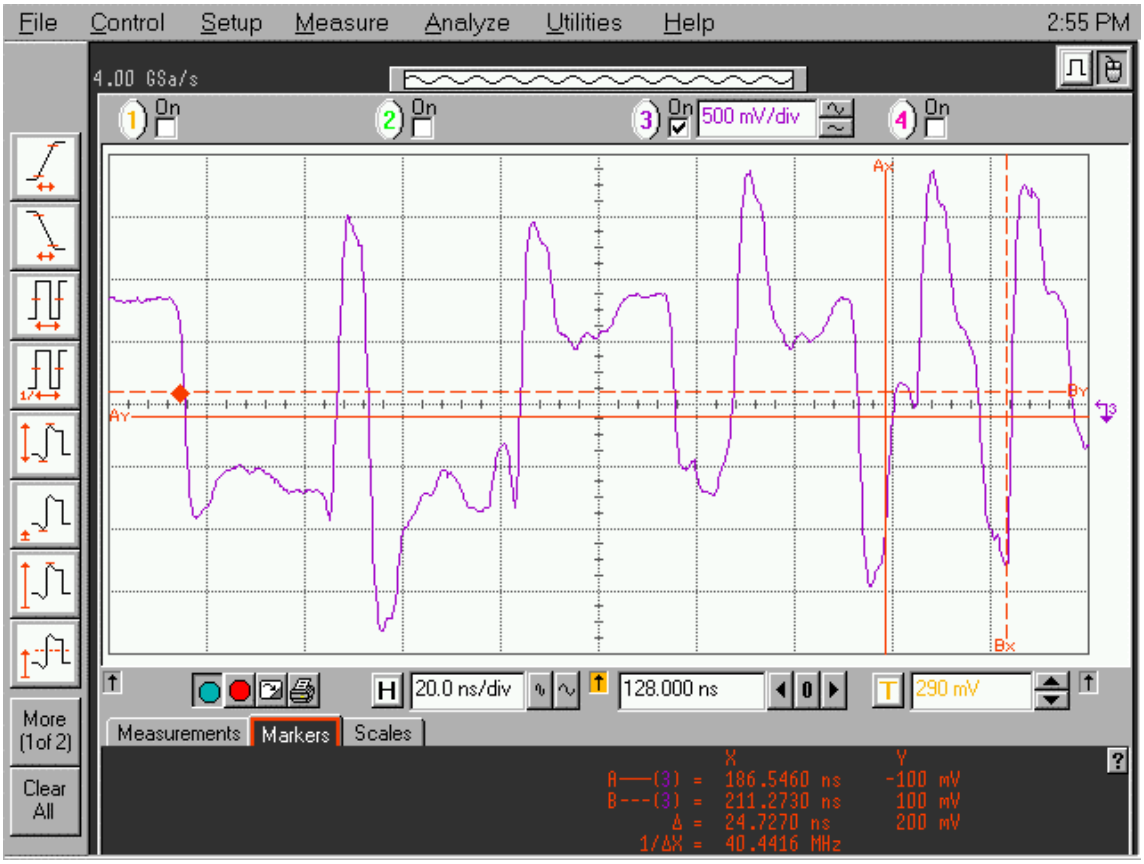


Figure 20 - Actual Waveforms at the SCSI Initiator Connector



8 Measurement and validation

Each model shall be validated to ensure its accuracy. Standard measurement points, instrumentation, and methods shall be used to guarantee repeatability.

8.1 Measurement points

Measurement points may be either model measurement points or physical element measurement points. There are limitations to either. In the case of model measurement points, model elements are measured at the model boundaries. In the physical case, measurements may be made at the element boundaries but there are certain exceptions. For example, cable assembly measurements may be obtained at the connectors, but measurements at the transition region and bulk cable region are problematical.

8.1.1 Physical measurement points

8.1.1.1 Transceiver

A transceiver shall be measured at the device pins.

8.1.1.2 Terminator

A terminator shall be measured at the device pins.

8.1.1.3 Transceiver board

An unpopulated transceiver board shall be measured at the transceiver pads and the connector pads.

8.1.1.4 Transceiver board assembly

A populated board shall be measured at the connector pads.

8.1.1.5 Cable assemblies (media, transitions, connectors)

Reflected measurements shall be performed at one specified extreme end of an assembly. Transmission measurements may be performed between any two or more connectors since any connector may carry input and output signals.

8.1.2 Device connector

All pins shall be used for physical measurement points.

8.1.3 Chip to board interface

The chip to board interface shall be measured at the transceiver pads on the printed circuit board.

8.1.4 Terminator connector

All pins shall be used for physical measurement points.

8.2 Acceptance criteria

Models shall be correlated to measured data.

8.3 Model Validation Procedure

8.3.1 Overview

This clause lists the model validation tests for each model type. The test fixtures and test procedures are defined in the Passive Interface Performance Standard (PIP).

Validation shall be performed using either reflected measurements or transmission measurements. Reflected measurements shall be obtained from a time domain reflectometer. Transmission measurements shall be obtained from a vector network analyzer.

8.3.2 Transceiver

Test shall be performed with specified signals, standard loads and standard instrumentation. Transceiver compliance shall be verified from the pins into specified loads using the test board and probe combination. Transceiver performance shall be measured into a load equal to the selected board and media.

8.3.3 Bulk Cable

The RLGC matrix can be verified using PIP measurements; specifically impedance, capacitance, propagation delay and insertion loss.

RLGC inductance is calculated from impedance and capacitance, or impedance and propogation delay.

RLGC resistance and conductance are verified using insertion loss measurements.

8.3.4 Cable assemblies

Tests shall be performed with specified signals, standard loads and standard instrumentation. The cable assembly element and the relevant instrumentation for each element is described in Table 15.

Table 15 - Cable assembly test instrumentation

Cable assembly element	Relevant instrumentation
Uniform transmission lines	Time domain reflectometer, network analyzer
Transition region	Time domain reflectometer
Connector	Vector network analyzer
Uniform transmission lines with integrated transition regions	Time domain reflectometer

8.3.5 Transceiver boards, target boards, and backplanes

Tests shall be performed on the bare boards with specified signals, standard loads and standard instrumentation. The test and relevant instrumentation are described in Table 16.

Table 16 - PCB test instrumentation

PCB test	Relevant instrumentation
Impedance	Time domain reflectometer
Time delay	Time domain reflectometer
Attenuation	Network analyzer

8.4 System model validation procedure

The system model validation is a comparison of the simulated model waveforms and the measured waveforms.

The example in 7.4 demonstrates the need to have the simulation models validated with the actual devices they purport to represent. The connector models need to be simplified multi-line models. The impedance of a loaded SCSI system is much lower than the unloaded system. The resistance values used for the termination of the bus should be matched to the actual system impedance. In the actual data, the waveform Figure 20 charged up the bus with a DC bias that was not shown in the simulation. A reflection into the switching region in the actual waveform did not show up in the simulation Figure 19. Nevertheless, the results obtained in the lab and in the simulation are similar enough to encourage the effort to continue.

9 Simulation strategy

9.1 System configuration

Receivers that modify the input signal, either adaptively or not, are not considered to be part of the system simulation configuration.

The following is a list of system configurations that require different considerations from a modeling perspective. Note that a SCSI device may be a SCSI expander.

a) basic structure shown in the trial simulation work (single initiator/cable/single target on backplane)
b) basic structure shown in the trial simulation work (single initiator/cable/multiple targets on backplane)
c) expander isolated backplane with multiple targets on backplane
d) multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). All connectors have SCSI devices attached.
e) multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). Only the far end connector has a SCSI device attached - all other connectors have no SCSI devices attached - requires an un-mated half-connector model.
f) single target in an enclosure with a cable connection on the enclosure bulkhead to a round cable to an HBA in a different enclosure.

9.2 Data patterns

9.2.1 Overview

Standardized data patterns shall be used when interchanging information about simulation results. These data patterns shall take the following into consideration:

a) inter-symbol interference effects on single lines
b) crosstalk from other SCSI lines
c) driver release effects (driven to hi Z)
d) residual jitter (clock like patterns)
e) word patterns as well as individual patterns
f) SSO (Simultaneous Switching Output)
g) worst case digital patterns
h) sinusoidal patterns

The training pattern specified in SPI-4 or SPI-5 shall be used as one input pattern. Clock-like patterns are also needed (full data rate, 1/32 of the data rate). Isolated “1's” and “0's” - stable period at least a round trip time before the isolated bit.

The training pattern for a DATA IN phase shall conform to SPI-5 10.7.4.2.2. The training pattern for a DATA OUT phase shall conform to SPI-5 10.7.4.2.3. The receiving SCSI device shall use some or all elements of the training pattern to achieve deskewing (see SPI-5 10.7.4.5). The transmitting SCSI device shall not make an intentional shift in relative timing between the data bus signals and the REQ or ACK signal during the DT data phase.

NOTE 1 - The requirement to not intentionally change relative timing does not include the effects of ISI, noise, or jitter.

The training pattern consists of three sections; A, B, and C. Each section contains a different pattern that may be used to train circuits within a receiver.

All data patterns listed is this section as text shall be considered as transmitting the rightmost character first (LSB).

9.2.1.1 TDT DATA IN phase training pattern

The SPI-4 DATA IN training pattern is depicted in Figure 21.

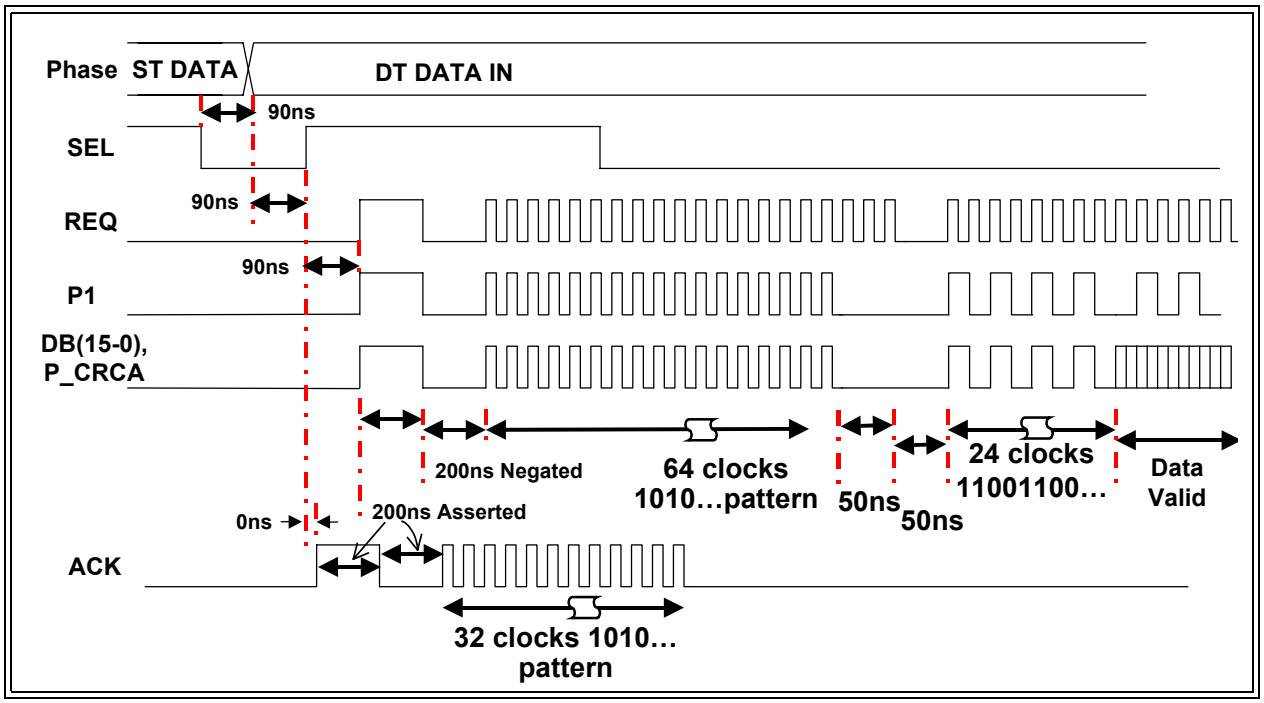


Figure 21 - DATA IN training pattern (SPI-4)

The target shall indicate a training pattern is going to occur on a DT DATA IN phase by:

1) releasing SEL for a minimum of two deskew delays;
2) asserting the SEL signal a minimum of two system deskew delays; and
3) then asserting the REQ signal.

The SCSI target port shall begin the section A of its training pattern only after all the signal restrictions between information transfers phases listed in SPI-5 10.12 or the signal restrictions between a RESELECTION phase and a DT DATA IN phase listed in SPI-5 10.6.2 are met.

For fast-160, the SCSI target port shall transmit the training pattern as described by section A, section B, and section C in this subclause. For fast-320 the SCSI target port shall transmit the training pattern as described by section A, section B, and section C in this subclause except that the polarity of DB(0, 1, 4, 5, 9, 10, 13, 14, and P_CRCA) shall be inverted during transmission of section A, section B, and section C (i.e., where it is specified that these signals shall be asserted, they shall be negated, and where it is specified that these signals shall be negated, they shall be asserted). These signals shall return to their normal polarity after completion of training pattern transmission.

Start of section A:

1) if precompensation is enabled then set the drivers to the strong driver state;
2) simultaneously assert REQ, P1, P_CRCA, and DB(15-0) signals;
3) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
4) simultaneously negate REQ, P1, P_CRCA, and DB(15-0) signals;
5) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
6) set precompensation to negotiated state;
7) negate SEL signal;

8) simultaneously assert and negate REQ, P1, P_CRCA, and DB(15-0) signals at the negotiated transfer period for 800 ns (e.g., the equivalent of 128 transfer periods at fast-160);

Start of section B:

1) wait 1200 ns from the first assertion of REQ in step 2 of section A (e.g., the equivalent of 192 transfer periods at fast-160);
2) keep the P1, P_CRCA, and DB(15-0) signals negated while continuing to assert and negate REQ at the negotiated transfer period for 50 ns (e.g., the equivalent of 8 transfer periods at fast-160);
3) keep the P1, P_CRCA, DB(15-0), and REQ signals negated for an additional 50 ns;
4) simultaneously assert and negate P1, P_CRCA, and DB(15-0) signals at twice the negotiated transfer period (i.e., simultaneously repeat a 1100b bit pattern on each signal) while asserting and negating REQ for 300 ns at the negotiated transfer period (e.g., the equivalent of 48 transfer periods at fast-160); and

Start of section C:

1) assert and negate REQ at the negotiated transfer period for 800 ns and at the same time assert and negate P1 at twice the negotiated transfer period while repeating a 0000010011111011b bit pattern on each of the P_CRCA and DB(15-0) signals (e.g., the equivalent of 128 transfer periods at fast-160).

The SCSI initiator port shall begin its training pattern independent of the start of the SCSI target ports training pattern if it detects the SEL, MSG, and I/O true and C/D false on the first assertion of the REQ signal. The SCSI initiator port shall transmit the following training pattern:

1) assert ACK signal within 200 ns of the first REQ assertion;
2) disable precompensation;
3) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
4) negate ACK signal;
5) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
6) set precompensation to negotiated state; and
7) assert and negate ACK signal at the negotiated transfer period for 400 ns (e.g., the equivalent of 64 transfer periods at fast-160).

At the completion of the training pattern the target continues asserting and negating the REQ signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12 ns transfer period at fast-160). When the target is ready to transfer data it shall reverse the phase of P1.

9.2.1.2 DATAOUT phase training pattern

The SPI-4 DATA OUT training pattern is depicted in Figure 22.

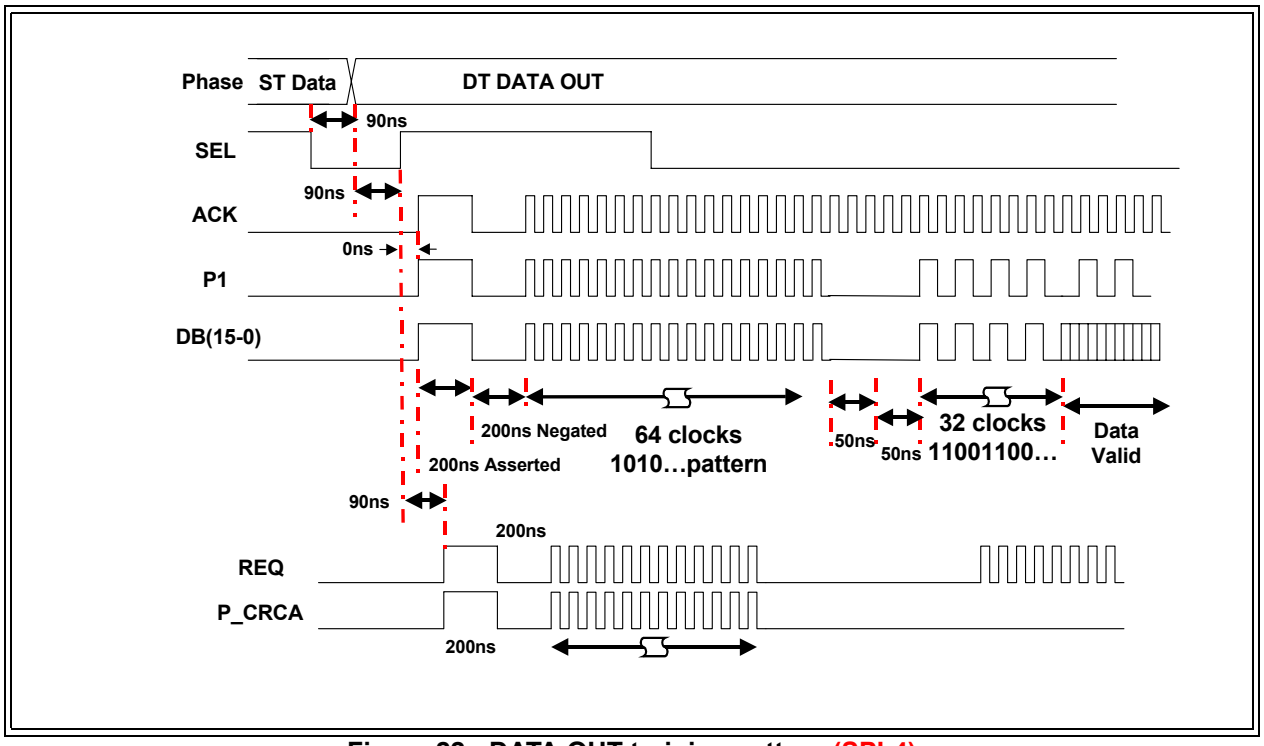


Figure 22 - DATA OUT training pattern (SPI-4)

The SCSI target port shall request a training pattern on a DT DATA OUT phase by asserting the SEL signal a minimum of two system deskew delays before asserting the REQ signal.

The SCSI target port shall begin its training pattern only after all the signal restrictions between information transfer phases listed in SPI-5 10.12 or the signal restrictions between a SELECTION phase and a DT DATA OUT phase listed in SPI-5 10.5.3 are met. The SCSI target port shall transmit the following training pattern:

1) if precompensation is enabled then set the drivers to the strong driver state;
2) simultaneously assert REQ and P_CRCA signals;
3) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
4) simultaneously negate REQ and P_CRCA signals;
5) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
6) set precompensation to negotiated state;
7) negate SEL signal;
8) simultaneously assert and negate REQ and P_CRCA signals for 400 ns (e.g., the equivalent of 64 transfer periods at fast-160);
9) negate REQ and P_CRCA for at least 100 ns (e.g., the equivalent of 16 transfer periods at fast-160); and
10) the SCSI target port shall begin asserting and negating REQ to indicate to the SCSI initiator port valid data may be sent. The number of REQ assertions shall not exceed the negotiated REQ/ACK offset.

The SCSI initiator port shall begin the section A of its training pattern independent of the start of the SCSI target ports training pattern if it detects the SEL and MSG true, and C/D and I/O false on the first assertion of the REQ signal. The SCSI initiator port shall transmit the training pattern described by section A, section B, and section C in this subclause:

For fast-320 the SCSI initiator port shall transmit the training pattern described by section A, section B, and section C in this subclause except that the polarity of DB(0, 1, 4, 5, 9, 10, 13, and 14) shall be inverted during transmission of section A, section B, and section C (i.e., where it is specified that these signals shall be asserted, they shall be negated, and where it is specified that these signals shall be negated, they shall be asserted). These signals shall return to their normal polarity after completion of training pattern transmission.

Start of section A:

1) if precompensation is enabled then set the drivers to the strong driver state;
2) simultaneously assert ACK, P1, and DB(15-0) signals within 200 ns of the first REQ assertion (e.g., the equivalent of 32 transfer periods at fast-160);
3) wait 200 ns (e.g., the equivalent of 32 transfer periods at fast-160);
4) simultaneously negate ACK, P1, and DB(15-0) signals;
5) wait 200 ns;
6) set precompensation to negotiated state;
7) simultaneously assert and negate ACK, P1, and DB(15-0) signals at the negotiated transfer period for 800 ns (e.g., the equivalent of 128 transfer periods at fast-160);

Start of section B:

1) wait the 1200 ns from the first assertion of ACK in step 2 of section A (e.g., equivalent of 192 transfer periods at fast-160);
2) keep the P1, and DB(15-0) signals negated while continuing to assert and negate ACK at the negotiated transfer period for 50 ns (e.g., the equivalent of 8 transfer periods at fast-160);
3) keep the P1, DB(15-0), and ACK signals negated for an additional 50 ns;
4) simultaneously assert and negate P1 and DB(15-0) signals at twice the negotiated transfer period (i.e., simultaneously repeat a 1100b bit pattern on each signal) while asserting and negating ACK 300 ns (e.g., the equivalent of 48 transfer periods at fast-160); and

Start of section C:

1) assert and negate ACK at the negotiated transfer period for 800 ns and at the same time assert and negate P1 at twice the negotiated transfer period while repeating a 0000010011111011b bit pattern on each of the DB(15-0) signals (e.g., the equivalent of 128 transfer periods at fast-160).

At the completion of its training pattern the SCSI initiator port continues asserting and negating the ACK signal at the negotiated transfer period (e.g., 6,25 ns transfer period at fast-160) and the P1 signal at twice the negotiated transfer period (e.g., 12,5 ns transfer period at fast-160). When the SCSI initiator port is ready to transfer data and the REQ/ACK offset value is not zero it shall reverse the phase of P1.

9.3 Data rates

Data transfer rates in SCSI are determined by the SCSI variant as listed in table 17. Specifically, single transition, double transition, width, specific protocol variant and adaptive filtering affect the data rate. Care shall be taken in simulation to ensure that the relationship between the analog signals and the application is understood.

Table 17 - Data rates and signal characteristics

SCSI variant	REQ/ACK maximum frequency	Data line maximum frequency	Minimum rise/fall time	Maximum launch amplitude
SCSI-1 SE	sync - NA	NA	NA	5,25V
SCSI-2 SE	5,0MHz	2,5MHz	NA	5,25V
SPI -1 SE	10,0MHz	5,0MHz	5,0ns	5,25V
Ultra SE	20,0MHz	10,0MHz	5,0ns	3,7V
Ultra2 LVD	20,0MHz	20,0MHz	1,0ns	2,2V DF_{pp}
Ultra160 LVD	40,0MHz	40,0MHz	1,0ns	2,2V DF_{pp}
Ultra320 LVD	80,0MHz	80,0MHz	1,0ns	2,2V DF_{pp}
Ultra640 LVD	160,0MHz	160,MHz	1,0ns	2,2V DF_{pp}

9.4 Instrumentation models

During simulation, care shall be used to include an instrumentation model when comparing measured data to simulation data. These models are the same as described in 6.5.

Annex A

Resources

(Informative)

A.1 Publications

The following is a list of publications that provide useful information, techniques, and processes for developing, simulating, and analyzing models.

Bissell & Chapman, *Digital Signal Transmission*, Cambridge University Press,1992

Buchanan, J., *Signal and Power Integrity in Digital Systems,* McGraw Hill, 1996

Chang, K. ed., *Microwave Passive & Antenna Components*, John Wiley & Sons, 1989

Dally & Poulton, *Digital Systems Engineering,* Cambridge University Press, 1998

Fast Logic Applications Handbook, National Semiconductor, 1990

Goel, A., *High-Speed VLSI Interconnections, Modeling, Analysis, and Simulation,* John Wiley & Sons, 1994

Gupta, K.C., et al, *Microstrip Lines and Slotlines,* Artech House, 1996

Johnson & Graham, *High-Speed Digital Design, A Handbook of Black Magic,* Prentice Hall, 1993

Karmel, Colef, & Camisa, *Introduction to Electromagnetic and Microwave Engineering,* John Wiley & Sons, 1998

Kraus & Fleisch, *Electromagnetics with Application,* McGraw-Hill, 1999

Kraus, J., *Electromagnetics,* McGraw Hill, 1992

Kronsowski & Helland, *Electronic Packaging of High Speed Circuitry,* McGraw Hill, 1997

Laverghetta, T., *Practical Microwaves,* Prentice Hall, 1996

Mardiguian, M., *Controlling Radiated Emissions by Design,* VNR, 1992

Matick, M., *Transmission Lines for Digital and Communications Networks,* IEEE Press, 1995

Medley, M., *Microwave and RF Circuits: Analysis, Synthesis and Design,* Artech House, 1993

Mongia, R., et al, *RF and Microwave Coupled-Line Circuits,* Artech House, 1999

Montrose, M., *EMC and the Printed Circuit Board, Design Theory and Layout Made Simple,* IEEE Press, 1999

Montrose, M., *Printed Circuit Board Design Techniques for EMC Compliance,* IEEE Press, 1996.

Ott, H., *Noise Reduction Techniques in Electronic Systems,* 2nd ed., John Wiley & Sons, 1988

Paul, C., *Analysis of Multiconductor Transmission Lines*, John Wiley & Sons, 1994

Paul, C., *Introduction to Electromagnetic Compatibility*, John Wiley & Sons, 1992

Peters, S., *I/O Buffer Modeling Cookbook*, IBIS Open Forum

Pozar, D., *Microwave Engineering,* 2nd ed., John Wiley & Sons, 1998

Ramo, Whinnery, & Van Duzer, *Fields and Waves in Communication Electronics,* 3rd ed., John Wiley & Sons, 1994

Ritchey, L. & Blankenhorn, J., *High Speed PCB Design,* SMT Plus & Ritchtek, 1996

Rizzi, P., *Microwave Engineering, Passive Circuits,* Prentice Hall, 1998

Rosenstark, S., *Transmission Lines in Computer Engineering,* McGraw Hill, 1994

Sevick, J., *Transmission Line Transformers,* Nobel Publishing, 1996

Wadell, B., *Transmission Line Design Handbook,* Artech House, 1991

Walker, C., *Capacitance, Inductance and Crosstalk Analysis,* Artech House, 1990

Williams, T., *EMC for Product Designers,* Butterworth-Heinemann, 1996.

A.2 Tools

There are a number of software tools that are useful in developing and using models. These are simulation tools and parameter extraction tools, and model creation tools. Simulation tools may be further broken down into SPICE tools, behavioral tools and structural simulator tools. The tool shall support IBIS models for the active components and RLGC models for the cables and connectors. These tools are listed below. The usage of these tools is explained in more detail in 5. All the below are example products, equivalent products exist. Within this document, whenever the below products are mentioned equivalent products may be used.

A.2.1 Simulation tools

SPICE
- Apsim Spice
- Berkeley SPICE
- HSPICE
- PSPICE

Behavioral
- HDL
- Hyperlynx
- Verilog
- VHDL
- Viewlogic XTK

High frequency structural simulator
- Ansoft HFSS
- HP-ADS (advanced design simulator)

A.2.2 Extraction tools

Maxwell
Maxwell-2D
Maxwell-3D
Pacific Numerix

A.2.3 Model creation tools

Mentor Graphics
Cadence
HP Suite

Annex B

N-Port Networks

(Informative)

B.1 Overview

The relationship between the voltages and currents at the various points in a transmission network can be described through the use of impedance and admittance matrices. These transmission networks can be defined as N-port networks where a port is a "two terminal pair".

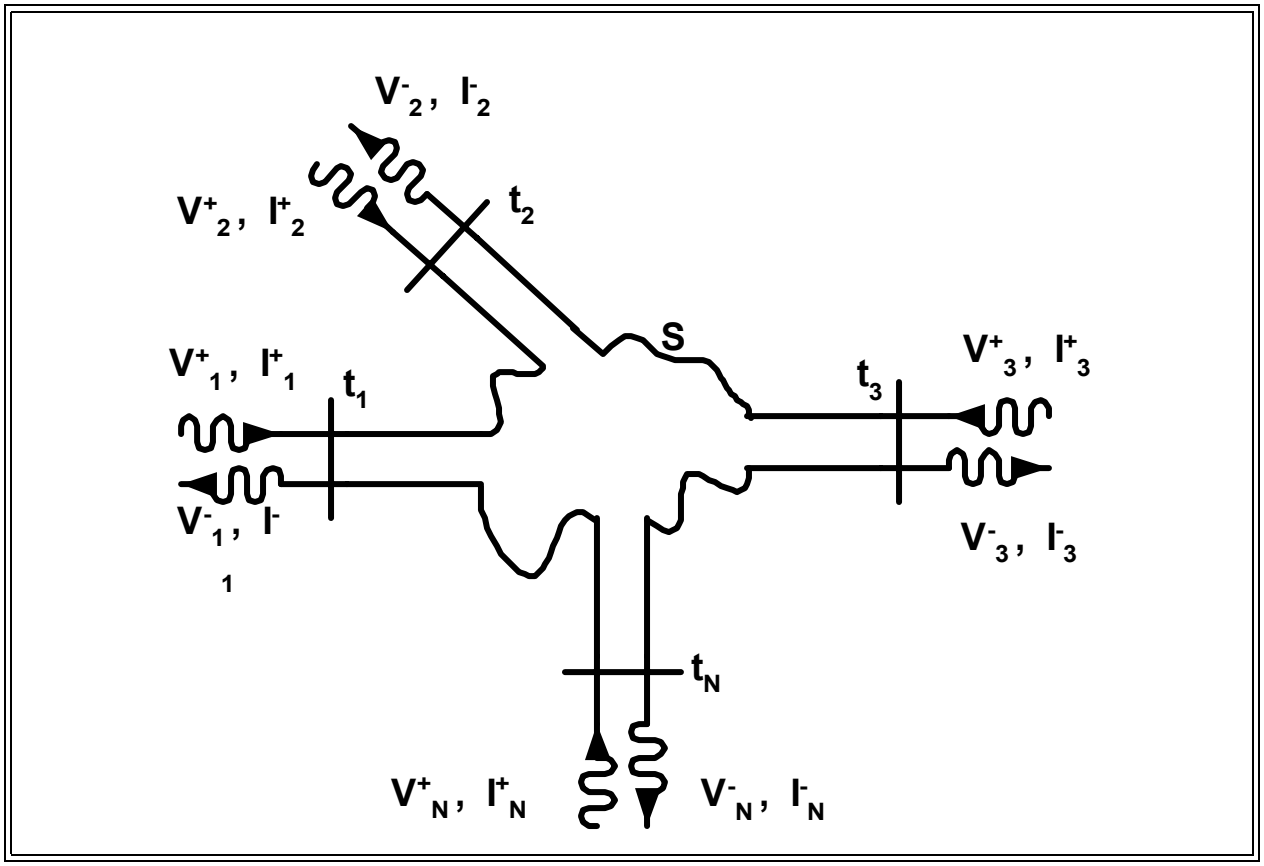


Figure B.1 - Arbitrary N-port network

The ports in Figure B.1 may be any transmission line or equivalent propagating a single mode. Multiple propagation modes need not be considered in the SCSI environment, since multiple propagation modes are only supported in waveguides. A terminal plane, t_N, is defined along with the incident and reflected wave's equivalent voltages and currents. The total voltage and current at the *n*th terminal plane is described in Equation B.1 when z=0.

$$V_n = V_n^+ + V_n^-$$

$$I_n = I_n^+ + I_n^-$$

Equation B.1 - N-port voltage and current

These voltages and currents are then related through an impedance [Z] matrix and admittance [Y] matrix, for the N-port network, Equation B.2 and Equation B.3 respectively.

$$\begin{bmatrix} V_1 \\ V_2 \\ Æ \\ V_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \dots & Z_{1N} \\ Z_{21} & & & Æ \\ Æ & & & Æ \\ Z_{N1} & \dots & \dots & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ Æ \\ I_N \end{bmatrix}$$

Equation B.2 - N-port impedance matrix

$$\begin{bmatrix} I_1 \\ I_2 \\ Æ \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & \dots & Y_{1N} \\ Y_{21} & & & Æ \\ Æ & & & Æ \\ Y_{N1} & \dots & \dots & Y_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ Æ \\ V_N \end{bmatrix}$$

Equation B.3 - N-port admittance matrix

In general the impedance and admittance matrices are symmetric. For example $Z_{ij} = Z_{ji}$.

In general it is difficult to define voltages and currents for non-TEM (non-tranverser electro-magnetic) modes of propagation. Fortunately SCSI interconnects presently only support TEM and quasi-TEM modes of propagation. A practical problem exists when trying to measure voltages and currents at high frequencies because of the relationships between magnitude and phase of the signal. The scattering matrix [S] solves this problem. The scattering parameters relate the incident and reflected voltage waves at the ports and does not unnecessarily need be symmetric, Equation B.4.

When the scattering parameters are measured or calculated, the incident wave to all ports except the ones in question shall be terminated in matched loads to avoid reflections. For example when determining S_{ii}, the reflection coefficient, all other ports except for $Port_{ii}$ are terminated in matched loads. When determining the transmission coefficient from $Port_i$ to $Port_j$ all ports except for $Port_i$ and $Port_j$ are terminated in matched loads.

The scattering parameters can be directly obtained with a vector network analyzer. Other N-port matrix parameters are easily obtained through conversion.

An n-port network can be characterized by Y, Z, and S parameters, but in general most networks consist of

$$\begin{bmatrix} I_1^- \\ I_2^- \\ Æ \\ I_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & & & Æ \\ Æ & & & Æ \\ S_{N1} & \dots & \dots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ Æ \\ V_N^+ \end{bmatrix}$$

Equation B.4 - N-port scattering matrix

a cascade of two-port networks. The one main exception being when a stub attaches to the bus. These are usually defined in terms of a transmission or *ABCD* matrix, Equation B.5. A series of cascaded two-port networks results in an *ABCD* matrix whose terms are found by multiplying the underlying matrices together.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

Equation B.5 - 2-port transmission matrix

B.2 2-Port network parameter conversions

	S	Y	Z	$ABCD$
S_{11}	S_{11}	$\frac{(Y_0 \angle Y_{11})(Y_0 + Y_{11}) + Y_{12}Y_{21}}{\Delta Y}$	$\frac{(Z_{11} \angle Z_0)(Z_{22} + Z_0) \angle Z_{12}Z_{21}}{\Delta Z}$	$\frac{A + B/Z_0 \angle CZ_0 \angle D}{A + B/Z_0 + CZ_0 + D}$
S_{12}	S_{12}	$\frac{\angle 2Y_{12}Y_0}{\Delta Y}$	$\frac{2Z_{12}Z_0}{\Delta Z}$	$\frac{2(AD \angle BC)}{A + B/Z_0 + CZ_0 + D}$
S_{21}	S_{21}	$\frac{\angle 2Y_{21}Y_0}{\Delta Y}$	$\frac{2Z_{21}Z_0}{\Delta Z}$	$\frac{2}{A + B/Z_0 + CZ_0 + D}$
S_{22}	S_{22}	$\frac{(Y_0 + Y_{11})(Y_0 \angle Y_{22}) + Y_{12}Y_{21}}{\Delta Y}$	$\frac{(Z_{11} + Z_0)(Z_{22} \angle Z_0) \angle Z_{12}Z_{21}}{\Delta Z}$	$\frac{\angle A + B/Z_0 \angle CZ_0 + D}{A + B/Z_0 + CZ_0 + D}$
Y_{11}	$Y_0\frac{(1 \angle S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) \angle S_{12}S_{21}}$	Y_{11}	$\frac{Z_{22}}{\lvert Z\rvert}$	$\frac{D}{B}$
Y_{12}	$Y_0\frac{\angle 2S_{12}}{(1 + S_{11})(1 + S_{22}) \angle S_{12}S_{21}}$	Y_{12}	$\frac{\angle Z_{12}}{\lvert Z\rvert}$	$\frac{BC \angle AD}{B}$
Y_{21}	$Y_0\frac{\angle 2S_{21}}{(1 + S_{11})(1 + S_{22}) \angle S_{12}S_{21}}$	Y_{21}	$\frac{\angle Z_{21}}{\lvert Z\rvert}$	$\frac{\angle 1}{B}$
Y_{22}	$Y_0\frac{(1 + S_{11})(1 \angle S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) \angle S_{12}S_{21}}$	Y_{22}	$\frac{Z_{11}}{\lvert Z\rvert}$	$\frac{A}{B}$
Z_{11}	$Z_0\frac{(1 + S_{11})(1 \angle S_{22}) + S_{12}S_{21}}{(1 \angle S_{11})(1 \angle S_{22}) \angle S_{12}S_{21}}$	$\frac{Y_{22}}{\lvert Y\rvert}$	Z_{11}	$\frac{A}{C}$
Z_{12}	$Z_0\frac{2S_{12}}{(1 \angle S_{11})(1 \angle S_{22}) \angle S_{12}S_{21}}$	$\frac{\angle Y_{12}}{\lvert Y\rvert}$	Z_{12}	$\frac{AD \angle BC}{C}$
Z_{21}	$Z_0\frac{2S_{21}}{(1 \angle S_{11})(1 \angle S_{22}) \angle S_{12}S_{21}}$	$\frac{\angle Y_{21}}{\lvert Y\rvert}$	Z_{21}	$\frac{1}{C}$
Z_{22}	$Z_0\frac{(1 \angle S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 \angle S_{11})(1 \angle S_{22}) \angle S_{12}S_{21}}$	$\frac{Y_{11}}{\lvert Y\rvert}$	Z_{22}	$\frac{D}{C}$
A	$\frac{(1 + S_{11})(1 \angle S_{22}) + S_{12}S_{21}}{2S_{21}}$	$\frac{\angle Y_{22}}{Y_{21}}$	$\frac{Z_{11}}{Z_{21}}$	A
B	$Z_0\frac{(1 + S_{11})(1 + S_{22}) \angle S_{12}S_{21}}{2S_{21}}$	$\frac{\angle 1}{Y_{21}}$	$\frac{\lvert Z\rvert}{Z_{21}}$	B
C	$\frac{(1 \angle S_{11})(1 \angle S_{22}) \angle S_{12}S_{21}}{2Z_0S_{21}}$	$\frac{\angle \lvert Y\rvert}{Y_{21}}$	$\frac{1}{Z_{21}}$	C
D	$\frac{(1 \angle S_{11})(1 + S_{22}) \angle S_{12}S_{21}}{2S_{21}}$	$\frac{\angle Y_{11}}{Y_{21}}$	$\frac{Z_{22}}{Z_{21}}$	D
$Y_0 = 1/Z_0$	$\Delta Y = (Y_{11} + Y_0)(Y_{22} + Y_0) \angle Y_{12}Y_{21}$	$\lvert Y\rvert = Y_{11}Y_{22} \angle Y_{12}Y_{21}$	$\Delta Z = (Z_{11} + Z_0)(Z_{22} + Z_0) \angle Z_{12}Z_{21}$	$\lvert Z\rvert = Z_{11}Z_{22} \angle Z_{12}Z_{21}$