# Symphony SoundBite

## Reference Manual

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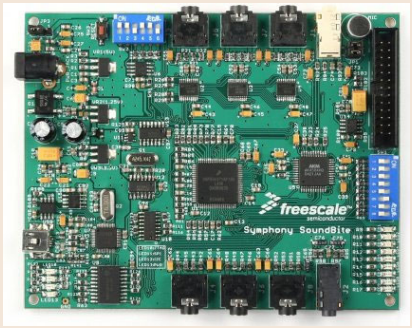
**Contents**





# 1 Introduction

The Symphony SoundBite is a versatile audio application development board built upon the DSPB56371 Digital Signal Processor. The Symphony SoundBite costs very little and is ideal for cost-sensitive organizations, like university digital signal processing labs, small engineering companies, and even the frugal hobbyist.

Capable of simultaneously processing 8 independent or 4 stereo pairs of audio input and output, the Symphony SoundBite has 4 stereo input and output jacks to connect to line-level analog audio. One pair of input and output jacks is shared with an optical S/PDIF receiver and transmitter, enabling direct digital audio input and output (mini TOS-link). Four 24-bit stereo codecs handle analog conversion at sampling rates up to 192 kHz. You can also interact with application code running on the DSP, using DIP switches and multi-colored LEDs (connected to GPIO pins).


**Figure 1. Symphony SoundBite Audio Demo Board**

The board includes an integral, multi-mode communication and debugging interface that enables low level JTAG debugging, in addition to high-level serial communications with the DSP via SPI or $I^2C$.

Features:

- Main Processor: 24-bit DSPB56371 Digital Signal Processor
  - — up to 180 million instructions per second (MIPS) at 180 MHz core clock
  - — 1.25 V core supply with 3.3 V peripheral I/O supply
  - — Dual-Harvard architecture core (two data memory spaces in addition to program space)
  - — On-chip memories:
    - – 4–44K x 24-bit words of PRAM
    - – 28–36K x 24-bit words of XRAM
    - – 16–48K x 24-bit words of YRAM
    - – User-configurable memory partitions
  - — Two Enhanced Serial Audio Interfaces (ESAIs) provide up to 8 channels of digital audio input and output
  - — Serial Host Interface (SHI) provides interface for high level serial communication
  - — Triple timer module
  - — Serial $I^2C$ boot EEPROM allows for fully stand-alone operation of Symphony SoundBite

- Audio Subsystem:
  - Three AK4556 24-bit 192 kHz stereo codecs connected to 3 sets of line-level 3.5 mm stereo jacks
  - AK4584 24-bit 192 kHz stereo codec with integrated S/PDIF transceiver
    - Provides master clock for all codecs, synchronizing all digital audio signals
    - One set of line-level 3.5mm stereo jacks shared with optical S/PDIF receiver and transmitter
  - On-board microphone and pre-amplifier
- General Purpose I/O
  - 8-position DIP switch provided for user inputs to DSP application software
  - 9 LEDs in red, yellow and green provide visual indication
  - Student Learning Kit (SLK) header provides compatibility with the University Relations Project Board
- Debugging and Communication Interface
  - On-board FT2232 dual USB UART provides for low-level JTAG/OnCE and high-level Symphony Debugger Interface debuggers
  - Operational mode of integrated debugger hardware is controlled by host PC application software
  - LEDs indicate the operational mode of the debugging interface
  - Push-button system reset switch
  - DSP boot mode configuration DIP switch
- Power Supply
  - 2.1 mm barrel jack allows for the use of an external 6–9 V AC/DC power supply (recommended configuration)
  - Capable of being powered exclusively from the USB of the host computer (Powering by USB power alone limits the analog performance capabilities of AK4584 codec)
  - Capable of being powered via SLK header
  - Power supply selected by a single jumper and indicated by an LED

# 2 Functional Blocks

The Symphony SoundBite development board consists of 4 functional blocks:

- Analog Audio Conversion
- Digital Signal Processor (DSP)
- Debug/Communication Interface
- Power Supply

See Figure 2.

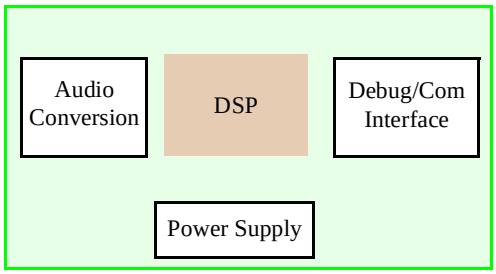



**Figure 2. Symphony SoundBite Major Functional Blocks**

**Digital Signal Processor:**
A DSPB56371 device (U1) comprises the bulk of the DSP functional block and sits at the heart of the Symphony SoundBite development board. Positions 1 through 4 of SW2 are connected to the MOD pins of the DSP and set the boot mode. An $I^2C$ serial EEPROM (U6), connected to the DSP through positions 5 and 6 of SW2, provides non-volatile data storage and allows the Symphony SoundBite to boot up and run application software in a stand-alone configuration (without a PC connected to download code). Audio data in $I^2S$ format is transmitted through the DSP's ESAI port and received via the DSP's ESAI_1 port. The balance of the DSP pins are connected to an expansion header (CON1), as well as to an 8-position DIP switch and to 9 LEDs for general purpose use.

The sytem clock is provided by two gates of U12 and a 24.576 MHz crystal. Power-on reset and manual reset of the DSP and codecs is controlled by the reset manager (U11, U13) and the reset switch (SW3).

**Audio Conversion:**
The Audio Conversion functional block consists of three AK4556 devices (U2, U3, and U4) and one AK4584 (U5) 24-bit codec. Digital audio data is transmitted and received in $I^2S$ format. The AK4584 generates the master left/right and bit clocks for all the codecs and the DSP's ESAI ports. Four stereo pairs (or 8 mono channels) of analog audio input and output are provided at jacks J1–J8.

Digital audio input/output in optical S/PDIF format is supported by combination analog/digital jacks (J1, J2) and an integrated digital audio receiver/transmitter in the AK4584 device. A built-in microphone is connected to a fixed gain preamplifier (U14) which in turn is connected through jumper JP1 to the analog inputs at jack J1. The microphone gain can be adjusted further through the internal amplifier within the AK4584. The AK4584 is configured by the DSP over serial control lines connected to dedicated GPIO pins on the DSP.

**Debug/Communication Interface:**
Debugging and communication between a host computer's USB port and the DSP is implemented using the FT2232 multi-mode USB device (U7). Three modes of communication are permitted between the host computer and the DSP: $I^2C$, SPI and JTAG/OnCE. The communication mode is selected by software on the host PC via the GPIO pins on the FT2232 device, which route the signal lines to the appropriate peripheral on the DSP via buffer U9 (SPI and JTAG/OnCE) and analog switch U10 (I2C).

JTAG/OnCE is used for low-level debugging of the DSP. The SHI port on the DSP can be used for high-level communication between the DSP and host PC using $I^2C$ or SPI protocol. The USB identity of the FT2232 is provided by the serial EEPROM (U8). LED10, LED11, and LED12 indicate which protocol is in use by the PC host application software.

**Power Supply:**
The Power Supply allows the Symphony SoundBite board to operate from an external power supply or directly from a host computer's USB port. Note that when the Symphony SoundBite is powered only from the USB port, AK4584 performance may not meet its data sheet specifications. For that reason, powering the Symphony SoundBite board with an external supply is recommended and preferred.

Jumper JP3 selects the source for the board's power supply: external power via jack PWR_JACK (short pins 1-2), power from the host computer's USB port (short pins 2-3). Alternately, if no pins of JP3 are shorted, the Symphony SoundBite can be supplied with regulated 5V via pin 1 of the expansion connector CON1.

**CAUTION**

If you power the board using the CON1 connector, JP3 must have no jumpers in place, or the Symphony SoundBite board will get damaged.

The external supply can be 6–9 VAC or 9–12 VDC with a current capacity of at least 400 mA. When USB powering is selected, the Symphony SoundBite board remains unpowered until the FT2232 is enumerated with the PC host. When this occurs, the FT2232 (U7) PWREN# signal is asserted low, applying 5V from the USB port through the the current limiting switch TPS2021 (U15) to the 3.3V and 1.25V regulators. LED13 is lighted when the Symphony SoundBite development board has powered up successfully.

Figure 3 shows a more detailed diagram of the off-board and interconnections between the various functional blocks on the board.

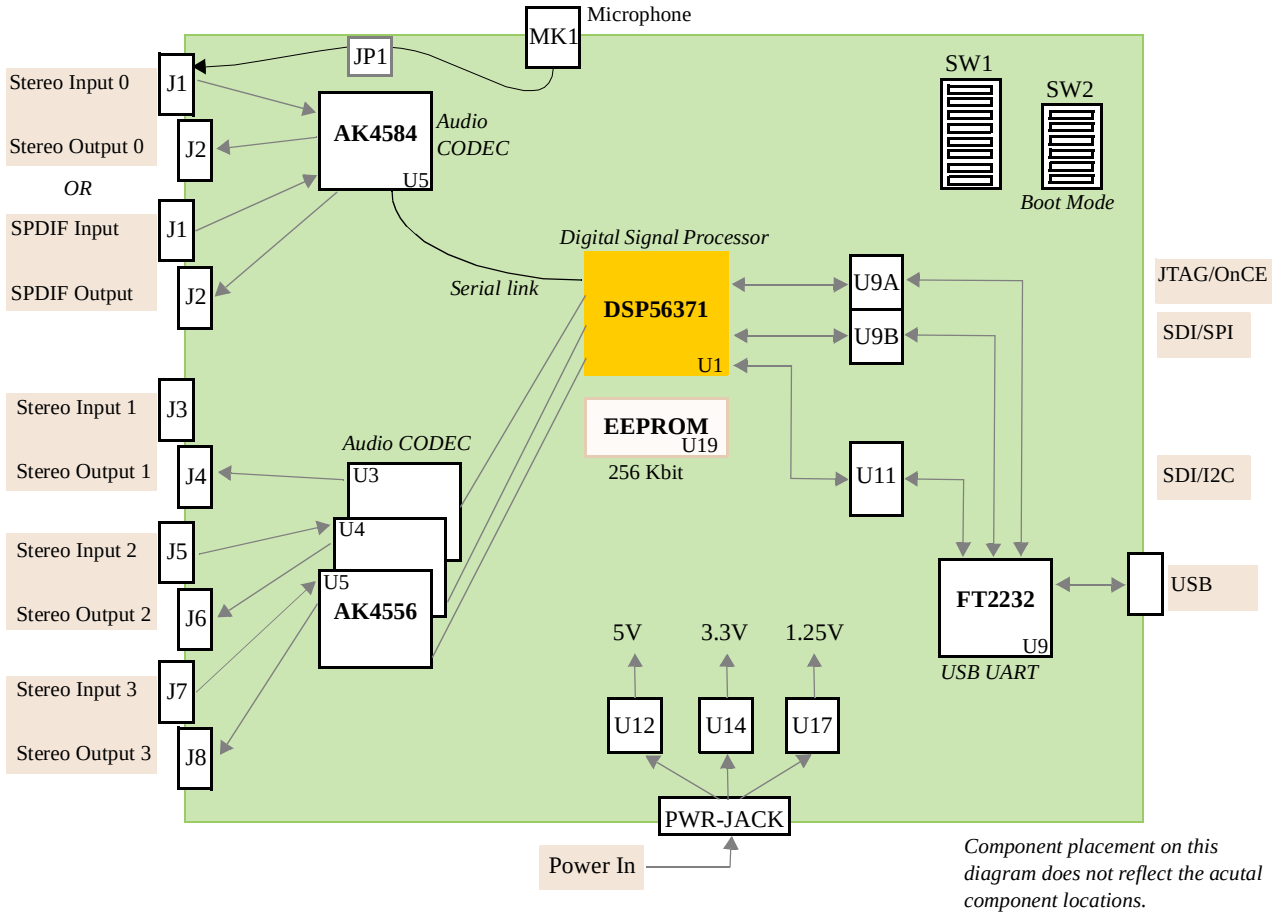



**Figure 3. Symphony SoundBite Board-Block Diagram**

# 3 Configuration and Connections

Configuring a Symphony SoundBite board is easy, because most configuration is done via software.

## 3.1 Select Power Source

**NOTE**

Powering the Symphony SoundBite from a USB port alone may degrade audio performance because:
(1) The supply voltage at the AK4584 may be under the specified minimum limit of 4.75V due to voltage drops in the USB cabling and in the power supply section of the Symphony SoundBite board.
(2) Noise from the USB port may be transmitted through the AK4584 device because there is no regulator in the power supply line to isolate and filter the noise.

The power source for the Symphony SoundBite board is selected using the JP3 jumper. See Table 1.

**Table 1. JP3 Jumper Selects Power Source**

| Jumper | |
|---|---|
| 1-2 | Selects external power, supplied through PWR_JACK. The polarity at PWR_JACK is unimportant due to the presence of the bridge rectifier G1. The external power supply should be in the range of 6–8 VAC or 8–10 VDC. |
| 2-3 | Selects USB power. When USB power is selected, the power indicator LED13 will not illuminate until the board enumerates with the host PC. |

## 3.2 System Reset

The Symphony SoundBite board can also be reset manually using the pushbutton switch SW3, which resets the DSP and all of the codecs.

## 3.3 Select Boot Mode

Select the boot mode of the DSP (and enable the $I^2C$ EEPROM) using the six-position DIP switch SW2. SW2 positions 4:1 correspond to pins MOD[D:A]. For the MOD pin switches (positions 4 through 1 only), the switch state is the *inverse* of the logic state presented to the pin, so that in the ON position, a logic low is presented to the corresponding pin. Table 2 shows the allowed boot modes for the DSP56371 device. In the table, for any SW2 position, “0” means OFF and “1” means ON.

**Table 2. SW2 Selects Boot Mode**

| Boot Mode | MOD[D:A] | SW2 [4:1] | |
|---|---|---|---|
| 2 | 0010 | 1101 | Jump to PROM starting address (Slave SPI mode) |
| 5 | 0101 | 1010 | Bootstrap from SHI (Slave SPI mode) |
| 6 | 0110 | 1001 | Bootstrap from SHI (Slave $I^2C$ mode) (HCKFR=1, 100 ns filter enabled) |
| 7 | 0111 | 1000 | Bootstrap from SHI (slave $I^2C$ mode) (HCKFR=0) |
| 9 | 1001 | 0110 | Bootstrap from SHI (Serial $I^2C$ EEPROM mode) (HCKFR=1, 100 ns filter enabled) |
| B | 1011 | 0100 | Bootstrap from SHI (Serial SPI EEPROM mode) |

**Table 2. SW2 Selects Boot Mode (continued)**

| Boot Mode | MOD[D:A] | SW2 [4:1] | |
|---|---|---|---|
| C | 1100 | 0011 | Bootstrap from GPIO (Serial SPI EEPROM mode) |
| D | 1101 | 0010 | Jump to PROM at default HLX (Slave SPI) |
| E | 1110 | 0001 | Jump to PROM starting address (Slave $I^2C$) (HCKFR=0) |
| F | 1111 | 0000 | Jump to PROM starting address (Slave $I^2C$) (HCKFR=1, 100 ns filter enabled) |

SW2 positions 6:5 enable the $I^2C$ serial EEPROM, allowing the Symphony SoundBite board to operate without a host PC (*If* the EEPROM has been appropriately programmed with valid DSP application data and SW2 switches 4:1 are set for boot mode 9). SW2 switches 6:5 connect or disconnect the SDA and SCL lines of the U6 device to the DSP. Switches 6:5 should always be in the *same state*, either both ON (enabling U6) or OFF (disabling U6).

**NOTE**

When the on-board communication interface is used in SPI mode, switches 6:5 of SW2 must be OFF. Also, when running applications that use SPI or $I^2C$ protocols on a host PC and the DSP, give careful consideration to all of the SW2 switches to avoid contention.

The default state for SW2 is 110110 (SW2 positions 6:1), which sets Boot Mode 9 and enables the $I^2C$ EEPROM (allowing stand-alone operations). As shipped from Freescale, the $I^2C$ EEPROM contains the Symphony SoundBite demonstration application program, which is documented separately in the Symphony SoundBite documentation.

## 3.4 Audio Input/Output Jacks: J1–J8

Jacks J1, J3, J5, and J7 accept line-level analog inputs and jacks J2, J4, J6, and J8 provide line-level outputs.

The analog and optical inputs and outputs of J1 and J2 are always enabled in hardware. Jack J1 can also accept optical digital audio input using an optical cable with mini-TOS-LINK termination. Optical digital audio output can be obtained through jack J2 using an optical cable with mini-TOS-LINK termination.

There is no automatic hardware detection of the input source type; all detection and source selection is done using application software in the DSP to program the appropriate registers of the AK4584 codec (U5). For more information about the setup and programming of the AK4584 codec (U5), see the associated materials in the Symphony SoundBite documentation.

The output of the onboard microphone preamplifier is connected to the input of U5 via jumper block JP1. See Table 3. The default state of JP1 is 1-2 and 3-4 both jumpered, enabling microphone audio input.

**Table 3. JP1 Jumper Selects Left/Right Input Channel**

| Jumper | |
|---|---|
| 1-2 | Connects the microphone output to the left input channel of U5. |
| 3-4 | Connects the microphone output to the right input channel of U5. |

**NOTE**

If you use the J1 jack for analog audio input, no jumpers should be present on JP1, or the input source and the microphone preamplifier output will contend with each other.

## 3.5 General Purpose Switches: SW1

DIP switches (SW1) are provided for general purpose use *by the application code running in the DSP.* The GPIO pins connected to SW1 should normally be configured to be GPIO inputs.

- In the ON state, the corresponding DSP GPIO line is pulled high and a logic high is presented to the input.
- In the OFF state, the internal pulldown resistor presents a logic low to the input.

## 3.6 General Purpose LEDs: LED1–9

Nine LEDs are provided for general purpose use by DSP application code. The GPIO pins connected to the LEDs should normally be configured as GPIO outputs.

- A logic high output on one of these GPIO pins turns ON the corresponding LED
- A logic low output on one of these GPIO pins turns OFF the corresponding LED.

Table 4 shows the schematic signal name and DSP GPIO pin that corresponds to each LED identifier.

**Table 4. General Purpose LEDs**

| LED | Color | Schematic | DSP Pin |
|---|---|---|---|
| D1 | Green | GPLED0 | PF7 |
| D2 | Green | GPLED1 | PF8 |
| D3 | Green | GPLED2 | PF9 |
| D4 | Green | GPLED3 | PF10 |
| D5 | Amber | GPLED4 | TIO0/PB0 |
| D6 | Amber | GPLED5 | TIO1/PB1 |
| D7 | Red | GPLED6 | PC2 |
| D8 | Red | GPLED7 | PC5 |
| D9 | Red | GPLED8 | PC6 |

## 3.7 Status LEDs: LED10–13

Four LEDs display the status of the board: D10–D12, D13.

**Table 5. Status LEDs**

| LED | Color | Description | |
|---|---|---|---|
| D10 | Amber | JTAG/OnCE | D10–D12 display the communication protocol in use by the host PC. |
| D11 | Amber | SDI/SPI | |
| D12 | Amber | SDI/I2C | |
| D13 | Green | Power Indicator | D13 indicates when power is applied to the DSP and Analog Conversion functional blocks of the Symphony SoundBite. |

## 3.8 Expansion Header: CON1

An expansion header (CON1) is provided to enable off-board expansion. The 5V and 3.3V power supplies and several grounds are present on the CON1 header, as well as all GPSWx and GPLEDx lines.

Although the GPSWx lines are normally GPIO *inputs*, the GPSWx lines can be used as either inputs or outputs at the CON1 header.

**NOTE**

When the GPSWx lines are used as an output, if the corresponding switch position of SW1 is ON, the pull-up resistor is enabled, presenting an additional load to the DSP GPIO pin when in the logic low state, which must be accounted for.

Although the GPLEDx lines are normally GPIO *outputs*, the GPLEDx lines can be used as either inputs or outputs at the CON1 header.

**NOTE**

When the GPLEDx lines are used as inputs, the external signal must be able to handle the load that the presence of the LED and current limiting resistor present to it. There are no provisions for disconnecting the LEDs from the GPLEDx lines.

Additionally, you can modify the Symphony SoundBite board by soldering jumpers between the 4 solder pads at CON1 to any of the 4 IRQ lines, IRQD:A, the $I^2C$ lines SDA and SCL, and GPIO pin PC7, as desired.

## 3.9 Connectors and Switches

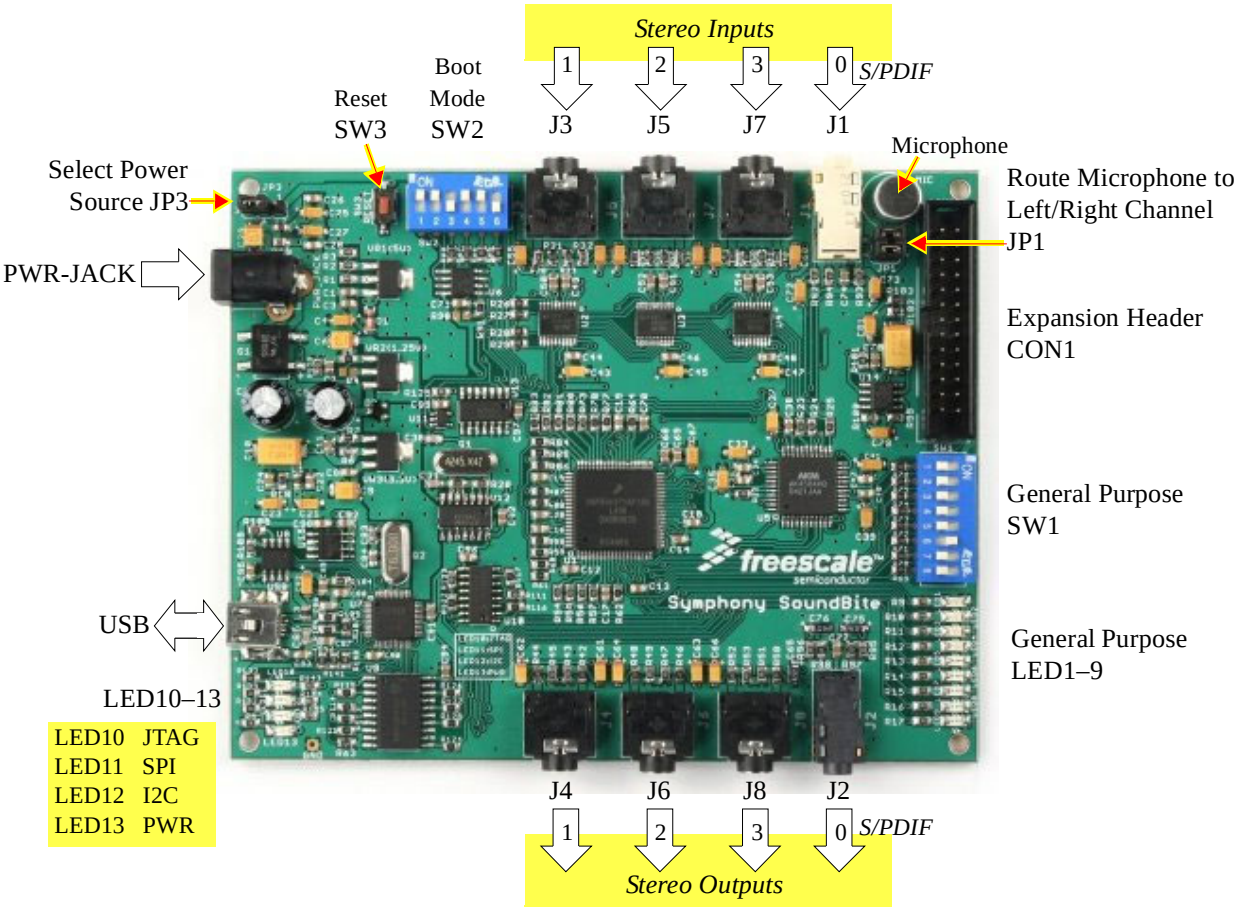



**Figure 4. Connectors, Switches, Headers**

**Table 6. Connectors, Switches, Jumpers**

| Connector | Function | |
|---|---|---|
| **J1** | Stereo Input 0 | Combination analog/digital optical.<br>The microphone preamplifier output is connected to both channels of J1 through jumper JP1. |
| **J2** | Stereo Output 0 | |
| **J3** | Stereo Input 1 | Analog only. |
| **J4** | Stereo Output 1 | |
| **J5** | Stereo Input 2 | Analog only. |
| **J6** | Stereo Output 2 | |
| **J7** | Stereo Input 3 | Analog only. |
| **J8** | Stereo Output 3 | Analog only. |

**Table 6. Connectors, Switches, Jumpers (continued)**

| Connector | Function | |
|---|---|---|
| CON1 | Expansion header | Do not populate with jumpers. |
| PWR_JACK | Power In | Coax jack, 2.1 x 5.5 mm |
| USB | USB | Mini-B USB jack |

| Switch | | |
|---|---|---|
| SW1 | Programmable | General purpose switches (8x), can be programmed by DSP applications. |
| SW2 | Mode Select | DSP boot mode select and EEPROM enable |
| SW3 | Board Reset | Momentary switch, resets the Symphony SoundBite board. |

| Jumper | | |
|---|---|---|
| JP1 | Microphone Select | Route Microphone output to Left or Right Channel |
| JP3 | Power Source Select | 3 pins.<br>• 1–2 jumper: Select external power supply.<br>• 2–3 jumper: Select USB (default).<br>• No jumpers: Select power through CON1. |

**Table 7. CON1 Expansion Header**

| Pin | | Pin | |
|---|---|---|---|
| 1 | +5V | 2 | +3.3V |
| 3 | GND | 4 | PAD1 |
| 5 | PAD2 | 6 | PAD3 |
| 7 | PAD4 | 8 | GPLED8 |
| 9 | GPLED0 | 10 | GPLED7 |
| 11 | GPLED1 | 12 | GPLED6 |
| 13 | GPLED2 | 14 | GPLED5 |
| 15 | GPLED3 | 16 | GPLED4 |
| 17 | GPSW0 | 18 | GPSW7 |
| 19 | GPSW1 | 20 | GPSW6 |
| 21 | GPSW2 | 22 | GPSW5 |
| 23 | GPSW3 | 24 | GPSW4 |
| 25 | GND | 26 | GND |

# 4 Additional Info

For additional information, please refer to the Symphony SoundBite Documentation Overview document, which provides an overview of all the documentation relevant to the programming and usage of the Symphony SoundBite audio development board.