



# **VIA Antaur Processor**

## **Datasheet**

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**VIA TECHNOLOGIES, INC.**

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## SECTION

## 1

## INTRODUCTION

The VIA Antaur processor is based on a unique internal architecture and is manufactured using an advanced 0.13 $\mu$  CMOS technology. This architecture and process technology provides a highly compatible, high-performance, low-cost, and low-power solution for the desktop PC, notebook, and Internet Appliance markets. The VIA Antaur processor is available in several GHz versions.

When considered individually, the compatibility, function, performance, cost, and power dissipation of the VIA Antaur processor family are all very competitive. When considered as a whole, the VIA Antaur processor family offers a breakthrough level of *value*.

## 1.1 DATASHEET OUTLINE

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The intent of this datasheet is to make it easy for a direct user—a board designer, a system designer, or a BIOS developer—to use the VIA Antaur processor.

**Section 1** of the datasheet summarizes the key features of the VIA Antaur processor. **Section 2** specifies the primary programming interface. **Section 3** does the same for the bus interface. **Sections 4, 5, and 6** specify the classical datasheet topics of AC timings, pinouts, and mechanical specifications.

Appendix A documents the VIA Antaur processor machine specific registers (MSRs).

## 1.2 BASIC FEATURES

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The VIA Antaur processor family currently consists of one basic model with several different GHz versions. The VIA Antaur processor is designed for low power, so it is ideally suited for both desktop and mobile applications. All versions share the following common features:

- Software-compatible with thousands of x86 software applications available
- MMX-compatible instructions
- SSE-compatible instructions
- Two large (64-KB each, 4-way) on-chip caches
- 64-KB Level 2 victim cache (16-way)
- Two large TLBs (128 entries each, 8-way) with two page directory caches
- Branch Target Address Cache with 1k entries each identifying 2 branches
- Unique and sophisticated branch prediction mechanisms
- Bus speeds up to 133 MHz
- Extremely low power dissipation
- Very small die (52 mm<sup>2</sup> in TSMC 0.13μ technology)



## 1.3 PROCESSOR VERSIONS

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Typically, there are five specification parameters that characterize different versions of a processor family: package, voltage, maximum case temperature, external bus speed, and internal MHz.

The VIA Antaur processor family is offered in enhanced BGA (EBGA) package. The current nominal voltage is 1.25V.

The internal MHz of a particular VIA Antaur processor chip is defined by two parameters: the specified external bus speed and the internal bus-clock multiplier. VIA Antaur processors operate the bus at 133 MHz bus. Bus frequency select pins (BSEL 0 and BSEL 1) identify the appropriate bus speed.

The bus-clock multiplier is hardwired into each VIA Antaur processor chip. That is, the ratio of the internal processor clock speed to the externally supplied bus clock is frozen for a particular chip<sup>1</sup>. Several different clock-multiplier versions are currently offered.

More information on these topics, please refer to Sections 4, 5, and 6 in this datasheet.

- The VIA Antaur processor is initially available in a variety of speed grades:
  - 1.00 GHz (7.5 x 133-MHz bus)
  - 1.13 GHz (8.5 x 133-MHz bus)
  - 1.20 GHz (9.0 x 133-MHz bus)
- Future versions of the VIA Antaur processor may provide other speed grades and bus speed combinations.
- Future versions of the VIA Antaur processor may have different voltages

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<sup>1</sup> Actually, it is semi-frozen. A VIA-unique machine specific register allows programming to temporarily change the hard-wired multiplier. This capability, documented in Appendix A, is intended for special BIOS situations and test and debug usage.

## 1.4 COMPATIBILITY

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A VIA Antaur processor can plug into existing EBGA motherboards and can operate without requiring changes to the system. In some cases, however, a special BIOS is needed. Currently, BIOS support for the VIA Antaur processor is available from Award, AMI, Phoenix, and Insyde.

The VIA Antaur processor integrates external termination of bus signals. Physical and bus compatibility is covered in more detail in Section 4 of this datasheet.

The VIA Antaur processor supports SSE instructions. The VIA Antaur processor currently does NOT support multiple processors. These functions are defined as optional by, and are identified to software via, the CUID instruction. The VIA Antaur processor carefully follows the protocol for defining the availability of these optional features. Both the additional and omitted optional features are covered in more detail in Section 2 of this datasheet.

To verify compatibility of the VIA Antaur processor with real PC applications and hardware, VIA has performed extensive testing of hundreds of PC boards and peripherals, thousands of software applications, and all known operating systems.

## SECTION

## 2

# PROGRAMMING INTERFACE

## 2.1 GENERAL

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The VIA Antaur processor's functions include:

- All basic x86 instructions, registers, and functions
- All floating-point (numeric processor) instructions, registers and functions
- All basic operating modes: real mode, protect mode, virtual-8086 mode
- System Management Interrupt (SMI) and the associated System Management Mode (SMM)
- All interrupt and exception functions
- All debug functions (including the new I/O breakpoint function)
- All input/output functions
- All tasking functions (TSS, task switch, etc.)
- Processor initialization behavior
- Page Global Enable feature

*The VIA Antaur processor, in addition to the MMX instructions, also includes SSE instructions to boost the performance of 3D graphics.*

However, there are some differences between the VIA Antaur processor and the Celeron processor. These differences fall into three groups:

- **Implementation-specific differences.** Examples are cache and TLB testing features, and performance monitoring features that expose the internal implementation features. These types of functions are incompatible among *all* different x86 implementations.
- **Omitted functions.** Some Intel Celeron processor functions are not provided on the VIA Antaur processor because they are not used or are not needed in the targeted PC systems. Examples are some specific bus functions such as functional redundancy checking and performance monitoring. Other examples are architectural extensions such as support for Physical Address Extensions, Page Attribute Tables, etc.

These types of differences are similar to those among various versions of the processors. The CPUID instruction is used by system software to determine whether these features are supported.

- **Low-level behavioral differences.** A few low-level VIA Antaur processor functions are different from Intel Celeron because the results are (1) documented in the documentation as *undefined*, and (2) known to be different for different x86 implementations. That is, compatibility with the Intel Celeron processor for these functions is clearly not needed for software compatibility (or they would not be different across different implementations).

This chapter summarizes the first three types of differences: additional functions, implementation-specific functions, and omitted functions. *Appendix A* contains more details on machine-specific functions.

## 2.2 ADDITIONAL FUNCTIONS

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The VIA Antaur processor includes SSE instructions to boost the performance of 3D applications.

## 2.3 MACHINE-SPECIFIC FUNCTIONS

### 2.3.1 GENERAL

All x86 processor implementations provide a variety of *machine-specific functions*. Examples are cache and TLB testing features and performance monitoring features that expose the internal implementation features.

This section describes the VIA Antaur processor machine-specific functions that are most likely used by software, and compares them to related processors where applicable. *Appendix A* describes the VIA Antaur processor machine-specific registers (*MSRs*).

This section covers those features of Intel Pentium-compatible processors that are used to commonly identify and control processor features. All Pentium-compatible processors have the same mechanisms, but the bit-specific data values often differ.

### 2.3.2 STANDARD CPUID INSTRUCTION FUNCTIONS

The CPUID instruction is available on all contemporary x86 processors. The CPUID instruction has two standard functions requested via the EAX register. The first function returns a vendor identification string in registers EBX, ECX, and EDX. The second CPUID function returns an assortment of bits in EAX and EDX that identify the chip version and describe the specific features available.

The EAX:EBX:ECX:EDX return values of the CPUID instruction executed with EAX == 0 are:

**Table 2-1. CPUID Return Values (EAX = 0)**

<b>REGISTER[BITS] – MEANING</b>	<b>VIA ANTAUR</b>
EAX (highest EAX input value understood by CPUID)	1
EBX:EDX:ECX (vendor ID string)	“Centaur Hauls”

The EAX return values of the CPUID instruction executed with EAX == 1 are:

**Table 2-2. CPUID EAX Return Values (EAX = 1)**

<b>EAX BITS - MEANING</b>	<b>VIA ANTAUR</b>
3:0 - Stepping ID	
7:4 - Model ID	Same as the return value in EDX after Reset (see next section)
11:8 - Family ID	
13:12 - Type ID	

The EDX return values of the CUID instruction with EAX == 1 are:

**Table 2-3. CUID EDX Return Values (EAX = 1)**

<b>EDX BITS – MEANING</b>	<b>VIA ANTAUR</b>	<b>NOTES</b>
0 - FPU present	1	
1 - Virtual Mode Extension	0	
2 - Debugging Extensions	1	
3 - Page Size Extensions (4MB)	1	
4 - Time Stamp Counter (TSC) supported	1	
5 - Model Specific Registers present	1	
6 - Physical Address Extension	0	
7 - Machine Check Exception	0	
8 - CMPXCHG8B instruction	1	1
9 - APIC supported	0	2
10- Reserved		
11- Fast System Call	0	
12- Memory Range Registers	1	
13 - PTE Global Bit supported	1/0	3
14- Machine Check Architecture supported	0	
15- Conditional Move supported	1	
16- Page Attribute Table	0	
17- 36-bit Page Size Extension	0	
18- Processor serial number	0	
19:22 - Reserved		
23- MMX supported	1	
24- FXSR	1	
25- Streaming SIMD Extension supported	1	
26:31 - Reserved		

**Notes On CUID Feature Flags:**

General: an “x/y” entry means that the default setting of this bit is x but the bit (and the underlying function) can be set to y using the FCR MSR.

1. The CMPXCHG8B instruction is provided and always enabled, however, it can be disabled in the corresponding CUID function bit 8 to avoid a bug in an early version of Windows NT. However, this default can be changed via bit 1 in the FCR MSR.
2. APIC will be available in future steppings.
3. The VIA Antaur processor’s support for Page Global Enable can be enabled or disabled by a bit in the FCR. The CUID bit reports the current setting of this enable control.

### 2.3.3 EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA Antaur processor supports extended CPUID functions. These functions provide additional information about the VIA Antaur processor. Extended CPUID functions are requested by executing CPUID with EAX set to any value in the range 0x80000000 through 0x80000005.

The following table summarizes the extended CPUID functions.

**Table 2-4. Extended CPUID Functions**

<i>EAX</i>	<i>TITLE</i>	<i>OUTPUT</i>
80000000	Largest Extended Function Input Value	EAX=80000006 EBX,ECX,EDX=Reserved
80000001	Processor Signature and Feature Flags	EAX=Processor Signature EBX,ECX=Reserved EDX=Extended Feature Flags
80000002	Processor Name String	EAX,EBX,ECX,EDX
80000003	Processor Name String	EAX,EBX,ECX,EDX
80000004	Processor Name String	EAX,EBX,ECX,EDX
80000005	TLB and L1 Cache Information	EAX = Reserved EBX = TLB Information ECX = L1 Data Cache Information EDX = L1 Instruction Cache Information
80000006	L2 Cache Information	EAX, EBX, EDX = Reserved ECX = L2 Cache Information

#### **Largest Extended Function Input Value (EAX==0x80000000)**

Returns 0x80000006 in EAX, the largest extended function input value.

#### **Processor Signature and Feature Flags (EAX==0x80000001)**

Returns processor version information in EAX.

#### **Processor Name String (EAX==0x80000002–0x80000004)**

Returns the name of the processor, suitable for BIOS to display on the screen (ASCII). The string can be up to 48 characters in length. If the string is shorter, the rightmost characters are padded with zero. The leftmost characters go in EAX, then EBX, ECX, and EDX. The leftmost character goes in least significant byte (little endian).

For example, the string “VIA Antaur” would be returned by extended function EAX=0x80000002 as follows:

EAX = 0x20414956

EBX = 0x6568654E

ECX = 0x6861696D

EDX = 0x00000000

Since the string is less than 17 bytes, the extended functions EAX=0x80000003 and EAX=0x80000004 return zero in EAX, EBX, ECX, and EDX.

### L1 Cache Information (EAX == 0x80000005)

Returns information about the implementation of the TLBs and caches:

**Table 2-5. L1 Cache & TLB Configuration Encoding**

REGISTER	DESCRIPTION	VALUE
EAX	Reserved	
EBX	TLB Information	
EBX[31:24]	D-TLB associativity	8
EBX[23:16]	D-TLB # entries	128
EBX[15: 8]	I-TLB associativity	8
EBX[ 7: 0]	I-TLB # entries	128
ECX	L1 Data Cache Information	
ECX[31:24]	Size (Kbytes)	64
ECX[23:16]	Associativity	4
ECX[15: 8]	Lines per Tag	1
ECX[ 7: 0]	Line Size (bytes)	32
EDX	L1 Instruction Cache Information	
EDX[31:24]	Size (Kbytes)	64
EDX[23:16]	Associativity	4
EDX[15: 8]	Lines per Tag	1
EDX[ 7: 0]	Line Size (bytes)	32

### L2 Cache Information (EAX == 0x80000006)

Returns information about the implementation of the L2 cache:

**Table 2-6. L2 Cache Configuration Encoding**

REGISTER	DESCRIPTION	VALUE
EAX, EBX, EDX	Reserved	
ECX	L2 Data Cache Information	
ECX[31:16]	Size (Kbytes)	64
ECX[24:12]	Associativity	0 <sup>1</sup> /16
ECX[11: 8]	Lines per Tag	1
ECX[ 7: 0]	Line Size (bytes)	32

Notes: Antaur Stepping 1 inadvertently reports 0. Stepping 2 and later reports 16 (decimal)



### 2.3.4 CENTAUR EXTENDED CPUID INSTRUCTION FUNCTIONS

The VIA Antaur processor supports special CPUID functions. These functions provide additional information about the VIA Antaur processor. Centaur CPUID functions are requested by executing CPUID with EAX set to 0xC0000000 or 0xC0000001.

<i>EAX INPUT</i>	<i>TITLE</i>	<i>OUTPUT</i>
0xC0000000	Largest Centaur Extended Function Input Value	EAX=0xC0000001
0xC0000001	Centaur Extended Feature Flags	EDX=Centaur Extended Feature Flags EAX,EBX,ECX=Reserved

<i>EDX BIT</i>	<i>VALUE</i>
0	EDX[0]=0 Alternate Instruction Set (AIS) not supported EDX[0]=1 Alternate Instruction Set (AIS) supported
1	EDX[1]=0 AIS Disabled EDX[1]=1 AIS Enabled
2	Reserved
3	Reserved
4	EDX[4]=0 Power Saver MSR 0x110A not available EDX[4]=1 Power Saver MSR 0x110A available
31:5	Reserved

### 2.3.5 PROCESSOR IDENTIFICATION

The VIA Antaur processor provides several machine-specific features. These features are identified by the standard CPUID function EAX=1.

Other machine-specific features are controlled by VIA Antaur MSRs. Some of these features are not backward compatible with the predecessors in the VIA C3 or Eden ESP family.

System software must not assume that all future processors in the VIA processor family will implement all of the same machine-specific features, or even that these features will be implemented in a backward-compatible manner. In order to determine if the processor supports particular machine-specific features, system software should follow the following procedure.

Identify the processor as a member of the VIA processor family by checking for a Vendor Identification String of “CentaurHauls” using CPUID with EAX=0. Once this has been verified, system software must determine the processor version in order to properly configure the machine-specific registers.

In general system software can determine the processor version by comparing the Family and Model Identification fields returned by the CPUID standard function EAX=1.

If the processor version is not recognized then system software must not attempt to activate any machine-specific feature.

### 2.3.6 EDX VALUE AFTER RESET.

After reset the EDX register holds a component identification number as follows:

	31:14	13:12	11:8	7:4	3:0
<b>EDX</b>	Reserved	Type ID	Family ID	Model ID	Stepping ID
	18	2	4	4	4

The specific values for the VIA Antaur processor are:

<b>PROCESSOR</b>	<b>TYPE ID</b>	<b>FAMILY ID</b>	<b>MODEL ID</b>	<b>STEPPING ID</b>
VIA Antaur	0	6	9	Begins at 0

### 2.3.7 CONTROL REGISTER 4 (CR4)

Control register 4 (CR4) controls some of the advanced features of the Celeron processor. The VIA Antaur processor provides a CR4 with the following specifics:

**Table 2-7. CR4 Bits**

<b>CR4 BITS - MEANING</b>	<b>VIA ANTAUR</b>	<b>CELERON MODEL 6</b>	<b>CELERON MODEL 8</b>	<b>NOTES</b>
0: VME: Enables VME feature	0	0/1	0/1	1
1: PVI: Enables PVI feature	0	0/1	0/1	1
2: TSD: Makes RDTSC inst privileged	0/1	0/1	0/1	
3: DE: Enables I/O breakpoints	0/1	0/1	0/1	
4: PSE: Enables 4-MB pages	0	0/1	0/1	1
5: PAE: Enables address extensions	r	r	r	
6: MCE: Enables machine check exception	0/1	0/1	0/1	2
7: PGE: Enables global page feature	0/1	0/1	0/1	
8: PCE: Enables RDPMC for all levels	0/1	0/1	0/1	
9: OSFXSR: Enables FXSAVE//FXRSTOR Support	0/1	r	0/1	
10: OSXMMEXCPT: O/S Unmasked Exception Support	0/1	r	0/1	
31:11 - reserved	r	r	r	

**Notes On CR4**

General: a “0/1” means that the default setting of this bit is 0 but the bit can be set to (1). A “0” means that the bit is always 0; it cannot be set. An “r” means that this bit is reserved. It appears as a 0 when read, and a GP exception is signaled if an attempt is made to write a 1 to this bit.

1. The VIA Antaur processor does not provide this “Appendix H” function and this CR4 bit cannot be set. However, no GP exception occurs if an attempt is made to set this bit.
2. The VIA Antaur processor Machine Check has different specifics than the Machine Check function of compatible processors.

**2.3.8 MACHINE-SPECIFIC REGISTERS**

The VIA Antaur processor implements the concept of Machine Specific Registers (MSRs). RDMSR and WRMSR instructions are provided and the CUID instruction identifies that the VIA Antaur processor supports MSRs.

In general, the MSRs have no usefulness to application or operating system software and are not used. (This is to be expected since the MSRs are different on each processor.) *Appendix A* contains a detailed description of the VIA Antaur processor’s MSRs.

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## 2.4 OMITTED FUNCTIONS

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This section summarizes those functions that are not in the VIA Antaur processor. A bit in the CPUID feature flags indicates whether these feature are present or not.

### **Virtual 8086 Mode Enhancements: VME**

This function is omitted since the target market for the VIA Antaur processor is portables and typical desktop systems which do not rely upon VME. This enhancement is not provided on the VIA Antaur processor.

### **Physical Address Extensions: PAE**

This function is omitted since the target market for the VIA Antaur processor is portables and typical desktop systems. These systems do not use 2 MB paging and have greater than 4 GB of system memory.

### **SYSENTER and SYSEXIT: SEP**

This function is omitted since the target operating systems for the VIA Antaur do not require fast system calls to system procedures.

### **Page Attribute Table: PAT**

This function is omitted since the target operating systems for the VIA Antaur do not require mapping of memory cache types to pages within linear addresses.

### **Page Size Extensions: PSE-36**

This function is omitted since the target operating systems for the VIA Antaur do not require greater than 4 GB of system memory.

### **Other Functions**

Model specific registers pertaining to Machine Check, and Debug, Performance Monitoring, and Trace features are not supported.

## SECTION

## 3

# HARDWARE INTERFACE

## 3.1 BUS INTERFACE

---

The VIA Antaur processor bus interface is commonly referred to as the 368 ball interface.

The majority of the pins within the bus interface are involved with the physical memory and I/O interface. The remaining pins are power and ground pins, test and debug support pins, and various ancillary control functions. The pins and associated functions are listed and described in this section.

### 3.1.1 DIFFERENCES

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The areas where the VIA Antaur processor differs from compatible processors should not cause operational compatibility issues. These differences are:

- Bus-to-core Ratio Control
- Bus Frequency Control
- Probe Mode / JTAG / TAP Port (see *Test and Debug Section*)

#### **Bus-to-Core Frequency Ratio Control**

The VIA Antaur processor supports both fused and software control of the bus-to-core frequency ratio. At reset, the factory-set, fused ratio is used. This ratio can then be adjusted via software. This adjustment lasts until the next reset.

Software can adjust the bus-to-core ratio using the VIA Antaur processor's PowerSaver extensions. These are documented separately in the VIA PowerSaver Specification.

### Bus Frequency Selection

The VIA Antaur processor supports automated bus frequency selection through the BSEL pins. The BSEL pins are used as a mechanism whereby the processor and the system board can negotiate to support high frequency bus frequencies. The standard BSEL decoding is shown in Table 3-1.

While the VIA Antaur processor is designed to operate at bus frequencies of 66, 100, or 133 MHz, performance is improved by running at higher bus frequencies. Various speed bins preclude 133 MHz operation because the available bus-to-core ratios do not permit operation at the desired core MHz.

Processors from these speed bins indicate this by shorting the BSEL[1] pin to ground internal to the package. For these processors the BSEL[0] pin is left floating. Processors from speed bins which permit 133 MHz bus operation indicate this by allowing both BSEL[1] and BSEL[0] to float.

It is anticipated that motherboards will pull up both BSEL pins. The resulting BSEL-indicated bus frequency will then be either 100 MHz or 133 MHz according to speed bin. Bus operation at 66MHz is not desirable.

**Table 3-1. BSEL Frequency Mapping**

<i>BSEL[1]</i>	<i>BSEL[0]</i>	<i>BUS FREQUENCY</i>
0	0	66 MHz
0	1	100 MHz
1	0	Reserved
1	1	133 MHz

### 3.1.2 CLARIFICATIONS

#### Power Supply Voltage

The VIA Antaur processor automatically controls its core processor power supply voltage with the VID pins.

The VID mapping for EBGA-packaged VIA Antaur processors is in Table 3-2. This mapping corresponds to the VRM8.5 specification.

**Table 3-2. Core Voltage Settings**

<i>VID4</i>	<i>VID3</i>	<i>VID2</i>	<i>VID1</i>	<i>VID0</i>	<i>VCORE</i>
0	0	1	0	0	1.050V
1	0	1	0	0	1.075V
0	0	0	1	1	1.100V
1	0	0	1	1	1.125
0	0	0	1	0	1.150V
1	0	0	1	0	1.175V
0	0	0	0	1	1.200V
1	0	0	0	1	1.225V
0	0	0	0	0	1.250V
1	0	0	0	0	1.275V
0	1	1	1	1	1.300V
1	1	1	1	1	1.325V
0	1	1	1	0	1.350V
1	1	1	1	0	1.375V
0	1	1	0	1	1.400V
1	1	1	0	1	1.425V
0	1	1	0	0	1.450V
1	1	1	0	0	1.475V
0	1	0	1	1	1.500V
1	1	0	1	1	1.525V
0	1	0	1	0	1.550V
1	1	0	1	0	1.575V
0	1	0	0	1	1.600V
1	1	0	0	1	1.625V
0	1	0	0	0	1.650V
1	1	0	0	0	1.675V
0	0	1	1	1	1.700V
1	0	1	1	1	1.725V
0	0	1	1	0	1.750V
1	0	1	1	0	1.775V
0	0	1	0	1	1.800V
1	0	1	0	1	1.825V

NOTE: VID4 may be referred as VID25mV.

## VCCCMOS

The VIA Antaur processor routes the VCC<sub>1.5</sub> pin to the VCCCMOS pin via the package. This signal is not used by the processor, but is intended to be used by the system as the power supply for CMOS level signals. VCCCMOS should not be expected to source more than 250mA.

## RESET#

The VIA Antaur processor is reset by the assertion of the RESET# pin. Current versions of the VIA Antaur processor connect this pin to AH-4 in the Socket370 pinout.

Board designers should always connect RESET# to both AH-4 and X-4 to ensure compatibility with all VIA processors.

## Thermal Monitoring

The VIA Antaur processor supports thermal monitoring via the THERMDN and THERMDP pins. However, it does not support the THERMTRIP# pin. The THERMTRIP# pin should be treated as reserved.

### 3.1.3 OMISSIONS

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## VTT\_PWRGD

The VTT\_PWRGD signal is not used. Care should be taken to prevent the VCC plane from powering up before the VTT plane.

## Advanced Peripheral Interrupt Controller (APIC)

The APIC is currently not supported by the VIA Antaur processor. Future steppings of the VIA Antaur will support the APIC. The APIC pins (PICCLK, PICD0, and PICD1) are specified as reserved, but can be connected on the motherboard for compatibility with future processors.

## Breakpoint and Performance Monitoring Signals

The VIA Antaur processor internally supports instruction and data breakpoints. However, the VIA Antaur processor does not support the external indication of breakpoint matches via the BP3-BP0 pins. Similarly, the VIA Antaur processor contains performance monitoring hooks internally, but it does not support the indication of performance monitoring events on PM1-PM0. The associated pins are unconnected on the VIA Antaur processor package.

## Error Checking

The VIA Antaur processor does not support error checking. The BERR#, BINIT#, AERR#, AP#[1:0], DEP#[7:0], IERR#, RP#, and RSP# pins do not exist and should be treated as reserved.

## V<sub>COREDET</sub>

The VIA Antaur processor does not connect to the VCOREDET pin.

## SLEWCTRL

The VIA Antaur processor does not connect to the SLEWCTRL pin. Future VIA processors may connect to the SLEWCTRL pin.



## 3.2 PIN DESCRIPTION

**Table 3-3. Pin Descriptions**

<i>Pin Name</i>	<i>Description</i>	<i>I/O</i>	<i>Clock</i>
A[31:3]#	The address Bus provides addresses for physical memory and external I/O devices. During cache inquiry cycles, A31#-A3# are used as inputs to perform snoop cycles.	I/O	BCLK
A20M#	A20 Mask causes the CPU to make (force to 0) the A20 address bit when driving the external address bus or performing an internal cache access. A20M# is provided to emulate the 1 MByte address wrap-around that occurs on the 8086. Snoop addressing is not affected.	I(1.5V)	ASYNC
ADS#	Address Strobe begins a memory/I/O cycle and indicates the address bus (A31#-A3#) and transaction request signals (REQ#) are valid.	I/O	BCLK
BCLK	Bus Clock provides the fundamental timing for the VIA Antaur CPU. The frequency of the VIA Antaur CPU input clock determines the operating frequency of the CPU's bus. External timing is defined referenced to the rising edge of CLK.	I(2.5V)	--
BNR#	Block Next Request signals a bus stall by a bus agent unable to accept new transactions.	I/O	BCLK
BPRI#	Priority Agent Bus Request arbitrates for ownership of the system bus.	I	BCLK
BSEL[1:0]	Bus Selection Bus provides system bus frequency data to the CPU.	O	BCLK
BR[1:0]#	BR0# drives the BREQ[0]# signal in the system to request access to the system bus. BR1# drives the BREQ[1]# signal in the system to request access to the system bus.	I/O	None
CPUPRES#	CPU Present is grounded inside the processor to indicate to the system that a processor is present.	O	None
D[63:0]#	Data Bus signals are bi-directional signals which provide the data path between the VIA Antaur CPU and external memory and I/O devices. The data bus must assert DRDY# to indicate valid data transfer.	I/O	BCLK
DBSY#	Data Bus Busy is asserted by the data bus driver to indicate data bus is in use.	I/O	BCLK
DEFER#	Defer is asserted by target agent (e.g., north bridge) and indicates the transaction cannot be guaranteed as an in-order completion.	I	BCLK
DRDY#	Data Ready is asserted by data driver to indicate that a valid signal is on the data bus.	I/O	BCLK
FERR#	FPU Error Status indicates an unmasked floating-point error has occurred. FERR# is asserted during execution of the FPU instruction that caused the error.	O(1.5V)	ASYNC
FLUSH#	Flush Internal Caches writing back all data in the modified state.	I(1.5V)	ASYNC
HIT#	Snoop Hit indicates that the current cache inquiry address has been found in the cache (exclusive or shared states).	I/O	BCLK
HITM#	Snoop Hit Modified indicates that the current cache inquiry address has been found in the cache and dirty data exists in the cache line (modified state).	I/O	BCLK
IGNNE#	Ignore Numeric Error forces the VIA Antaur CPU to ignore any pending unmasked FPU errors and allows continued execution of floating point instructions.	I(1.5V)	ASYNC
INIT#	Initialization resets integer registers and does not affect internal cache or floating point registers.	I(1.5V)	ASYNC
INTR	Maskable Interrupt	I(1.5V)	ASYNC
NCHCTRL	Control integrated I/O pull-ups. Connect this signal to VTT with a 14 $\Omega$ resistor.	I	ASYNC
NMI	Non-Maskable Interrupt	I(1.5V)	ASYNC
LOCK#	Lock Status is used by the CPU to signal to the target that the operation is atomic.	I/O	BCLK
PICCLK	APIC clock for operation with the system I/O APIC	I	APIC

<i>Pin Name</i>	<i>Description</i>	<i>I/O</i>	<i>Clock</i>
PICD[1:0]	Bi-directional serial pins for communicating APIC messages to the system.	I/O	APIC
PWRGD	Indicates that the processor's VCC is stable.	I	ASYNC
REQ[4:0]#	Request Command is asserted by bus driver to define current transaction type.	I/O	BCLK
RESET#	Resets the processor and invalidates internal cache without writing back.	I	BCLK
RS[2:0]#	Response Status signals the completion status of the current transaction when the CPU is the response agent.	I	BCLK
RTTCTRL	Control the output impedance on the on-die termination resistance. Connect this signal to VSS with a 56Ω resistor if relying upon on-die termination. Connect this signal to VSS with a 110Ω resistor if relying upon board termination.	I	ASYNC
SLP#	Sleep, when asserted in the stop grant state, causes the CPU to enter the sleep state.	I(1.5V)	ASYNC
SMI#	System Management (SMM) Interrupt forces the processor to save the CPU state to the top of SMM memory and to begin execution of the SMI services routine at the beginning of the defined SMM memory space. An SMI is a high-priority interrupt than NMI.	I(1.5V)	ASYNC
STPCLK#	Stop Clock causes the CPU to enter the stop grant state.	I(1.5V)	ASYNC
TRDY#	Target Ready indicates that the target is ready to receive a write or write-back transfer from the CPU.	I	BCLK
VID[4:0]	Voltage Identification Bus informs the regulatory system on the motherboard of the CPU Core voltage requirements.	O(1.5V)	ASYNC

**Table 3-4. BGA only Pin Descriptions**

<i>Pin Name</i>	<i>Description</i>	<i>I/O</i>	<i>Clock</i>
BR[4:0]	Hardware strapping options for setting the processors internal clock multiplier. VIA Antaur processors do not have their clock multiplier set to a factory default value. Use jumpers or populate 0Ω resistors to select the rated multiplier. The BR[4:0] balls should be wired to VSS for a value of "0" or wired to OPEN for setting of "1." See Table 3-5 for ratio values.	I	

Table 3-5. Clock Ratio

BR[4]	BR[3]	BR[2]	BR[1]	BR[0]	Bus Ratio
0	0	0	0	0	9.0X
0	0	0	0	1	3.0X
0	0	0	1	0	4.0X
0	0	0	1	1	10.0X
0	0	1	0	0	5.5X
0	0	1	0	1	3.5X
0	0	1	1	0	4.5X
0	0	1	1	1	9.5X
0	1	0	0	0	5.0X
0	1	0	0	1	7.0X
0	1	0	1	0	8.0X
0	1	0	1	1	6.0X
0	1	1	0	0	12.0X
0	1	1	0	1	7.5X
0	1	1	1	0	8.5X
0	1	1	1	1	6.5X
1	0	0	0	0	Reserved
1	0	0	0	1	11.0X
1	0	0	1	0	12.0X
1	0	0	1	1	Reserved
1	0	1	0	0	13.5X
1	0	1	0	1	11.5X
1	0	1	1	0	12.5X
1	0	1	1	1	10.5X
1	1	0	0	0	13.0X
1	1	0	0	1	15.0X
1	1	0	1	0	16.0X
1	1	0	1	1	14.0X
1	1	1	0	0	Reserved
1	1	1	0	1	15.5X
1	1	1	1	0	Reserved
1	1	1	1	1	14.5X

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### 3.3 POWER MANAGEMENT

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The VIA Antaur processor provides both static and dynamic power management.

The VIA Antaur processor supports five power management modes: NORMAL state, STOP GRANT state, AUTOHALT state, SLEEP state, and DEEP SLEEP state.

The VIA Antaur processor uses dynamic power management techniques to reduce power consumption in the NORMAL state. In NORMAL state, the on-chip arrays, selected datapaths, and the associated control logic are powered down when not in use. In addition, units that are in use attempt to minimize switching of inactive nodes.

- NORMAL state is the normal operating state for the processor.
- STOP GRANT state is the low power state where most of the processor clocks do not toggle. It is entered when the STPCLK# signal is asserted. Snoop cycles are supported in this state.
- AUTO HALT state is the low power state where most of the processor clocks do not toggle. It is entered when the processor executes the HALT instruction. Snoop cycles are supported in this state.
- SLEEP state is the very low power state where only the processor's PLL (phase lock loop) toggles. It is entered from STOP GRANT state when the processor samples the SLP# signal asserted. Snoop cycles that occur while in SLEEP state or during a transition into or out of SLEEP state will cause unpredictable behavior.
- DEEP SLEEP state is the lowest power state. It is entered when the BCLK signal is stopped while the processor is in the SLEEP state. Snoop cycles will be completely ignored in this state.

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## 3.4 TEST & DEBUG

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### 3.4.1 BIST

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A Built-in Self-Test (BIST) can be requested as part of the VIA Antaur processor reset sequence by holding INIT# asserted as RESET# is de-asserted.

The VIA Antaur processor BIST performs the following general functions:

- A hardware-implemented exhaustive test of (1) all internal microcode ROM, and (2) the X86 instruction decode, instruction generation, and entry point generation logic.
- An extensive microcode test of all internal registers and datapaths.
- An extensive microcode test of data and instruction caches, their tags, and associated TLBs.

BIST requires about four million internal clocks.

#### EAX Value After Reset

The result of a BIST is indicated by a code in EAX. Normally EAX is zero after reset. If a BIST is requested as part of the Reset sequence, EAX contains the BIST results. A 0 in EAX after BIST Reset means that no failures were detected. Any value other than zero indicates an error has occurred during BIST.

### 3.4.2 JTAG

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The VIA Antaur processor has a JTAG scan interface that is used for test functions and the proprietary Debug Port. However, the VIA Antaur processor does not provide a fully compatible IEEE 1149.1 JTAG function.

From a practical user viewpoint, JTAG does not exist and the associated pins (TCLK, and so forth) should not be used.

### 3.4.3 DEBUG PORT

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Certain processors have a proprietary Debug Port which uses the JTAG scan mechanism to control internal debug features (“probe mode”). These interfaces are not documented and are available (if at all) only under a non-disclosure agreement.

The VIA Antaur processor does not have a debug interface.

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## SECTION

## 4

## ELECTRICAL SPECIFICATIONS

## 4.1 AC TIMING TABLES

Table 4-1. System Bus Clock AC Specifications (133 MHz)<sup>1</sup>

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
	System Bus Frequency		133	MHz		
T <sub>1S</sub>	BCLK Period	7.5	7.65	ns	Figure 4-1	(2)
T <sub>1Sabs</sub>	BCLK Period – Instantaneous Minimum	7.25				(2)
T <sub>2S</sub>	BCLK Period Stability		±250	ps		(2),(3),(4)
T <sub>3S</sub>	BCLK High Time	1.4		ns	Figure 4-1	at>2.0V
T <sub>4S</sub>	BCLK Fall Time	1.4		ns	Figure 4-1	at<0.5V
T <sub>5S</sub>	BCLK Rise Time	0.4	1.6	ns	Figure 4-1	(5)
T <sub>6S</sub>	BCLK Fall Time	0.4	1.6	ns	Figure 4-1	(5)

**Notes:**

1. All AC timings for bus and CMOS signals are referenced to the BCLK rising edge at 1.25V.
2. Period, jitter, skew and offset measured at 1.25V.
3. Not 100% tested. Specified by design/characterization
4. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5V and 2.0V.

**Table 4-2. System Bus Clock AC Specifications (100 MHz)<sup>1</sup>**

<i>SYMBOL</i>	<i>PARAMETER</i>	<i>MIN</i>	<i>MAX</i>	<i>UNIT</i>	<i>FIGURE</i>	<i>NOTES</i>
	System Bus Frequency		100	MHz		
T <sub>1S1</sub>	BCLK Period		10	ns	Figure 4-1	(2)
T <sub>1S1abs</sub>	BCLK Period – Instantaneous Minimum	9.75		ns		(2)
T <sub>2S1</sub>	BCLK Period Stability			ps		(2),(3),(4)
T <sub>3S1</sub>	BCLK High Time	2.70		ns	Figure 4-1	at>2.0V
T <sub>4S1</sub>	BCLK Fall Time	2.45		ns	Figure 4-1	at<0.5V
T <sub>5S1</sub>	BCLK Rise Time	0.4		ns	Figure 4-1	(5)
T <sub>6S1</sub>	BCLK Fall Time	0.4		ns	Figure 4-1	(5)

**Notes:**

1. All AC timings for bus and CMOS signals are referenced to the BCLK rising edge at 1.25V.
2. Period, jitter, skew and offset measured at 1.25V.
3. Not 100% tested. Specified by design/characterization
4. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.
5. Measured between 0.5V and 2.0V.



**Table 4-3. Bus Signal Groups AC Specifications<sup>1</sup>**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>	<b>FIGURE</b>	<b>NOTES</b>
T <sub>7</sub>	Bus Output Valid Delay	0.40	3.25	ns	Figure 4-2	
T <sub>8</sub>	Bus Input Setup Time	0.95		ns	Figure 4-3	(2),(3),(6)
		1.30				(7)
T <sub>9</sub>	Bus Input Hold Time	1		ns	Figure 4-3	(4)
T <sub>10</sub>	RESET# Pulse Width	1		ms	Figure 4-3	(5)

**Notes:**

1. All AC timings for Bus and CMOS signals are referenced to the BCLK rising edge at 1.25V. All bus signals are referenced at VREF. Unless specified, all timings apply to both 100 MHz and 133 MHz bus frequencies.
2. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
3. Specification is for a minimum 0.4V swing from VREF-200 mV to VREF+200 mV.
4. Specification is for a maximum 0.8V swing from VTT-0.8V to VTT.
5. After VCC, VTT and BCLK become stable and PWRGOOD is asserted.
6. Applies to processors supporting 133 MHz bus clock frequency.
7. Applies to processors supporting 100 MHz bus clock frequency.

**Table 4-4. CMOS and Open-drain Signal GROUPS AC Specifications<sup>1,2</sup>**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>	<b>FIGURE</b>	<b>NOTES</b>
T <sub>14</sub>	1.5V Input Pulse Width, except PWRGOOD	2		BCLKs	Figure 4-2	Active and inactive states
T <sub>15</sub>	PWRGOOD Inactive Pulse Width	2		μs	Figure 4-2	(3)

**Notes:**

1. All AC timings for CMOS and Open-drain signals are referenced to the rising edge of BCLK at 1.25V. All CMOS and Open-drain signals are referenced at 1.0V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.

When driven inactive, or after VCC, VTT and BCLK become stable. PWRGOOD must remain below  $V_{IL18,MAX}$  until all the voltage planes meet the voltage tolerance specifications in Table 4-7 through Table 4-9 and BCLK have met the BCLK AC specifications in Table 4-1 and Table 4-2 for a least 2  $\mu$ s.

**Table 4-5. Reset Configuration AC Specifications and Power On/Power Down Timings**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	FIGURE	NOTES
T <sub>16</sub>	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#) Setup Time	4			BCLKs	Figure 4-4	Before deassertion of RESET#
T <sub>17</sub>	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT) Hold Time	2		20	BCLKs	Figure 4-4	After clock that deasserts RESET#
T <sub>18</sub>	RESET#/PWRGOOD Setup Time	1			ms	Figure 4-5	Before deassertion of RESET# <sup>1</sup>
T <sub>18B</sub>	VCC to PWRGOOD Setup Time		10		ms	Figure 4-5	
T <sub>18D</sub>	RESET# inactive to Valid Outputs	1			BCLK	Figure 4-4	
T <sub>18E</sub>	RESET# inactive to Drive Signals	4			BCLKs	Figure 4-4	
T <sub>19A</sub>	Time from VCC(nominal)-12% to PWRGOOD low			0	ns	Figure 4-6	VCC(nominal) is the VID voltage setting
T <sub>19B</sub>	All outputs valid after PWRGOOD low	0			ns	Figure 4-6	
T <sub>19C</sub>	All inputs required valid after PWRGOOD low	0			ns	Figure 4-6	
T <sub>20B</sub>	All outputs valid after VTT-12%	0			ns	Figure 4-7	
T <sub>20C</sub>	All inputs required valid after VTT-12%	0			ns	Figure 4-7	
T <sub>20D</sub>	VID, BSEL signals valid after VTT-12%	0			ns	Figure 4-7	

**Notes:** At least 1 ms must pass after PWRGOOD rises above  $V_{IH18min}$  and BCLK meet their AC timing specification until RESET# may be deasserted.

**Table 4-6. StopGrant/Deep Sleep AC Specifications**

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE	NOTES
T <sub>45</sub>	Stop Grant Cycle Completion to SLP# assertion	100		BCLKs	Figure 4-8	
T <sub>46</sub>	Stop Grant Cycle Completion to Input Signals Stable		0	$\mu$ s	Figure 4-8	
T <sub>47</sub>	Sleep PLL Lock Latency	0	30	$\mu$ s	Figure 4-8	(2)
T <sub>48</sub>	STPCLK# Hold Time from PLL Lock	0		$\mu$ s	Figure 4-8	
T <sub>49</sub>	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	Figure 4-8	

**Notes:**

1. Input Signals other than RESET# and BPRI# must be held constant in the Stop Grant state.
2. The BCLK Settling Time specification (T<sub>60</sub>) applies to Deep Sleep state exit under all conditions.

Figure 4-1. BCLK Generic Clock Timing Waveform

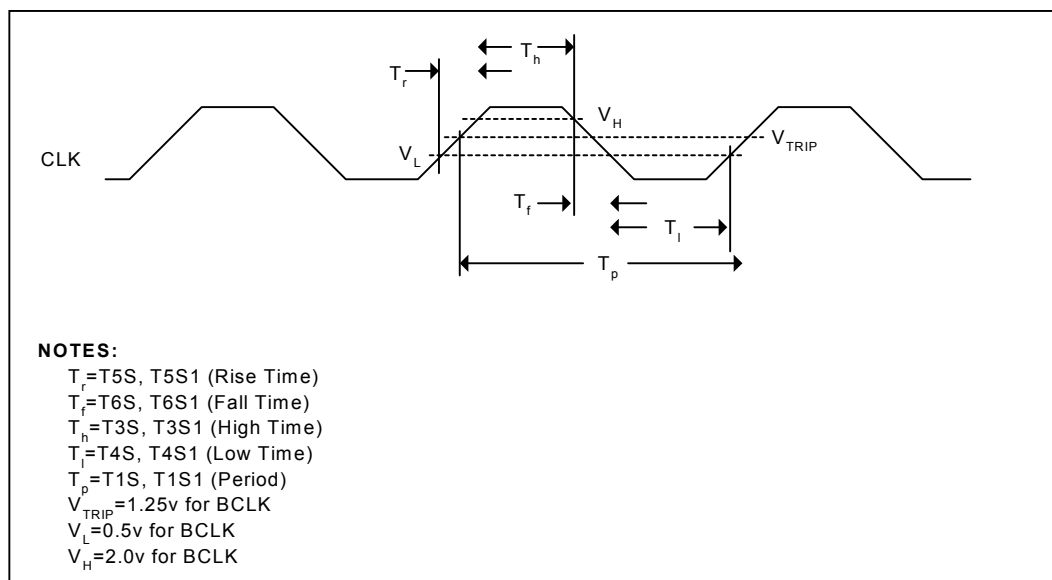


Figure 4-2. Valid Delay Timings

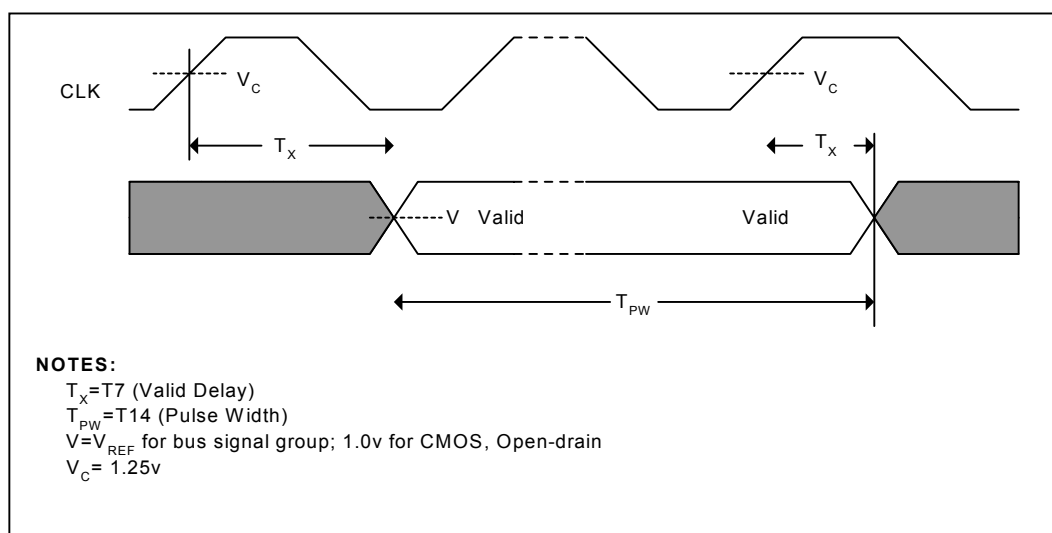


Figure 4-3. Setup and Hold Timings

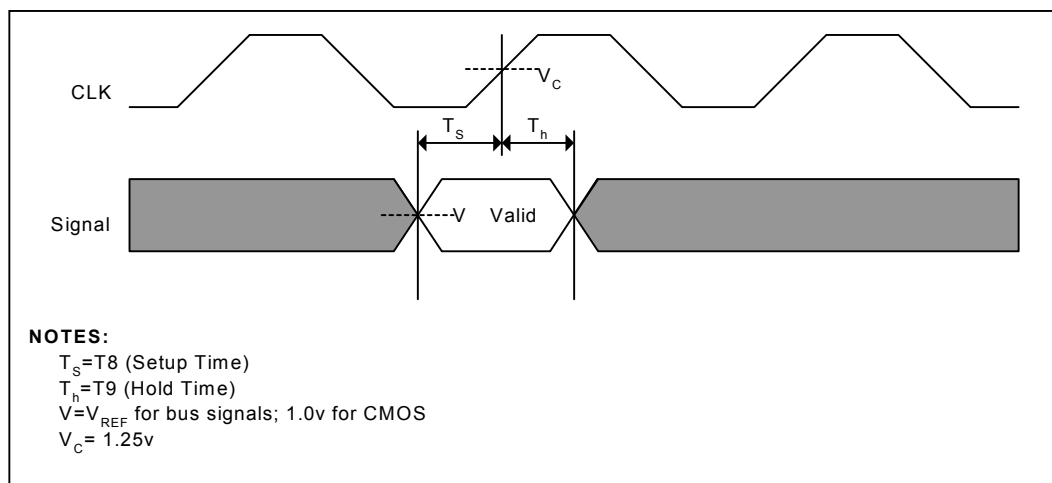


Figure 4-4. Cold/Warm Reset and Configuration Timings

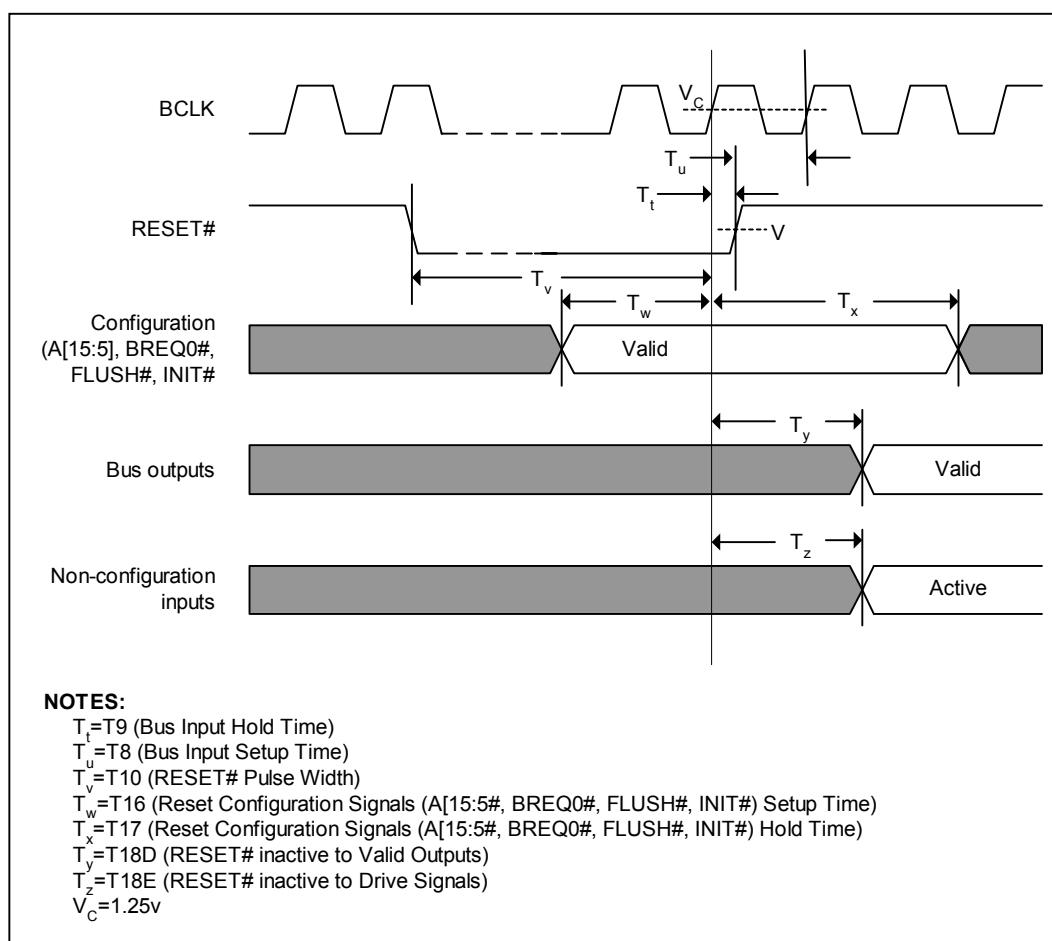


Figure 4-5. Power-on Sequence and Reset Timings

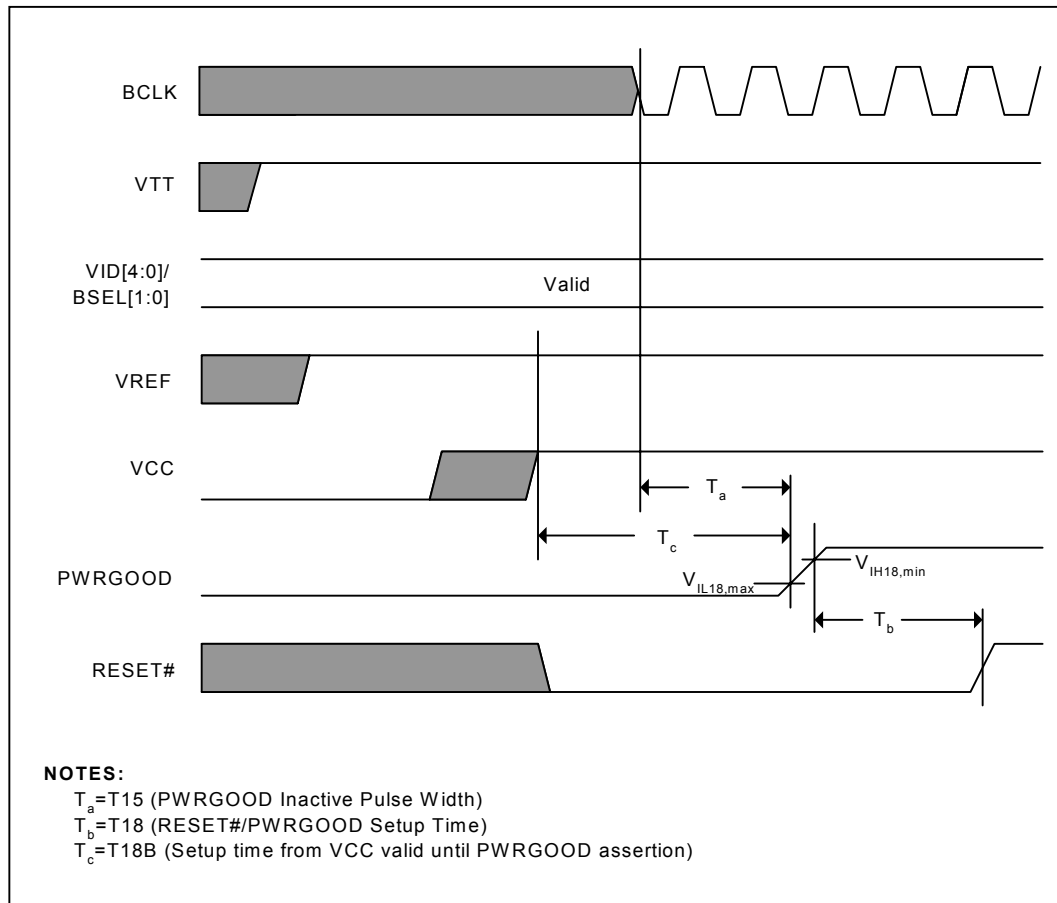


Figure 4-6. Power Down Sequencing and Timings (VCC Leading)

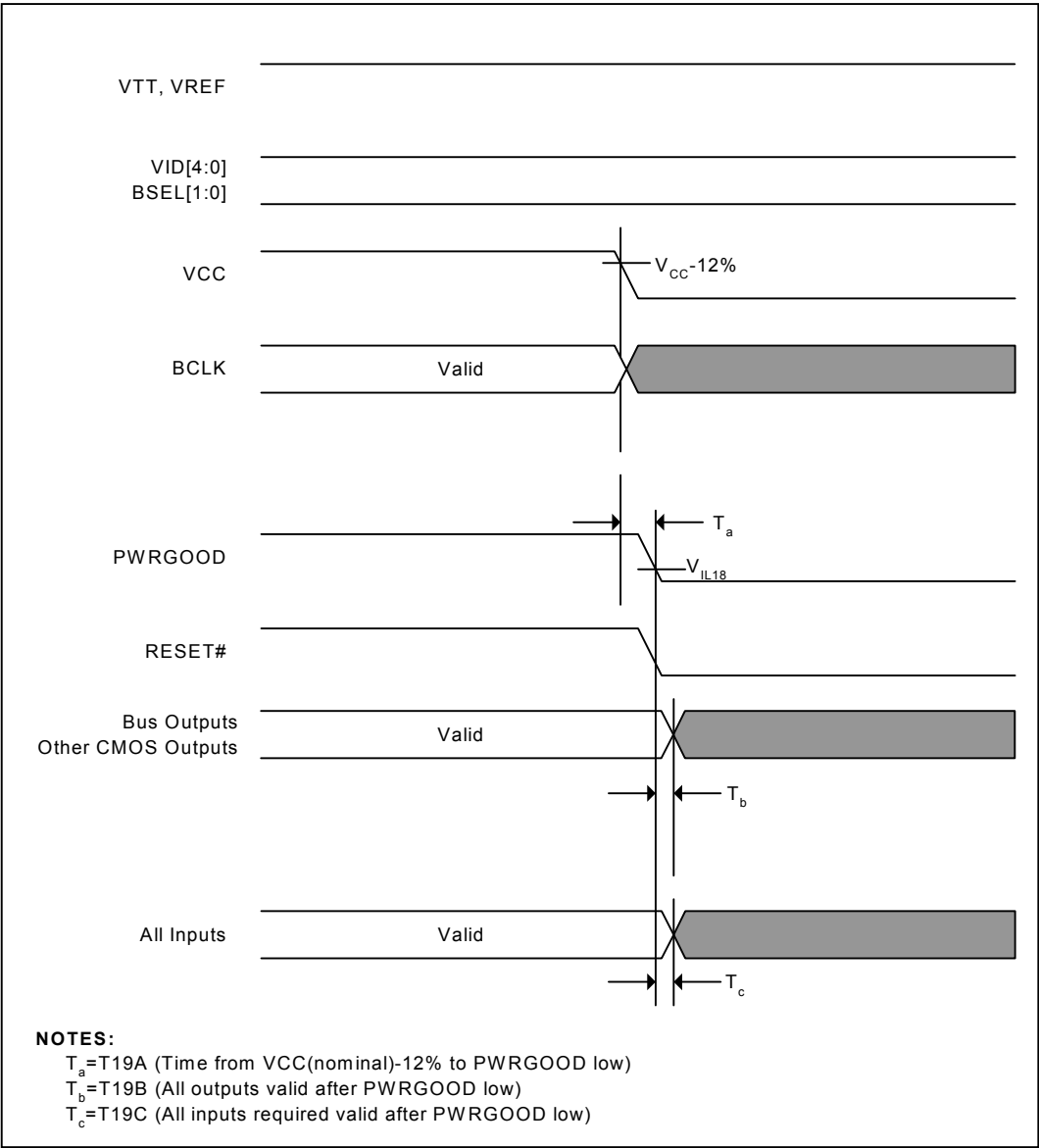


Figure 4-7. Power Down Sequencing and Timings (VTT Leading)

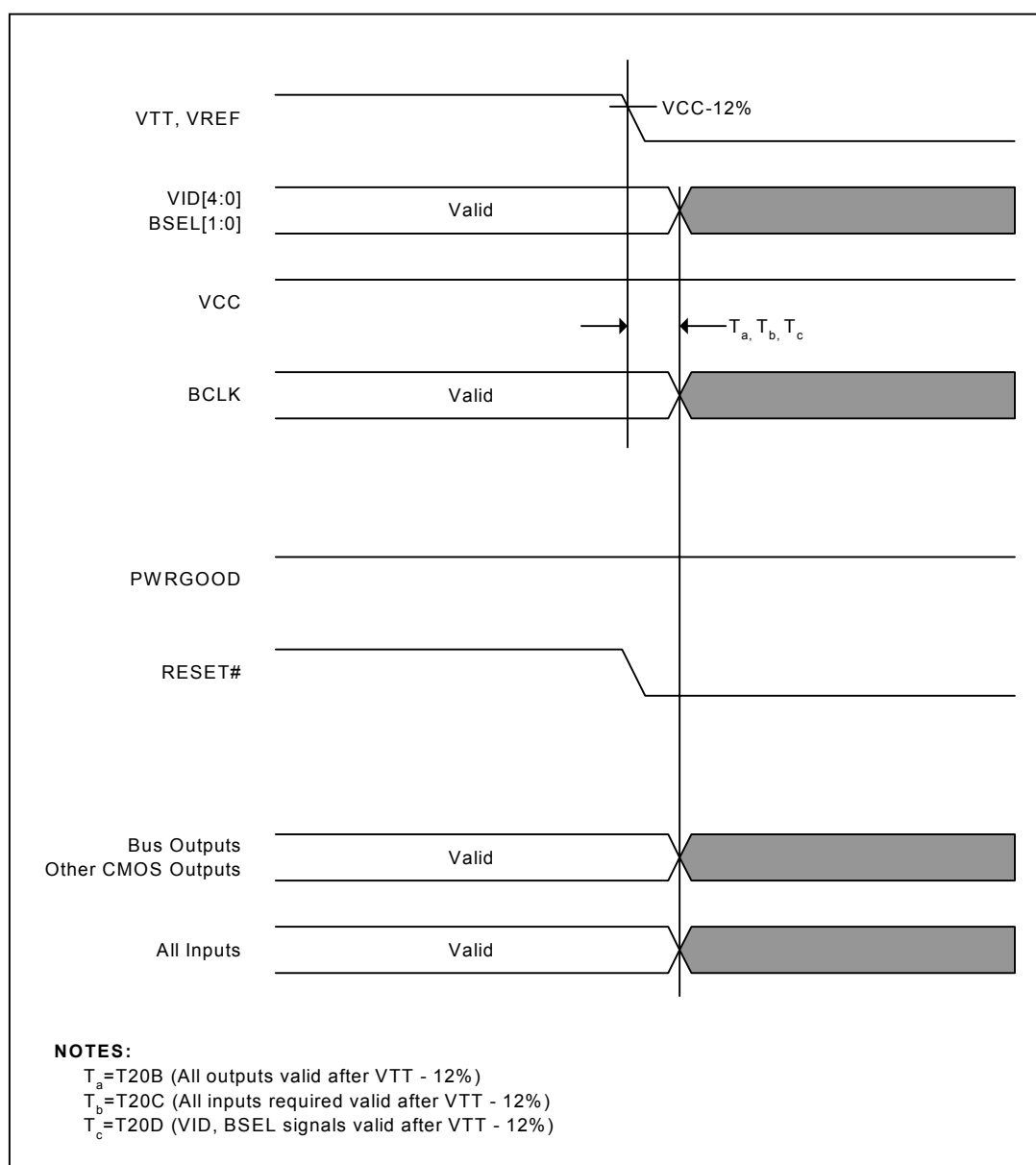
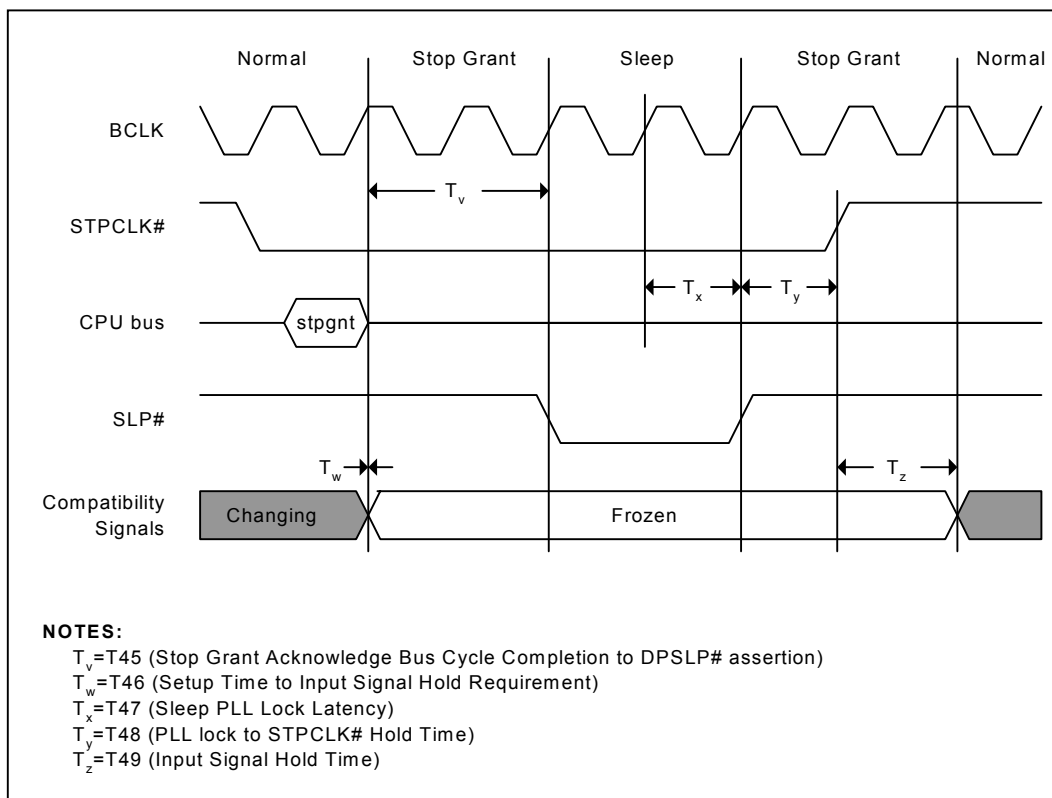


Figure 4-8. Stop Grant/Sleep Timing (SLP# Assertion Method)





## 4.2 DC SPECIFICATIONS

### 4.2.1 RECOMMENDED OPERATING CONDITIONS

Functional operation of the VIA Antaur processor is guaranteed if the conditions in Table 4-7 are met. Sustained operation outside of the recommended operating conditions may damage the device.

**Table 4-7. Recommended Operating Conditions**

PARAMETER	MIN	NOM	MAX	UNITS	NOTES
Operating Case Temperature	0		85	°C	EBGA
V <sub>CORE</sub> Voltage		1.25		V	
V <sub>CORE</sub> Static Tolerance	See Table 4-8			V	(1)
V <sub>CORE</sub> Dynamic Tolerance				V	(2)
V <sub>TT</sub> Voltage	1.1375	1.25	1.635	V	1.25V±3%
V <sub>TT</sub> Voltage	1.365	1.5	1.635	V	
I <sub>VTT</sub> Termination Supply Current			800	mA	(3)
V <sub>REF</sub>	-2%	2/3 V <sub>TT</sub>	+2%	V	
R <sub>TT</sub>	50	56	115	Ω	(4)
V <sub>1.5</sub> – 1.5V Supply Voltage	1.365		1.635	V	

**Notes:**

1. DC measurement.
2. AC noise measured with bandwidth limited to 20MHz.
3. DC measurement. Measured with 250 μs sampling rate.
4. R<sub>TT</sub> is controlled by RTTCTRL pin. RTTCTRL should be 56Ω when relying upon on-die bus termination. RTTCTRL should be 110Ω when relying upon board termination.

Table 4-8.  $V_{CC}$  Static and Transient Tolerance

I <sub>cc</sub> (A)	Voltage Deviation from VID Setting (mV)			
	Static Tolerance		Transient Tolerance	
	Min	Max	Min	Max
0	15	65	5	85
2	5	55	-5	74
4	-5	45	-15	62
6	-15	35	-25	51
8	-25	25	-35	40
10	-35	15	-45	28
12	-45	5	-55	17
14	-55	-5	-65	6
16	-65	-15	-76	-5
18	-75	-25	-87	-15
20	-85	-35	-98	-25
22	-95	-45	-110	-35
24	-105	-55	-121	-45
26	-115	-65	-132	-55
28	-125	-75	-144	-65
30	-135	-85	-155	-75

## 4.2.2 MAXIMUM RATINGS

While functional operation is not guaranteed beyond the operating ranges listed in Table 4-7, the device may be subjected to the limits specified in Table 4-9 without causing long-term damage.

These conditions must not be imposed on the device for a sustained period—any such sustained imposition may damage the device. Likewise exposure to conditions in excess of the maximum ratings may damage the device.

Table 4-9. Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Storage Temperature	-65	150	°C	
Supply Voltage ( $V_{CC}$ )	-0.5	1.7	V	
CMOS I/O Voltage	-0.5	$V_{CMOS} + 0.5$	V	
I/O Voltage	-0.5	$V_{TT} + 0.5$	V	

### 4.2.3 DC CHARACTERISTICS

**Table 4-10. DC Characteristics**

PARAMETER	MIN	MAX	UNITS	NOTES
$I_{OL}$ – Low level output current	-9.0		mA	@ $V = V_{OL(max)}$
$V_{OH}$ – High Level Output Voltage		$V_{TT}$	V	
$V_{OL}$ – Low Level Output Voltage	0	0.4	V	@ $I_{ol} = -8mA$
$I_L$ – Input Leakage Current		$\pm 15$	$\mu A$	
$I_{LU}$ – Input Leakage Current for inputs with pull-ups		200	$\mu A$	
$I_{LD}$ – Input Leakage Current for inputs with pull-downs		-400	$\mu A$	

**Table 4-11. CMOS DC Characteristics**

PARAMETER	MIN	MAX	UNITS	NOTES
$V_{IL}$ – Input Low Voltage	-0.58	0.700	V	
$V_{IH1.5}$ – Input High Voltage	$V_{REF} + 0.2$	$V_{TT}$	V	(2)
$V_{IH2.5}$ – Input High Voltage	2.0	3.18	V	(3)
$V_{OL}$ – Low Level Output Voltage		0.40	V	@ $I_{OL}$
$V_{OH}$ – High Level Output Voltage		$V_{CMOS}$	V	(1)
$I_{OL}$ – Low Level Output Current	9		mA	@ $V_{OL}$
$I_{LI}$ – Input Leakage Current		$\pm 100$	$\mu A$	(4)
$I_{LO}$ – Output Leakage Current		$\pm 100$	$\mu A$	(4)

**Notes:**

1. All CMOS signals are open drain.
2. Applies to all CMOS signals except **BCLK**.
3. Applies only to **BCLK**.
4. Leakage current is specified for the range between VSS and VCC. I/O's are diode clamped to the VCC and VSS rails. **BCLK** has three series diodes between the input and VCC and a single diode between the input and VSS. All other signals have a single diode between the signal and VCC and another single diode between the signal and VSS.

## 4.2.4 POWER DISSIPATION

Table 4-12 provides the core power consumption for the VIA Antaur processor at the various operating frequencies and voltages. Note that this does not include the power consumed by the I/O pads.

**Table 4-12. EBGAThermal Design Power Information**

PARAMETER	TDP MAX <sup>1,2</sup>	UNITS	VOLTAGE	NOTES
Normal Mode				
VIA Antaur 1.00 GHz (7.5 X 133 MHz)	12	W	1.25	4
VIA Antaur 1.13 GHz (8.5 X 133 MHz)	13	W	1.25	
VIA Antaur 1.20 GHz (9.0 X 133 MHz)	15	W	1.25	
StopGrant / AutoHalt Mode				
VIA Antaur 1.00 GHz (7.5 X 133 MHz)	2.0	W	1.25	4
VIA Antaur 1.13 GHz (8.5 X 133 MHz)	TBD	W	1.25	
VIA Antaur 1.20 GHz (9.0 X 133 MHz)	TBD	W	1.25	
Sleep Mode				
VIA Antaur 1.00 GHz (7.5 X 133 MHz)	1.5	W	1.25	4
VIA Antaur 1.13 GHz (8.5 X 133 MHz)	TBD	W	1.25	
VIA Antaur 1.20 GHz (9.0 X 133 MHz)	TBD	W	1.25	
Deep Sleep Mode				
VIA Antaur 1.00 GHz (7.5 X 133 MHz)	1.0	W	1.25	4
VIA Antaur 1.13 GHz (8.5 X 133 MHz)	TBD	W	1.25	
VIA Antaur 1.20 GHz (9.0 X 133 MHz)	TBD	W	1.25	

**Notes:**

1. Maximum power is generated from running publicly available application software that consumes the most power. Synthetic applications or “thermal virus” applications may consume more power.
2. TDP AverageMax is average value of all parts while running the worst case instruction sequence. Not 100% guaranteed or tested. Consider these power numbers as an average of all parts and some deviation is expected.
3. TDP FactoryMax is the factory limit for power consumption while running the worst case instruction sequence. Factory will reject parts that exceed these specified values.
4. The above power consumption is preliminary and based on 85°C case.
5. Conservative thermal solutions must be designed to account for worst-case core and I/O power consumption.

**Table 4-13. V<sub>TT-I/O</sub> Power Consumption**

PARAMETER	TYPICAL	MAX	UNITS	NOTES
PTT-I/O – I/O Operating Power Consumption	0.3	1.2	W	

## SECTION

## 5

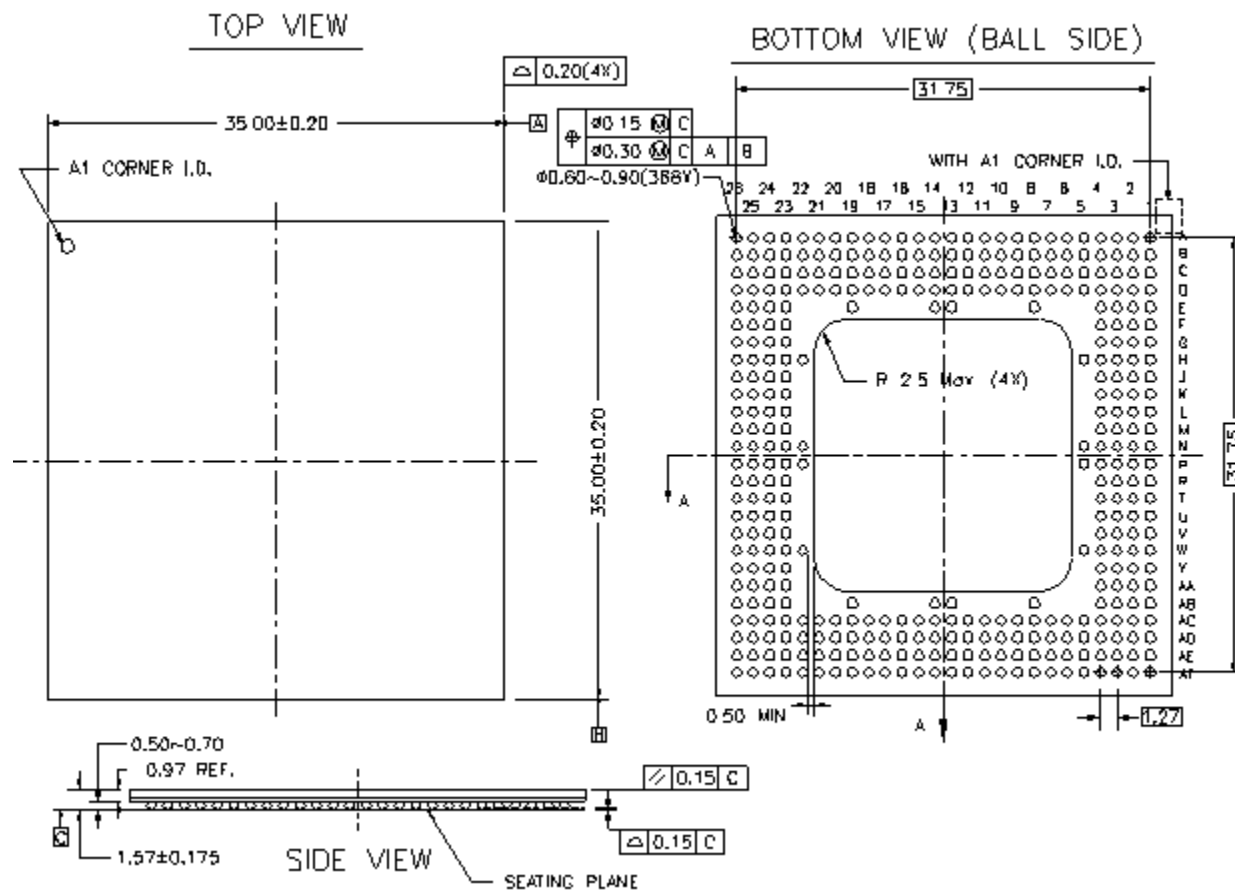
# MECHANICAL SPECIFICATIONS

## 5.1 EBGA PACKAGE

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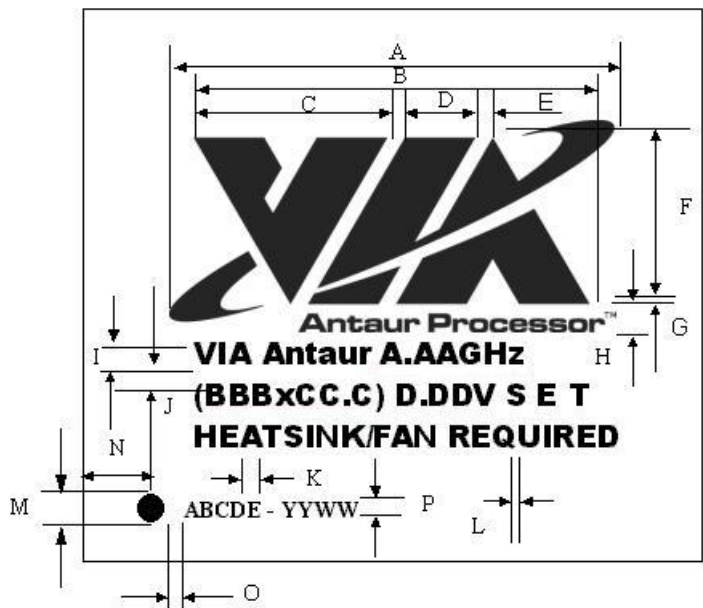
The VIA Antaur in EBGA is packaged in a unique enhanced ball grid array that facilitates compact and economical surface mounting. The VIA Antaur in EBGA bus is functionally similar to Socket 370 used by conventional CPGA VIA Antaurs but is obviously not mechanically compatible.

Figure 5-1. EPGA Mechanical Specification



Allowable Pressure on the top of the package is 800 kPa (116 Psi)

Figure 5-2. Processor Top Marking



Symbol Descriptions			
S	Indicates that M/B jumpers should be implemented to adjust the clock-ratio.		
E	Indicates that the Tc spec. of 85°C.		
T	Indicates termination on die.		
Part Number		Mechanical Dimensions (mm)	
A	Wafer Revision	A	19.70
B	Package Method	B	18.40
C	Wafer Vendor	C	9.18
D	Fab#	D	3.24
E	Package Code	E	0.81
Date Code		F	7.74
YY	Year of Assembly	G	0.50
WW	Week of Assembly	H	1.15
Speed Code – core and FSB speed		I	1.28
A.A	1.0	J	0.65
BBB	133	K	0.78
CC.C	7.5	L	0.22
D.DD	1.25	M	1.30
Descrip-	1.0AGHz	N	5.00
		O	0.50
		P	0.80

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## SECTION

## 6

# THERMAL SPECIFICATIONS

## 6.1 INTRODUCTION

---

The VIA Antaur is specified for operation with device case temperatures in the range of 0°C to 70°C (85°C for EBGA). Operation outside of this range will result in functional failures and may potentially damage the device.

Care must be taken to ensure that the case temperature remains within the specified range at all times during operation. An effective heat sink with adequate airflow is therefore a requirement during operation.

## 6.2 TYPICAL ENVIRONMENTS

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Typical thermal solutions involve three components: a heat sink, an interface material between the heat sink and the package, and a source of airflow. The best thermal solutions rely on the use of all three components. To the extent that any of these components are not used, the other components must be improved to compensate for such omission. In particular, the use of interface material such as thermal grease, silicone paste, or graphite paper can make a 40°C difference in the case temperature. Likewise, the imposition of airflow is realistically a requirement.

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## 6.3 MEASURING $T_C$

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The case temperature ( $T_C$ ) should be measured by attaching a thermocouple to the center of the VIA Antaur package. The heat produced by the processor is very localized so measuring the case temperature anywhere else will underestimate the case temperature.

The presence of a thermocouple is inherently invasive; effort must be taken to minimize the effect of the measurement. The thermocouple should be attached to the processor through a small hole drilled in the heat sink. Thermal grease should be used to ensure that the thermocouple makes good contact with the package, but the thermocouple should not come in direct contact with the heat sink.

### Physical Test Conditions

Case temperature measurements should be made in the worst case operating environments. Ideally, systems should be maximally configured, and tested at the worst-case ambient temperature.

### Test Patterns

During normal operation the processor attempts to minimize power consumption. Consequently, normal power consumption is much lower than the maximum power consumption. Thermal testing should be done while running software which causes the processor to operate at its thermal limits.

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## 6.4 MEASURING $T_J$

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The junction temperature of the die can be measured by using the processor's on-chip diode.

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## 6.5 VRM 8.5 SPECIFICATION

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Please be noted that the VIA Antaur Processor could only be used under the VRM 8.5 specification.

## APPENDIX



# MACHINE SPECIFIC REGISTERS

## A.1 GENERAL

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Table A-1 and Table A-2 summarize the VIA Antaur processor machine-specific registers (MSRs). Further description of each MSR follows the table. MSRs are read using the RDMSR instruction and written using the WRMSR instruction.

There are four basic groups of MSRs (not necessarily with contiguous addresses). Other than as defined below, a reference to an undefined MSR causes a General Protection exception.

1. Generally these registers can have some utility to low-level programs (like BIOS).

Note that some of the MSRs (address 0 to 0x4FF) have no function in the VIA Antaur processor. These MSRs do not cause a GP when used on the VIA Antaur processor; instead, reads to these MSRs return zero, and writes are ignored. Some of these undocumented MSRs may have ill side effects when written to indiscriminately. Do not write to undocumented MSRs.

2. There are some undocumented internal-use MSRs used for low-level hardware testing purposes. Attempts to read or write these undocumented MSRs cause unpredictable and disastrous results; so do not use MSRs that are not documented in this datasheet!
3. MSRs used for cache and TLB testing. These use MSR addresses that are not used on compatible processor. These test functions are very low-level and complicated to use. They are not documented in this datasheet but the information will be provided to customers given an appropriate justification

*MSRs are not reinitialized by the bus INIT interrupt; the setting of MSRs is preserved across INIT.*

Table A-1. Category 1 MSRs

<i>MSR</i>	<i>MSR NAME</i>	<i>ECX</i>	<i>EDX</i>	<i>EAX</i>	<i>TYPE</i>	<i>NOTES</i>
TSC	Time Stamp Counter	10h	TSC[63:32]	TSC[31:0]	RW	
EBL_CR_POWERON	EBL_CR_POWERON	2Ah	n/a	Control bits	RW	
PERFCTR0	Performance counter 0	C1h	TSC[39:32]	TSC[31:0]	RW	1
PERFCTR1	Performance counter 1	C2h	0	Count[31:0]	RW	
BBL_CR_CTL3	L2 Hardware Disabled	11Eh	n/a	00800000h	RO	
EVNTSEL0	Event counter 0 select	186h	n/a	00470079h	RO	1
EVNTSEL1	Event counter 1 select	187h	n/a	Control bits	RW	
MTRR	MTRRphysBase0	200h	Control bits	Control bits	RW	
MTRR	MTRRphysMask0	201h	Control bits	Control bits	RW	
MTRR	MTRRphysBase1	202h	Control bits	Control bits	RW	
MTRR	MTRRphysMask1	203h	Control bits	Control bits	RW	
MTRR	MTRRphysBase2	204h	Control bits	Control bits	RW	
MTRR	MTRRphysMask2	205h	Control bits	Control bits	RW	
MTRR	MTRRphysBase3	206h	Control bits	Control bits	RW	
MTRR	MTRRphysMask3	207h	Control bits	Control bits	RW	
MTRR	MTRRphysBase4	208h	Control bits	Control bits	RW	
MTRR	MTRRphysMask4	209h	Control bits	Control bits	RW	
MTRR	MTRRphysBase5	20Ah	Control bits	Control bits	RW	
MTRR	MTRRphysMask5	20Bh	Control bits	Control bits	RW	
MTRR	MTRRphysBase6	20Ch	Control bits	Control bits	RW	
MTRR	MTRRphysMask6	20Dh	Control bits	Control bits	RW	
MTRR	MTRRphysBase7	20Eh	Control bits	Control bits	RW	
MTRR	MTRRphysMask7	20Fh	Control bits	Control bits	RW	
MTRR	MTRRfix64K_00000	250h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_80000	258h	Control bits	Control bits	RW	
MTRR	MTRRfix16K_A0000	259h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C0000	268h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_C8000	269h	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D0000	26Ah	Control bits	Control bits	RW	
MTRR	MTRRfix4K_D8000	26Bh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E0000	26Ch	Control bits	Control bits	RW	
MTRR	MTRRfix4K_E8000	26Dh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F0000	26Eh	Control bits	Control bits	RW	
MTRR	MTRRfix4K_F8000	26Fh	Control bits	Control bits	RW	
MTRR	MTRRdefType	2FFh	Control bits	Control bits	RW	

**Notes:**

1. PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR that reflects this limitation.

**Table A-2. Category 2 MSRs**

MSR	MSR NAME	ECX	EDX	EAX	TYPE	NOTES
FCR	Feature Control Reg	1107h	n/a	FCR value	RW	
FCR2	Feature Control Reg 2	1108h	FCR2_Hi	FCR2 value	RW	1
FCR3	Feature Control Reg 3	1109h	FCR3_Hi	FCR3 value	WO	1

**Notes:**

1. FCR2 and FCR3 provide system software with the ability to specify the Vendor ID string returned by the CPUID instruction.

## A.2 CATEGORY 1 MSRS

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### 10H: TSC (TIME STAMP COUNTER)

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VIA Antaur processor has a 64-bit MSR that materializes the Time Stamp Counter (TSC). System increments the TSC once per processor clock. The TSC is incremented even during AutoHalt or StopClock. A WRMSR to the TSC will clear the upper 32 bits of the TSC.

### 2AH: EBL\_CR\_POWERON

---

31:27	27	26	25:22	21:20	19:18	17:15	14	13	12:0
Res '11000'	BF4	Low-PowerEn '1'	BF[3:0]	Res	BSEL	Res	1MPOV	IOQDepth	Reserved (Ignored on write; returns 0 on read)
5	1	1	4	2	2	3	1	1	13

**IOQDepth:** 0 = In Order Queue Depth with up to 8 transactions  
1 = 1 transaction

**1MPOV:** 0 = Power on Reset Vector at 0xFFFFFFFF0 (4Gbytes)  
1 = Power on Reset Vector at 0x000FFFFF0 (1 Mbyte)

**BSEL:** 01 = 133 MHz Bus  
10 = 100 MHz Bus

**BF[4:0]: Bus Clock Frequency Ratio**

Antaur	MSR 0x2A [27]	MSR 0x2A [25:22]
5.0	0	0000b
16.0	0	0001b
Reserved	0	0010b
10.0	0	0011b
5.5	0	0100b
Reserved	0	0101b
Reserved	0	0110b
9.5	0	0111b
9.0	0	1000b
7.0	0	1001b
8.0	0	1010b
6.0	0	1011b
12.0	0	1100b
7.5	0	1101b
8.5	0	1110b
6.5	0	1111b
9.0	1	0000b
Reserved in Steppings 0 &1 11.0 otherwise	1	0001b
12.0	1	0010b
10.0	1	0011b
13.5	1	0100b
11.5	1	0101b
12.5	1	0110b
10.5	1	0111b
13.0	1	1000b
15.0	1	1001b
16.0	1	1010b
14.0	1	1011b
12.0	1	1100b
15.5	1	1101b
Reserved	1	1110b
14.5	1	1111b

**LowPowerEn:** This bit always set to '1'

**C1H-C2H: PERFCTR0 & PERFCTR1**

These are events counters 0 and 1. VIA Antaur processor's PERFCTR0 is an alias for the lower 40 bits of the TSC.

**11EH: BBL\_CR\_CTL3**

31:24	23	22:0
<i>Reserved</i>	L2_Hdw_Disable '1'	<i>Reserved</i> (Ignored on write; returns 0 on read)
8	1	23

The VIA Antaur processor does contain an L2 cache. For compatibility, this read-only MSR indicates to the BIOS or system software that the L2 is disabled even if the L2 is enabled.

**L2\_Hdw\_Disable:** This bit always set to '1'

**186H: EVNTSEL0 (EVENT COUNTER 0 SELECT)**

31:24	23:16	15:9	8:0
<i>Reserved</i>	<i>Reserved</i>	<i>Reserved</i>	CTR0 Event Select = 79h
8	8	7	9

PERFCTR0 is an alias for the lower 40 bits of the Time Stamp Counter. EVNTSEL0 is a read only MSR which reflects this limitation. The CTR0\_Event Select field always returns 0x0079, which corresponds to counting of processor clocks.

**187H: EVNTSEL1 (EVENT COUNTER 1 SELECT)**

31:24	23:16	15:9	8:0
<i>Reserved</i>	<i>Reserved</i>	<i>Reserved</i>	CTR1 Event Select
8	8	7	9

VIA Antaur processor has two MSRs that contain bits defining the behavior of the two hardware event counters: PERFCTR0 and PERFCTR1.

The CTR1\_Event\_Select control field defines which of several possible events is counted. The possible Event Select values for PERFCTR1 are listed in the table below. Note that CTR1\_Event\_Select is a 9-bit field.

The EVNTSEL1 register should be written before PERFCTR1 is written to initialize the counter. The counts are not necessarily perfectly exact; the counters are intended for use over a large number of events and may differ by one or two counts from what might be expected.

Most counter events are internal implementation-dependent debug functions, having no meaning to software. The counters that can have end-user utility are:

<b>EVENT</b>	<b>DESCRIPTION</b>
C0h	Instructions executed
1C0h	Instructions executed and string iterations
79h	Internal clocks (default event for CTR0)



## A.3 CATEGORY 2 MSRS

### 1107H: FCR (FEATURE CONTROL REGISTER)

The FCR controls the major optional feature capabilities of the VIA Antaur processor. Table A-3 contains the bit values for the FCR. The default settings shown for the FCR bits are not necessarily exact. The actual settings can be changed as part of the manufacturing process and thus a particular VIA Antaur processor version can have slightly different default settings than shown here. All reserved bit values of the FCR must be preserved by using a read-modify-write sequence to update the FCR.

**Table A-3. FCR Bit Assignments**

<i><b>BIT</b></i>	<i><b>NAME</b></i>	<i><b>DESCRIPTION</b></i>	<i><b>DEFAULT</b></i>
0	ALINST	<i>Reserved for test &amp; special uses</i>	0
1	ECX8	Enables CPUID reporting CX8	1
2		<i>Reserved</i>	0
3		<i>Reserved</i>	0
4		<i>Reserved</i>	0
5	DSTPCLK	Disables supporting STPCLK	0
6		<i>Reserved</i>	0
7	EPGE	Enables CR4.PGE and CPUID.PGE (Page Global Enable)	1
8	DL2	Disables L2 Cache	0
9		<i>Reserved</i>	1
10		<i>Reserved</i>	0
11	DPDC	Disables Page Directory cache	0
12	EBRPRED	Enables Branch Prediction	1
13	DIC	Disables I-Cache	0
14	DDC	Disables D-Cache	0
31:15		<i>Reserved</i>	0/1

- ALTINST:** 0 = Normal x86 instruction execution.  
1 = Alternate instruction set execution is enabled (see details below)
- ECX8:** 0 = The CPUID instruction does not report the presence of the CMPXCHG8B instruction (CX8 = 0). The instruction actually exists and operates correctly, however.  
1 = The CPUID instruction reports that the CMPXCHG8B instruction is supported (CX8 = 1).
- DSTPCLK:** 0 = STPCLK interrupt properly supported.  
1 = Ignores SPCLK interrupt.
- EPGE:** 0 = The processor does not support Page Global Enable and therefore CPUID Feature Flags reports EDX[13]=0; attempts to set CR4.PGE are ignored.  
1 = The processor supports Page Global Enable and therefore CPUID Feature Flags reports EDX[13]=1; CR4.PGE can be set to 1.
- DL2:** 0 = L2 Cache enabled.  
1 = L2 Cache disabled.
- DPDC:** 0 = Enables use of internal Page Directory Cache.  
1 = Disables use of internal Page Directory Cache.
- EBRPRED:** 0 = Disables branch prediction function.  
1 = Enables branch prediction function.
- DIC:** 0 = Enables use of I-Cache.  
1 = Disables use of I-Cache: cache misses are performed as single transfer bus cycles, PCD is de-asserted. This overrides any setting of CR0.CD and CR0.NW.
- DDC:** 0 = Enables use of D-Cache.  
1 = Disables use of D-Cache: same semantics as for DIC except for D-Cache.

## ALTERNATE INSTRUCTION EXECUTION

---

When set to 1, the ALTINST bit in the FCR enables execution of an alternate (not x86) instruction set. While setting this FCR bit is a privileged operation, executing the alternate instructions can be done from any protection level.

This alternate instruction set includes an extended set of integer, MMX, floating-point, and 3DNow! instructions along with additional registers and some more powerful instruction forms over the x86 instruction architecture. For example, in the alternate instruction set, privileged functions can be used from any protection level, memory descriptor checking can be bypassed, and many x86 exceptions such as alignment check can be bypassed.

This alternate instruction set is intended for testing, debug, and special application usage. Accordingly, it is not documented for general usage. If you have a justified need for access to these instructions, contact your VIA representative.

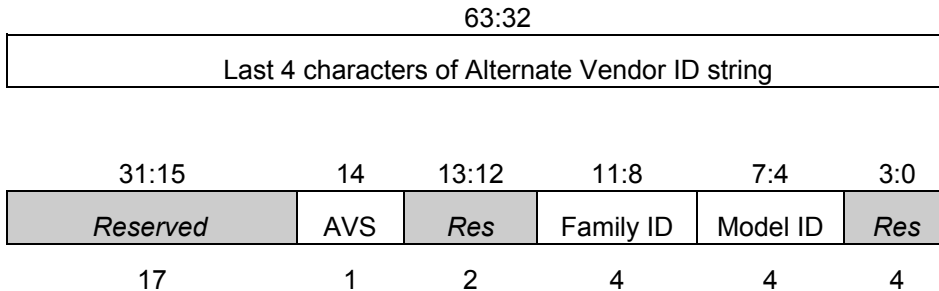
The mechanism for initiating execution of this alternate set of instructions is as follows:

1. Set the FCR ALTINST bit to 1 using WRMSR instruction (this is a privileged instruction). This should be done using a read-modify-write sequence to preserve the values of other FCR bits.
2. The ALTINST bit enables execution of a new x86 jump instruction that starts execution of alternate instructions. This new jump instruction can be executed from any privilege level at any time that ALTINST is 1. The new jump instruction is a two-byte instruction: 0x0F3F. If ALTINST is 0, the execution of 0x0F3F causes an Invalid Instruction exception.
3. When executed, the new 0x0F3F x86 instruction causes a near branch to CS:EAX. That is, the branch function is the same as the existing x86 instruction
  - `jmp [eax]`
  - In addition to the branch, the 0x0F3F instruction sets the processor into an internal mode where the target bytes are not interpreted as x86 instructions but rather as alternate instruction set instructions.
4. The alternate instructions fetched following the 0x0F3F branch should be of the form
  - `0x8D8400XXXXXXXX` where `0XXXXXXXX` is the 32-bit alternate instruction
  - That is, the alternate instructions are presented as the 32-bit displacement of a
    - `LEA [EAX+EAX+disp]`
    - instruction. This example assumes that the current code segment size is 32-bits, if it is 16-bits, then an address size prefix (0x67) must be placed in front of the LEA opcode.
5. Upon fetching, the LEA “wrapper” is stripped off and the 32-bit alternate instruction contained in the displacement field is executed.
6. The alternate instruction set contains a special branch instruction that returns control to x86 fetch and execute mode. The x86 state upon return is not necessarily what it was when alternate instruction execution is entered since the alternate instructions can completely modify the x86 state.

While all VIA ANTAUR processor processors contain this alternate instruction feature, the invocation details (e.g., the 0x8D8400 “prefix”) may be different between processors. Check the appropriate processor datasheet for details.

**1108H: FCR2 (FEATURE CONTROL REGISTER 2)**

This MSR contains more feature control bits — many of which are undefined. It is important that using a read-modify-write sequence to update the MSR preserves all reserved bits.



- AVS:** 0 = The CPUID instruction vendor ID is “CentaurHauls”  
 1 = The CPUID instruction returns the alternate Vendor ID. The first 8 characters of the alternate Vendor ID are stored in FCR3 and the last 4 characters in FCR2[63:32]. These 12 characters are undefined after RESET and may be loaded by system software using WRMSR.
- Family ID:** This field will be returned as the family ID field by subsequent uses of the CPUID instruction
- Model ID:** This field will be returned as the model ID field by subsequent uses of the CPUID instruction

**1109H: FCR (FEATURE CONTROL REGISTER 3)**

This MSR contains the first 8 characters of the alternate Vendor ID. The alternate Vendor ID is returned by the CPUID instruction when FCR2[AVS] is set to ‘1’. FCR3 is a write-only MSR.

